Ninevah University
College of Electronics Engineering
Systems & Control Engineering

Decoders

A binary code of n bits is capable of representing up to 2^n distinct elements of coded information. A decoder is a combinational circuit that converts binary information from **n** input lines to a maximum of 2^n unique output lines.

As an example, consider A three to eight decoder.

1. Problem Statement & Variable Assignment

Three inputs (A, B, C) are decoded into eight outputs (D_0 - D_7)

2. Truth Table

Inputs			Outputs							
x	***y***	***z***	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

3. Boolean Functions

$$D_0 = \bar{X}\bar{Y}\bar{Z}$$

$$D_1 = \bar{X}\bar{Y}Z$$

$$D_2 = \bar{X}Y\bar{Z}$$

$$D_3 = \bar{X}YZ$$

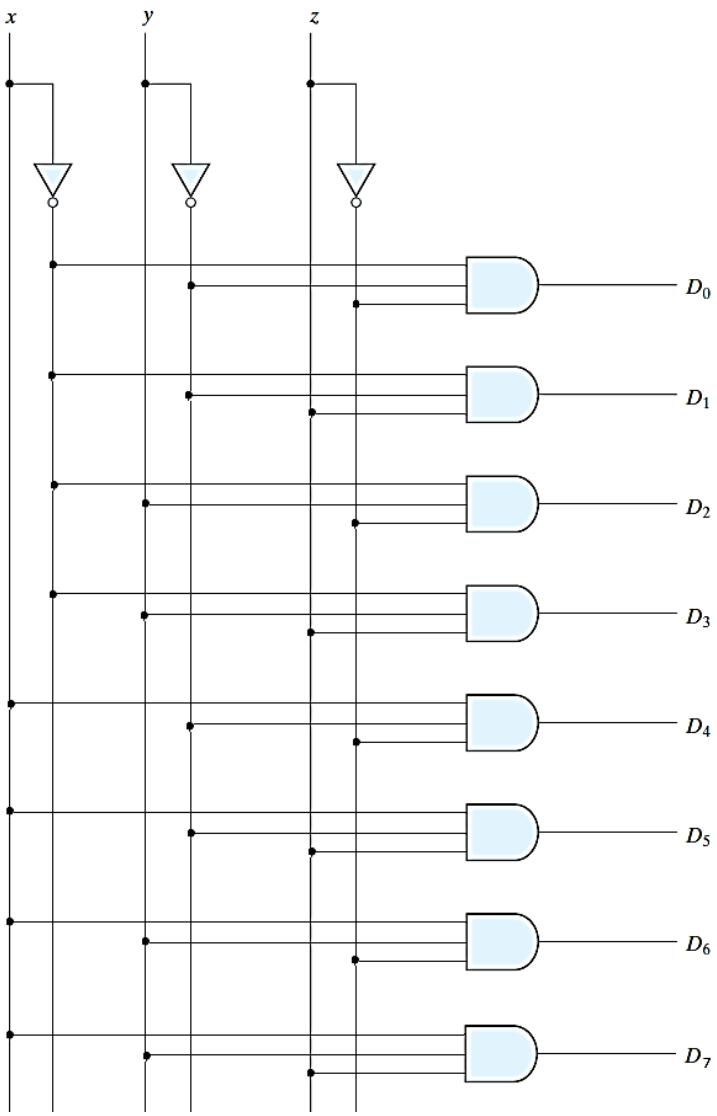
$$D_4 = X\bar{Y}\bar{Z}$$

$$D_5 = X\bar{Y}Z$$

$$D_6 = XY\bar{Z}$$

$$D_7 = XYZ$$

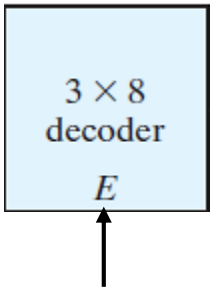
4. Logic Diagram



Prepared by: Mohammed N. Y. Almaged

It is important to notice that decoders include enable input to control the circuit operation.

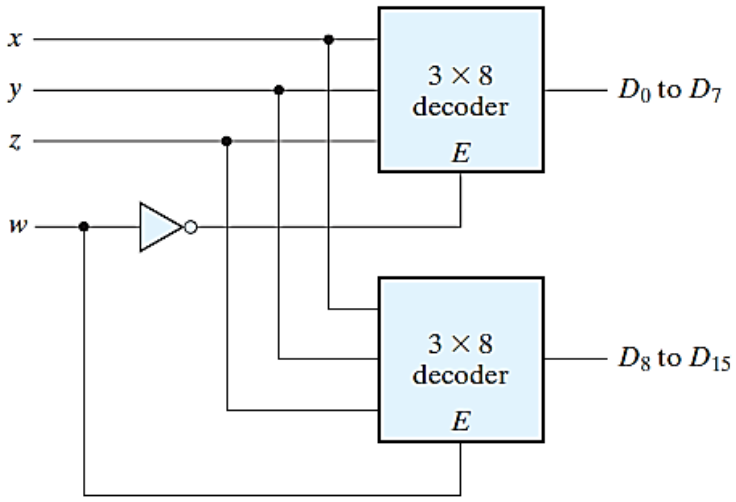
- The circuit is disabled when E is equal to 0 and hence all the outputs are equal to zero regardless (بغض النظر) of the values of the inputs.
- The circuit is enabled when E is equal to 1.



Higher Order Decoders

Higher order decoders like 4 to 16 lines, 5 to 32 lines, are available in MSI packages (IC) where the internal circuits are similar to the 3-8 decoder. Thus, Decoders with enable inputs can be connected together to form a larger decoder circuit.

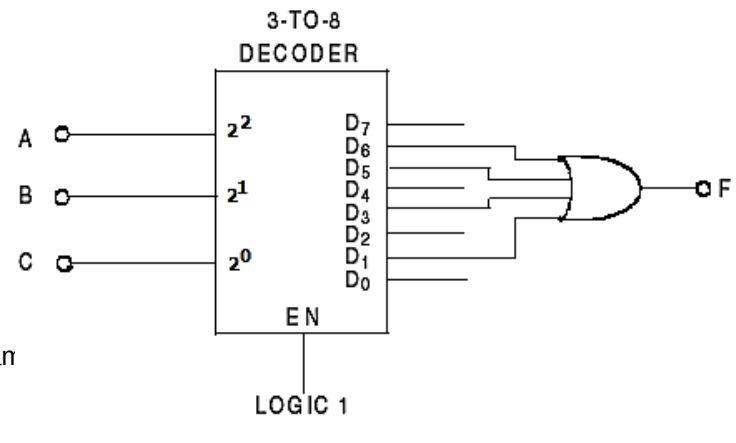
For example, two 3-8-line decoders with enable inputs connected to form a 4-16 decoder.



Boolean Functions Implementation

Since the decoders generates all the minterms of the inputs, any Boolean function can be implemented by selecting the required minterms and then OR them together.

Ex) Implement the Boolean function $F\ (A, B, C)\ =\ \sum(1,3,5,6)$ using a decoder IC.



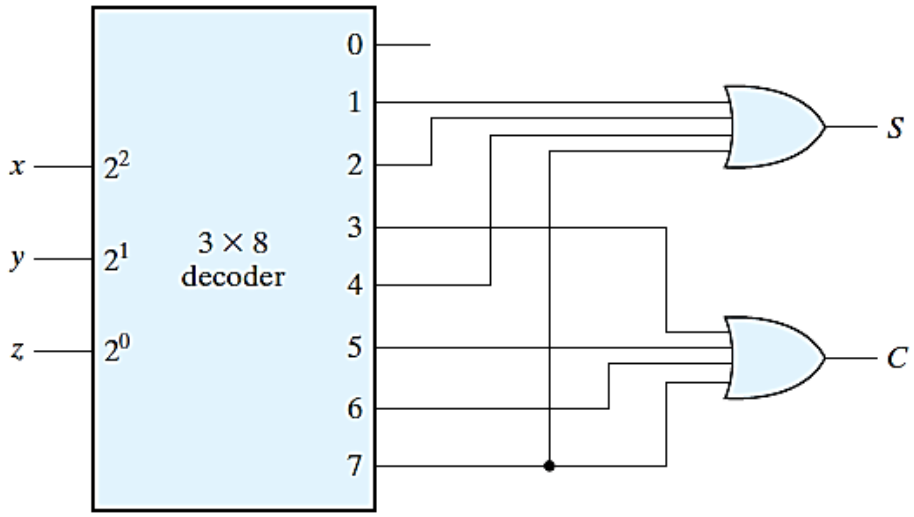
Ex) design a full adder circuit using a decoder IC.

The truth table of the full adder is as follow:

Input variables			*Outputs*	
X	*A*	*B*	*S*	*C*
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$S(x, y, z) = \Sigma(1, 2, 4, 7)$$
$$C(x, y, z) = \Sigma(3, 5, 6, 7)$$

The circuit is shown below



BCD to 7 Segments Decoder

7-segment display is a special modules consisting of seven LEDs '*a*, *b*, *c*, *d*, *e*, *f*, and *g*' of a certain shape and placed at a certain orientation as below:

(a) Segment designation (b) Numerical designation for display

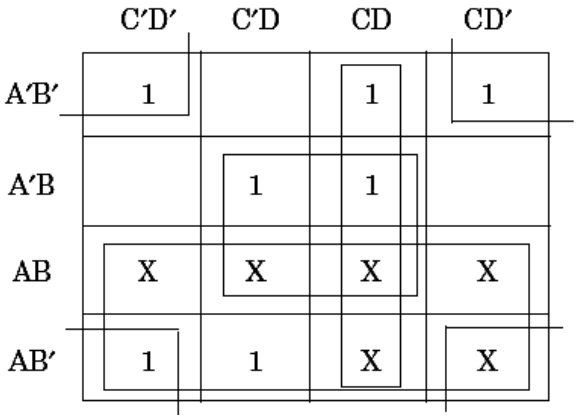
Decimal digits 0 to 9 can be displayed by glowing some particular LED segments. As an example, digit '1' may be represented by glowing the segments *a* and *b* only.

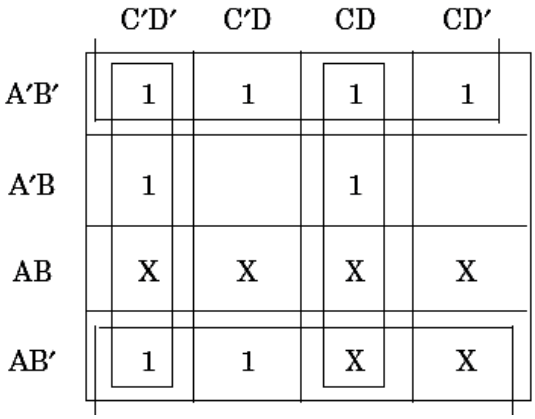
Truth Table

Decimal	*Input Variables*				*Output Variables as Seven Segment Display*						
Numbers	*A*	*B*	*C*	*D*	*a*	*b*	*c*	*d*	*e*	*f*	*g*
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	0	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	0	0	1	1

K-Map

K- map should be constructed for all outputs. Here, we will only show K-map for a & b.





The Boolean expressions for a to g are given as

$a = A + CD + BD + B'D'$

$b = B' + C'D' + CD$

$c = B + C' + D$

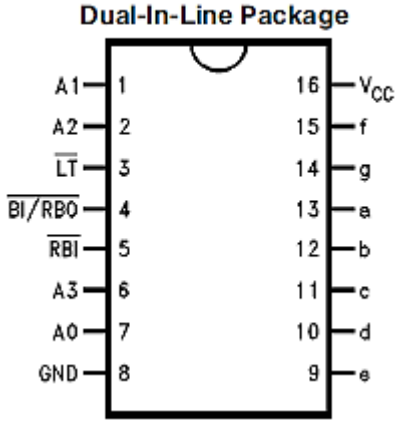
$d = B'D' + CD' + B'C + BC'D$

$e = B'D' + CD'$

$f = A + C'D' + BC' + BD'$

$g = A + BC' + CD' + B'C.$

The BCD-to-seven-segment decoders are available in a single IC package.



Prepared by: Mohammed N. Y. Almaged