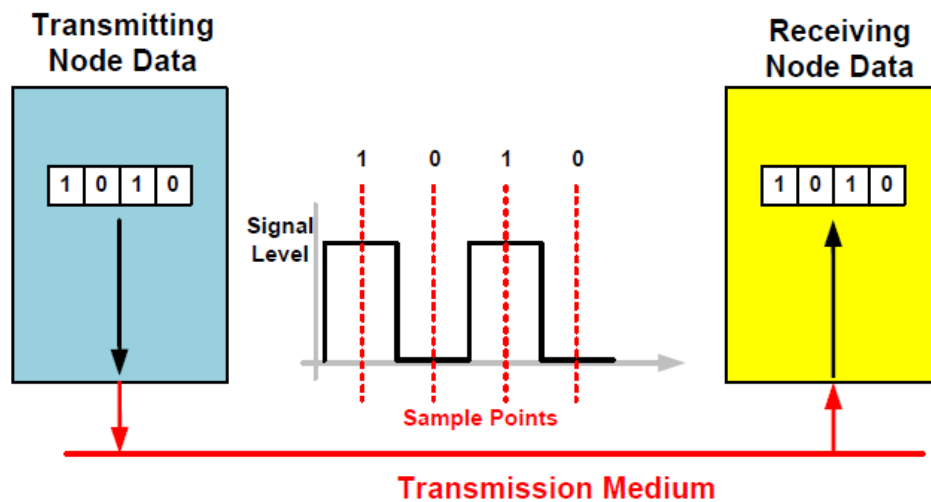


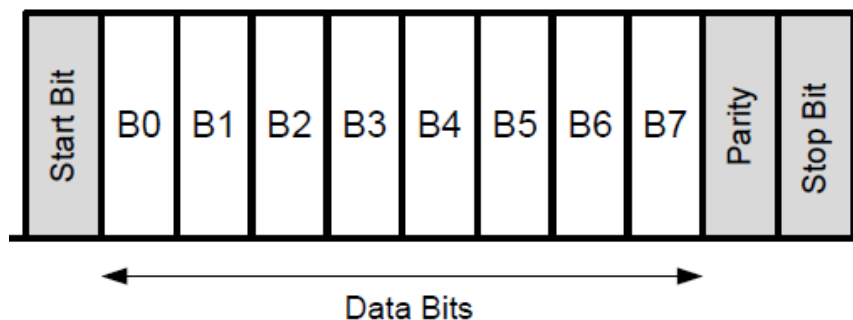


Bit Parity

External noise on the transmission medium and loss of signal strength cause loss of data bit information while transporting data from one device to other device.



To detect errors during the transmission of information from one location to another, an extra **parity bit** is inserted with the message to make the total number of **ONES** (1'S) either even or odd.



Bit Parity Generator Circuit

A parity generator is a combination logic system to generate the parity bit at the transmitting side.

Consider a three-bit message to be transmitted together with an even-parity bit. Design a three-bit parity generator circuit.

Even-Parity-Generator Truth Table

Three-Bit Message			Parity Bit
<i>x</i>	<i>y</i>	<i>z</i>	<i>P</i>
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

The parity bit function is as follow

$$P = \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} + XYZ$$

$$P = \bar{X}(\bar{Y}Z + Y\bar{Z}) + X(\bar{Y}\bar{Z} + YZ)$$

$$P = \bar{X}(Y \oplus Z) + X(Y \oplus Z)'$$

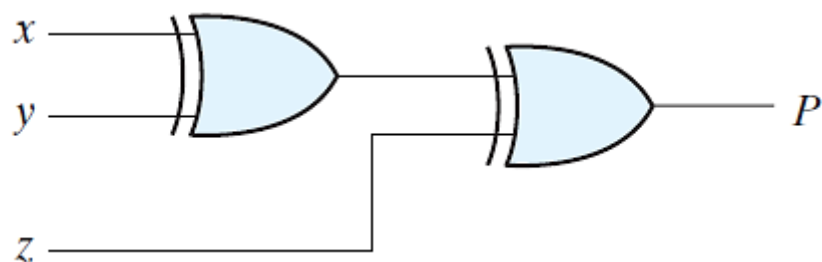
$$\text{Let } (Y \oplus Z) = W$$

$$P = \bar{X}W + X\bar{W}$$

$$P = (X \oplus W)$$

$$P = (X \oplus Y \oplus Z)$$

The Logic diagram of a 3-bit parity generator is



The same procedure can be followed to design a 4-bit parity generator

<i>Four bit Message</i>				<i>Even Parity</i>
A	B	C	D	(P)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

		<i>C</i>			
		00	01	11	10
<i>A</i>	00	m_0	m_1 1	m_3	m_2 1
	01	m_4 1	m_5	m_7 1	m_6
	11	m_{12}	m_{13} 1	m_{15}	m_{14} 1
	10	m_8 1	m_9	m_{11} 1	m_{10}
		<i>D</i>			

The function can be derived from the truth table or K-map:

$$P = \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}BCD + A\bar{B}\bar{C}\bar{D} + A\bar{B}C\bar{D} + AB\bar{C}\bar{D} + ABC\bar{D}$$

This function can be simplified into

$$P = (A \oplus B \oplus C \oplus D) \quad (H.W.)$$

Therefore, we can design an even parity generator circuit for any number of bits by using cascaded **Exclusive-OR gates**.

It is important to notice that this method detects one, three, or any odd combination of errors in each message that is transmitted. However, an even combination of errors goes undetected.

Binary to Gray Code Converter

The truth table below shows the **four-input** bits of binary numbers designated as A, B, C, and D while the equivalent **four-output** gray code bits are marked as W, X, Y, and Z.

<i>Binary</i>				<i>Gray</i>			
<i>A</i>	<i>B</i>	<i>C</i>	<i>D</i>	<i>W</i>	<i>X</i>	<i>Y</i>	<i>Z</i>
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

The Karnaugh maps of each output is shown as

	C'D'	C'D	CD	CD'
A'B'				
A'B				
AB	1	1	1	1
AB'	1	1	1	1

Karnaugh map for W.

	C'D'	C'D	CD	CD'
A'B'				
A'B	1	1	1	1
AB				
AB'	1	1	1	1

Karnaugh map for X.

	C'D'	C'D	CD	CD'
A'B'			1	1
A'B	1	1		
AB	1	1		
AB'			1	1

Karnaugh map for Y.

	C'D'	C'D	CD	CD'
A'B'		1		1
A'B		1		1
AB		1		1
AB'		1		1

Karnaugh map for Z.

The output functions are as follow

$$W = A,$$

$$Y = BC' + B'C = B \oplus C, \text{ and}$$

$$X = A'B + AB' = A \oplus B,$$

$$Z = C'D + CD' = C \oplus D.$$

