Ninevah University
College of Electronics Engineering
Systems & Control Engineering

Multiplexer

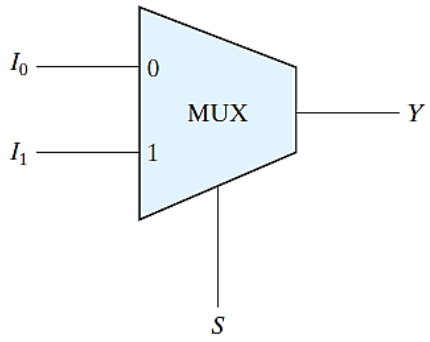
A multiplexer is a combinational circuit that selects one inputs from many input lines and directs it to a **single output** line. It also has another input called **Selector (S).**

Normally, there are 2^n input lines and n selection lines whose bit combinations determine which input is selected.

2-1 multiplexer

A 2-1 multiplexer has two data input lines, one output line and one selection line S.

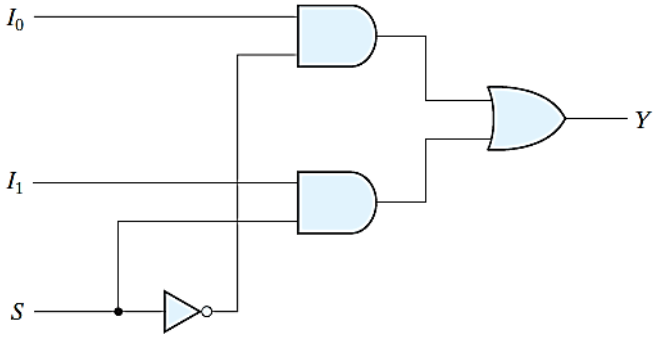
- When S = 0, the upper input I_0 will be transferred to the output.
- When S = 1, the lower input I_1 will be transferred to the output.



Block diagram

Truth Table

Selection Input	Input		Output
S	**I_0**	**I_1**	**Y**
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1



$$Y = \bar{S}I_0 + SI_1$$

4-1 multiplexer

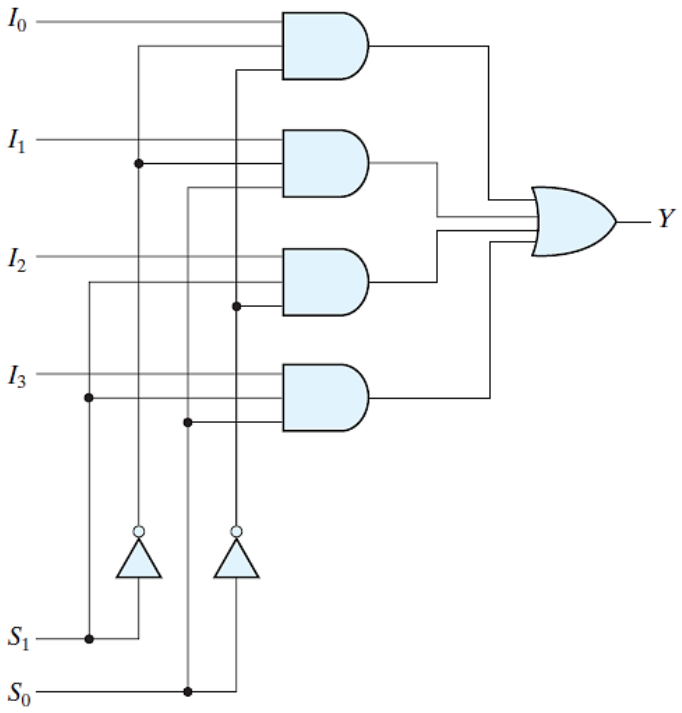
A 4-1 multiplexer has 4 data input lines, one output line and two selection line S_1, S_0.

Selection Inputs		*Input Channels*				*Output*
S_1	S_0	I_0	I_1	I_2	I_3	Y
0	0	0	X	X	X	0
0	0	1	X	X	X	1
0	1	X	0	X	X	0
0	1	X	1	X	X	1
1	0	X	X	0	X	0
1	0	X	X	1	X	1
1	1	X	X	X	0	0
1	1	X	X	X	1	1

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$Y = \overline{S_1}\,\overline{S_0}\;I_0 + \overline{S_1}\,S_0\;I_1 + S_1\,\overline{S_0}\;I_2 + S_1\,S_0\,I_3$$

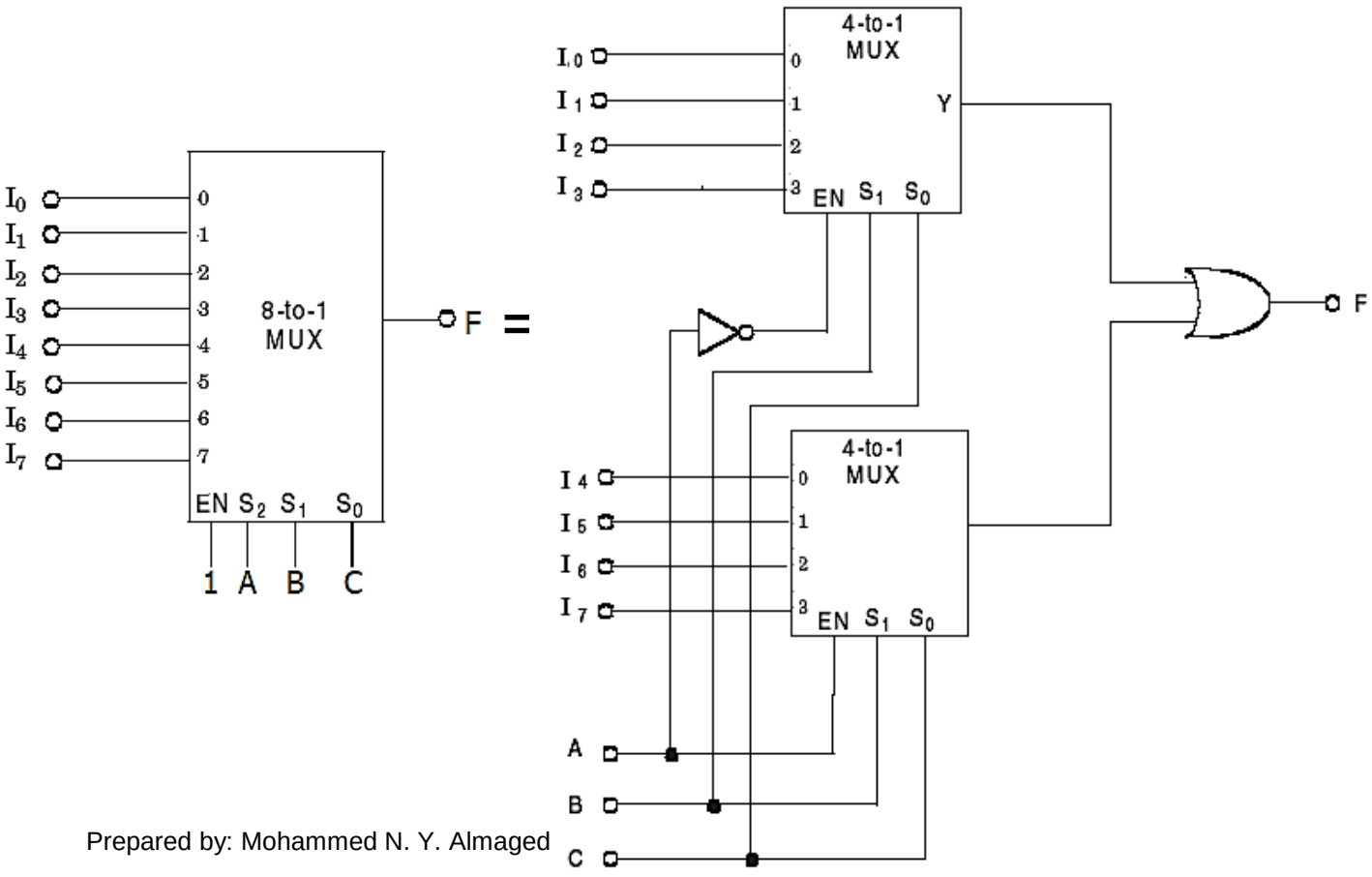
Logic Diagram



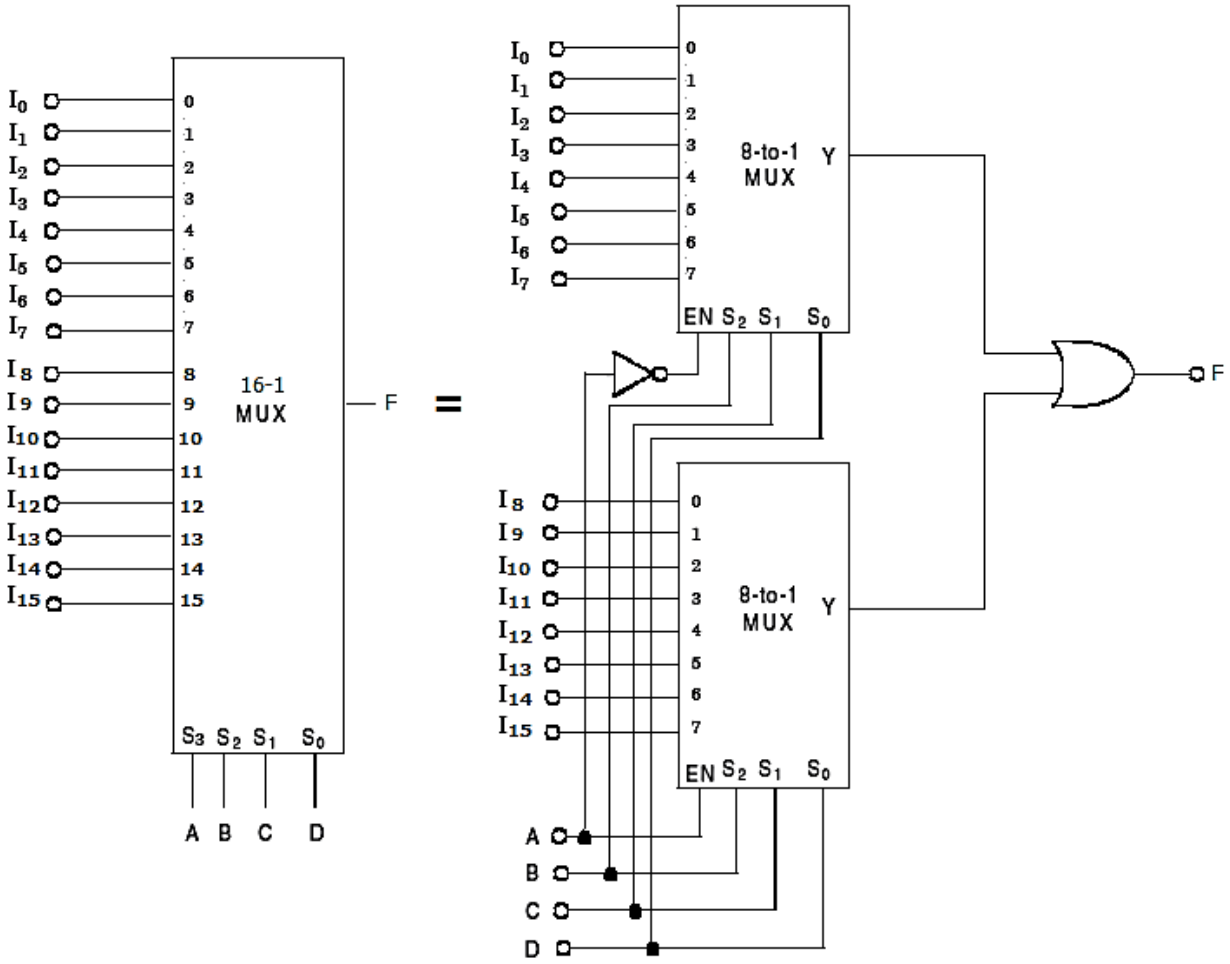
Cascading of Multiplexers

Multiplexers of a larger number of inputs can be implemented by the multiplexers of a smaller number of input lines.

Ex) Design an 8-1 multiplexer by using two 4-1 multiplexers.



Ex) Design a 16-1 multiplexer by using two 8-1 multiplexers.



HW) Design a 16-1 multiplexer by using 2-1 multiplexers.

Boolean Function Implementation

A Boolean function of n variables, for example (x, y, z), can be implemented with a multiplexer that has n - 1 selection inputs (S_1 & S_0). The first n - 1 variables of the function (x, y) are connected to the selection inputs of the multiplexer (S_1 & S_0). The remaining single variable (z) of the function is used for the data inputs (I_0, I_1, I_2, I_3).

The relationship between the remaining variable (z) and the data inputs of the multiplexer (I) is determined from the **truth table**. Each data input of the multiplexer will be either equal to Z , $\bar{Z}$, 0 , 1

Ex) Design the $F\ (x, y, z)\ = \sum(1, 2, 6, 7)$ using Multiplexer.

This function of three variables can be implemented with a multiplexer that has 2 selectors, thus we use 4 -1 multiplexer.

X is connected to S_1

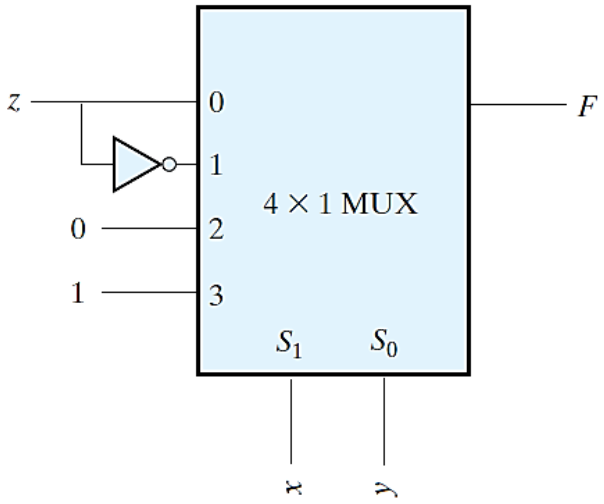
Y is connected to S_0

Then, we find the relationship between Z and the data inputs I_0, I_1, I_2, I_3 from the truth table as follow:

Truth Table

x	y	z	F	
0	0	0	0	$F = z$
0	0	1	1	
0	1	0	1	$F = z'$
0	1	1	0	
1	0	0	0	$F = 0$
1	0	1	0	
1	1	0	1	$F = 1$
1	1	1	1	

Logic Diagram



Ex) Design the $F\ (A, B, C, Z) = \sum(1, 3, 4, 11, 12, 13, 14, 15)$ using Multiplexer.

This function of 4 variables can be implemented with a multiplexer that has 3 selectors, thus we use 8 -1 multiplexer.

A is connected to S_2, B is connected to S_1, C is connected to S_2

Then, we find the relationship between D and the data inputs I_0 – I_7 from the truth table as follow:

Truth Table **Logic Diagram**

A	B	C	D	F	
0	0	0	0	0	$F = D$
0	0	0	1	1	
0	0	1	0	0	$F = D$
0	0	1	1	1	
0	1	0	0	1	$F = D'$
0	1	0	1	0	
0	1	1	0	0	$F = 0$
0	1	1	1	0	
1	0	0	0	0	$F = 0$
1	0	0	1	0	
1	0	1	0	0	$F = D$
1	0	1	1	1	
1	1	0	0	1	$F = 1$
1	1	0	1	1	
1	1	1	0	1	$F = 1$
1	1	1	1	1