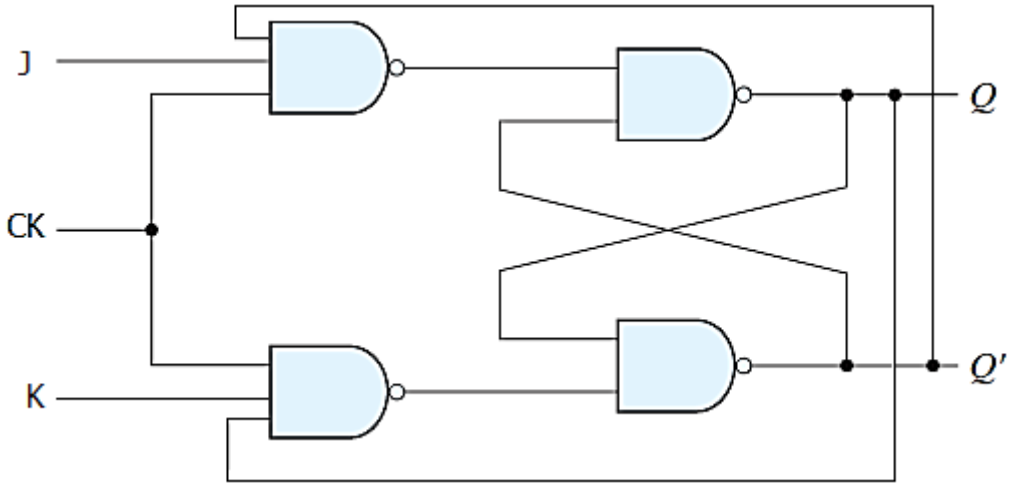
Ninevah University
College of Electronics Engineering
Systems & Control Engineering

JK flip flop

To avoid the **Not Use** case in SR flip flop, JK flip flop is designed, which is basically a SR flip flop with a feedback inputs as follow:



Circuit Analysis

It can be seen from the **NAND gate Truth Table** that if one input (A) is equal to 0, the output is 1 regardless the value of the other input (B).

The Truth table of the SR Flip flop becomes

			Previous State		Present State	
CK	J	K	Q_n	$\overline{Q_n}$	Q_{n+1}	$\overline{Q_{n+1}}$
0	X	X	0	1	Q_n (Memory)	$\overline{Q_n}$ (Memory)
0	X	X	1	0	Q_n (Memory)	$\overline{Q_n}$ (Memory)
1	0	0	0	1	Q_n (Memory)	$\overline{Q_n}$(Memory)
1	0	0	1	0	Q_n (Memory)	$\overline{Q_n}$(Memory)
1	0	1	0	1	0 (Reset)	1 (Reset)
1	0	1	1	0	0 (Reset)	1 (Reset)
1	1	0	0	1	1 (Set)	0 (Set)
1	1	0	1	0	1 (Set)	0 (Set)
1	1	1	0	1	1 (Toggle)	0 (Toggle)
1	1	1	1	0	0 (Toggle)	1 (Toggle)

This can be summarized as:

CK	J	K	Q_{n+1}
0	X	X	Q_n (Memory)
1	0	0	Q_n (Memory)
1	0	1	0 (Reset)
1	1	0	1 (Set)
1	1	1	$\overline{Q_n}$ (Toggle)

Prepared by: Mohammed N. Y. Almaged

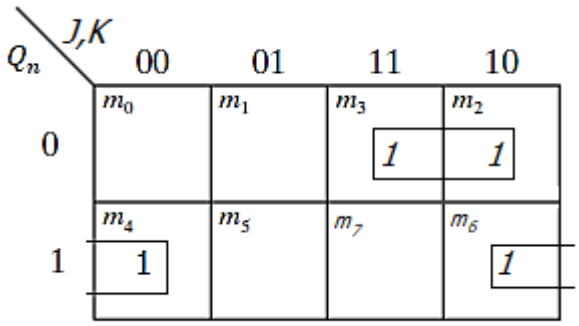
Characteristic Table

Table that defines the next state Q_{n+1} (the state that results from a clock transition) as a function of the inputs and the present state Q_n.

The characteristic table of JK flip flop has 3 inputs (J, K, Q_n) and one output (Q_{n+1})

Q_n	J	K	Q_{n+1}	
0	0	0	0	Memory
0	0	1	0	Set
0	1	0	1	Reset
0	1	1	1	Toggle
1	0	0	1	Memory
1	0	1	0	Set
1	1	0	1	Reset
1	1	1	0	Toggle

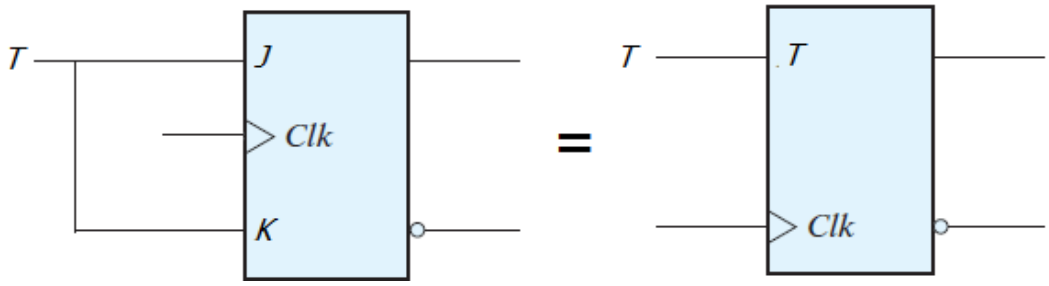
The function Q_{n+1} can be found using K-Map



$$Q_{n+1} = \overline{Q_n}\, J + Q_n\, \overline{K}$$

T Flip Flop

A T (Toggle) flip flop can be obtained by shorting the inputs of the JK flip flop as follow:



The Truth table of the SR Flip flop becomes

CK	T	Q_{n+1}
0	X	Q_n (Memory)
1	0	Q_n (Memory)
1	1	$\overline{Q_n}$ (Toggle)

The characteristic table of T flip flop has 2 inputs (T, Q_n) and one output (Q_{n+1})

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

$$Q_{n+1} = Q_n \oplus T$$

Counters

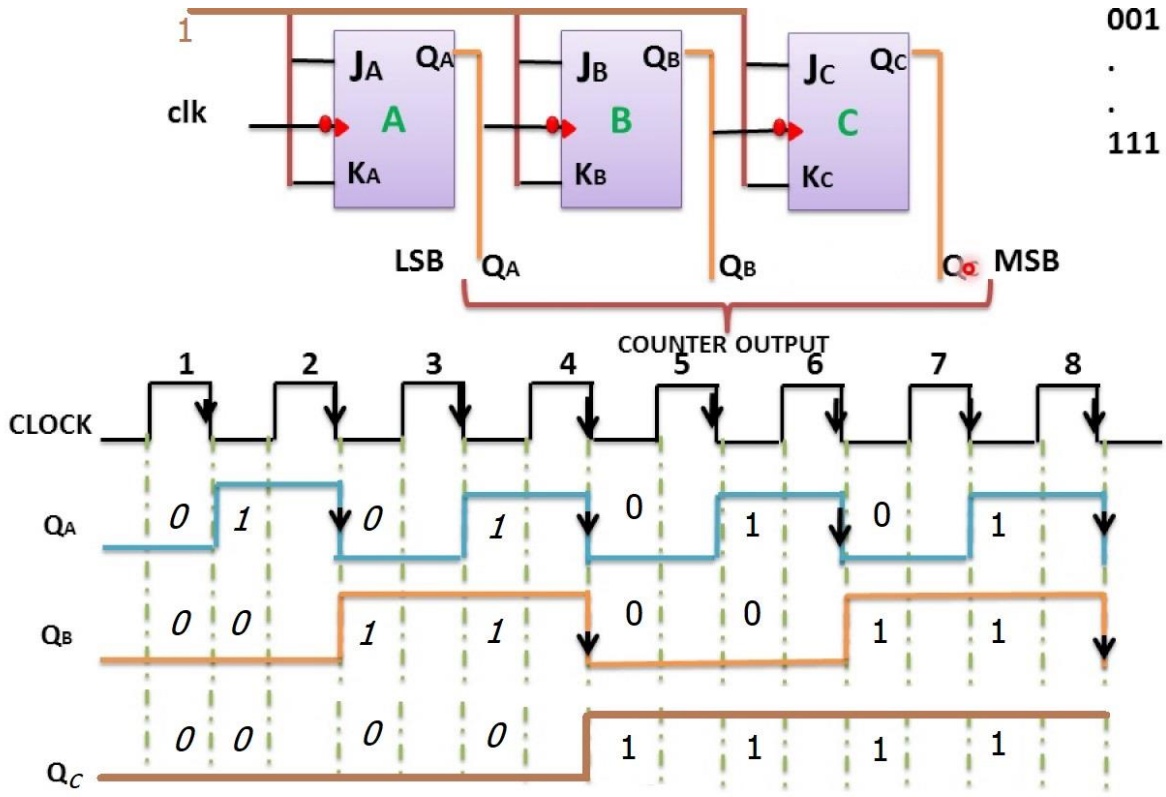
One of the applications of flip flop is the designing counters. There are mainly two types of counters, UP & Down counters.

The number of flip flops required = Number of counting bits

Up counter

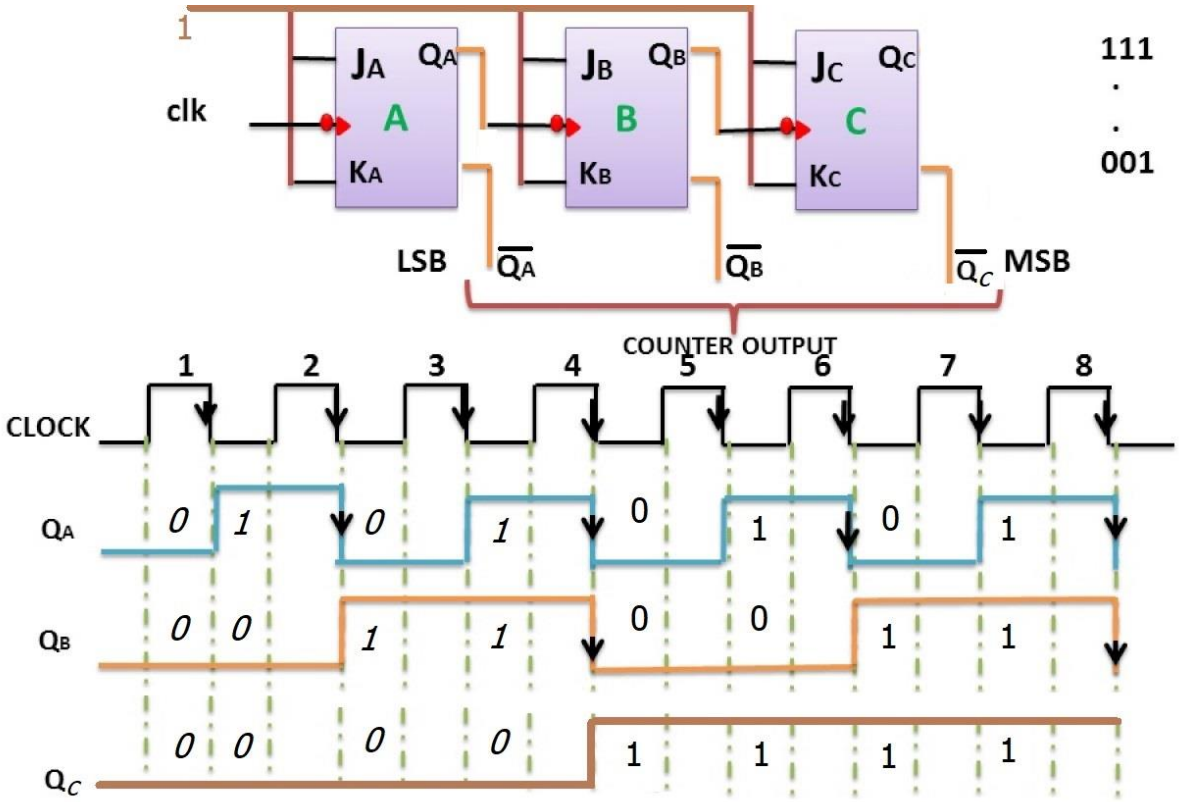
Design a 3-bit Asynchronous up counter.

The number of flip flops required = 3



Down counter

The same configuration will be used but the output will be taken from $\overline{Q_A}$, $\overline{Q_B}$, $\overline{Q_C}$



(HW) Complete the above timing diagram by drawing $\overline{Q_A}$, $\overline{Q_B}$, $\overline{Q_C}$ signals.