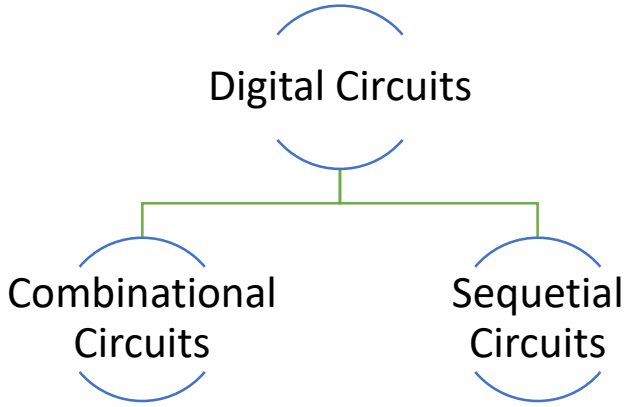
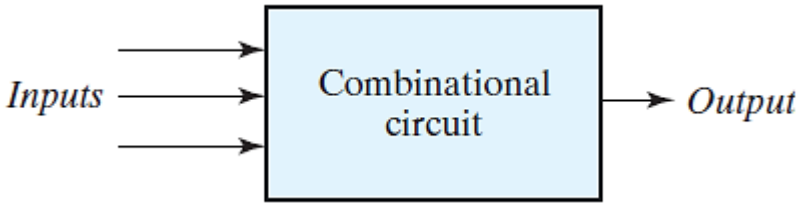
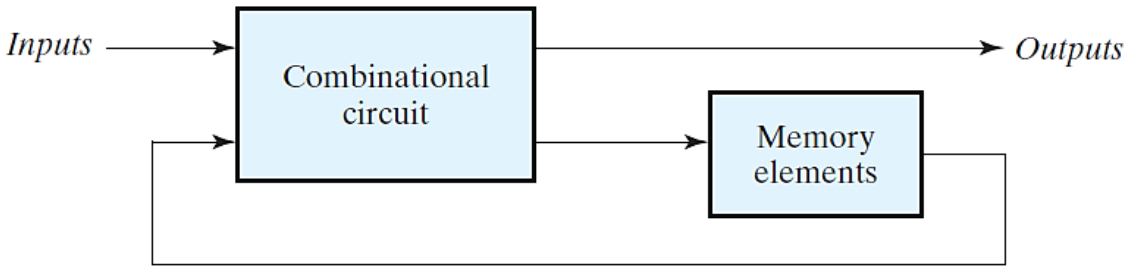


Combinational circuits: A logic circuits whose outputs at any instant of time depend only on the input signals.



Sequential circuits: A logic circuits whose outputs at any instant of time depend on the present inputs as well as on the past outputs. It consists of a combinational circuit with storage elements that are used to feed the value of the previous states.

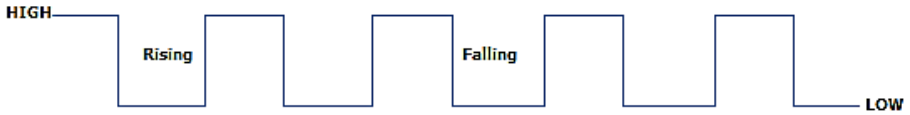


The storage elements are devices capable of storing binary information. Storage element mainly classified into Latches & Flip Flops.

Latches: storage elements that operate with signal levels (High or LOW). Latches are level sensitive devices.

Flip-flops: storage elements whose controlled by a clock transition (Rising or Falling). Flip-flops are edge-sensitive devices.

Clock signal: Square wave signal with adjustable frequency***.***

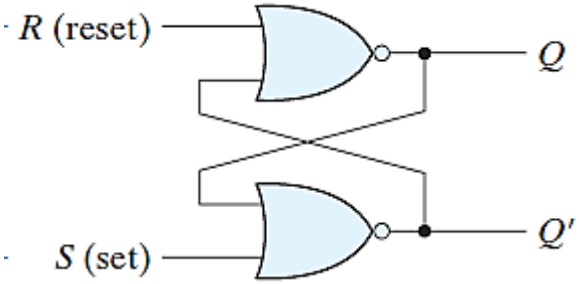


Timing diagram of clock pulses

Storage Elements

S-R Latch

The SR latch is a circuit designed with two cross-coupled **NOR gates** or two cross-coupled **NAND gates** and two inputs labeled S (set), R (reset) and two outputs $Q, \bar{Q}$.



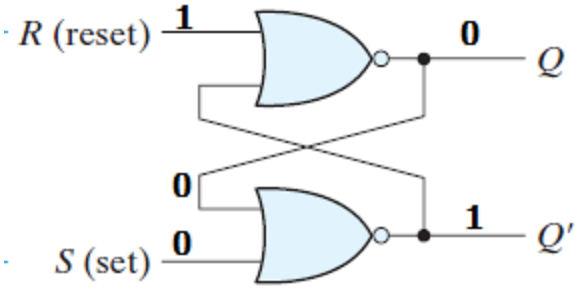
NOR gate Truth Table		
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Circuit Analysis

It can be seen from the **NOR gate Truth Table** that if one input (A) is equal to 1, the output is 0 regardless the value of the other input (B).

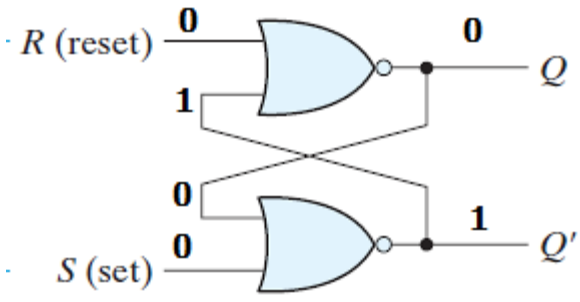
Case I

As $R = 1$, regardless the other input, the output of the top NOR gate (Q) is equal to 0. Then, this 0 is feed to the bottom NOR gate. According to the Truth table, if the inputs are (0,0), the output ($\bar{Q}$) is 1.



$S = 0, R = 1 \rightarrow Q = 0, \bar{Q} = 1 : Reset$

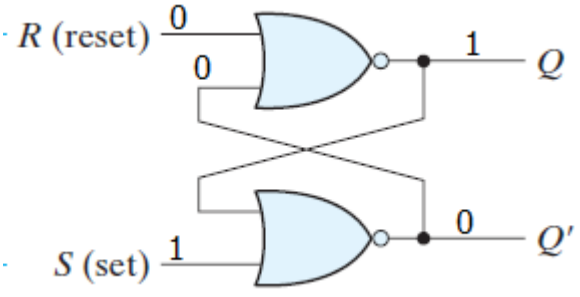
Now, if $S = 0, R = 0$. Then 1 is feed to the top NOR gate and hence the inputs will be (0,1). According to the Truth table, if the inputs are (0,1), the output (Q) is 0. This 0 is feed to the bottom NOR gate and the inputs will be (0,0). If the input is (0,0) the output ($\bar{Q}$) will be 1.



$S = 0, R = 0 \rightarrow Q = 0, \bar{Q} = 1 : Memory$

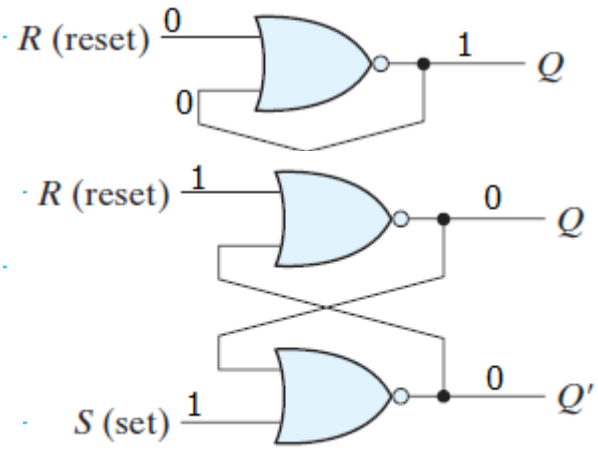
Case II

Similarly, As $S = 1$, regardless the other input, the output of the bottom NOR gate ($\bar{Q}$) is equal to 0. Then, this 0 is feed to the top NOR gate. According to the Truth table, if the inputs are (0,0), the output (Q) is 1.



$S = 1, R = 0 \rightarrow Q = 1, \bar{Q} = 0 : Set$

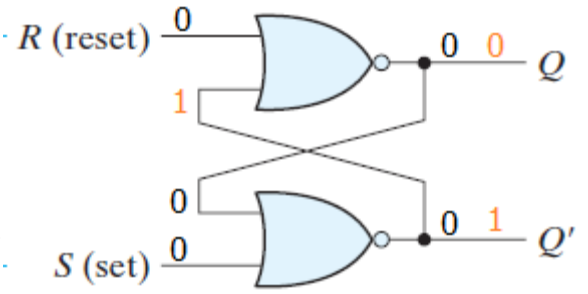
Case III



As $R\,\&\,S = 1$, regardless the other inputs, the outputs of the TWO NOR gates are equal to 0.

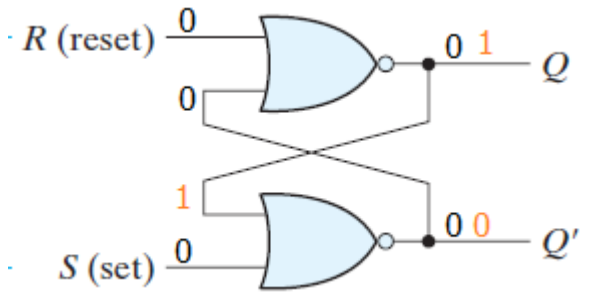
$S = 1, R = 1 \rightarrow Q = 0, \bar{Q} = 0 : Not\ Used$

Now, if $S = 0, R = 0$. Start the analysis from Q, then 0 is feed to the bottom NOR gate and hence the inputs will be (0,0). According to the Truth table, if the inputs are (0,0), the output ($\bar{Q}$) is 1. This 1 is feed to the top NOR gate and the inputs will be (0,1). If the input is (0,1) the output (Q) will be 0.



$S = 0, R = 0 \rightarrow Q = 0, \bar{Q} = 1 : Not\ Used$

Similarly, if we start the analysis from $\bar{Q}$ the output will be

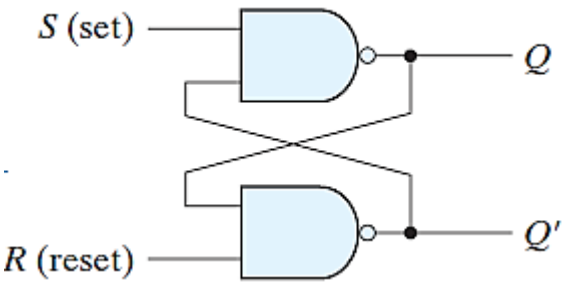


$S = 0, R = 0 \rightarrow Q = 1, \bar{Q} = 0 : Not\ Used$

These three cases can be summarized with the Truth Table

S	R	Q_{n+1}	$\overline{Q_{n+1}}$
0	0	Q_n (Memory)	$\overline{Q_n}$(Memory)
0	1	0	1
1	0	1	0
1	1	Not Used	Not Used

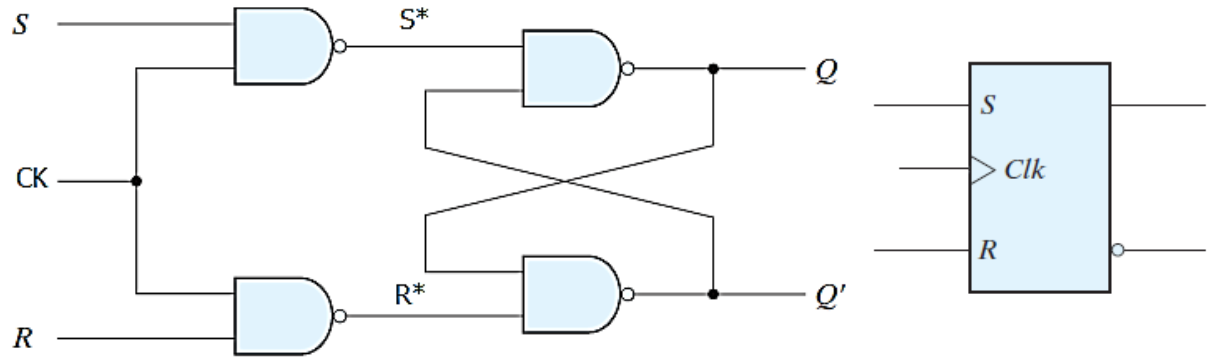
Also, SR lip flop can be designed by NAND Gate (HW)



S	R	Q_{n+1}	$\overline{Q_{n+1}}$
0	0	Not Used	Not Used
0	1	1	0
1	0	0	1
1	1	Q_n (Memory)	Q_n (Memory)

SR Flip Flop

It is basically a SR latch with a trigger control of operation (clock signal).



The Truth table of the SR Latch is

S*	R*	Q_{n+1}	$\overline{Q_{n+1}}$
0	0	Not Used	Not Used
0	1	1	0
1	0	0	1
1	1	Q_n (Memory)	Q_n (Memory)

$$S^* = \bar{S} + \overline{CK}$$

$$R^* = \bar{R} + \overline{CK}$$

The Truth table of the SR Flip flop is

CK	S	R	S*	R*	Q_{n+1}	$\overline{Q_{n+1}}$
0	X	X	1	1	Q_n (Memory)	$\overline{Q_n}$ (Memory)
1	0	0	1	1	Q_n (Memory)	$\overline{Q_n}$(Memory)
1	0	1	1	0	0	1
1	1	0	0	1	1	0
1	1	1	1	1	Not Used	Not Used

Characteristic Table

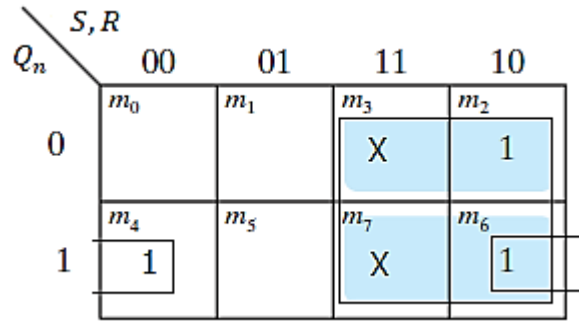
Table that defines the next state Q_{n+1} (the state that results from a clock transition) as a function of the inputs and the present state Q_n.

The characteristic table of SR flip flop has 3 inputs (S, R, Q_n) and one output (Q_{n+1})

Q_n	S	R	Q_{n+1}	
0	0	0	0	Memory

0	0	1	0	Set
0	1	0	1	Reset
0	1	1	X	Not Used
1	0	0	1	Memory
1	0	1	0	Set
1	1	0	1	Reset
1	1	1	x	Not Used

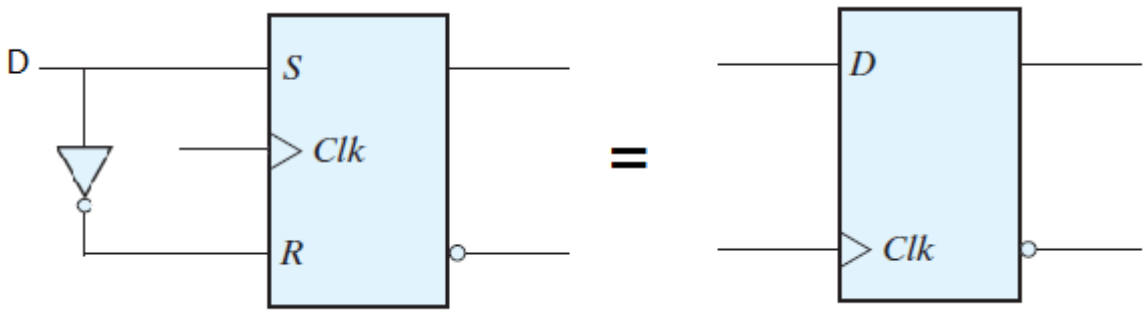
The function Q_{n+1} can be found using K-Map



$$Q_{n+1} = S + Q_n \bar{R}$$

D Flip Flop

From the truth table of SR flip flop, we can see that If I want to store 0, we need to give S = 0 & R = 1. Similarly, if we want to store 1, we need to give S = 1 & R = 0. Therefore, S and R are complement of each other and thus they can be replaced by only one input D.



The Truth table of the D Flip flop is

CK	D	Q_{n+1}	$\overline{Q_{n+1}}$
0	X	Q_n (Memory)	$\overline{Q_n}$ (Memory)
1	0	0	1
1	1	1	0

In this case, we will never get the invalid state (1,1) because S and R are always complement of each other.

The characteristic table of D flip flop has 2 inputs (D, Q_n) and one output (Q_{n+1})

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

$$Q_{n+1} = D$$