Magnitude Comparator

A magnitude comparator is a combinational circuit that compares two numbers A and B and determines whether one number is greater than, less than, or equal to the other number.

1-bit magnitude comparator

Let us assume that the two input variables are A & B. The output of the comparison is specified by three binary variables that are whether A > B or A = B or A < B. The truth table of a 1-bit magnitude comparator is as follow

A	B	A > B	A = B	A < B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

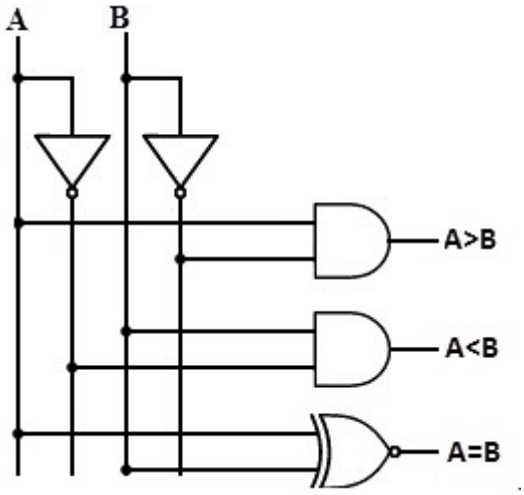
The output functions can be derived from the truth table

$A > B = A\bar{B}$

$(A = B) = \bar{A}\bar{B} + AB$

$A < B = \bar{A}B$

These functions are implemented by basic logic gates

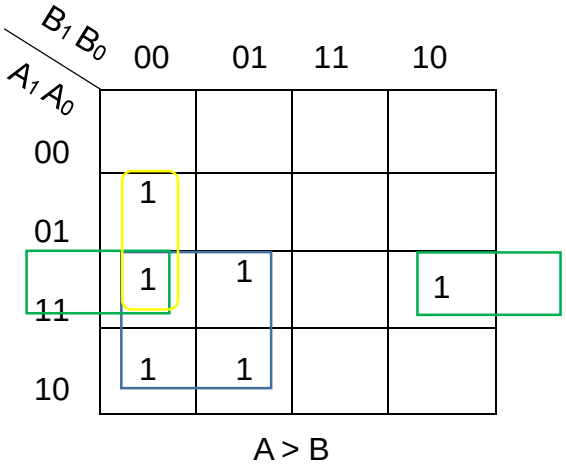


2-bit Magnitude Comparator

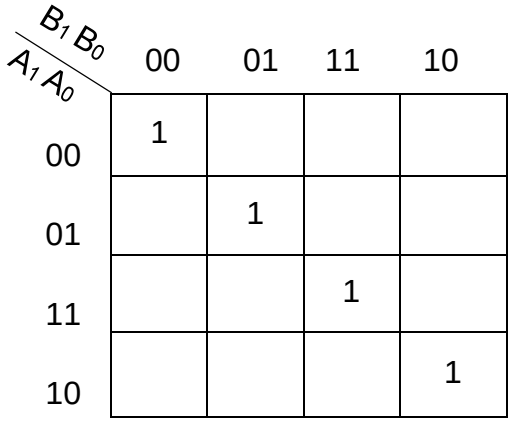
Following the same procedure, we can design a 2-bit magnitude comparator. The truth table of this circuit is shown below:

A_1	A_0	B_1	B_0	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

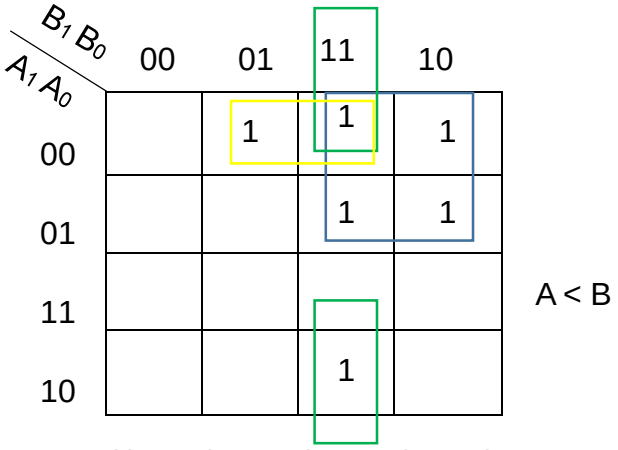
The k-maps of the three outputs are



A > B



A = B



A < B

Prepared by: Mohammed N. Y. Almaged

The three functions can be derived from k-map

$$A>B = A0\,\overline{B1}\;\overline{B0} + A1\,\overline{B1} + A1\;A0\,\overline{B0}$$

$$A=B: = \overline{A1}\;\overline{A0}\;\overline{B1}\;\overline{B0} + \overline{A1}\;A0\;\overline{B1}\;B0 + A1\;A0\;B1\;B0 + A1\,\overline{A0}\;B1\;\overline{B0}$$

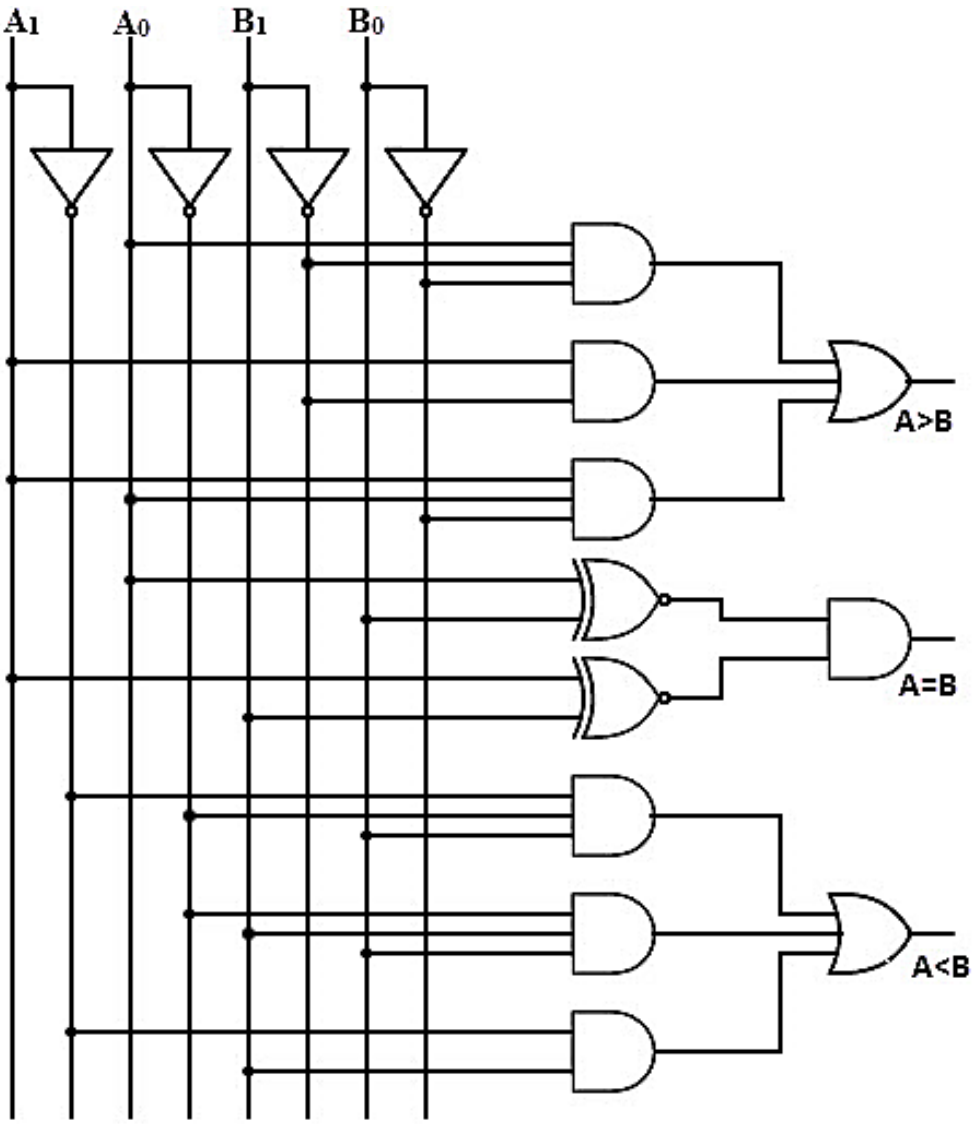
$$= \overline{A1}\;\overline{B1}\;(\overline{A0}\;\overline{B0} + A0\,B0) + A1\,B1\;(A0\,B0 + \overline{A0}\;\overline{B0})$$

$$= (A0\,B0 + \overline{A0}\;\overline{B0})\;(A1\,B1 + \overline{A1}\;\overline{B1})$$

$$= (A0 \oplus B0)'(A1 \oplus B1)'$$

$$A<B = \overline{A1}\,B1 + \overline{A0}\,B1\,B0 + \overline{A1}\;\overline{A0}\,B0$$

This can be implemented by the following logic gates



Multi-Bit Comparator

As the number of bits increases, it is obvious that the design process becomes more complex. However, multi-bit comparator can be designed by using 1-bit comparator with a set of logic gates.

Consider two numbers, A and B, with four digits each.

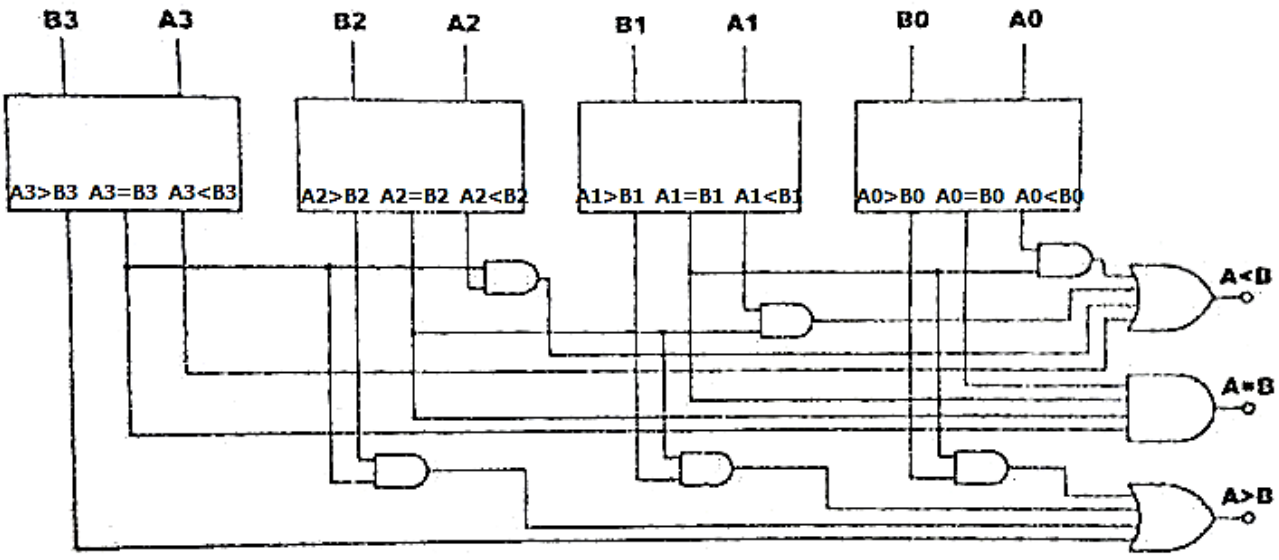
$A = A_3\, A_2\, A_1\, A_0$

$B = B_3\, B_2\, B_1\, B_0$

The two numbers are equal if all pairs of significant digits are equal. That is $A_3 = B_3$, $A_2 = B_2$, $A_1 = B_1$, $A_0 = B_0$

To determine whether A is greater or less than B, we inspect the relative pairs starting from the most significant position (MSB).

If the two MSBs are equal, we compare the next lower significant pair of digits. The comparison continues until we reach the last bit in the number (LSB).



Code Conversion – Part II

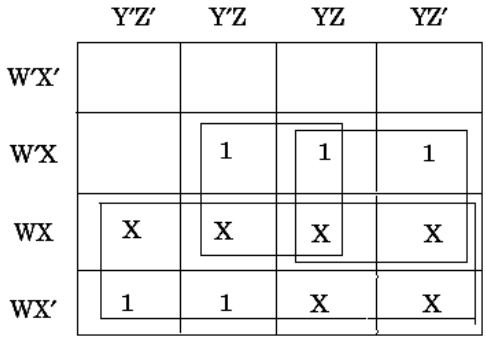
BCD to 2421 code

2421 code is a self-complementary code, that is, the 9's complement of the decimal number is obtained by changing the 1s to 0s and 0s to 1s. The 2421 code is the same as that in BCD from 0 to 4. However, it varies from 5 to 9.

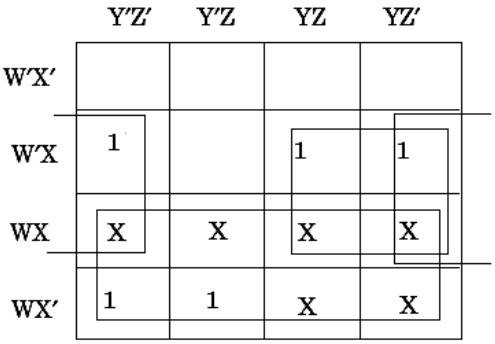
The Truth Table is as follow

Decimal Equivalent	Input varibles				Output variables			
	BCD code				2421 code			
	W	X	Y	Z	A	B	C	D
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	0	1	0	1	1	0	1	1
6	0	1	1	0	1	1	0	0
7	0	1	1	1	1	1	0	1
8	1	0	0	0	1	1	1	0
9	1	0	0	1	1	1	1	1

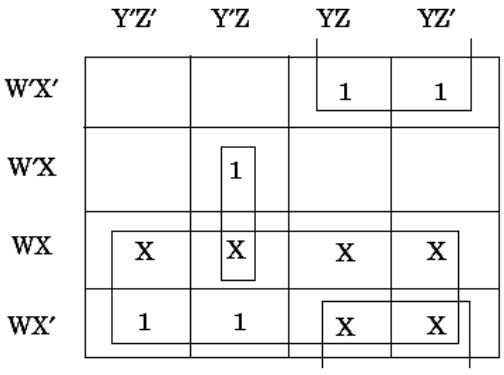
The K-Map of the 4-output variables can be obtained from the truth table



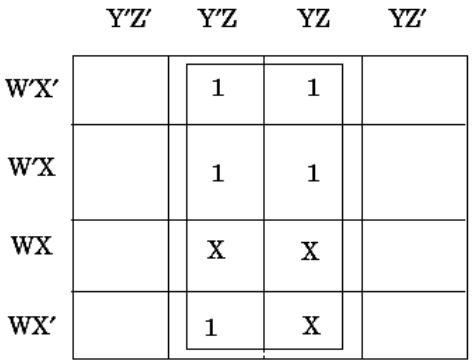
Karnaugh map for A.



Karnaugh map for B.



Karnaugh map for C.



Karnaugh map for D.

$A = W + XZ + XY$

$B = W + X\bar{Z} + XY$

$C = W + X\bar{Y}Z + \bar{X}Y$

$D = Z$

The logic diagram can be implemented using basic logic gates **(H.W)**