Programmable Logic Devices

- **Digital Electronic systems:**
  - Memory
  - Microprocessor
  - Logic Devices
    - Fixed Function Logic Devices.
    - Programmable Logic Devices.

Programmable Logic Devices

- **Advantages Programmable Logic Devices:**
  - Less board space.
  - Easy to change with rewiring.
  - Faster.
  - Less cost.

Programmable Logic Devices

- (PLDs) introduced in the mid 1970s.
- The idea: to construct logic circuits that were programmable.
- Microprocessors: can run a program but posses a fixed hardware.
- Programmability of PLDs was intended at the hardware level (reconfigured).

Programmable Logic Devices

- **PAL (Programmable Array Logic) PLA (Programmable Logic Array)**
- used only logic gates (no flip-flops), combinational circuits.

- **registered PLDs**: one flip-flop at each output; simple sequential functions.

- In the beginning of the 1980s, additional logic circuitry was added to each PLD output.
- Macrocell, contained (besides the flip-flop) logic gates and multiplexers.

Programmable Logic Devices

- Moreover, the cell itself was programmable, allowing several modes of operation.
- provided a ‘return’ (feedback) signal from the output of the circuit to the programmable array, which gave the PLD greater flexibility.
- This new PLD structure was called **generic PAL (GAL)**.

- **PALCE** (**PAL CMOS** Electrically erasable/programmable).

Programmable Logic Devices

- (**PAL**, **PLA**, **registered PLD**, and **GAL**/**PALCE**) are now collectively referred to as **SPLDs** (**Simple PLDs**).
- Today **GAL/PALCE** device is the only still manufactured in a standalone package.

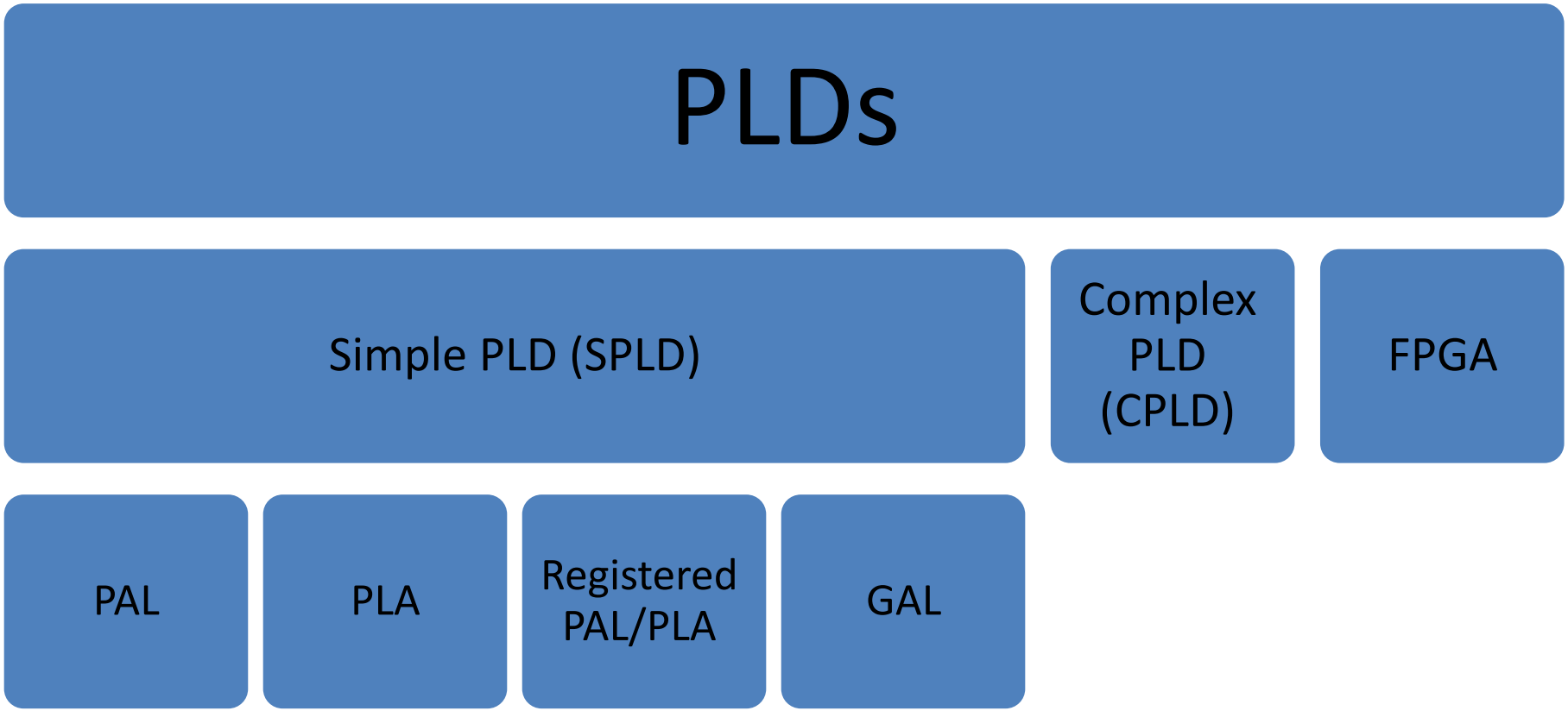
Programmable Logic Devices

- several **GAL** devices were fabricated on the same chip.
- This approach known as **CPLD** (**Complex PLD**).
- **CPLDs** are currently very popular due to:
- their high density,
- high performance,
- and low cost
- (CPLDs under a dollar can be found).

Programmable Logic Devices

- In the mid 1980s: **FPGAs** (**Field Programmable Gate Arrays**) were introduced.
- FPGAs differ from **CPLDs** in architecture, technology, built-in features, and cost.
- implementation of large size, high-performance circuits.

Programmable Logic Devices



SPLDs (Simple PLDs): PAL Devices

- Introduced by Monolithic Memories in the mid 1970s.
- programmable array of **AND gates**, followed by a fixed array of **OR gates**.
- based on the fact that any combinational function can be represented by a Sum-of-Products (**SOP**).

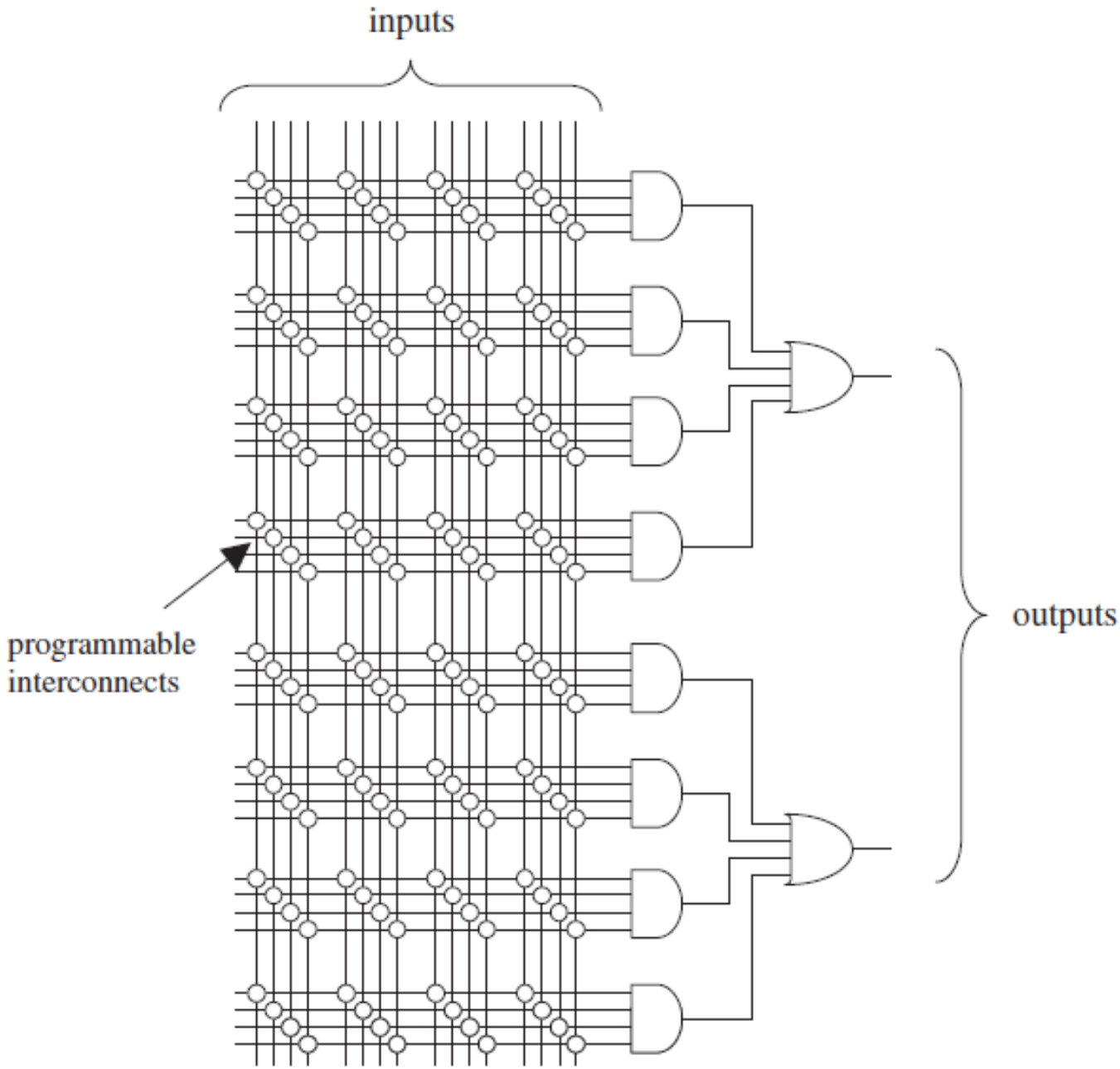


Figure A1
Illustration of PAL architecture.

SPLDs (Simple PLDs): PAL Devices

- The main limitation: allowed only the implementation of combinational functions.
- registered PALs launched end of the 1970s.
- These included a flip-flop at each output (after the OR gates in figure A1), allowing the implementation of sequential functions.

SPLDs (Simple PLDs): PAL Devices **PAL16L8**

- An example : **PAL16L8**
- **16** inputs and **8** outputs
- only **18 I/O** available, because it was a 20-pin DIP package
- 10 IN pins, 2 OUT pins, 6 IN/OUT pins, plus VCC and GND.

SPLDs (Simple PLDs): PAL Devices **PAL16L8**

- Its registered counterpart was the 16R8 chip (where R stands for Registered).

- fabrication technology :bipolar.
- 5 V supply.
- current consumption : 200 mA.

- maximum frequency : 100 MHz.
- programmable cells: of PROM (fuse links) or EPROM (20min UV erase time) type.

SPLDs (Simple PLDs): PLA Devices

- programmable array of **AND gates**, followed by a programmable array of **OR gates**.
- Advantage: was greater flexibility than PAL.
-
- However, higher time constants at the internal nodes lowered the circuit speed.

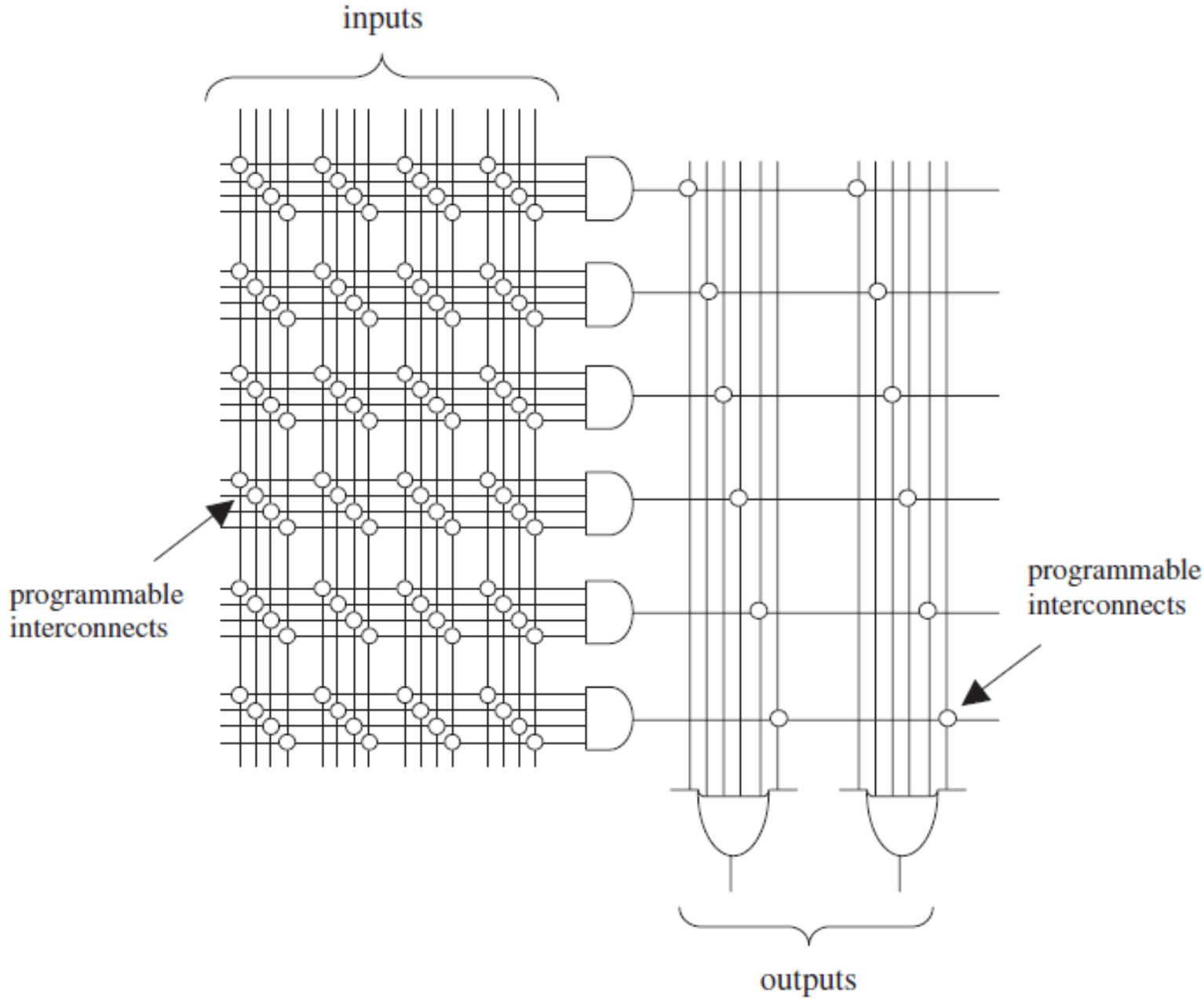


Figure A2
Illustration of PLA architecture.

SPLDs (Simple PLDs): PLA Devices

- example :Signetics PLS161 device.
- 12 inputs and 8 outputs,
- A total of **48** 12-input AND gates, followed by a total of **8** 48-input OR gates.
- At the outputs, additional programmable XOR gates were also available.