Ninevah University

College of Electronics Engineering

Electronic Department

A fully integrated CMOS realization of active inductor for RF applications

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M.Sc./ Thesis

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Supervised by

Assistant Professor

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Ninevah University

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A fully integrated CMOS realization of active inductor for RF applications

A Dissertation Submitted by

Jolyana Awni Oraha

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In

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Supervised by

Assistant Professor

Dr. Ahmad T. Younis

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Abstract

Radio Frequency (RF) circuits such as low noise amplifier (LNA), voltage controlled oscillators (VCO), and RF filters need inductors in their realizations. Passive and spiral implementations of the inductors have many limitations specifically when these RF circuits are designed and realized as integrated circuit. These limitations may include the generated noise effects and the occupation of large chip area.

This study presents an alternative active CMOS realization of inductors needed in most RF applications. This realization is based on the use of gyrator-c configuration suitable for IC fabrication. Various CMOS active realizations are presented and investigated, these may include the basic realization, topology with feedback resistor, active MOS transistor feedback, and the voltage divider type structure. Five topologies at operating frequency of 2.4 GHz is designed, optimized and simulated. A comparative study between these realizations is performed using a proper selected circuit design element values to obtain a proper active inductor performance parameters. The most important parameters that have to be investigated are quality factor, range of inductors value at specified operating frequency, the self-resonant frequency, power consumption, and chip area required.

Analytically, a design difficulty arise since performance parameters behave in a different manner with respect to design component values. Therefore an optimization technique is needed to deal with this problem. Genetic Algorithm (GA) method in MATLAB is used to obtain the optimum performance parameters, maximum inductance values, maximum quality factor, minimum power consumption, and minimum device dimensions. Applying GA to various active inductor topologies provides significant improvement in these performance parameters.

Advanced Design System (ADS) simulation package is used to verify the resultant designs that meet the required design specifications.

It is shown that the TF1 realization resulted in a significant improvement LQ=347.743 without GA and compared to other topologies and LQ=655.431 for TF1 with GA. In BPF, the best value of quality factor for TF1 (Q=27.188) and the best value of gain for VD (S_{21}= -0.157) . In HPF, the best value of quality factor for TF1 (Q=35.821) and the best value of gain for Rf (S_{21} = -1.288). It is shown that the use of passive feedback improves active inductor performance, however large passive resistance is required that is not suitable for IC fabrication.

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List Of Abbreviations

Abbreviations	Description
RF	Radio frequency
CMOS	Complementary Metal-Oxide Semiconductor
GA	Genetic Algorithm
BPF	Band Pass Filter
HPF	High Pass Filter
ADS	Advanced design System
MATLAB	Math Laboratory
NMOS	N-Channel Metal-Oxide Semiconductor
SP	Scattering Parameters
Q	Quality Factor
FAI	Floating Active Inductor
SOI	Silicon On Insulator
N	Number of turns
G	Gain
V_T	Threshold Voltage
SRF	Self-Resonant Frequency
L	Inductance
ES	Evolution Strategies
EP	Evolutionary Programming
IC	Integrated Circuit
Pc	Probability of Crossover
Pm	Probability of Mutation
C_{ox}	Capacitor per unit area of the gate oxide
K_n	NMOS Transistor Transconductance Parameter
T_{ox}	Oxide Thickness
W	MOS Transistor Gate Width
I_d	MOS Transistor dc Drain Current
TF1	Feedback MOS Transistor 1
TF2	Feedback MOS Transistor 2
VD	Voltage Divider
Chr	Chromosome
MOGA	Multi Objective Genetic Algorithm
F	Fitness Function
EDA	Electronic Design Automation
MEMS	Microelectromechanical systems
PGS	Patterned Ground Shield

List Of Symbols

Symbol	Description
ε_{ox}	Permittivity of the silicon oxide
ε_o	Dielectric constant for free space
BW	Bandwidth
S_{11}	Input reflection coefficient
S_{12}	Reverse voltage gain
S_{21}	Forword voltage gain
S_{22}	Output reflection coefficient
ρ	Resistivity of the material
ε_s	Dielectric constant for silicon
V_{GS}	D.c gate to source voltage
V_{Tn}	threshold voltage
μ_n	Electron mobility
C_{ox}	Oxide Capacitance per unit area
μ_p	Hole mobility
T_{ox}	Oxide Thickness
P	Power Consumption
V	Supply Voltage
R	Source/load Impedance
R_p	parallel resistance
C_s	Series capacitance
R_s	Series resistance
Cgs	Gate to Source Capacitor
g_m	Channel Transconductor
K'	Transconductance parameter
C_P	Parallel Capacitance
σ	Conductivity

Chapter 1

Introduction and literature review

1.1 Overview

Many Radio frequency (RF) circuits such as low noise amplifiers, voltage-controlled oscillators, and RF filters need inductors for realization. The inductor element plays an important role in radio frequency circuit design [1]. Passive and spiral implementations of the inductors have many limitations precisely when these RF circuits are designed and implemented as integrated circuits. Typically, standard structure realized active inductors provide high inductance value and high quality factor. Passive inductors provided a low quality factor, a small inductance values, and low self-resonant frequency, and required a large chip area in fabrication [2].

This thesis presents an alternative active Complementary Metal-Oxide (CMOS) Semiconductor realization based on the use of a gyrator-c configuration concept that is suitable for integrated circuit fabrication. A comparative study between various active inductor realization topologies is performed to obtain and improve active inductance performance. The most important parameters that have to be investigated are the quality factor, the range of inductors value at the specified operating frequency, and the self-resonant frequency.

An alternative modified MOS transistor structure and the voltage divider structure using MOS transistor are developed and modified to replace the passive feedback resistor that improves performance without requiring a large chip area for fabrication. Therefore, minimized transistors dimensions are required for minimum chip area, and also minimized current values are required to minimize power consumption.

Active CMOS realizations based on gyrator-C technique are modified and investigated. This includes Basic topology, feedback resistor structure, MOS transistor feedback realization, and the voltage divider structure were realized, designed, and simulated. A comparison of these topologies was made using active inductor performance parameters such as inductance value and quality factor.

With the development of technology, RF circuit design is becoming more difficult and complex. There have been various attempts to develop design and optimization schemes for RF circuit, these attempts require the experience and knowledge of the designer in order to find an optimal circuit design [3]. Although there have been efforts to create optimization tools for analog circuit design, they have mostly relied on the gradient search approach [4].

The genetic algorithm (GA) is a popular optimization tool for finding appropriate and optimal solutions. The basis for GA is biological evolution, in which the organisms that are best suited to a particular environment reproduce over a number of generations while others gradually disappear.

To meet the specified requirement and to improve performance, five different topologies for active inductor are designed, optimized, and simulated. The use of Genetic Algorithms in the design of the Band Pass Filter (BPF) and High Pass Filter (HPF) based on the use of active inductor resulted in a significant improvement in design performance and specifications. In addition to these capabilities, genetic algorithm is applied for minimizing power consumption and chip area while increasing inductor and quality factor. The LQ product factor is introduced as a comparison parameter, i.e. to maximize this factor since inductance value and quality factor.

Advanced design System (ADS) simulation methods are used to verify the operation of active inductor and to compare between the performance of these topologies at different design variables.

The application of the realized active inductor topologies are utilized to realize RF filter.

Band pass filter and High pass filter structures are designed and simulated at 2.4GHz using active inductor topology as an example of application.

1.2 Literature Survey

Active networks made up primarily of MOS transistors are CMOS active inductors. Resistors are occasionally utilized as feedback components to enhance the performance of active inductors. The aforementioned networks display an inductive characteristic in a specific frequency range under certain dc biasing conditions [5, 6].

Indeed, CMOS active inductors are increasingly being used in industries where an inductive characteristic is not only desirable but also necessary. Active inductors have several applications, including LC and ring oscillators, RF band pass filters, optical communications limiting amplifiers, and low-noise amplifiers [13, 7].

In 2010, Jafari et al. created analog integrated circuits using genetic algorithms. Additionally, it used genetic algorithms to determine the device sizes in an analog integrated circuit [8]. The work involved synthesis and optimization to speed up this type of circuit's development and improve precision.

In 2011, there was a suggestion for an improved inductor layout that features variable coil spacing and variable metal width based on an arithmetic progression format. On the format of geometric progression. The Q factor improvement for the inductor with the improved layout is primarily brought on by the suppression of eddy current loss by weakening the effect of current crowding in the center. For the novel inductor, the patterned ground shield (PGS) structure is used on the substrate with an optimized layout in order to achieve the highest Q factor possible. Within a 5% inductance variation, the novel inductor

outperforms the other four inductors in terms of Q factor, which will eventually help with RFIC design [9].

In 2012, Depending on the process rule, the metal wire of the spiral inductor is divided into a number of paths. Usually, the single path's width is less than or equal to the thickness of the skin. In order to increase the Q-factor and decrease the occupying area, the multipath technique can effectively reduce the proximity and skin effect [10].

In 2014, in order to lower the inductor's metal and substrate losses, a suspended spiral inductor was created on a silicon substrate using Microelectromechanical systems (MEMS) technology. It is possible to create an inductor of high quality and small size [11].

In 2015, it was presented a high-Q floating active inductor (FAI) that is appropriate for RF and microwave applications. Two cascaded pairs of highly linear capacitance gyrators, which offer a symmetric and reciprocal structure, are the foundation of the proposed FAI. The suggested FAI exhibits high quality factor, high linearity, and fully symmetrical two-port characteristics. A designed FAI prototype and an LC series band-pass filter have both been created as a proof-of-concept. The equivalent FAI's real part of impedance is extremely low at the operating frequency, offering a very high quality factor [12].

In 2017, Two grounded active inductor circuits were presented in this work. Each circuit contain only two MOS transistors and two biasing currents. This study bridge that gap by introducing a grounded inductance simulator based solely on MOS. These circuits require no additional

passive components and provide area reduction, low power supply, low noise, and power consumption [13].

In 2018, the designs present a thorough examination of gyrator-based CMOS active inductors. Several techniques are employed to improve the performance of active inductors [14].

In 2019, a novel design for a large active inductor with a wide tuning range is presented. The design circuit can be used as a large multiplication factor resistance and capacitance multiplier. The design circuit has many applications in analog filters and applications requiring the implementation of large time constant values in a small silicon area, as well as applications requiring a large active inductor [15].

In 2020, to improve quality factor, the performance of the proposed resistive feedback based cascode double feedback active inductor is investigated [16].

In 2021, a gyrator-C active inductor with a regulated cascode structure is proposed to improve noise performance. Furthermore, using a feedback resistor between positive and negative transconductances improved the proposed inductor's quality factor [17].

From a motivational standpoint, it is remarkable that not only the proposed active inductor ability is used control the inductance Q-factor, but also the fact that a filter can exhibit oscillatory behavior, analogous to a parallel RLC-circuit, due to their wide tuning capabilities.

1.3 Aim of work

The aim of this work is concerned with the design, realization, and optimization of CMOS Active inductor to improve circuit performance. In addition an RF filter application is investigated that based on active inductor to prove its proper operation, The following points may summarize the main objectives of work.

1- A modified topologies from basic structure counterpart are realized to increase inductance and quality factor values.
2- A comparative study is performed between various active inductor topologies in terms of its performance to obtain the proper topology.
3- To obtain the maximum inductance and quality factor for active inductor, Genetic Algorithm (GA) is applied as an optimization procedure.
4- To reduce the chip area (device dimensions) required for fabrication and to reduce the power consumption needed for active inductor topologies.
5- To prove the operation of the realized active inductor topologies, an RF filter (Band pass filter and High pass filter) are designed as an application examples for active inductor.

1.4 Thesis Organization

Six chapters make up the thesis, and the following is a description of its structure:

- Chapter two presents an theoretical background for active inductor and Genetic Algorithm.
- Chapter three involved design of CMOS active inductor at frequencies 2.4GHz.
- Chapter four involved design and optimization of CMOS active inductor at frequencies 2.4GHz using genetic algorithm.
- Chapter five design and optimization of BPF and HPF using CMOS active inductor at frequencies 2.4GHz.
- Chapter six includes the conclusions of this thesis and suggestions for future researches.

Chapter 2

Theoretical Background

2.1 Introduction

This chapter presents a theoretical background on CMOS active inductor design, analysis and topologies. In addition, an introductory and illustration of optimization technique is applied to improve the performance of active inductor, the Genetic Algorithm (GA) method is explained.

2.2 Passive inductor realizations

An inductor is a passive component that stores energy in its magnetic field. In electronic and power systems, inductors have a wide range of applications. Power supply, transformers, radios, televisions, radars, and electric motors [18].

Any electric current conductor has inductive qualities and can be considered an inductor. A practical inductor, on the other hand, is commonly fashioned into a cylindrical coil with several turns of conducting wire, as shown in Figure (2-1)

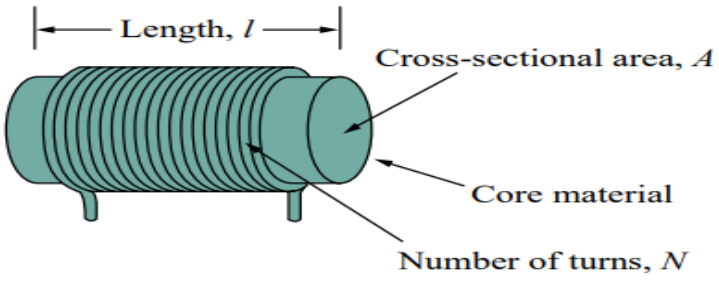


Figure (2-1) Typical form of an inductor.

When current is allowed to flow through an inductor, the voltage across the inductor is found to be directly proportional to the current's temporal rate of change.

$$V = L\frac{di}{dt} \quad \ldots\ldots\ldots\ldots(2.1)$$

V is the voltage

L is the inductance value

i: is the current

t : is the time

Inductance values are determined by its physical dimensions and construction. Formulas for estimating the inductance of various forms of inductors are developed from electromagnetic theory. For example, in the case of the inductor (solenoid) depicted in Figure (2-1)[18].

$$L = \frac{N^2 \mu A}{\ell} \quad \ldots\ldots\ldots\ldots(2.2)$$

Where N is the number of turns, ℓ denotes the length, A denotes the cross-sectional area, and μ is the core's permeability. It can observe this from eq. (2.2) that increasing the number of turns may increase inductance coil with a higher permeability as the core, increasing the lowering the coil's length or increasing its cross-sectional area [18].

Inductors are available in a variety of values and types. Inductance levels of typical practical inductors range from a few microhenrys (μH) in communication systems to tens of henrys (H) in power systems. Inductors can be either fixed or variable. The core material can be iron, steel, plastic,

or air. Inductors are also referred to as coils and chokes. Figure (2-2) depicts common inductors. Figure (2-3) depicts the circuit symbols for inductors using the passive sign convention [18].

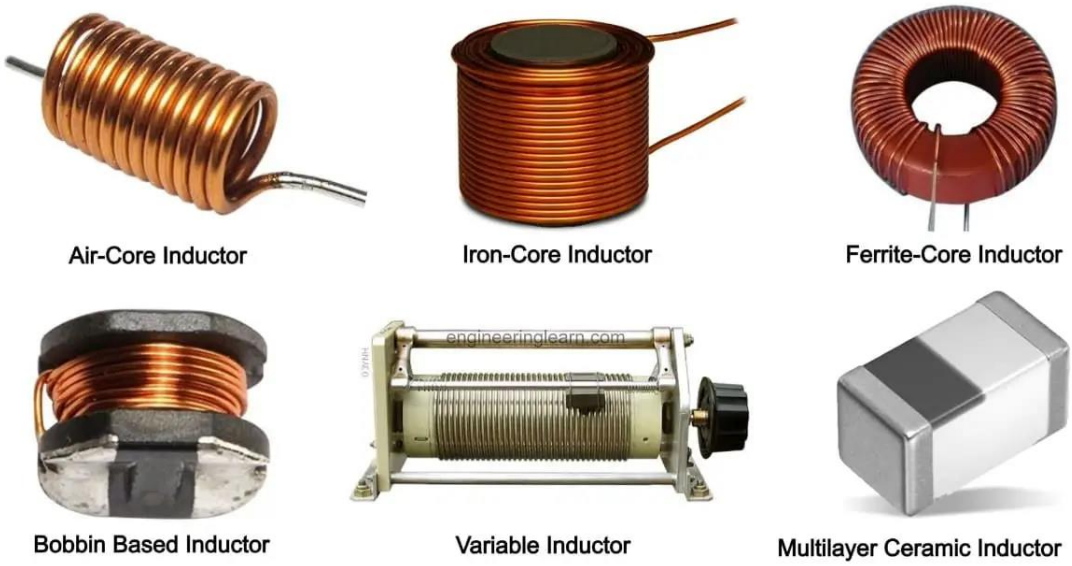


Figure (2-2) Various types of inductors.

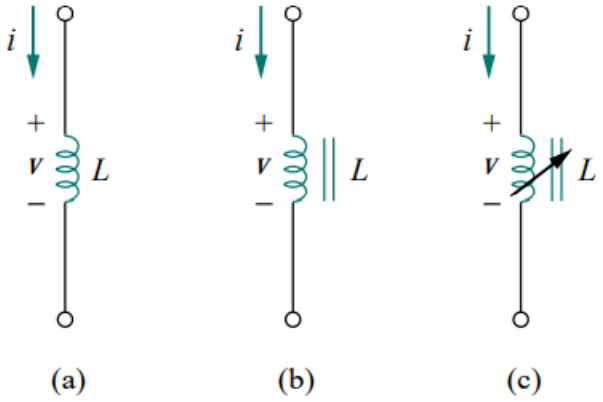


Figure (2-3) Circuit symbols for inductors: (a) air-core, (b) iron-core, (c) variable iron-core.

2.2.1 Spiral inductor realization

When a spiral inductor on silicon runs at high frequency, two substrate-related energy loss mechanisms occur. The first is created by the transient electric field radiating from the inductor metal strips, while the second is caused by the quasi-TEM EM wave propagating from the inductor core. As the electric field penetrates the silicon substrate, ohmic dissipation occurs. Furthermore, the EM wave's time-varying magnetic field would produce an eddy current in the lossy substrate, leading to energy dissipation. As a result, the inductor's stored energy is subtracted, and its value decreases. Until now, great work has been expended in reducing substrate loss, such as the micromachining technique or the silicon-on-insulator (SOI) structure [19, 20]. However, most procedures include a lengthy procedure. The resistive losses in the spiral coil and the substrate losses limit the inductors' quality factor (Q). Three major loss mechanisms degrade the quality factor of on-chip inductors: energy loss due to the spiral's series resistance, electric coupling between the spiral and the substrate, and magnetically induced eddy currents [21].

A typical layout and model for a spiral inductor can be shown as given in Figure (2-4) respectively.

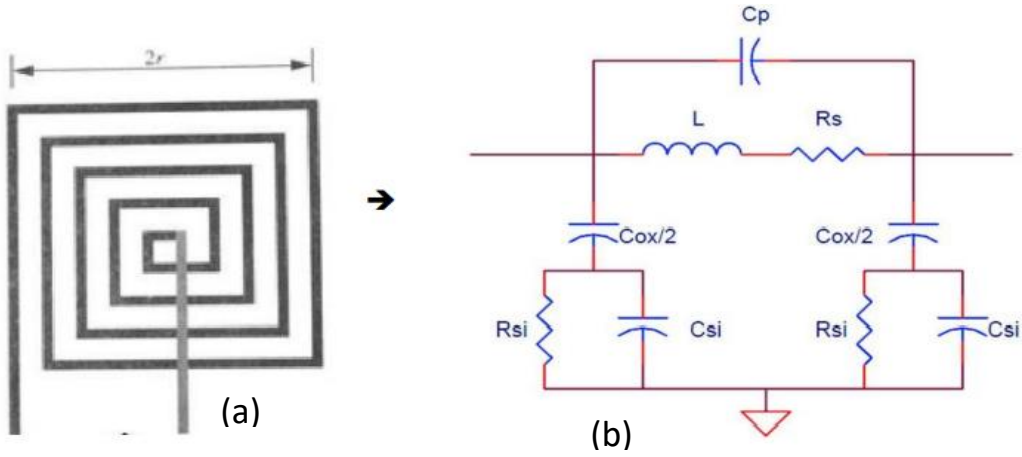


Figure (2-4):(a) Typical layout of a spiral inductor, (b) Typical model of spiral inductor.

$$R_s = \sqrt{\frac{2}{\omega \mu_o \sigma}} \quad \ldots\ldots(2.3)$$

$$C_{ox} = W.L.\frac{\varepsilon_{ox}}{t_{ox}} \quad \ldots\ldots.(2.4)$$

Where

R_s is the Series resistance, ω is the self-resonant frequency, σ is the conductivity, C_{ox} is the oxide capacitance per unit area, W is the width, L is the length, ε_{ox} is the permittivity of the silicon oxide and t_{ox} is the oxide thickness[21].

Assuming a ground (GND) connection, A parallel equivalent model is get as shown in Figure (2-5), to the model of spiral inductor (given in Figure(2-4)) [21]:

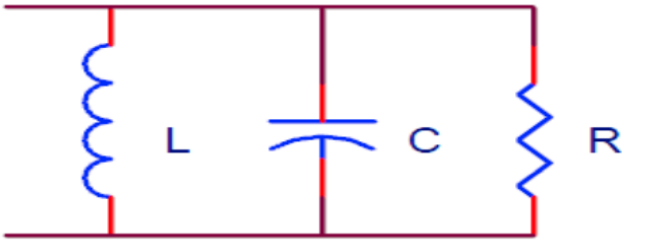


Figure (2-5) Parallel equivalent model of spiral inductor.

2.3 Realization of CMOS Active Inductor

An alternative form that replaces the spiral inductor to avoid noise and space in integrated circuit realization is the active realization of inductor.

Active networks primarily made up of MOS transistors are referred to as CMOS Active Inductors .

To enhance the performance of active inductors, resistors are frequently used as feedback components.

Active inductor displays an inductive characteristic in a given frequency range as a result of signal-swing restrictions and dc biasing conditions.

2.3.1 Characteristics of CMOS Active Inductor

- **Low silicon area:** Because CMOS active inductors are frequently implemented using only MOS transistors, and the inductance of the aforementioned networks is inversely proportional to the MOS transistor transconductances, CMOS active inductors have a negligible silicon consumption.

- **High inductance:** The larger the inductance can be obtained with the need of narrower transistor width. Furthermore, the inductance may be properly tuned by altering the dc biasing condition of the transistors synthesizing the inductor with a large inductance tuning range.
- **High Self-resonant frequency:** The pass band center frequency of an active inductor RF band pass filter is often set to the active inductor of the filter's self-resonant frequency.
- **High Quality Factor:** The quality factor of CMOS active inductors is defined as the inductors' ohmic loss, which is mostly caused by the inductors' finite output resistance of the transconductors. [22]

  The quality factor depends on the frequency ratio to resonator bandwidth [23].

  $Q = \frac{f_r}{\Delta f}$ …….(2.5)

  $Where\ f_r\ is\ the\ resonant\ frequency\ and\ \Delta f$ is the bandwidth. Other common definition of Q is given in equations below [24]:

  $$Q = 2\pi \times \frac{Energy\ stored}{Energy\ dissipated\ cycle}$$…….(2.6)

  $$Q = \frac{X_l}{R}$$…….(2.7)

  X_L represent reactance of inductor, when R represent the total inductor equivalent resistance.

- **Gain**

It is defined as the ratio between the output and the input signal, and is often defined as decibels [25].

$$\text{Voltage Gain} = 10\log \frac{\frac{V_{out}^2}{R_{out}}}{\frac{V_{in}^2}{R_{in}}} = 20log\ \frac{V_{out}}{V_{in}} \quad \text{.....(2.8)}$$

Power gain is a measure of an Active Inductor ability to amplify signal power, measured by the ratio of the signal output to signal input power. Power gain is usually defined in terms of decibel (dB) on a logarithmic scale [26].

- **Power Dissipation**

With technology scaling down the need for integrated circuits that consume less power becomes more significant. However, since the supply voltage is reduced, the available voltage may become too small [27].

- **Scattering Parameters**

S-parameters play an important role in RF communication systems design due to the fact that usual open and short circuit measurements are no longer applicable at radio frequencies. S-parameters are the best way of describing those two-port network parameters. The scattering parameters, or S-parameters, relate incident voltages and reflected waves through the scattering matrix, at n-ports, as shown in eq. (2.11).[28]

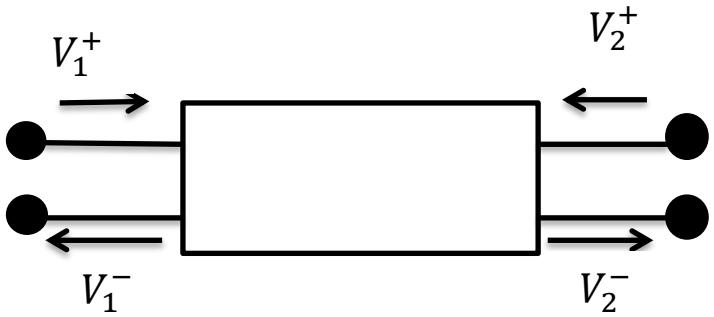
$$\begin{bmatrix} V_1^- \\ \dots \\ V_n^- \end{bmatrix} = \begin{bmatrix} S_{11} & \dots & S_{1n} \\ \dots & & \dots \\ S_{n1} & \dots & S_{nn} \end{bmatrix} \begin{bmatrix} V_1^+ \\ \dots \\ V_n^+ \end{bmatrix} \text{.....(2.9)}$$

Where Vi is the voltage amplitude at port I and the signal, positive and negative sign are the incident and the reflected waves are related respectively. Through the equation specific S-parameter can be determined:

$$S_{ij} = \frac{V_i^-}{V_j^+} \text{ .....(2.10)}$$

This mean that the S-parameter S_{ij} can be determined as the ratio between the reflected wave voltage at port I and the incident wave at port j when the other ports are switched off with the corresponding load to avoid reflections[28].

- S_{11}-Input reflection coefficient
- S_{12}-Reverse voltage gain
- S_{21}-Forword voltage gain
- S_{22}-Output reflection coefficient



Figure(2-6) Incident and reflected waves in a two port network.

2.4 Integrated Components fabrication:

The practical steps for creating integrated component devices are covered in this section. The integrated resistor, capacitor, inductor, and MOS transistor are among the parts needed to implement active inductors in integrated circuits.

2.4.1 Integrated resistor

A resistor in integrated technology is constructed from a thin resistive layer strip [29, 30]. Its typical construction shown in Figure (2-7): two ohmic contacts link a lengthy sheet of resistive material to metal terminals.

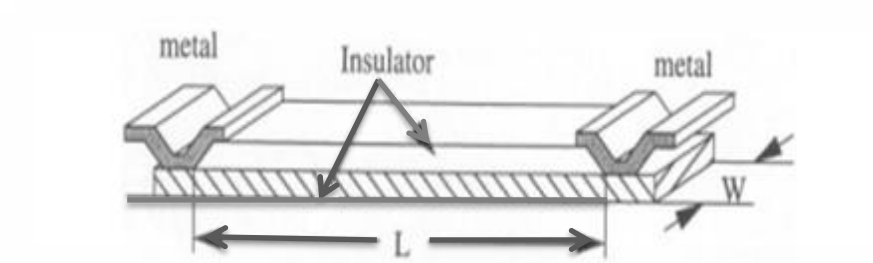


Figure (2-7) Typical integrated Resistor

Equations (2.11), which is provided below, is the general equation that connects a material's uniform resistivity and geometry (assumes rectangular geometry) to total resistance:

$$R = \rho \times \frac{\ell}{A} \text{.....(2.11)}$$

Where R is the resistance, ρ is the resistivity of the material, ℓ is the length and A is the area.

Figure 2-8-a illustrates this relationship between the resistivity of a material and its length in the current direction, width perpendicular to the current direction, and depth in ρ (Ω.μm). The layout and various dimensions of an integrated resistor are shown in Figure (2-8-b) [29].

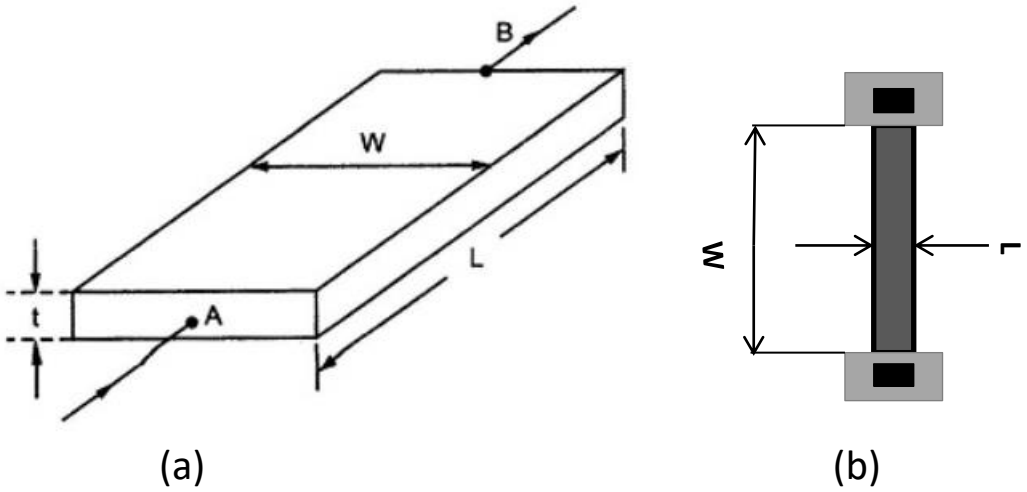


Figure (2-8) : (a) Resistor's dimensions, (b) Layout of an integrated resistor.

2.4.2 Integrated capacitor

In CMOS technology, a capacitor is built as a parallel plate structure. The electrodes are made possible by the technology's availability of conductive layers (metal, polysilicon, diffused layers). Silicon dioxide, polysilicon dioxide, or, in rare cases, Chemical vapor deposition (CVD) oxide provide insulation. In figure(2-9) the top plate is made of polysilicon, while the bottom plate is made of p+ or n+ diffusion. Usually, the thick oxide area's contribution to capacitance is disregarded.

The area of the capacitor is determined by the overlap of the two plates in the thin oxide region[29,31].

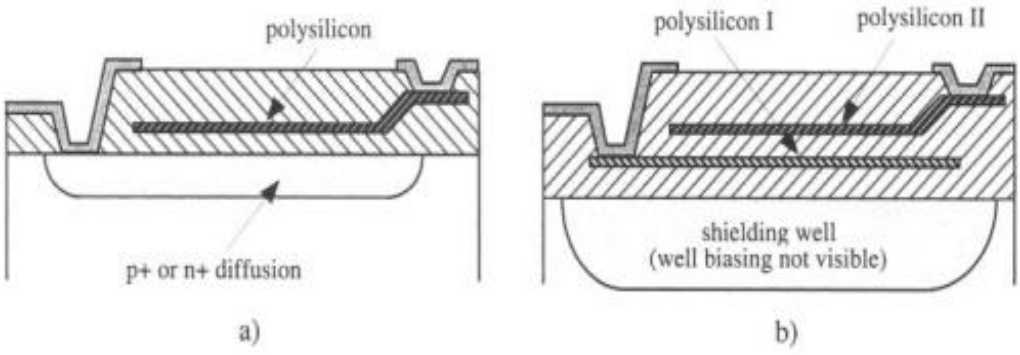


Figure (2-9) Two possible cross section of integrated capacitor

The bottom and top plates of the capacitor are created using two poly-silicon layers, as shown in Figure (2-9-b) [32]. Again, the capacitor can be isolated from the substrate by means of an optional well beneath the structure.

The value of the capacitor can be determined using the following equation [33]:

$$Cgs = \frac{\varepsilon_o \varepsilon_r}{t_{ox}} \times W \times L \quad \ldots\ldots\ldots (2.12)$$

Where ε_r are the permittivity of free space and ε_o is the dielectric constant for free space, t_{ox} is the oxide thickness, and W and L are the geometrical dimensions of the plates.

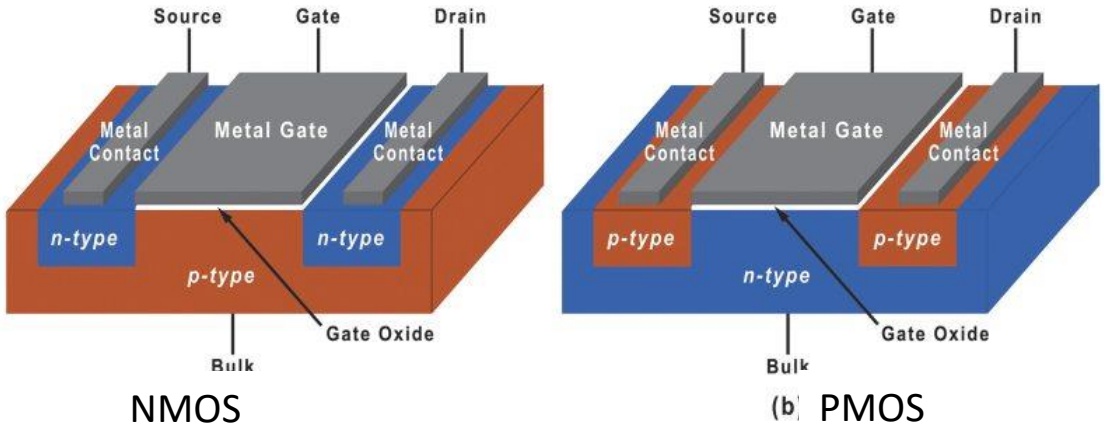
2.4.3 MOS Transistor fabrication:

The construction of MOS transistors is thought to be one of the key components in the realization of MOS active inductors; figure (2-10) shows how enhancement mode MOS transistors are put together. An NMOS transistor's structure starts with a P-type structure with high resistivity. Two N-type low-resistance regions are diffused into the substrate, as seen. A layer of silicon dioxide insulation is then applied to the structure's exterior. An insulating layer of silicon dioxide oxide has holes drilled into it. To make contact with the N-regions (source and drain), holes are drilled into the oxide layer. The oxide layer is then covered with a metal contact to allow for contact from source to drain. This metal area is connected by the gate terminal [31].

A conductive path is made from the source to the drain using the gate. The gate area, oxide layer, The capacitor is made up of a capacitor and a semiconductor channel. The gate area is located on the top plate, the P-Substrate is located on the bottom plate, and silicon dioxide acts as the dielectric.

As a result, a MOS capacitor is created, and the metal plate becomes positively charged when a positive voltage is applied to the gate. On the top of the semiconductor surface, a negative electron charge is created by this positive charge [33].

In the region below the oxide becomes an N-type semiconductor region as the gate positive voltage rises due to the P-type semiconductor's ability to repel holes. Current can now move through this induced N-channel from source to drain by biasing the drain positively in relation to the source[29,34].



(a)MOS structure

(b) MOS symbol

Figure (2-10) (a) Structure of the enhancement mode transistor for NMOS and PMOS transistor (b) symbols.

The lowest gate voltage value at which drain current starts to flow is known as the threshold voltage (VT). Similar to an N-channel enhancement mode MOSFET, a P-channel enhancement mode MOSFET is constructed, with the exception that all P and N regions are switched [29, 34].

2.5 CMOS Fabrication

CMOS fabrication can be done in a variety of ways. P-well, N-well, twin-tub, and silicon-on-insulator processes are examples. CMOS structures are made up of n-type substrates on which P-devices can be formed using appropriate masking and diffusion to accommodate the n-type substrate [31, 35].

The P-well in the parent substrate functions as a substrate for the n-device. Electrical barriers separate the two zones. Connect the N-substrate to the circuit's highest positive voltage (VDD) to establish a reverse between the N-substrate and source in order to prevent the body effect. This will set Voltage between source and bulk (V_{SB}) to zero for any PMOS transistors in the circuit. The source in NMOS transistors is simply connected to the P-well region.

MOS Transistor Theory

Figure (2-11) illustrates a typical N-channel drain characteristics curves. According to the Id-V_{DS} characteristics curves, there are three operational regions [33].

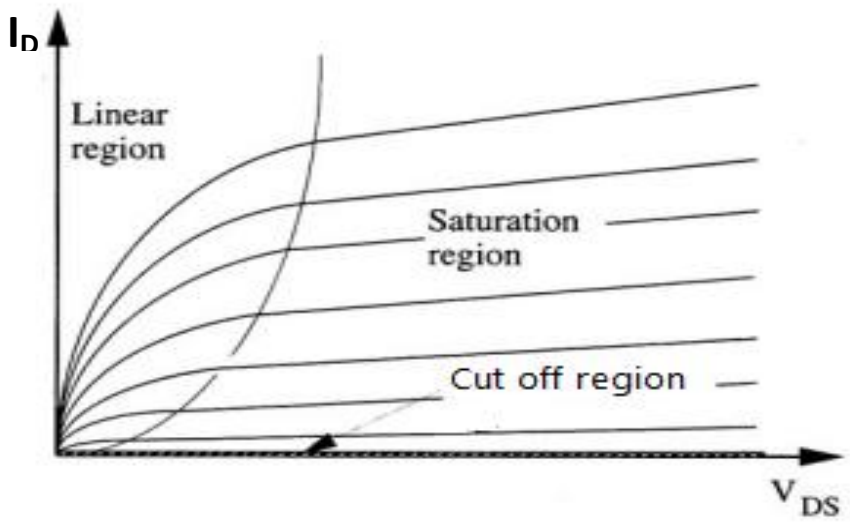


Figure (2-11) $I_d - V_{DS}$ characteristics for n-channel Transistor.

As shown from the figure above, these regions are stated as follows:

1- Cut off region when $V_{GS} < V_T$

2- Saturation region when $V_{DS} > V_{GS} - V_T$

3- Liner region when $V_{DS} < V_{GS} - V_t$

The MOS transistor transconductance is at its maximum in the saturation region, making it ideal for analog operations. As a result, the MOSFET is frequently biased toward its saturation region, and this example will show how the analysis works. It does, however, apply equally to equipment running in the linear (i.e., non-saturated) operating range [31, 35].

The mathematical summary of the enhancement mode NMOS transistor's operation in the saturation region is given below [33, 34, 35].

The drain current I_D is given by:

$$I_D = \frac{K_n}{2} \times \left(\frac{W}{L}\right) \times (V_{GS} - V_{Tn})^2 \quad \ldots\ldots(2.13)$$

Where :

V_{GS} : D.c gate to source voltage.

V_{Tn} …Threshold voltage.

W, L … Device dimensions.

K_n … Device transconductance parameter (K_P, for PMOS)given as:

$K_n = \mu_n \times C_{ox}$ ……(2-14)

Where :

C_{ox} … Gate oxide capacitance per unit area.

μ_n … Electron mobility (for NMOS transistor).

μ_p … Hole mobility (for PMOS transistor).

The Transconductance g_m is defined mathematical as:

$$g_m = 2\sqrt{\frac{K_n}{2}\ x\ \left(\frac{W}{L}\right) x\ I_D} \qquad \ldots\ldots(2.15)$$

2.6 Lossless single-ended gyrator-C active inductor

Active inductor is basically composed of two transconductors connected in series. As shown in Figure (2-12), the gyrator-C network is formed when one of the gyrator's ports is terminated by a capacitor. A gyrator-C network is considered to be lossless when both the input and output impedances of the network's transconductors are infinite and their transconductances are constant [5].

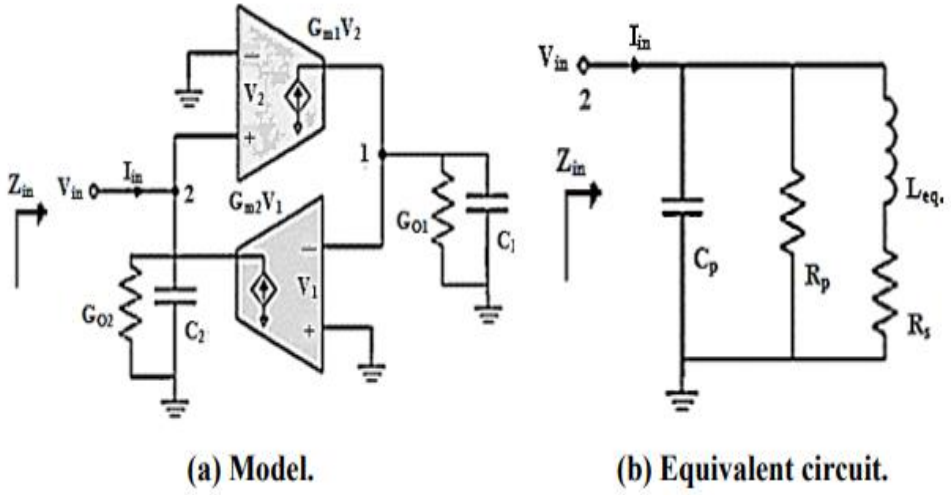


Figure (2-12) Lossless single-ended gyrator-C active inductor

The admittance to the gyrator-C network can be obtained to be:

$$Y_{in} = \frac{1}{Z_{in}} = \frac{I_{in}}{V_{in}} = SC_2 + G_{O2} + \frac{1}{S\left(\frac{C_1}{G_{m1}G_{M2}}\right)+\left(\frac{G_{O1}}{G_{m1}G_{m2}}\right)} \quad \text{……..(2.16)}$$

Equation (2.16) can be represented and modeled by an RLC network that is shown in Figure (2-12)-b, where:

$$R_p = \frac{1}{G_{O2}} \quad \text{.....(2.17)}$$

$$R_S = \frac{G_{o1}}{G_{m1}G_{m2}} \quad \text{.....(2.18)}$$

$$C_P = C_2 \quad \text{.....(2.19)}$$

$$L_{eq} = \frac{C_1}{G_{m1}G_{m2}} \quad \text{.....(2.20)}$$

As a result of the presence of these parasites, inductor behavior occurs. As a result, the most important condition for approaching ideal behavior is to eliminate or reduce these parasites. Because of the existence of parasitic parallel resistance (R_p), parallel capacitance (C_p), and series resistance (R_s), the gyrator-C network acts similarly to a lossy inductor. To the minimization of the ohmic loss, maximization of Rp and minimization of Rs should be considered. However, the value of active inductor's is unaffected by the finite input and output impedances of the transconductors in the gyrator-C network .The self-resonant frequency (ω_o) of this active inductor is given by [5, 36]

$$\omega_o = \frac{1}{\sqrt{LC_P}} = \sqrt{\frac{G_{m1}G_{m2}}{C_1C_2}} \quad \text{.....(2.21)}$$

2.7 Basic Topology Active Inductor

A typical active realization of an inductor based on gyrator-C concept is shown in figure (2-13) .The positive transconductance is achieved by configuring transistor M_2 as a common drain . In a common source arrangement, M_1 realizes the negative transconductance.

M_1 and M_2 must be biased to operate in active region using two current sources I_1 and I_2 in addition to supply voltage V_{DD}. The performing of small signal analysis results in to an equivalent inductance and equivalent quality factor for the grounded inductor that are given in eqs. (2.22) and (2.23) [37].

$$L = \frac{C_{gs1}}{g_{m1}g_{m2}} \qquad \ldots\ldots(2.22)$$

$$Q = \frac{g_{m2}C_{gs1}}{g_{m1}C_{gs2}} \qquad \ldots\ldots.(2.23)$$

L is the inductance value

C_{gs1} is the Gate to source capacitance of transistor 1.

C_{gs2} is the Gate to source capacitance of transistor 2.

g_{m1} is the channel transconductor of transistor 1.

g_{m2} is the channel transconductor of transistor 2.

Q is the quality factor.

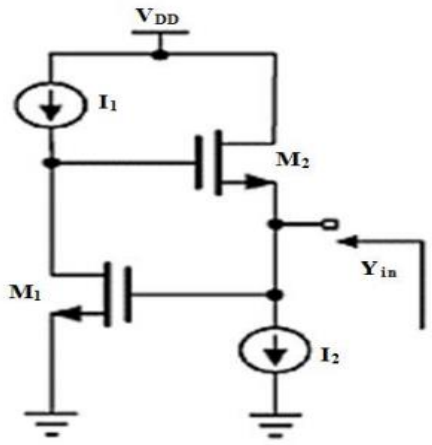


Figure (2-13) Schematic diagram of basic topology active inductor.

The self-resonance frequency (SRF) is therefore can be written as in eq. (2.24).

$$\omega_o = \sqrt{\frac{1}{C_P L_{eq}}} = \sqrt{\frac{g_{m1} g_{m2}}{C_{gs1} C_{gs2}}} \qquad \ldots\ldots\ldots(2.24)$$

The total power consumption is therefore given by eq. (2.25)

$P = (I_1+I_2)\ V_{DD}$ .....(2.25)

P is the power consumption

I_1 is the power consumption of transistor 1.

I_2 is the power consumption of transistor 2.

V_{DD} is the voltage source.

2.8 Genetic algorithms

As previously illustrated, active inductor performance depend on many design variable that require a numerical solution to obtain the appropriate performance, Genetic Algorithm (GA) is employed as an optimization tool to perform that.

2.8.1 Genetic algorithms Theory

Genetic algorithms, a subset of evolutionary algorithms, are an appealing tool for integrating with numerical instrument models to create an instrument design tool. Evolutionary algorithms are a type of search algorithm that is based on natural biological processes such as selection, crossover, and mutation [38]. Evolutionary algorithms are built from a population of individuals, each representing a set of problem parameters. Each person is given a score based on how well they perform in terms of an objective function (fitness function).

These individuals compete and evolve according to probabilistic rules that differ between available algorithms, but the basic idea is that better solutions have a higher chance of surviving and reproducing, with the overall quality of the population increasing with each successive generation and the entire population evolving towards an optimal solution[39].

Essentially, evolutionary methods seek a solution to a problem by applying principles and ideas derived from biological evolution. The evolutionary method is a type of search algorithm; one of its distinguishing features is that it is a blind search. They neither sample other solutions at random nor do they rely on gradient data or any knowledge of "nearby" solutions in the search space. Instead, natural evolutionary processes drive them[40].

An initial population of coded individuals is randomly selected for evolutionary algorithms; each one represents a search point in the area of potential solutions. Each person's goodness is measured using a fitness function that is derived from the optimization problem's objective function[41].

After that, using both random and probabilistic biological operations, the population evolves toward increasingly better search space regions. Because they each prioritized different biological operators as being essential to a successful evolution process, the three main evolutionary algorithms—Genetic Algorithms (Gas), Evolution Strategies (ES), and Evolutionary Programming (EP)—were developed independently of one another [41, 42].

Several advantages may be associated with using evolutionary algorithms in search/optimization problems:

- Optimizes with discrete or continuous variables.
- Don’t need derivative information.
- Searches at the same time from a wide sampling of the cost surface.
- Deals with a significant number of variables.
- Is suitable for parallel PCs.
- Optimizes variables that have extremely complex cost surfaces (they can leap from a minimum local level).
- Gives a list of optimal variables and not just a single solution.
- Can encode the variables so that the encoded variables are optimized.
- Works with data generated numerically, experimental data, or analytical functions.

However, there are some drawbacks to evolutionary algorithms. Because they are population-based, they necessitate numerous function evaluations, which can be a problem if the objective function requires a lot of computation. They can quickly approach the ideal solution, but it may take many generations for them to accurately evolve toward the solution [38]. They are also slow to complete.

Although evolutionary algorithms typically outperform algorithms created specifically for a single problem, they do so on a variety of challenging problems. When performing multi-objective optimization, dealing with noisy, multi-modal search spaces, and when traditional

search techniques fall short or are not yet available, evolutionary algorithms perform best [39].

2.8.2 Genetic Algorithms Operation

Using of genetic algorithms is described in general, along with some potential applications. The goal of doing this is to quickly acquaint the reader with the topic and lay a solid foundation for the subsequent, more in-depth explanation of the algorithm's components. This overview does not only address the issue of designing analogue IC circuits; it is presented in broad strokes[41].

Usually, a target characteristic is required to tell the GA what to look for. The target characteristic is the way the problem is stated that needs to be solved. It is a technique for outlining the conditions necessary for a workable resolution. The required cut off frequency, pass band attenuation, or a combination of several parameters may be the target characteristic when optimizing an analog circuit, such as a filter [40].

A population of potential answers to a given problem is monitored by genetic algorithms. These potential answers are typically encoded in a manner appropriate for presenting the solution to the issue. The fitness function being used determines how each member of this population is measured in order to calculate their fitness score. This rating reflects how effectively a particular person resolves the given issue [43].

The population is processed using a variety of genetic operations, of which the typical GA defines three types (selection, crossover, mutation). Based on their fitness score, the selection operator selects a certain number of individuals to move on to the following generation. Then, crossover, another genetic operator, is applied to some of these people. The primary method for guiding the search process and the primary purpose of GAs is crossover. Two people are picked, and they are split in some way. Two new offspring are created by combining the fragments of each parent, and both of them have traits from both parents.

The offspring of two fit parents will inherit characteristics from both. If those characteristics prove beneficial, the offspring will be even more fit. Otherwise, unfit offspring will be exterminated from the population. As a result, crossover is the primary means of guiding the blind search [38, 44].

Crossover is followed by the application of the last operator. This is the mutation operator, which randomly selects people and then modifies a subset of them[45].

Mutation is important because it allows new solutions to enter the population. Typical GA flowchart is shown in figure , this figure includes the main parts of Genetic Algorithm procedure (2-14) [45].

The three operators are used, and the result is the creation of a brand-new population. This will mainly consist of the fitter individuals from the original population or the descendants of mainly fitter individuals crossing over. There will be some mutated individuals in the new population[45].

The aim is for the overall fitness of each generation to increase as this loop is repeated. This cycle is continued until either the maximum number of generations is reached or a person is identified who offers a workable solution to the initial issue. Despite being created at random, the initial population may be subject to restrictions depending on the application[44].

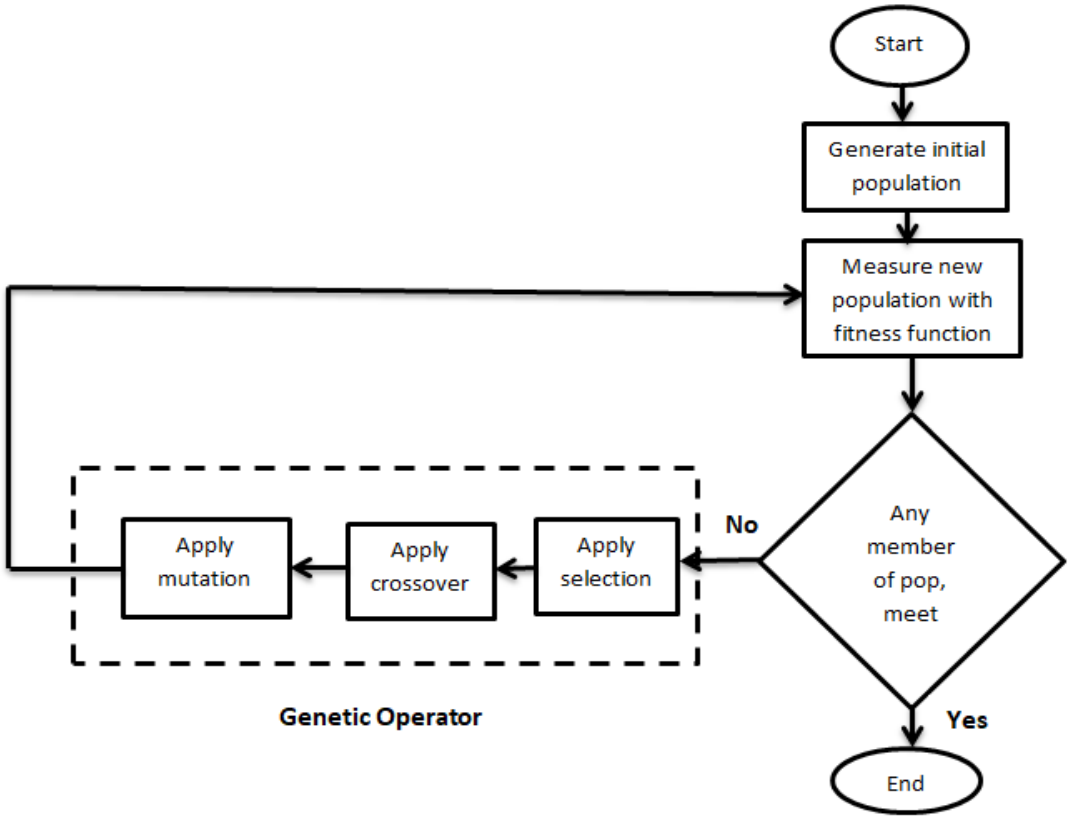


Figure (2-14) Typical genetic algorithm

The following paragraph presents a definition of various topics usually used in optimization tools in general.

2.8.3 Design Constraints

Constraints refer to all restrictions imposed on a design. Most designs require that certain functions be greater or less than a certain value. Conditions are also imposed on some variables. These conditions are expressed as constraints in the problem, which must be met by the design solution [46].

2.8.3.1 Feasibility

A feasible solution is one that meets all constraints. Obviously, the best solution is a feasible solution. Infeasible solutions are those that violate at least one constraint[47].

2.8.3.2 Implicit constraints

The design variables have an indirect influence on some constraints. They can't be expressed explicitly in terms of variables. These are referred to as implicit constraints [47].

2.8.3.3 Linear/Nonlinear constraints

Linear constraints are constraints functions that contain only first order terms of the design variables. Non-linear constraints are defined as having at least one term with an order greater than one [48].

2.8.3.4 Equality/ Inequality constraints

Equality constraints are limitations that need to be exact in order to be satisfied. Most restrictions call for a value that is "at least" or "at most" a particular value. These are constraints on inequality, and by definition, the set of solutions to problems with only such constraints is larger [46].

2.8.4 Genetic Operators

Following the selection of initial populations, genetic algorithms are run in a series of stages. Among these operations are the following:

2.8.4.1 Selection

Selecting two parents from the population to cross is referred to as selection. The next step after choosing an encoding is to decide how to perform selection, or how to pick people within the population who will have children for the following generation and how many children each of them will have. In order to ensure that their offspring are also fitter, selection aims to prioritize the population's fitter members.

For reproduction, chromosomes from the population are chosen as parents. How to select these chromosomes is the problem. According to Darwin's theory of evolution, only the strongest individuals survive to bear new offspring. According to their evaluation function, chromosomes are randomly chosen from a population in the selection method [49]. The likelihood that a candidate will be selected increases with the fitness function. The degree to which superior individuals are preferred is what is meant by selection pressure. The quality of people increases with selection pressure. The GA is motivated to raise population fitness over time by this selection pressure. The roulette wheel, rank, and tournament selection are just a few of the selection options available [50].

2.8.4.2 Crossover

When two parent solutions are combined through crossover, new offspring solutions can be produced. For the GA to function, the crossover operation is essential. In the search space, it serves as the GA's main source of direction. One can use single-point, two-point, multi-point, arithmetic, and uniform crossover operators, among other crossover operator types [45]. The cutting point is randomly selected in the case of a single point crossover, and as depicted in figure (2-15), the first section of parent A is spliced into the first section of parent B to produce the first new offspring, and vice versa for the second new offspring [51].

The parent solutions are divided into smaller pieces, which are then combined to create new offspring, as shown. It's hoped that the solutions will combine beneficial qualities from both parents and be better than either. This thesis makes use of the single point crossover. To increase genetic blending, it is possible to select two or more crossover points, but doing so can reduce performance [52]. The cutting point of both strings must be identical. This is required to maintain the strings' constant length. This fundamental crossover operation always produces two new offspring and always requires two parents. Crossover is applied probabilistically to a set of parent solutions. The crossover rate (Pc) is the likelihood that crossover will be applied to parents [53].

This rate predicts the number of chromosomes that will undergo crossover in the overall population.

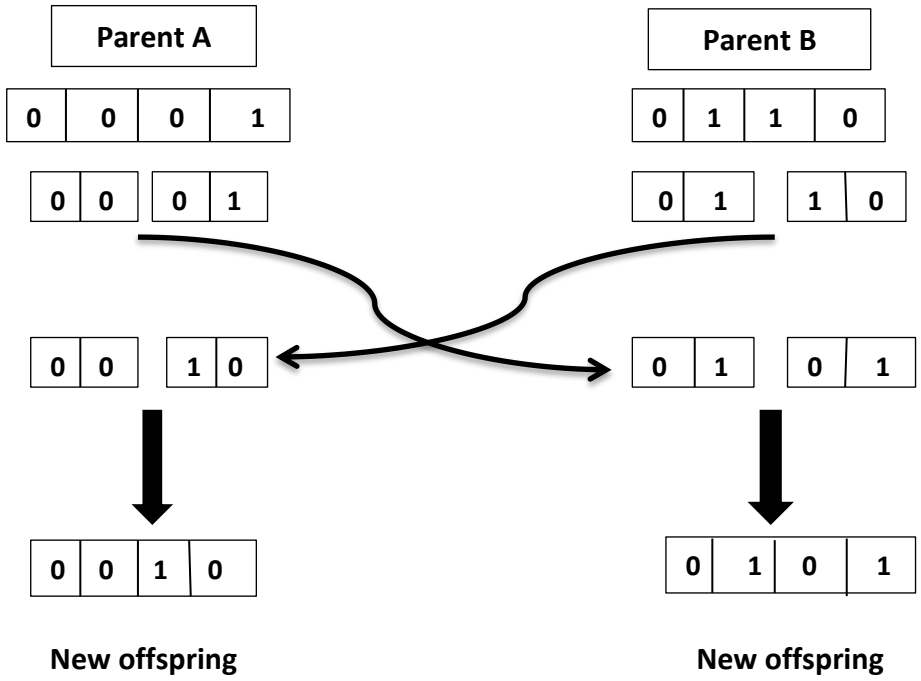


Figure (2-15) An example crossover of simple 4-bit binary strings.

2.8.4.3 Mutation

The search can be slightly widened thanks to the mutation operator. To put it simply, the operator modifies randomly chosen portions of random strings. It is utilized following crossover and is significant because it infuses the population with new "blood" or "genetic material" [48]. This enables the GA to evaluate a novel solution. The likelihood that a mutation will be passed down to parents is known as the mutation rate (Pm) [41, 45, 50].

When Pm is low, it is possible for the population to become dominated by extremely fit individuals, trapping the GA in a local minimum. When PM is elevated, the GA starts to act like a random search.

2.8.5 Fitness Function Formulation

A fitness function is an equation that is designed to define the quality of a solution. It is designed in such a way that better solutions outperform worse solutions in terms of fitness function value [53, 54]. The fitness function is very important in the selection process. The type of encoding used and the definition of the fitness function (objective function) are by far the most important parameters [43]. Although genetic algorithms are sufficiently robust to perform well in a variety of settings, chromosome encoding and the definition of a fitness function that accurately represents the problem of interest are required [4].

A quantitative evaluation of a chromosome's performance in addressing the pertinent issue is its fitness. The decoded chromosomes should be applied to the problem by the fitness function, and it should then return a result based on how well they perform. For example, if cutting costs associated with product development is the primary goal, the fitness function may describe a chromosome containing parameter values for design variables such as device parameters, component values, and so on, calculate the performance, and then return the performance as the fitness. Since the parameter being optimized can easily be used to represent the fitness, defining a fitness function for a problem where one parameter (specification, power, etc.) is optimized against multiple variables that represent this performance may be used [55].

Due to the necessity of optimizing several parameters (cost, performance, and time) for numerous design variables, multi-objective optimization problems are more challenging [47]. The fitness function needs to be created in a way that it only gives back a single parameter that results how well the chromosome optimizes each of these design factors. Another factor effecting the fitness function is the constraints. It is important to directly apply problem constraints to genetic algorithms because they contain abstract encodings of the problem parameters. Instead, a very low fitness value based on some sort of penalty function is automatically assigned to a chromosome if it constrains one or more parameters that go against a problem constraint [48,56].

Low fitness chromosomes will struggle to reproduce and will eventually be pushed out of the population. This method has the advantage that the strength of the constraints can be changed, allowing for some exploration outside of the constraints at a price [57].

2.8.6 Search Termination (Convergence Criterion)

The search is finally ended by the termination or convergence criterion. It is preferable to use user-defined convergence criteria that are more appropriate for the issue at hand.

Most termination methods lay in the following [58, 59]:

- When the desired fitness function is achieved, the fitness function has reached a reasonable value.
- Maximum generations: After the allotted number of generations, the genetic algorithms come to an end.
- Elapsed time: When a certain amount of time has passed, the genetic process will be finished.
- No change in fitness: If the population's best fitness does not change over a predetermined number of generations, the genetic process will come to an end.

Chapter 3

Active inductor design and simulation results

3.1 Introduction

This chapter presents a design, realization and simulation of Active Inductor topologies. To illustrate the design techniques and topologies, an operating frequency at 2.4GHz is used to be implemented on length of channel is 0.18μm CMOS process and design the parameters of structures. Advanced design system (ADS) is employed for the simulation purposes to verify the active inductor operation.

3.2 Mathematical Design of basic Topology Active Inductor

Since the basic structure performance is completely dependent on widths and currents W_1, W_2, I_1 and I_2, a typical design procedure mathematically starts with proper selection of current sources and device dimensions.

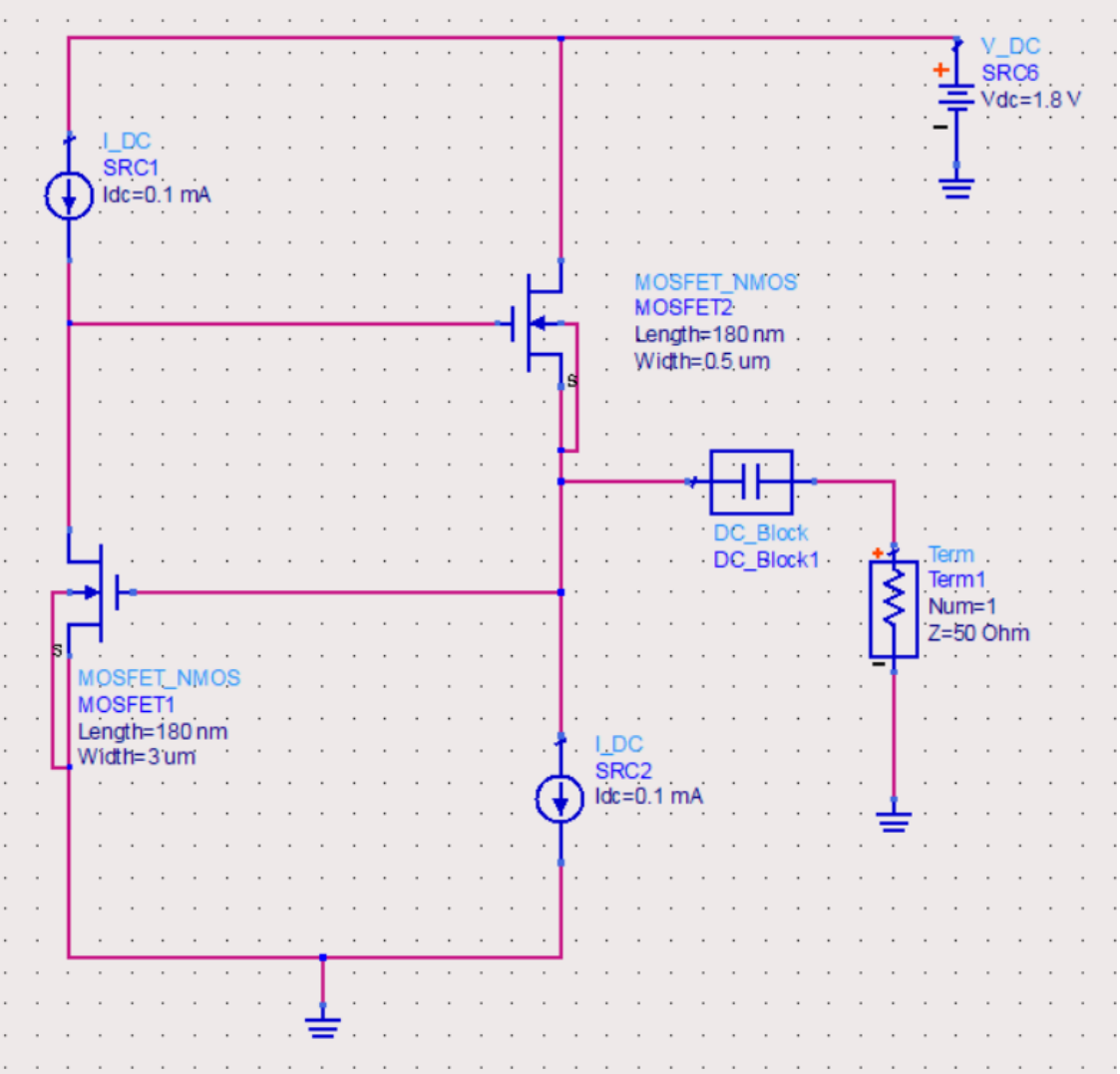


Figure (3-1) Basic Topology Active Inductor.

The design must meet the most important parameter values of the specified performance requirements. These could include the width MOSFET transistors W_1 and W_2, and the value of currents I_1 and I_2.

The design is performed to provide a parameter results on structure that can be fabricated using a fabrication process of 0.18μm and the operating frequency is be 2.4GHz.

Different parameter values are properly selected to illustrate the design variation according to variation of these variables.

As a case study the following design variables are selected as follow:

V_{DD}=1.8 V, W_1=3μm, W_2=0.5μm, I_1=0.1mA, I_2=0.1mA.

The process parameters for a 0.18μm process are listed as :

$\mu_o=288\times10^{-4}$ m^2/VS, $Tox=4.1\times10^{-9}$, $\varepsilon_o=8.854\times10^{-12}$, ε_r=3.9 for Sio_2,

$C_{ox} = 7.7$.

- Transconductance (g_{m1} and g_{m2}) of MOSFET1 and MOSFET2 (M_1 and M_2) calculated to be :

  $g_{m1} = \sqrt{2 \times \mu_n \times C_{ox} \times \frac{W_1}{L} \times I_{d1}}$ = 0.86 mS, and

  $g_{m2} = \sqrt{2 \times \mu_n \times C_{ox} \times \frac{W_2}{L} \times I_{d2}}$ = 0.35 mS

- The Gate to source capacitor C_{gs} is then calculated as:

  $C_{gs1} = \frac{2}{3} \times C_{ox} \times W_1 \times L$ = 2.772 PF, and

  $C_{gs2} = \frac{2}{3} \times C_{ox} \times W_2 \times L$ = 0.462 PF

- The values of resultant simulated inductance value for the above design variables is given as:

  $L = \frac{C_{gs1}}{g_{m1} \times g_{m2}} = 9.2$ nH

- And the corresponding quality factor is also determined to be:

  $Q = \frac{g_{m2} \times C_{gs1}}{g_{m1} \times * C_{gs2}} = 2.4$

- The power dissipation is then calculated to be:

  $P_D = V_{DD}(I_1 + I_2) = 0.36$ mW

To verify the operation of the active inductor operation under these design variables, an advanced system design (ADS) simulation package is now used to show that the design results satisfy the specified performance.

Figure(3-2) and figure(3-3) illustrate the ADS simulation results of inductance an quality factor respectively.

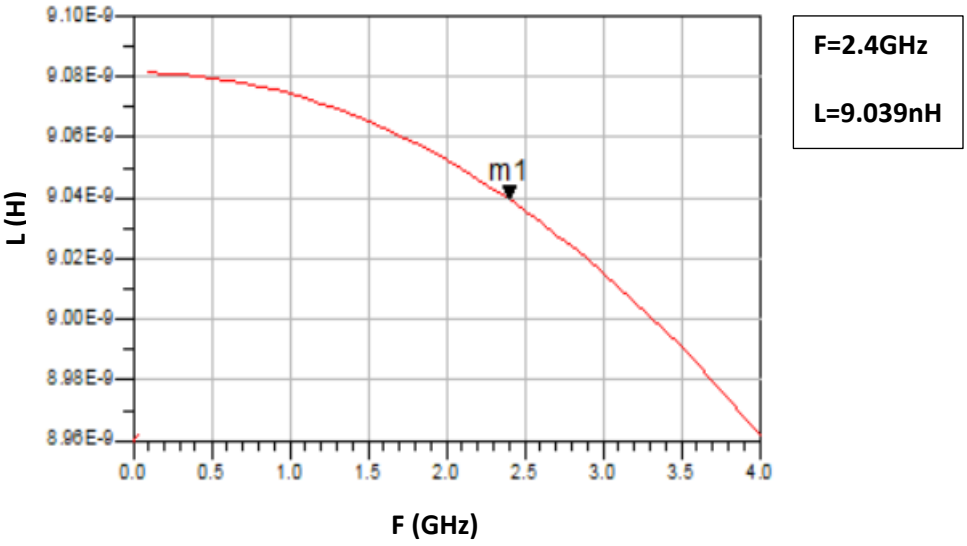


Figure (3-2) Inductance value of Basic Topology Active Inductor.

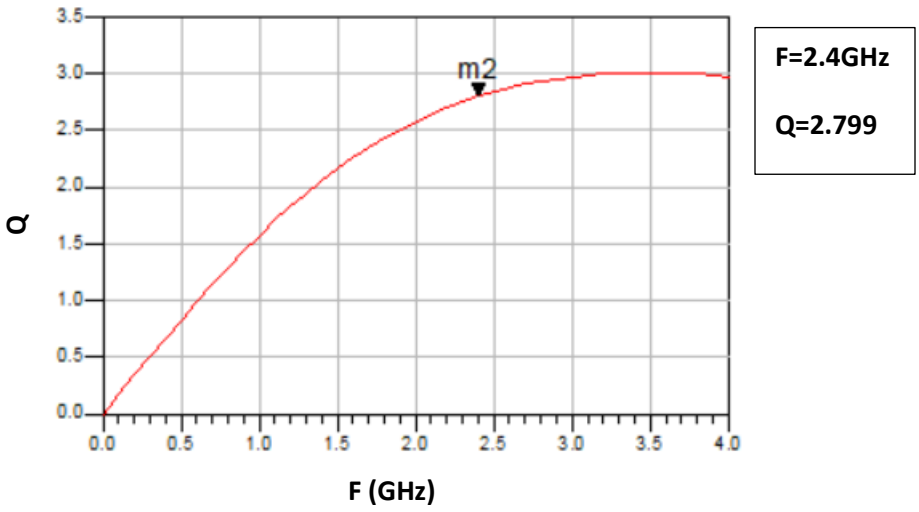


Figure (3-3) Quality factor of Basic Topology Active Inductor.

The variation of inductance value and quality factor according to variation of design variable is presented in table (3-1).

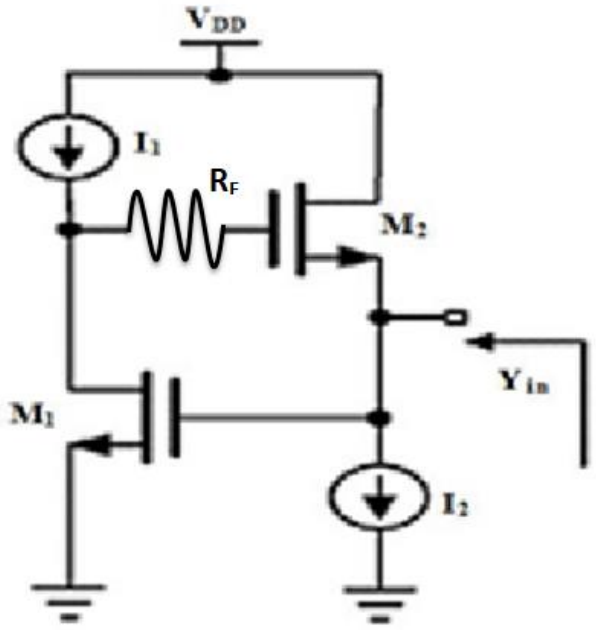
The design variables are selected randomly to illustrate the effect of the variation of these design variable on active inductor performance parameters.

Table (3-1) Design parameter vs inductance performance of basic topology at F=2.4GHz.

W_1(µm)	W_2(µm)	I_1 (mA)	I_2(mA)	L_{ads}(nH)	Q_{ads}	LQ_{ads}
3	0.5	0.1	0.1	9.039	2.799	25.3
4	0.2	0.2	0.1	11.9	1.41	16.779
6	0.4	0.2	0.1	7.854	1.801	14.145
8	0.4	0.5	0.2	5.772	1.361	7.856
9	1	0.2	0.1	5.136	2.517	12.927

3.3 Active Inductor With Feedback Resistor (R_f)

A passive resistance RF is added that acts as negative feedback as shown in figure (3-4) to improve active inductor performance and to decrease its sensitivity. The value of inductance and quality factor are given as [44]:



Figure(3-4) Schematic diagram of active inductor with feedback resistor.

$$G = g_{ds2} + \frac{g_{m1}}{1+R_F g_{ds1}} \qquad \text{.....(3-1)}$$

$$L = \frac{C_{ds2}(1+R_f g_{ds1})}{g_{m1} g_{m2}} \qquad \text{.....(3-2)}$$

$$Q = \frac{g_{m2} C_{gs1}(1+R_f g ds_1)}{g_{m1} C_{gs2}} \qquad \text{.....(3-3)}$$

Equations (1,2, and 3) illustrate the effect of the addition of passive resistance R_f. This resulted equivalent conductance loss (G) is to be minimized, as well as an increasing of the equivalent inductance (L) by $(I+ R_f g_{ds1})$ factor [44].

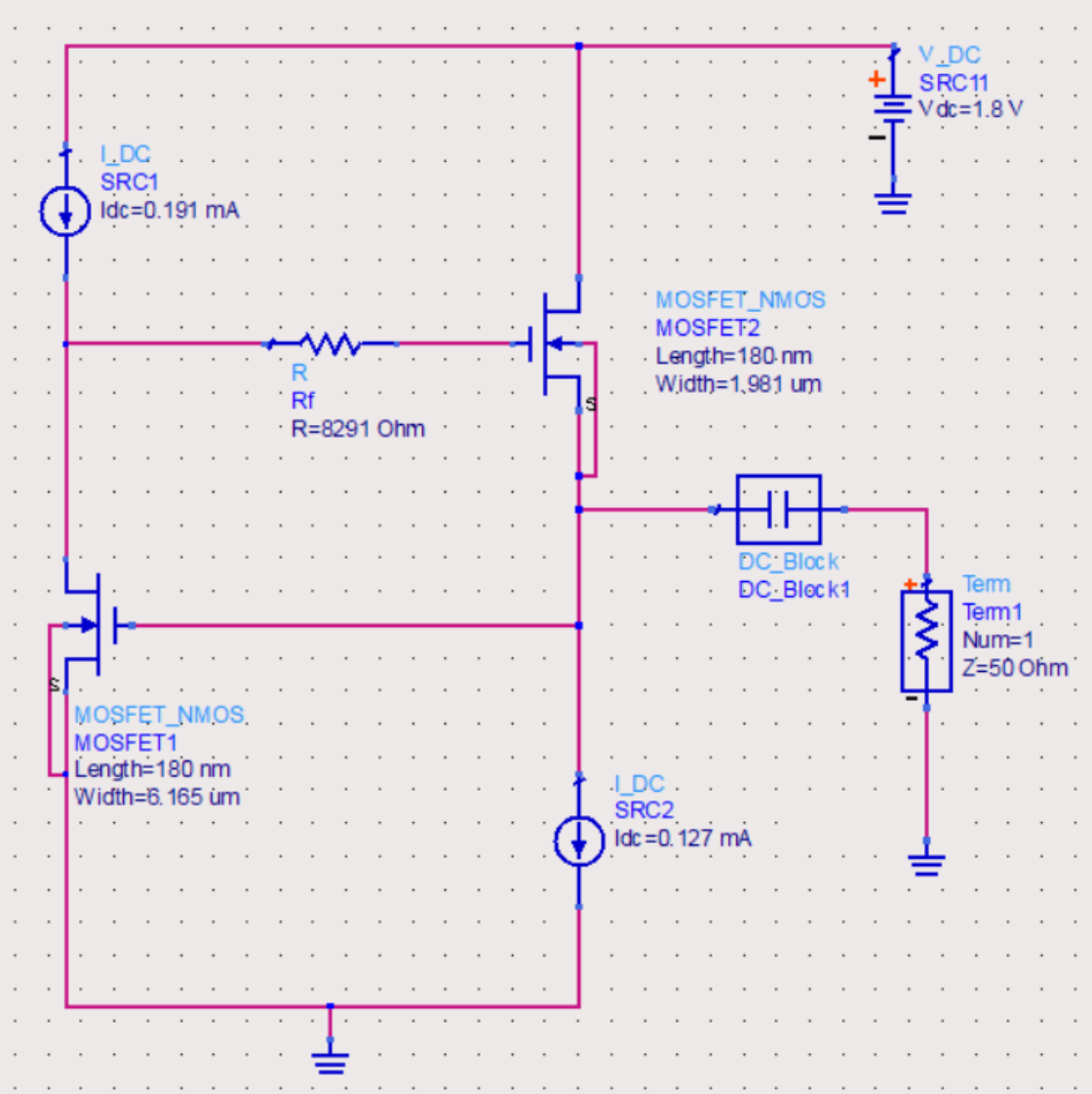


Figure (3-5) Active inductor with feedback resistor topology.

To improve active inductor performance a negative feedback is applied by adding a feedback resistor R_f. To illustrate the effect of the factor R_f. This resulted equivalent conductance loss (G) is to be minimized, as well as an increasing of the equivalent inductance (L) by (I+ $R_f g_{ds1}$) factor as is shown in figure (3-5).

The numerical design is performed by random selection of W_1, W_2, I_1, I_2 and R_f as follows:

W_1=6.165µm, W_2=1.981µm, I_1=0.191mA, I_2=0.127mA, and R_f=8291Ω.

The resultant conductance loss is given as:

$$G = g_{ds2} + \frac{g_{m1}}{1+R_F g_{ds1}}$$

Where

$g_{m1}=\sqrt{2 \times \mu_n \times C_{ox} \times \frac{W_1}{L} \times I_{d1}}$ =1.699 mS, and

$g_{m2}=\sqrt{2 \times \mu_n \times C_{ox} \times \frac{W_2}{L} \times I_{d2}}$ =2.493 mS.

The values of parasitic gate capacitances are given as:

$C_{gs1}=\frac{2}{3} \times C_{ox} \times W_1 \times L$= 5.69 PF

$C_{gs2}=\frac{2}{3} \times C_{ox} \times W_2 \times L$= 1.83 PF.

Therefore the resultant inductance value and quality factor are given as:

$$L = \frac{C_{gs2}(1+R_f g_{ds1})}{g_{m1}g_{m2}} = 4.685 \text{ nH}$$

and

$$Q = \frac{g_{m2}C_{gs1}(1+R_F gds_1)}{g_{m1}C_{gs2}} = 12.24$$

The simulation results are given in figure(3-6) and figure (3-7) for inductance variation and quality factor respectively.

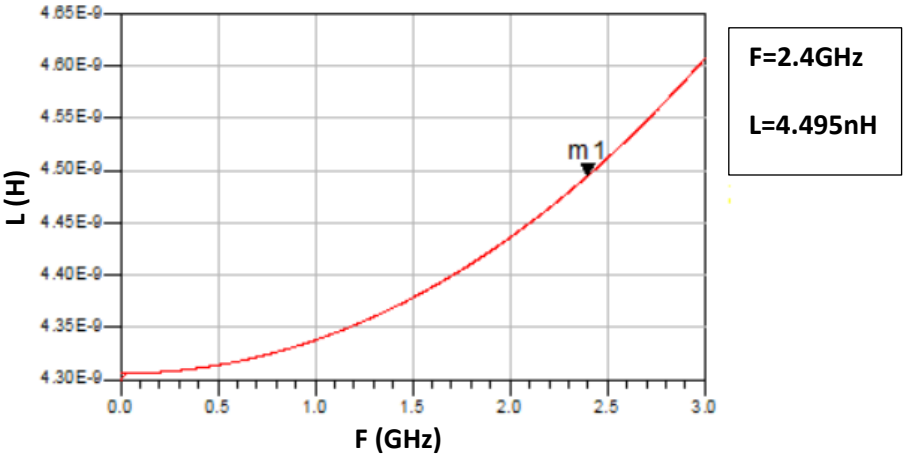


Figure (3-6) Inductance of active inductor with feedback resistor.

It is shown from the above figures that the simulation results satisfy the design specification and significantly agree with mathematical results.

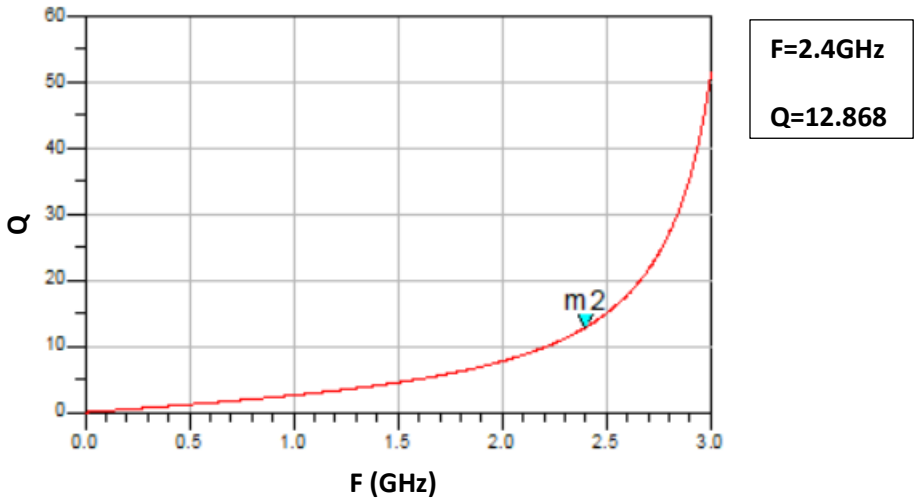


Figure (3-7) Quality factor of active inductor with feedback resistor.

Table (3-2) presents the simulated inductance value and quality factor for different design circuit variables. Table (3-3) illustrates the influence of feedback resistor on active inductor performance parameters.

Table (3-2) Design parameter vs inductance performance of active inductor with feedback resistor topology at F=2.4GHz.

W_1(µm)	W_2(µm)	I_1(mA)	I_2(mA)	R_f(Ω)	L_{ASD}(nH)	Q_{ASD}	LQ_{ADS}
6.165	1.981	0.191	0.127	8291	4.495	12.892	57.949
4	2	0.2	0.1	7500	5.167	6.873	35.513
3	1	0.1	0.15	4000	6.96	4.926	34.285
4	2	0.2	0.1	8000	5.204	7.314	38.062
5	2	0.3	0.2	6000	3.673	5.495	21.832

Table (3-3) Effect of R_f variation on active inductor performance at F=2.4GHz.

W_1(µm)	W_2(µm)	I_1(mA)	I_2(mA)	R_f(Ω)	L_{ASD}(nH)	Q_{ASD}	LQ_{ADS}
10	1	0.1	0.2	1000	7.877	3.988	31.413
10	1	0.1	0.2	3000	8.044	4.758	38.273
10	1	0.1	0.2	6000	8.301	6.615	54.911
10	1	0.1	0.2	9000	8.566	10.607	90.859

The effect of different feedback resistance values on inductance value and quality factor is illustrated in figure(3-8) for inductance variation and in figure (3-9) for quality factor.

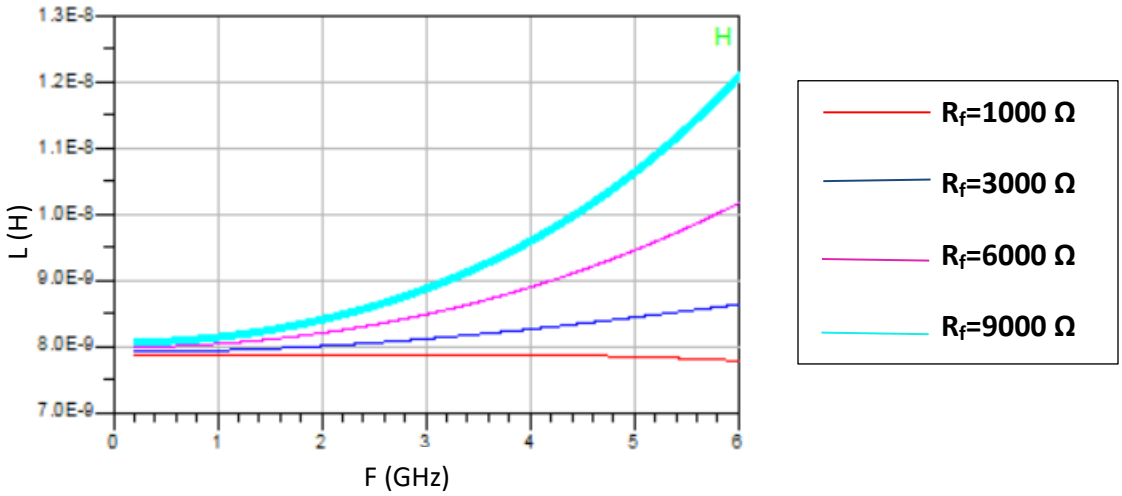


Figure (3-8) Inductance of active inductor with feedback resistor.

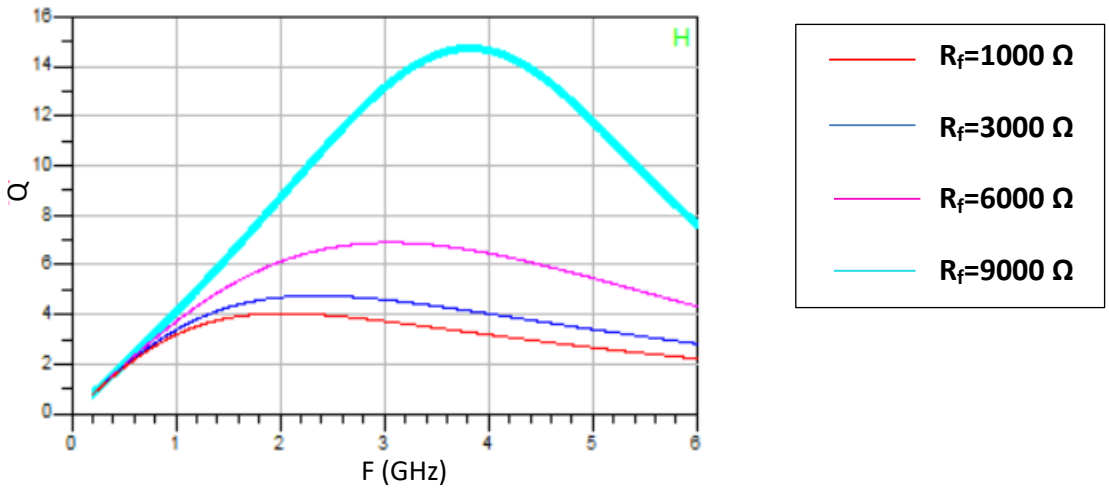


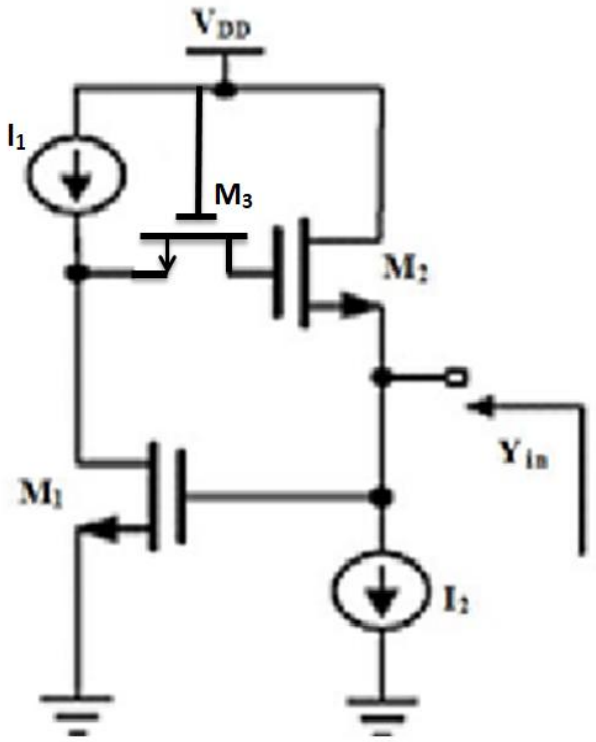
Figure (3-9) Quality factor of active inductor with feedback resistor.

It is obvious from the above figures that the increase of feedback resistance increases the inductance values and quality factor. However the increase in feedback resistance is not suitable in CMOS integrated circuit fabrication.

3.4 Active Inductor With Feedback MOS Transistor 1 (TF1)

To improve active inductor performance an MOS transistor is added instead of passive resistor R_f as shown in figure(3-10).

This new realization is based on the use of negative feedback element by utilizing active transistor (M_3) .The inductance value and quality factor are significantly improved.



Figure(3-10) Schematic diagram of active inductor with feedback MOS transistor 1.

The effective feedback resistance modeled by MOS transistor is given by:

$$R_{M_3} = \frac{L}{K'W(V_{GS}-V_T-V_{DS})} \qquad \text{.....(3-4)}$$

Where K' is transconductance parameter.

Since active inductor applications are almost realized in integrated circuits, this requires minimum chip area for fabrication. As is previously shown in figure(3-9), as feedback resistance increases, the performance of active inductor is improved. Large resistance values need large chip area for fabrication as well as accuracy will be critical. Therefore active MOS structure will be realized to avoid passive resistance.

A new realization based on the use of negative feedback element by utilizing active transistor (M_3) is presented in figure(3-11).

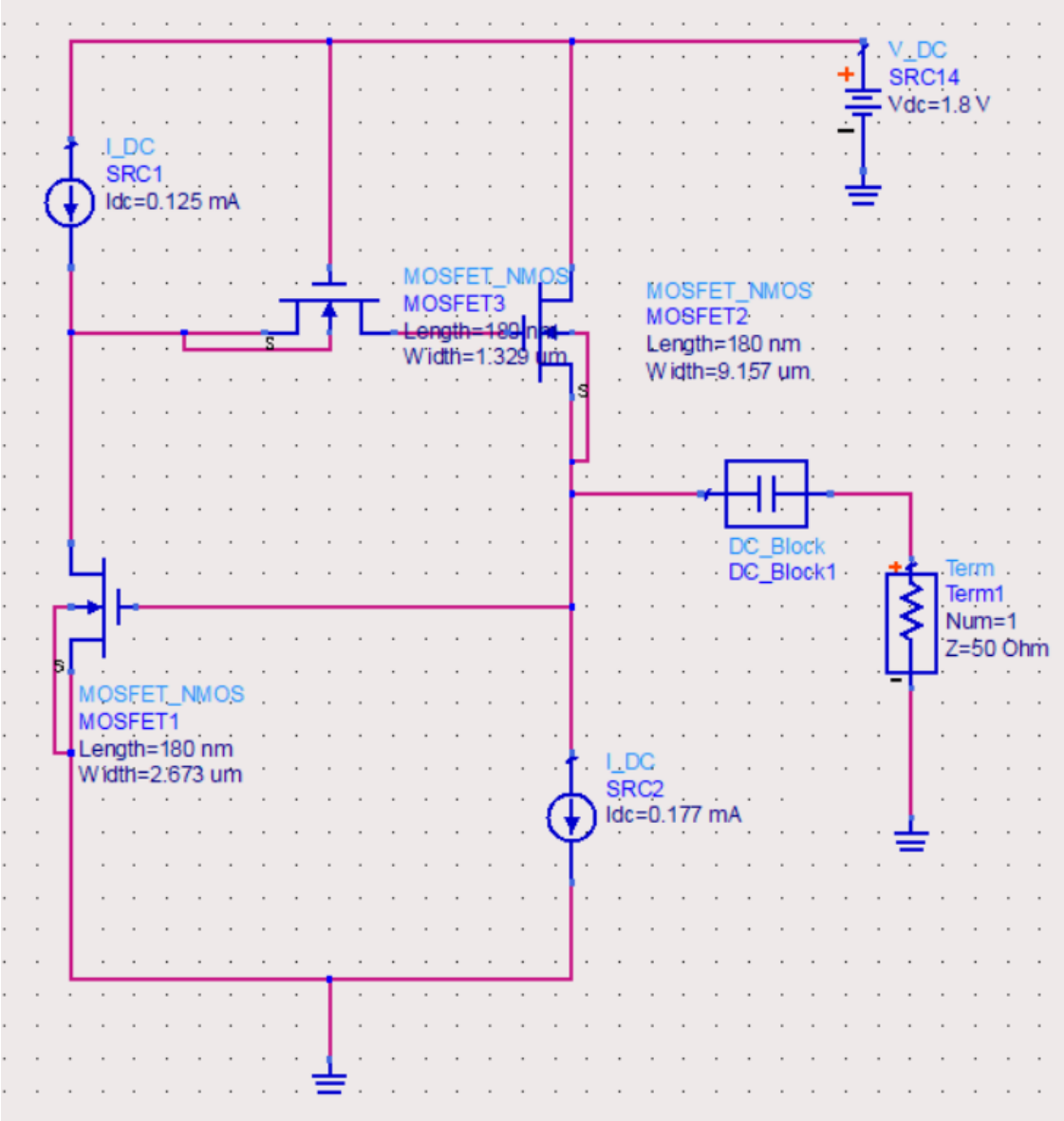


Figure (3-11) Active inductor with feedback MOS transistor 1.

As a case study, assume again for selected design variable W_1=2.673µm, W_2=9.157µm, W_3=1.329 µm, I_1=0.125mA, I_2=0.177 mA.

The effective feedback resistance modeled by MOS transistor is given as:

$$R_{M_3} = \frac{L}{K'W(V_{GS}-V_T-V_{DS})} = 2.3\ \text{k}\Omega$$

The value of trasconductances are given as:

$$g_{m1} = \sqrt{2 \times \mu_n \times C_{ox} \times \frac{W_1}{L} \times I_{d1}} = 0.9\ \text{mS. and}$$

$$g_{m2} = \sqrt{2 \times \mu_n \times C_{ox} \times \frac{W_2}{L} \times I_{d2}} = 1.9\ \text{mS.}$$

The resulted MOS transistors gate capacitances are:

$$C_{gs1} = \frac{2}{3} \times C_{ox} \times W_1 \times L = 2.5\ \text{PF, and}$$

$$C_{gs2} = \frac{2}{3} \times C_{ox} \times W_2 \times L = 8.5\ \text{PF.}$$

The resultant active inductor value and quality factor for the selected design variables are given by:

$$L = \frac{C_{gs2}(1+R_f g_{ds1})}{g_{m1}g_{m2}} = 8.912\ \text{nH, and}$$

$$Q = \frac{g_{m2}C_{gs1}(1+R_F gds_1)}{g_{m1}C_{gs2}} = 36.104$$

Figures (3-12) and figure(3-13) present the simulation results for L and Q for the given case study analysis variable designs.

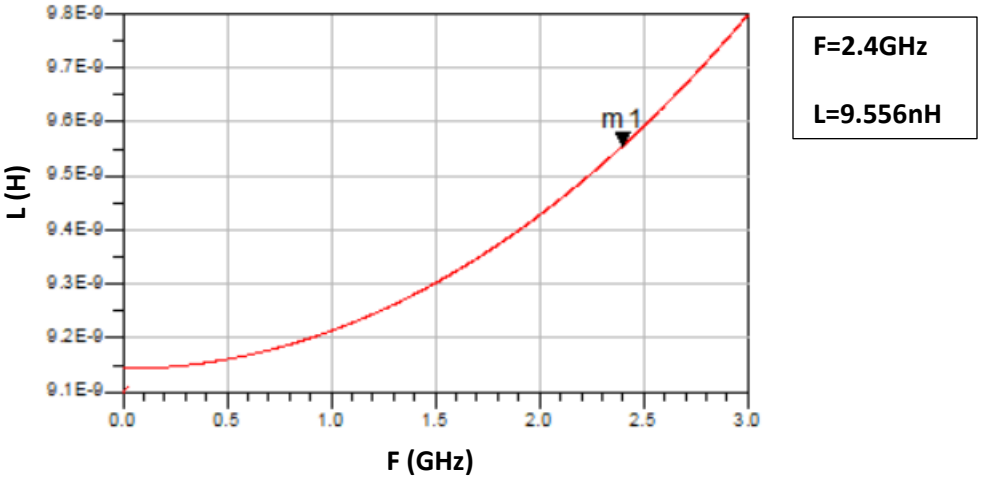


Figure (3-12) Inductance of active inductor with feedback MOS transistor 1.

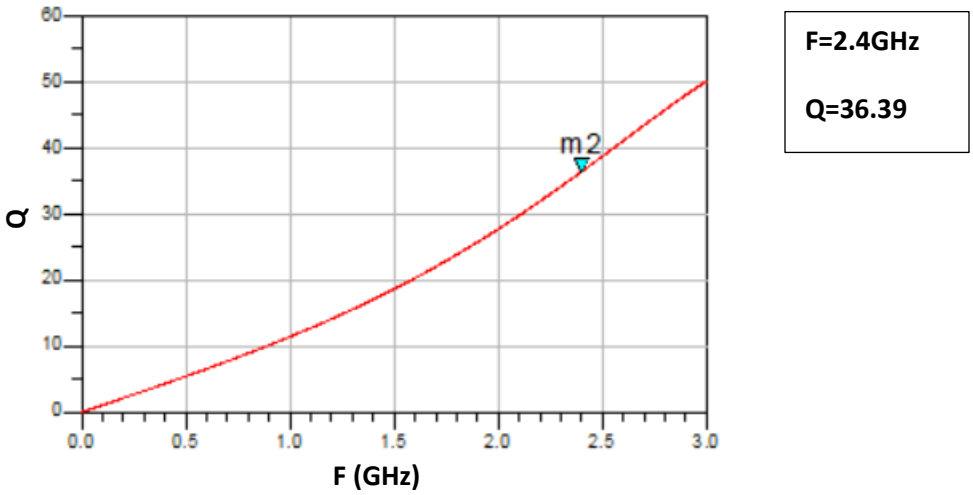


Figure (3-13) Quality factor of active inductor with feedback MOS transistor 1.

Table (3-4) presents the simulated inductance value, quality factor for different design circuit variables.

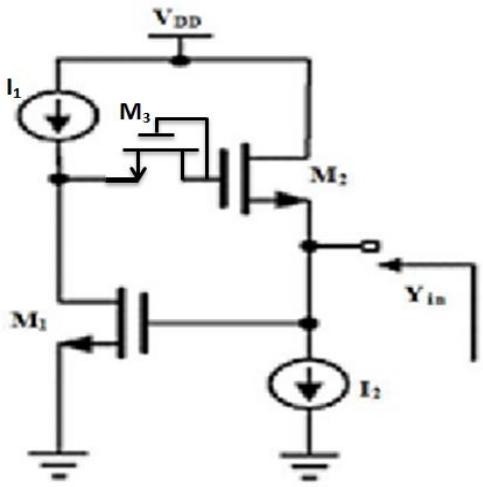
Table (3-4) Design parameter vs inductance performance of active inductor with feedback MOS transistor 1 topology at F=2.4GHz.

W_1(µm)	W_2(µm)	W_3(µm)	I_1(mA)	I_2(mA)	L_{ADS}(nH)	Q_{ADS}	LQ
2.673	9.157	1.329	0.125	0.177	9.556	36.39	347.743
3.209	9.827	1.682	0.142	0.205	7.979	41.206	328.783
4.328	2.942	4	0.216	0.097	9.707	31.124	302.121
5.714	3.183	1.5	0.117	0.106	7.569	19.22	145.476
5.714	3.183	2.5	0.117	0.106	8.728	10.664	93.075

Another new active realization for the feedback resistance based on the use of negative feedback element by utilizing active transistor (M_3) is presented in figure (3-10).

3.5 Active Inductor with feedback MOS Transistor (TF2)

Figure(2-14) shows an alternative feedback realization using saturated MOS transistor to replace the feedback element.



Figure(3-14) Schematic diagram of active inductor with feedback MOS transistor 2.

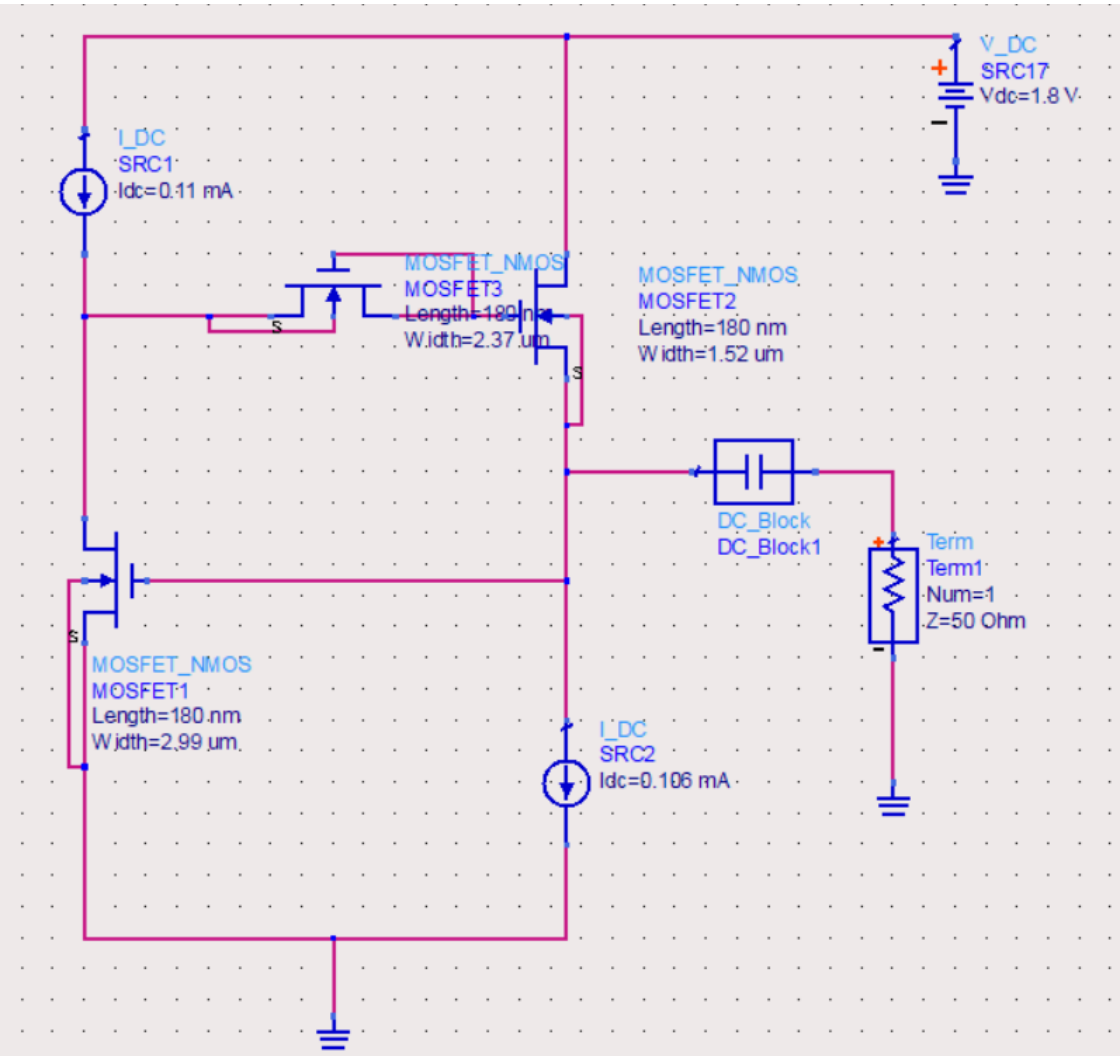


Figure (3-15) Active inductor with feedback MOS transistor 2.

The design procedure is applied for a case study given a selected deign variables as:

W_1=2.99µm, W_2=1.52µm, W_3=2.37µm, I_1=0.11mA, I_2=0.106mA.

The mathematical analysis based on the use of the following parameter values, the effective modeled FB resistance is given by:

$R_{M_3} = \frac{L}{K'W(V_{GS}-V_T-V_{DS})} = 1\text{k}\Omega$,

The device transcoductances are

$g_{m1} = \sqrt{2 \times \mu_n \times C_{ox} \times \frac{W_1}{L} \times I_{d1}}$ = 0.9 mS, and

$g_{m2} = \sqrt{2 \times \mu_n \times C_{ox} \times \frac{W_2}{L} \times I_{d2}}$ = 0.63 mS

The gate parasitic capacitances are to be as follows:

$C_{gs1} = \frac{2}{3} \times C_{ox} \times W_1 \times L$= 2.76 PF, and

$C_{gs2} = \frac{2}{3} \times C_{ox} \times W_2 \times L$= 1.4 PF

These design variables provide the following active inductance values and quality factors.

The ADS simulation results are illustrated in figure(3-16) and figure (3-17) for inductance and quality factor respectively.

$L = \frac{C_{ds2}(1+R_f g_{ds1})}{g_{m1} g_{m2}}$ = 9.25 nH

$Q = \frac{g_{m2} C_{gs1}(1+R_F gds_1)}{g_{m1} C_{gs2}}$ = 2.622

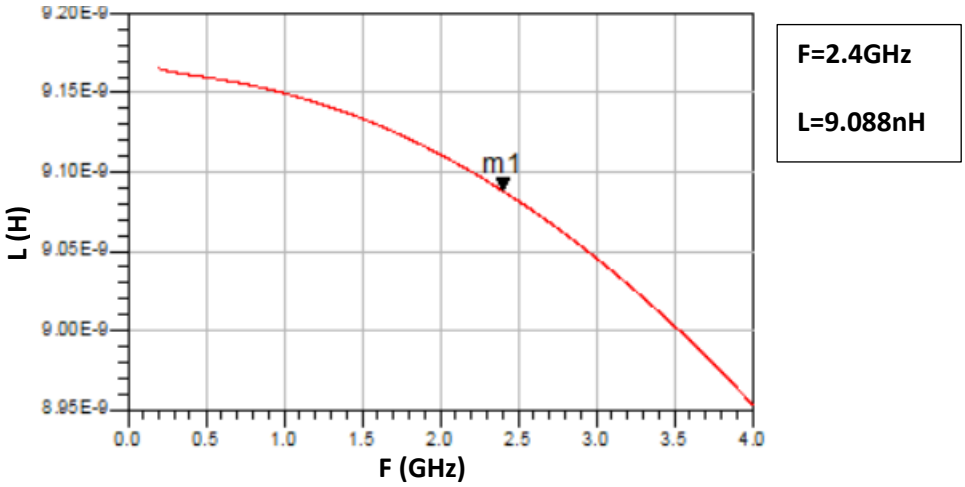


Figure (3-16) Inductance of active inductor with feedback MOS transistor 2.

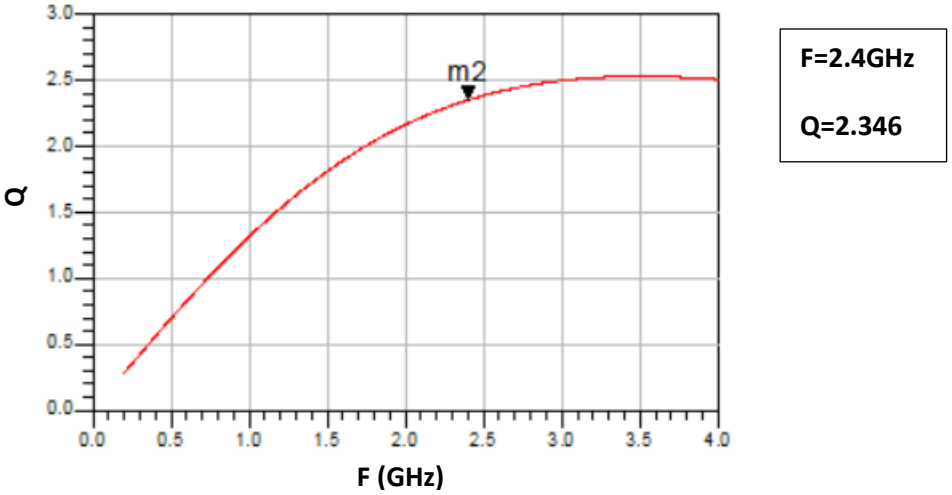


Figure (3-17) Quality factor of active inductor with feedback MOS transistor 2.

Table (3-5) presents the simulated inductance value, quality factor for different design circuit variables. Table (3-6) illustrates the influence active inductor with feedback MOS transistor 2 topology. performance parameters.

Table (3-5) Design parameter vs inductance performance of active inductor with feedback MOS transistor 2 topology at F=2.4GHz.

W_1(µm)	W_2(µm)	W_3(µm)	I_1(mA)	I_2(mA)	L(nH)	Q	LQ
2.99	1.52	2.37	0.11	0.106	9.088	2.346	21.321
5.714	3.183	4	0.117	0.106	7.995	2.657	21.243
6.204	4.982	4	0.251	0.113	5.992	1.781	10.682
5.714	3.183	1.5	0.117	0.106	11.6	1.612	18.699
5.714	3.183	2.5	0.117	0.106	9.443	2.137	20.179

Table (3-6) Effect of feedback transistor dimension on active inductor performance at F=2.4GHz.

W_1(µm)	W_2(µm)	W_3(µm)	I_1(mA)	I_2(mA)	L(nH)	Q	LQ
4	2	1	0.2	0.1	9.879	1.137	11.232
4	2	3	0.2	0.1	6.706	1.879	12.6
4	2	5	0.2	0.1	5.905	2.231	13.174
4	2	7	0.2	0.1	5.547	2.45	13.59

The effect the feedback MOS transistor dimensions on active inductor inductance value and quality factor are presented figure (3-18) and (3-19) respectively. This variation of active inductor performance is due to variation of effective feedback resistance simulated by MOS transistor.

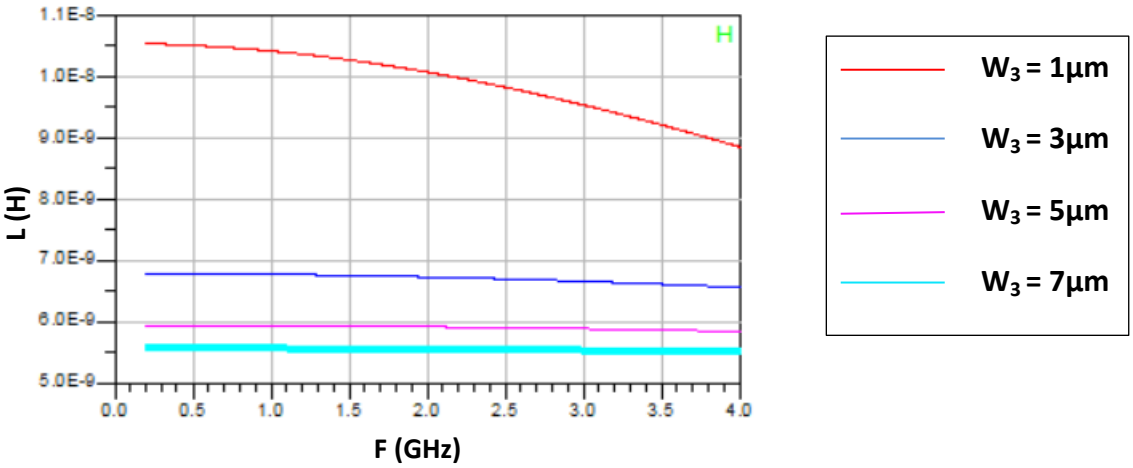


Figure (3-18) Inductance of active inductor with feedback MOS transistor 2.

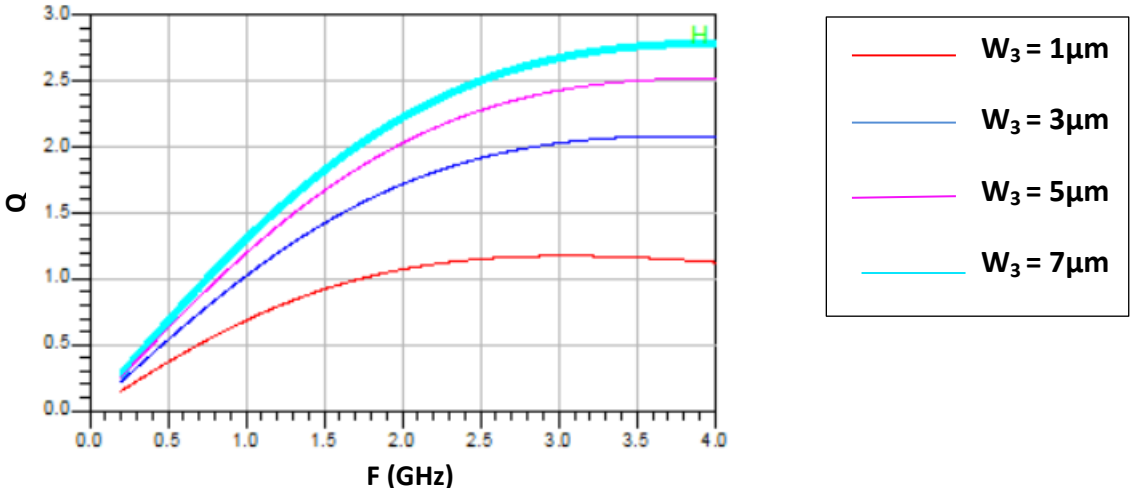


Figure (3-19) Quality Factor of active inductor with feedback MOS transistor 2.

3.6 Active inductor with feedback Voltage Divider (VD)

Another modified structure is illustrated in figure (3-20) that utilizes variable gate voltage on feedback transistor M_3. The voltage divider is applied to control the gate voltage, therefore controlling the equivalent feedback resistance of that representing MOS transistor M_3.

This is performed by controlling and selecting the proper gate voltage, this will provide an equivalent feedback resistance that improve the active inductor performance.

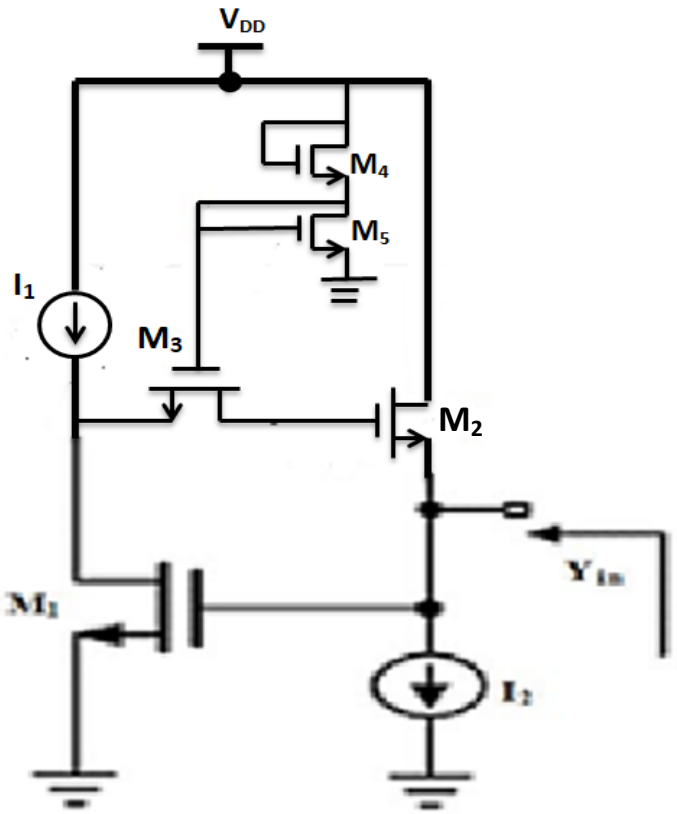


Figure (3-20) Schematic diagram of active inductor with feedback voltage divider.

The gate voltage can be represented by aspect ratios of MOS transistors M_4 and M_5 and can be written as:

$$V_G = \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_4+\left(\frac{W}{L}\right)_5} V_{DD} \qquad \ldots\ldots(3\text{-}5)$$

As the performance of active inductor depend strongly on the feedback resistance as previously presented, at active realization of this feedback resistance using MOS structure, the equivalent simulated resistance is determined by gate voltage and device dimensions.

A modified structure is illustrated in figure (3-21) that utilizes variable gate voltage on feedback transistor (M_3). The voltage divider is applied to control the gate voltage, therefore controlling the simulated resistance value of the feedback transistor.

As a mathematical analysis for this structure, assume a design variables are selected to be as:

W_1=2.894µm, W_2=1.226µm, W_3=0.721µm, W_4=3.948µm, W_5=2.047µm, I_1=0.119mA, and I_2=0.228mA.

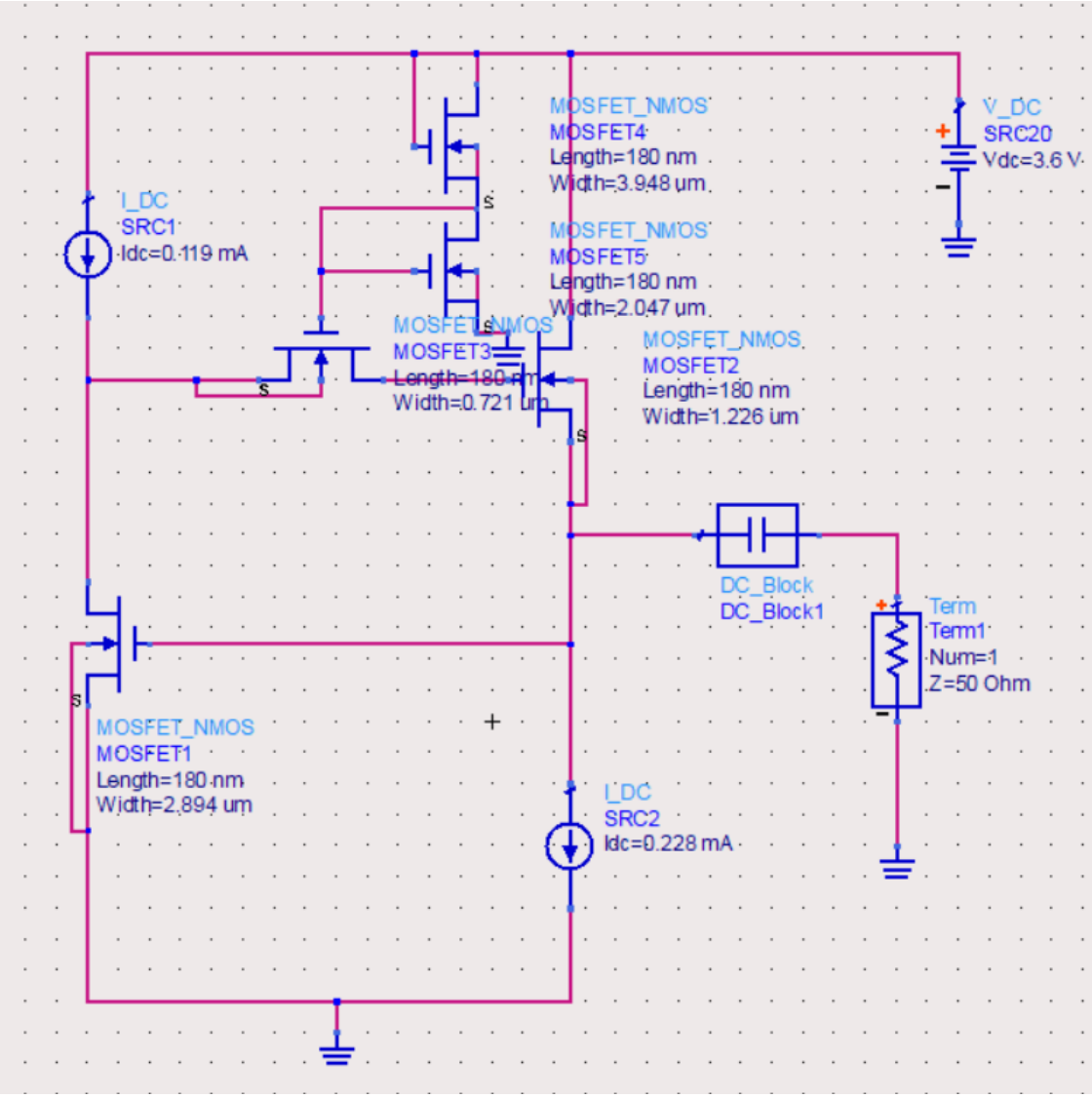


Figure (3-21) Active inductor with feedback voltage divider.

The gate voltage is controlled by device dimension W_4 and W_5 well as the supply voltage V_{DD}.

$$V_G = \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_4 + \left(\frac{W}{L}\right)_5} V_{DD} = 2.37 \text{ V}$$

Therefore the modeled resistance is given by:

$$\text{Ron} = \frac{L}{K'W(V_{GS}-V_T-V_{DS})} = 2.2\ \text{K}\Omega$$

The transconductance g_{m1}, and g_{m2} can be determined to be:

$$g_{m1}=\sqrt{2 \times \mu_n \times C_{ox} \times \frac{W_1}{L} \times I_{d1}} = 0.92\ \text{mS, and}$$

$$g_{m2}=\sqrt{2 \times \mu_n \times C_{ox} \times \frac{W_2}{L} \times I_{d2}} = 0.81\ \text{mS}$$

The parasitic gate capacitance C_{gs1} and C_{gs2} are given by:

$$C_{gs1}=\frac{2}{3} \times C_{ox} \times W_1 \times L = 2.67\ \text{PF}$$

$$C_{gs2}=\frac{2}{3} \times C_{ox} \times W_2 \times L = 1.13\ \text{PF}$$

Therefore the resultant simulated active inductor and quality factor are given as:

$$L = \frac{C_{ds2}(1+R_f g_{ds1})}{g_{m1}g_{m2}} = 6.99\ \text{nH, and}$$

$$Q = \frac{g_{m2}C_{gs1}(1+R_F g ds_1)}{g_{m1}C_{gs2}} = 15.81$$

The ADS simulation is used to compare and to verify the mathematical analysis with that simulated.

Figure (3-22) and figure (3-23) present the simulation results for inductor and quality factor respectively.

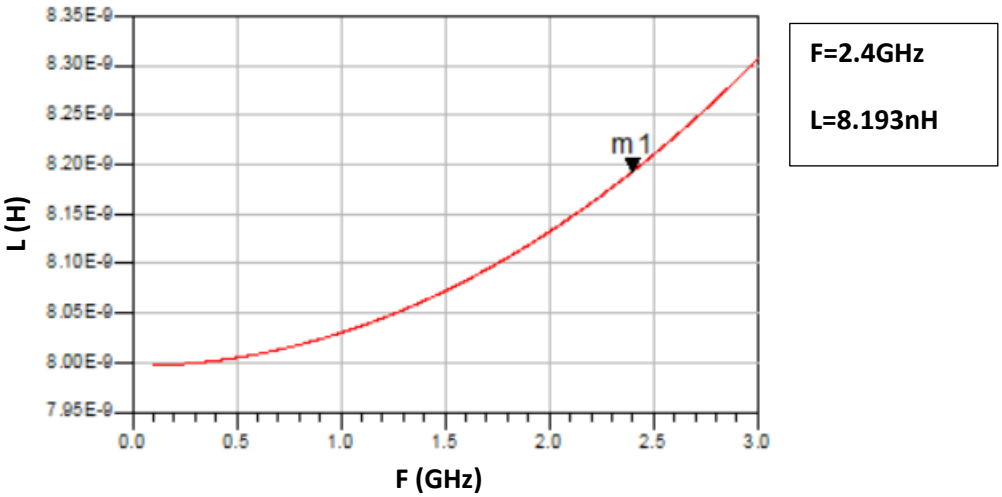


Figure (3-22) Inductance of active inductor with feedback voltage divider.

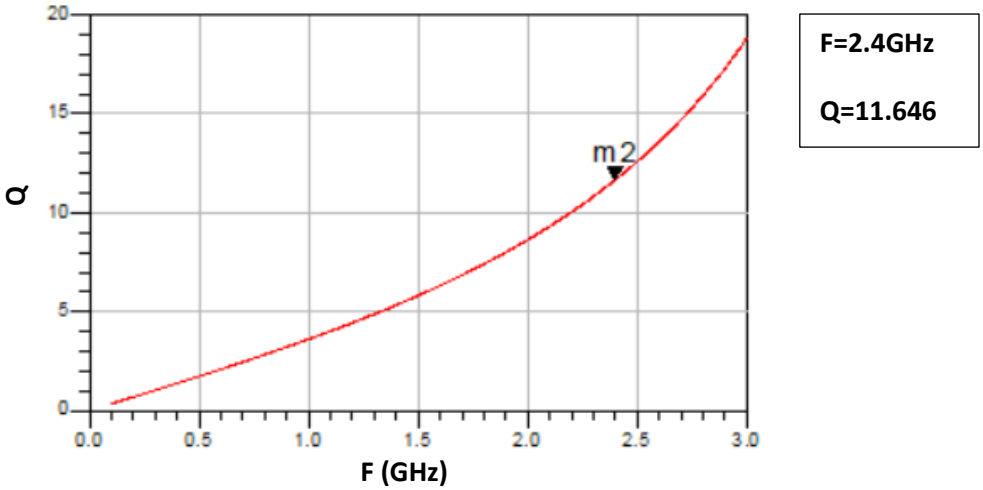


Figure (3-23) Quality factor of active inductor with feedback voltage divider.

Table (3-7) presents the simulated inductance value, quality factor for different design circuit variables of active inductor with feedback voltage divider topology.

Table (3-7) Design parameter vs inductance performance of active inductor with feedback voltage divider topology F=2.4GHz.

W_1(µm)	W_2(µm)	W_3(µm)	W_4(µm)	W_5(µm)	I_1(µm)	I_2(mA)	L_{ADS}(nH)	Q_{ADS}	LQ
2.894	1.226	0.721	3.948	2.047	0.119	0.218	8.193	11.646	95.416
3.507	2.715	1.297	3.859	2.083	0.193	0.399	5.295	16.548	87.622
5.102	2.549	1.128	2.867	1.563	0.185	0.392	4.467	15.068	67.309
5.714	3.183	4	3	2	0.117	0.106	9.92	4.655	46.178
4.328	2.942	4	3	2	0.216	0.097	9.136	4.316	39.431

3.7 Comparison between mathematical and simulation results

Table (3-8) summarizes the comparison between mathematical and ADS simulation results of the previous active inductor topologies in terms of inductance value, and table (3-9) for the comparison of the quality factor. These tables present the result of one set of a selected design variables for each active inductor topology.

Table (3-8) Comparison between mathematical and ADS simulation results of Inductance value at 2.4GHz

Topologies	Mathematical (nH)	ADS simulation(nH)
Basic	9.2	9.039
RF	4.685	4.495
TF1	8.912	9.556
TF2	9.25	9.088
VD	5.87	8.193

Table (3-9) Comparison between mathematical and ADS simulation results of quality factor at 2.4GHz

Topologies	**Mathematical**	**ADS simulation**
Basic	2.4	2.799
RF	12.24	12.862
TF1	36.104	36.39
TF2	2.622	2.346
VD	13.188	11.646

It can be seen that as inductance value improved, this may lead to reduce the quality factors. Therefore it may be suitable to compare the LQ factor product to decide the best topology. In addition to that it can be seen from the above tables, that there is a very small discrepancy between analytical results and simulated counterpart, this is due to real components used in ADS simulation that contains all parasitic elements that models the practical devices.

Chapter 4

Active Inductor performance improvement and its application in RF Filters

4.1 Introduction

This chapter presents the application of Genetic Algorithm (GA) to obtain an optimum various design topologies for active inductor. The aim of using GA is to maximize inductor values, frequency range and maximize the quality factor. In addition to that the GA is employed to minimize the chip area by minimizing the required device dimensions and power consumption while reserving the desired performances and specifications.

As a practical application of active inductor an active filters operating at RF frequencies continue to be the most design challenge because of its complexity to integrate. Despite significant improvements in the performance of monolithic integrated inductors in the CMOS process, the huge surfaces occupied by spiral inductors and the conductive substrate kept passive inductors a hesitant choice for use in high-frequency circuit design [60].

4.2 Optimum design of CMOS Active Inductor topologies

As illustrated in chapter 3, different design parameter values results in a different inductor performance. This is due to nonlinear behavior of inductor performance with respect to these design parameters.

Therefore a proper selection and a design experience are required to obtain an acceptable performance, hence it is a very difficult and impossible task to find manually the optimal design variables values in nanometer design. To overcome this complexity, time-consuming task optimization algorithm, the optimum value of variables is commonly used [61].

A multi-objective optimization method is needed because of usually existing numerous parameters for RF circuits. Together they are opposed, and designers need to make tradeoff between such goals as gain, power consumption and so on. Among the other algorithms, the basis for choosing MOGA is the low complexity and high efficiency of its optimization algorithm [62].

Figure (4-1) presents a design flowchart procedure for applying GA to optimize inductor performances.

The procedure starts by defining the problem parameter and the creation of initial population that are the initial design variables.

The next step is to formulate the fitness function that expresses a maximizing or minimizing a specified performance parameters. Then the design variables are determined that formulate the chromosome that defines the fitness function, in addition to this a constraints are also determined and specified. Then the genetic algorithm operation is applied that include selection, crossover, and mutation until the fitness function is satisfied under specified stopping conditions to reach the optimum solution [63].

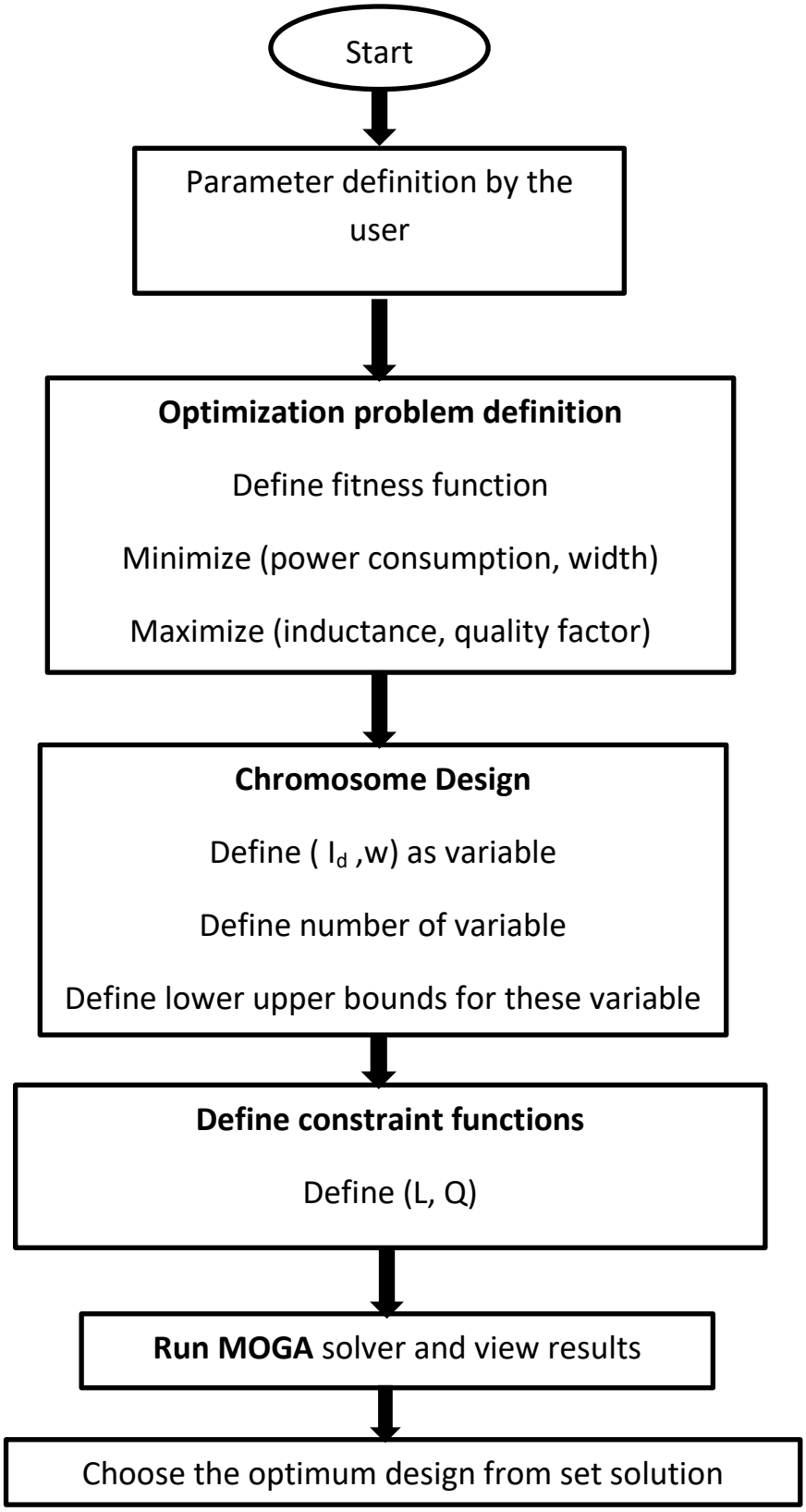


Figure (4-1) Flowchart of Genetic Algorithm procedure based on MATLAB

4.2.1 Population creation

The chromosome formulation is determined by the design variables that govern the fitness function.

These variables are treated as the genes of the chromosome.

The genes may include different parameter variables as is shown in figure(4-2), for the active inductor design.

Chr 1	W1	W2	I1	I2	W4	RF
Chr 2	W1	I1	I2	W4	W5	
Chr 3	W1	RF	I1	W3		
Chr 4	W1	I1	W5			

Figure(4-2) Various chromosomes representation.

The selection of the chromosome is influenced by a variety of factors, including convergence criteria and processing time. Before selecting the design chromosome for the Active Inductor in question, all possibilities must be explored (genes). Less genes (variables) per chromosome may increase flexibility and make it simpler to work with GA operators.

Chr1 to Chr3 have more genes than the chosen Chr4, as seen in figure (4-2). This can be accomplished by reducing the number of variables in the chromosome through a number of iterations. However, all of the parameters that affect how the design works, including device dimension, are implicitly included in these variables.

The design variables that are selected to be the device dimensions and the current values the chromosome of GA are designed to contain these variables as is shown in table (4-1).

Table (4-1) Design variables and constraints limit using MOGA

Variables name	**Constraints values**
W_1, W_2, W_3, W_4, W_5	0.01-30 um
I_d	0.01-30 mA
R_f	1-10KΩ

4.3 Fitness function formulation

The second step is to define fitness function. Once a population is created, the fitness of each chromosome in population is defined.

The fitness function (F) can be formulated as:

$F=\sum_{i=1}^{m} W_i \times f_i$ .....(4-1)

f_i is the desired value for object i.

W_i is the weight coefficient of object i.

M is the number of objects.

There is no set approach to solving these issues (multi-objective). Giving weight factors (Wi) for each function is one strategy. Since they might not have the same order or units, the weight factors are required to normalize the functions. The following formulation of the fitness function incorporates chip area and power consumption minimization:

$$F=\frac{1}{A_T \times W_1 + P \times W_2} \quad \text{.....(4-2)}$$

Where: A_T is the total chip area.

P … total power consumption,

$W_{1...}$ weighting factor for area.

W_2 … weighting factor for power consumption.

The total chip area is given by:

$$A_T = \sum_{i=1}^{K} W_i \times L_i \quad \text{.....(4-3)}$$

Where:

A_T is the total chip area required, for a given process with specified channel length L, the total chip area may represented by the total device width in the design topology.

K is the number of transistors in the circuit.

W_i, L_i are device dimensions

And the power consumption is given as:

$P= (I_1+I_2) \times V_{DD}$ ……..(4-4)

Where V_{DD} is positive and negative power supply voltages and I_1 and I_2 are drain currents of M_1 and M_2 as shown in figure (4-2)

4.4 Genetic Algorithm results

The designed genetic algorithm is employed for various active inductor topologies with different fitness functions.

Table(4-2) presents an Active Inductor required specifications and constraints for 0.18μm CMOS process.

Table(4-2) Active Inductor specifications design

Parameter	**Value**
Frequency(GHz)	2.4
Supply voltage (V)	1.8
Power consumption (mW)	<5
Source/load Impedance (Ω)	50

Any optimization routine and genetic algorithm is one of these optimization techniques that need constraint variables.

Table (4-3) illustrates the selection of active inductor performance parameters to be either fitness variables or constraints variable according to the required design.

Table (4-3) Design constraints and specifications for Active Inductor topologies.

Specifications/Constraints	**Type**	**Equation**
Inductance	Fitness	(2.22)
Quality factor	Fitness	(2.23)
Power consumption	Fitness	(2.25)
Gate to Source Capacitor Cgs	Constraint	(2.12)
Transconductance g_m	Constraint	(2.15)

The optimum design parameters are obtained from genetic algorithm as presented in table (4-4). Since inductor values improvement is the expense of quality factor increase and vice versa, it is convenient to introduce the LQ product factor as another performance parameter that include both parameters, and the maximum LQ factor represents the tradeoff between L and Q. The LQ product is introduced to give an indication of optimum L and Q parameter. In addition to that a comparison between optimum results obtained from GA and that obtained previously in chapter 3 without using GA are presented.

Table (4-4) the values of the optimum selected variables and results of Active inductor Topologies

Parameters	**Basic**	**R_f**	**TF1**	**TF2**	**VD**
W_1**(µm)**	2.01	6.827	2.826	9.97	3.906
W_2**(µm)**	0.2	2.119	7.972	0.99	1.128
W_3**(µm)**	-	-	0.955	1.174	0.743
W_4**(µm)**	-	-	-	-	3.848
W_5**(µm)**	-	-	-	-	2.147
$R_F(\Omega)$	-	6607	-	-	-
I_1**(mA)**	0.09	0.148	0.126	0.09	0.161
I_2**(mA)**	0.1	0.132	0.134	0.254	0.199
$\mathbf{L_{ADS}}$**(nH)**	15.88	4.784	9.9	16.54	7.213
$\mathbf{L_{GA}}$**(nH)**	12.81	5.122	13.57	23.56	7.803
$\mathbf{Q_{ADS}}$	2.103	15.845	44.852	1.511	14.284
$\mathbf{Q_{GA}}$	3.416	11.769	48.3	5.388	17.462
$\mathbf{LQ_{(GA)}}$	43.759	60.2808	655.431	127.156	136.256
P (mW)	0.342	0.28	0.468	0.344	1.296

To compare and to illustrate the advantage of using GA, table (4-5) presents a comparison of performance parameter of active inductor with and without using optimization. It is shown that the TF1 realization resulted in a significant improvement LQ= 655.431 compared to other topologies.

Table (4-5) Comparison between inductance, quality factor and LQ with and without optimization.

Topology	L (nH)		Q		LQ	
	With optimization	**Without optimization**	**With optimization**	**Without optimization**	**With optimization**	**Without optimization**
Basic	15.88	9.039	2.103	2.799	33.396	25.3
With R_f	4.784	4.495	15.845	12.868	75.803	57.842
TF1	9.9	9.556	44.852	36.39	444.035	348.07
TF2	16.54	9.088	1.511	2.346	24.992	21.3477
VD	7.213	8.193	14.284	11.646	103.031	95.416

It is obvious from the above table that a significant improvement in the LQ product by applying a genetic algorithm is obtained compared with that obtained previously without optimization.

This improvement is true for all active inductor topologies considered.

The ADS simulation results are presented in figure (4-3) and figure (4-4) for inductance and quality factor performance respectively for various topologies to verify that the GA results satisfy the required specification.

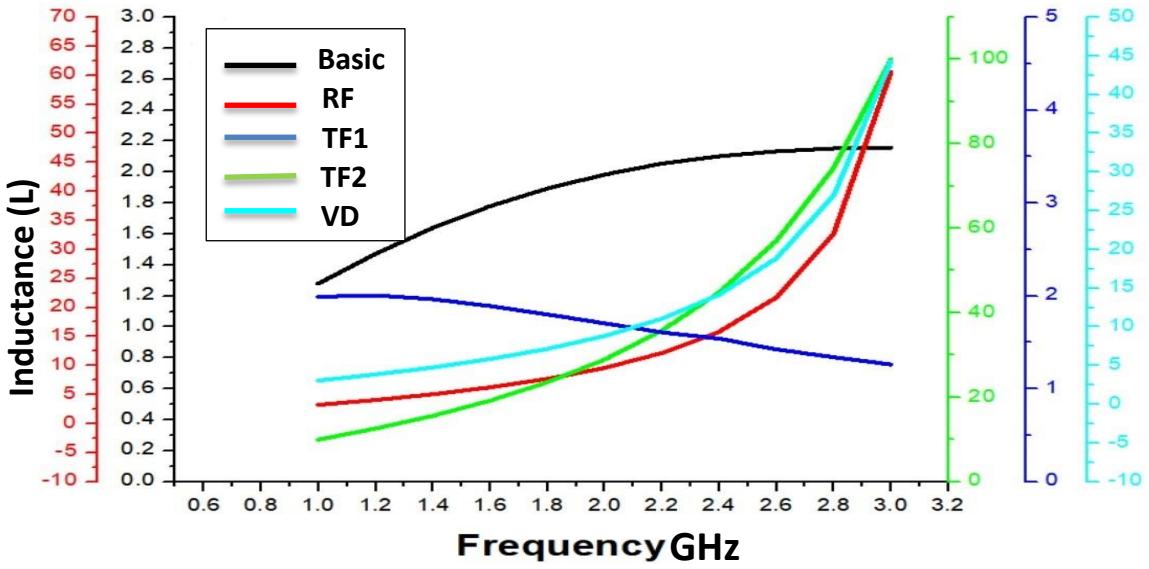


Figure (4-3) Inductance values of Active inductor topologies.

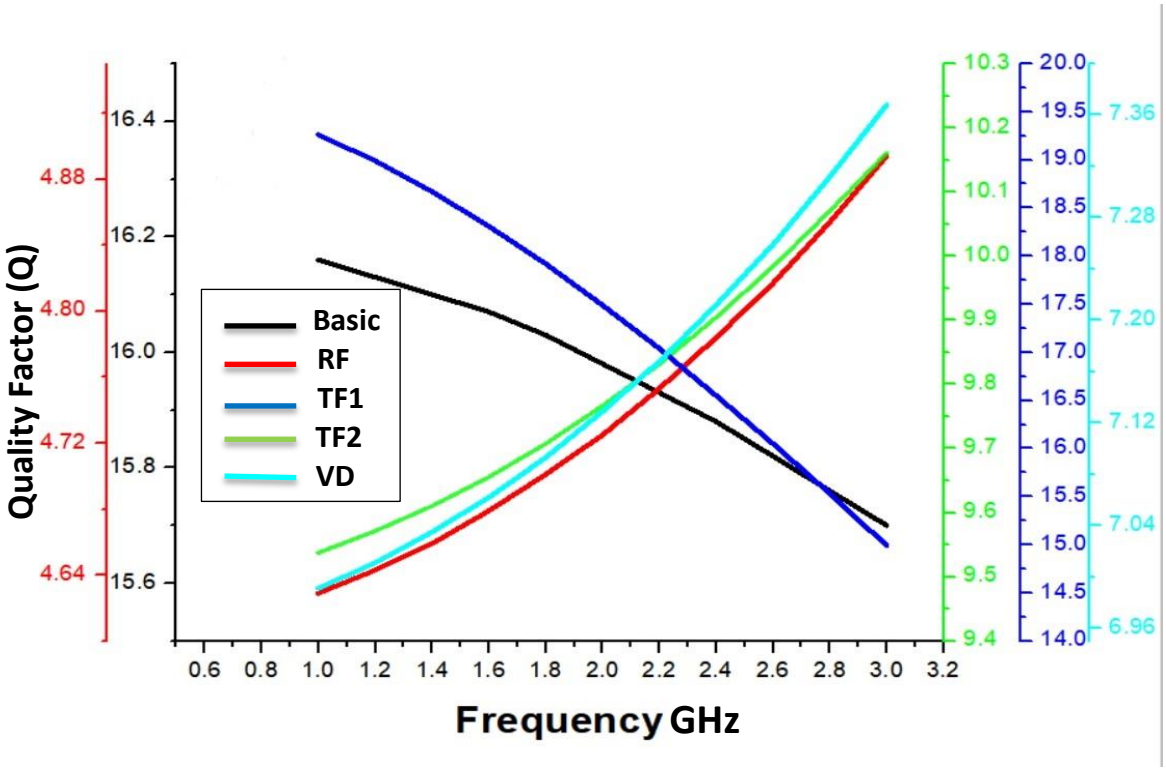


Figure (4-4) Quality factor values of Active inductor topologies.

As stated before the stopping conditions for the genetic algorithm may be used to the number of generations or may a specified error between adjacent results.

Figure(4-5) and figure (4-6) present the comparison between fitness functions versus GA generations of various active inductor topologies for inductance value and quality factor respectively.

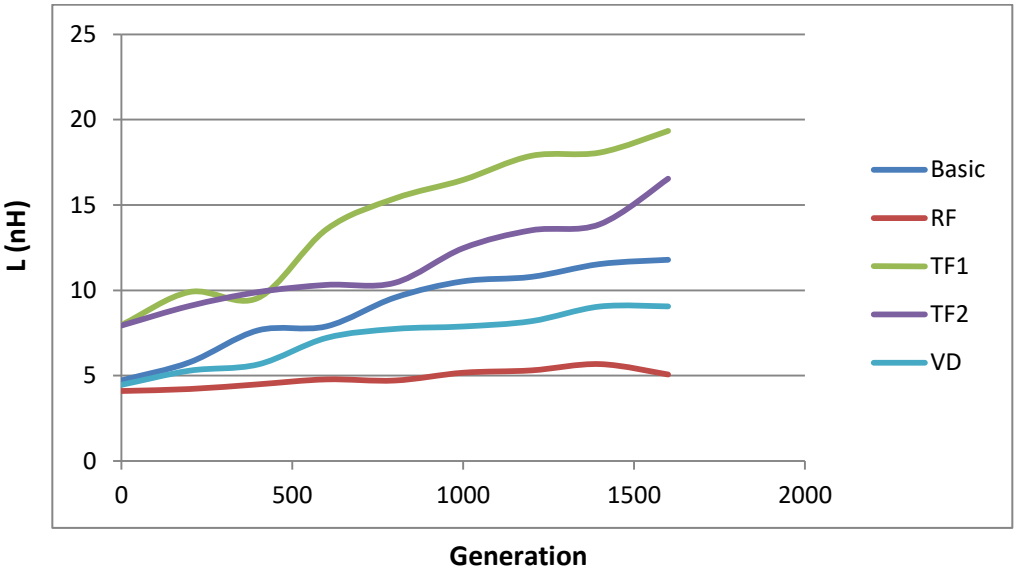


Figure (4-5) Fitness function versus generation for inductances.

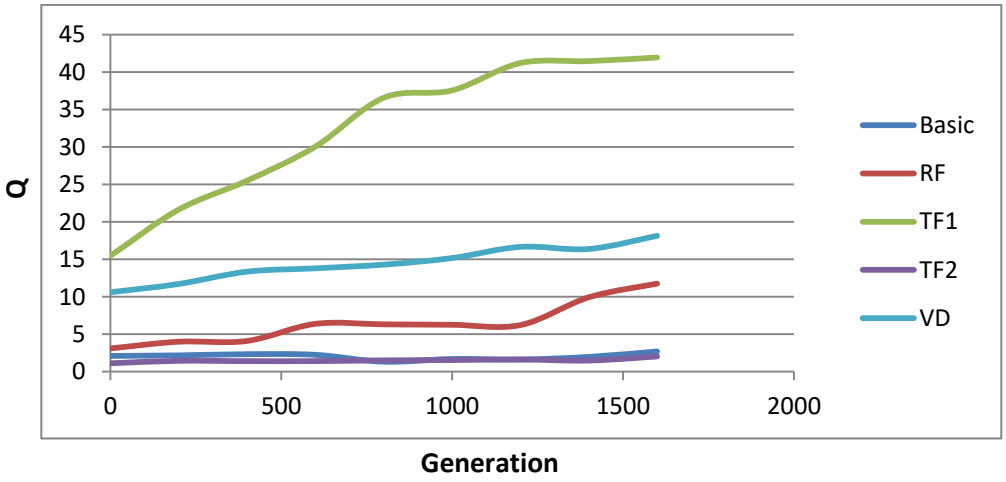


Figure (4-6) fitness function versus generation and inductances for quality factor.

4.5 Performance Comparison

A performance comparison is performed between these topologies to indicate the best behavior in terms of inductance values, and quality factor for each structure.

A genetic algorithm procedure is used to obtain the optimum design parameters for different active inductor topologies operating at 2.4 GHz frequency for RF applications. The design performances, such as inductance value range, inductance, quality factor, power consumption, and chip area, have been significantly improved. An appropriate comparison may be suitable by introducing the LQ product factor that contains inductance and quality factor. Figure (4-7) presents the LQ variation versus frequency for different active inductor topologies. The design variables that comprise the GA chromosome and values of variables are the currents I_1 and I_2, as well as the device widths W_1 and W_2. Multi-objective fitness functions are developed to acquire the best variables, which are then translated into the best performance parameters. It is clear from this comparison figure that the improvement of active inductor performance is included in the LQ factor, the higher LQ product the better performance.

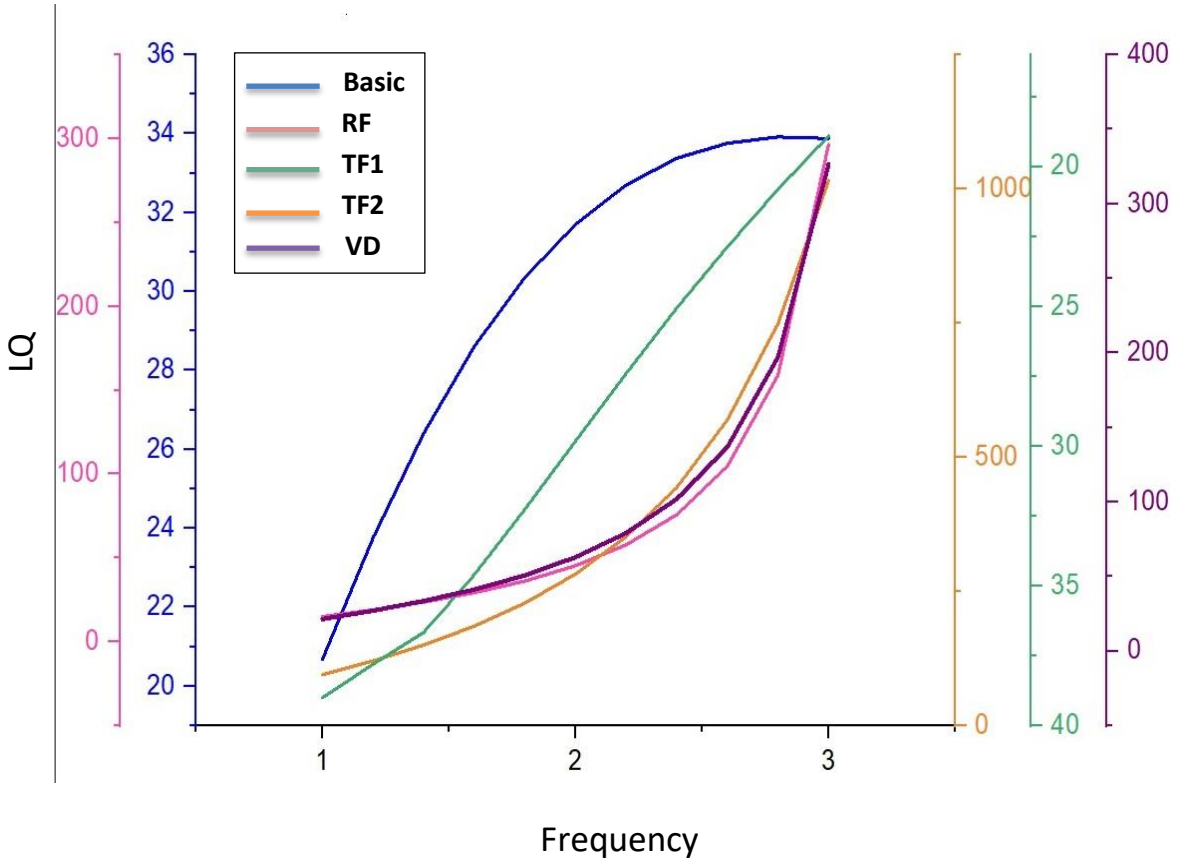


Figure (4-7) LQ values of active inductor topologies.

4.6 Current Source realization for active inductor

A P-channel transistor is used to implement a current source in Figure (4-8-a). The source and the gate are both brought to a fixed potential. Figure (4-8-a) of the source's definition of V_{out} and I_{out} is followed by Figure (4-8-b) of the I-V characteristic [32].

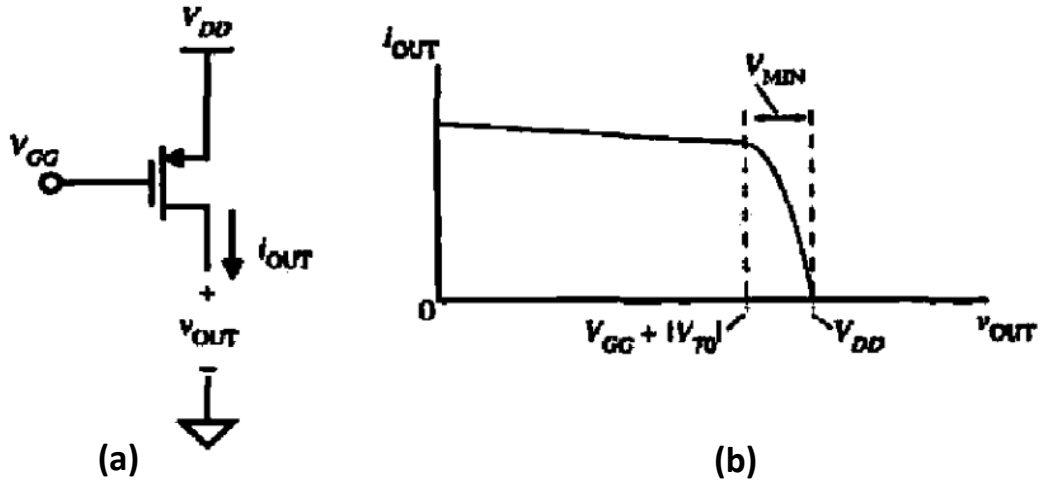


Figure (4-8) (a) Current source, (b) Current-Voltage characteristics.

The current source's small-signal output resistance is given by Eq (4-5). This current source needs a source-drain voltage greater than Vmin to function properly. The values of Vout that are supported by this source at this time come from:

$$V_{out} \leq V_{GG} + \left| V_{T_P} \right| \qquad \ldots\ldots\ldots (4\text{-}5)$$

Several CMOS realizations can be used to realize the current sources needed in active inductor topologies. Figure(4-9) presents one of these realizations techniques and represents a complete CMOS realization of basic active inductor topology.

A CMOS basic topology active inductor using current source is shown in figure(4-9)

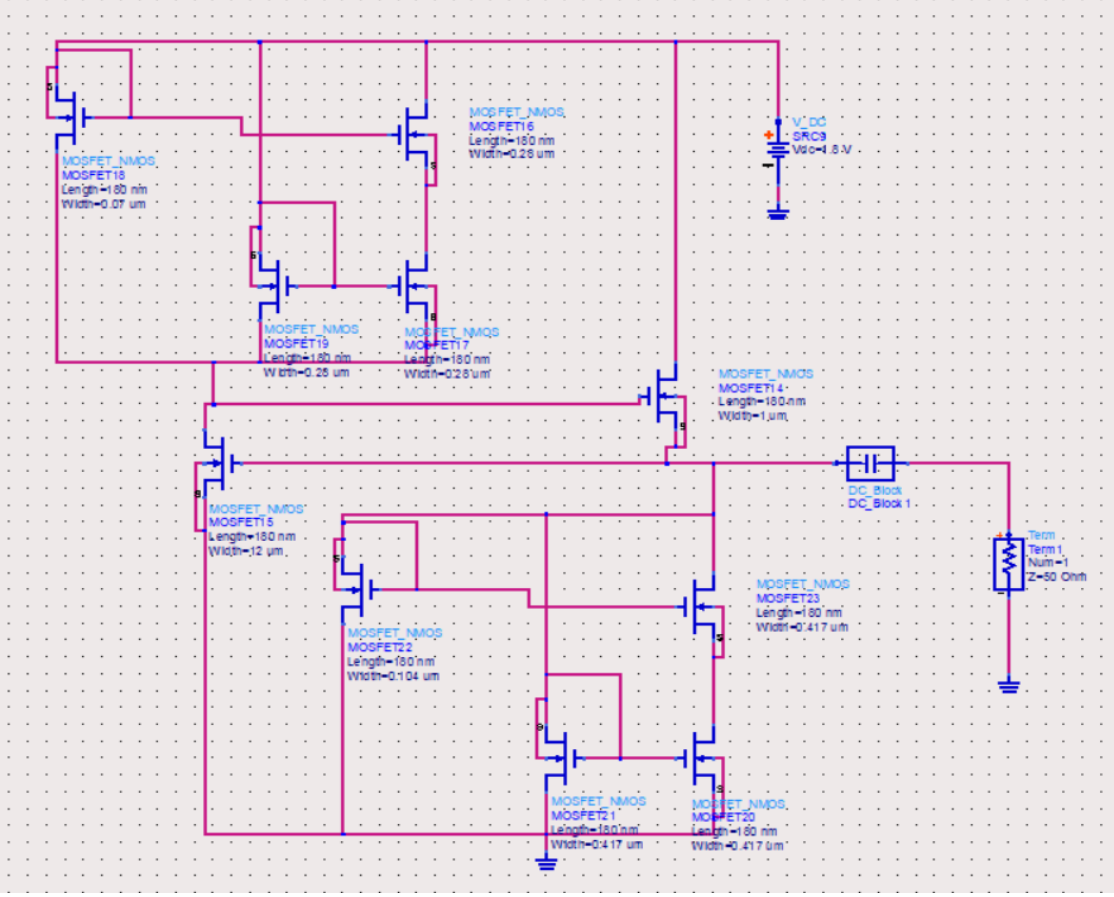


Figure (4-9) Basic topology active inductor.

4.7 Minimization of power consumption

An important performance parameter to be minimized using GA is the power consumption. The current sources that determine the power consumption are used as GA variables and device dimensions are set to be constraints.

Tables (4-6) illustrates the results of GA for minimum power consumption.

It is illustrated that the power consumption is significantly decreased while maintaining the device dimensions as constraints .

Table(4-6) GA results for active inductor topologies with minimum power consumption.

Parameter	**Basic**	**R_f**	**TF1**	**TF 2**	**VD**
W_1 (µm)	5.366	9.307	8.812	7.426	8.02
W_2 (µm)	1.256	4.951	2.476	1.189	6.136
W_3 (µm)	-	-	6.733	2.278	1.684
W_4 (µm)	-	-	-	-	4.753
W_5 (µm)	-	-	-	-	3.268
R_f (Ω)	-	3160	-	-	-
I_1 (mA)	0.05	0.086	0.035	0.086	0.079
I_2 (mA)	0.08	0.101	0.054	0.077	0.044
L (nH)	10.59	7.313	24.2	15.61	15.94
Q	5.407	34.818	3.325	8.232	4.293
LQ	57.26	254.624	80.465	128.502	64.43
P(mW)	0.234	0.337	0.1602	0.293	0.443
Total Width(µm)	7.777	16.807	18.816	12.345	24.329

The advantage of using GA in minimizing power consumption is illustrated in table (4-7). It is clear from this table that a significant reduction in power consumption is obtained after the application of genetic algorithm to minimize the power consumption.

Table (4-7) Comparison between minimum power consumption with optimization and without optimization.

Topology	power consumption (mW)	
	Minimized with optimization	**Without optimization**
Basic	0.234	0.36
R_f	0.337	0.572
TF1	0.1602	0.544
TF2	0.293	0.389
VD	0.4443	1.213

4.8 Minimization of chip area

Another important performance parameter is the minimization of required chip area for fabrication. The chip area is required for fabrication. The chip area is determined by the device dimensions that realize the active inductor while maintain the current source as constraints.

Total Width $W = W_1 + W_2 + \ldots\ldots\ldots\ldots + W_N$

As an example, the genetic algorithm is applied to a various active inductor topologies.

As a case study let us assume that the I_1 and I_2 are set to be from 0.1mA to 1mA .

Table(4-8) presents the optimum device dimensions obtained by applying GA routine.

Table (4-8) GA results for active inductor topologies with minimum chip area.

Parameter	**Basic**	**R_f**	**TF1**	**TF2**	**VD**
W_1 (µm)	0.575	0.423	0.48	2.766	1.316
W_2 (µm)	0.86	0.746	0.66	0.824	0.67
W_3 (µm)	-	-	0.985	1.482	0.575
W_4 (µm)	-	-	-	-	0.689
W_5 (µm)	-	-	-	-	0.271
R_f (Ω)	-	5320	-	-	-
I_1 (mA)	0.226	0.136	0.226	0.479	0.139
I_2 (mA)	0.307	0.163	0.145	0.107	0.145
L (nH)	19.25	22.09	27.02	3.582	15.46
Q	3.069	3.851	1.246	14.195	10.649
LQ	59.078	85.069	33.66	50.846	164.634
P(mW)	0.9594	0.5382	0.6678	1.0548	1.022
Total Width(µm)	1.435	1.169	2.125	5.072	3.521

It is clear from table (4-7) and table (4-8) that the improvement of power consumption is at the expense of chip area required that is described by total width of the devices and vice versa. As a comparison task table (4-9) presents the results of using GA to minimize chip area represented by total device widths.

Table (4-9) Comparison between minimum total widths with optimization and without optimization.

Topology	**Total device widths (µm)**	
	With optimization	**Without optimization**
Basic	1.435	3.5
R_f	1.169	8.146
TF1	2.125	13.159
TF2	5.072	6.88
VD	3.521	10.836

Again using genetic algorithm provides a significant reduction in total device widths as presented in table (4-9). However, the improvement of power consumption is at the expense of increased chip area, similarly the reduction of total width is at the expense of increasing the power dissipation, table (4-10) that illustrates this variations. Therefor the selection of importance of which performance parameter to be concentrated on it, is set by designer and the application.

Table (4-10) Comparison between chip area minimization and power consumption minimization.

Topology	**Power consumption Minimization**		**Chip area minimization**	
	Power (mW)	**Width (µm)**	**Width (µm)**	**Power (mW)**
Basic	0.234	7.777	1.143	0.9594
R_f	0.337	16.807	1.169	0.5382
TF1	0.1602	18.816	2.125	0.6678
TF2	0.293	12.345	5.072	1.0548
VD	0.443	24.329	3.521	1.022

4.9 RF Applications of active inductor

RC filters are mostly used at low frequencies. They are commonly used at audio frequencies but are rarely used above about 100 kHz. Their pass band attenuation is simply too great at radio frequencies, and the cutoff slope is too gradual. Inductors and capacitors are more commonly used in LC filters. Lower frequency inductors are large, bulky, and expensive, whereas higher frequency inductors are very small, light, and inexpensive [64].

The design methodology and genetic algorithm has been employed previously in chapter four to produce an optimal design to be applied for Band Pass Filter and High Pass Filter with active inductor.

BPF and HPF are designed and analyzed then optimized using GA at frequencies of 2.4GHz. The devices and their features used in the designs are based on the 0.18µm RF CMOS process.

Performance analysis is performed using Advanced Design System (ADS) tools for electronic design automation (EDA).

4.9.1 Band Pass Filter active realization

The first RF application of active inductor is the band pass filter realization. The band pass filter frequency response is defined as the frequency range through which the filter sends and receives signals. It is the frequency range between the cutoff frequencies or between the cutoff frequency and the cutoff frequency and zero (for a low-pass filter) or between the cutoff frequency and infinity (for high-pass) [64].

To illustrate the use of active inductor let us assume a simple RLC circuit shown in figure (4-10) shown the design parameter of BPF with passive inductor.

For a practical design of BPF at 2.4GHz, if capacitor C of 1pF is selected the required inductor L=4.4nH according to the fundamental equation:

$$F = \frac{1}{2\pi\sqrt{LC}} \quad \text{.....(5-1)}$$

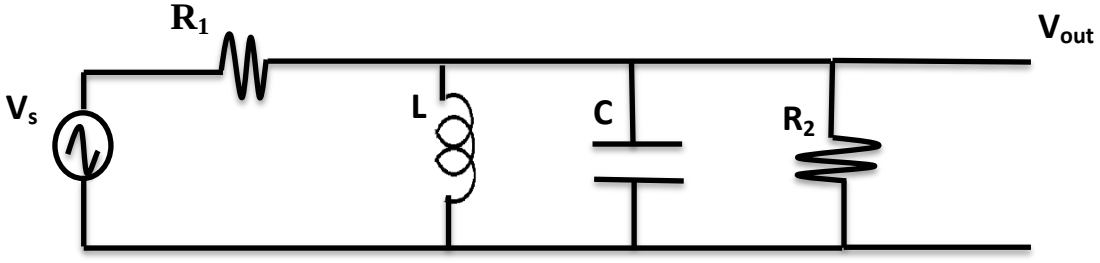


Figure (4-10) Band pass filter with passive inductor.

The active realization must meet the most important parameter values of the specified performance requirements. These could include the width MOSFET transistor W_1, W_2, that determine chip area and the value of currents I_1 and I_2, that determine power consumption.

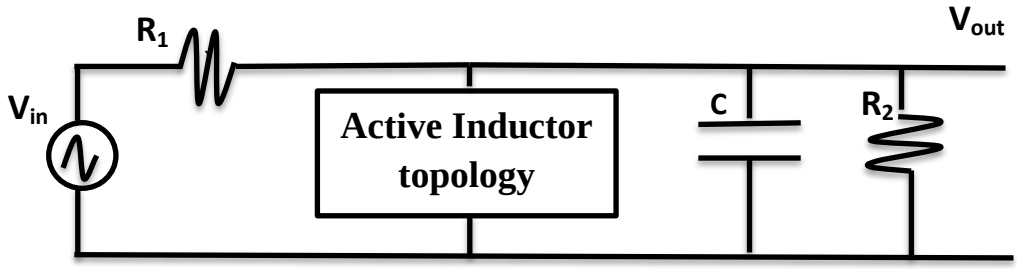


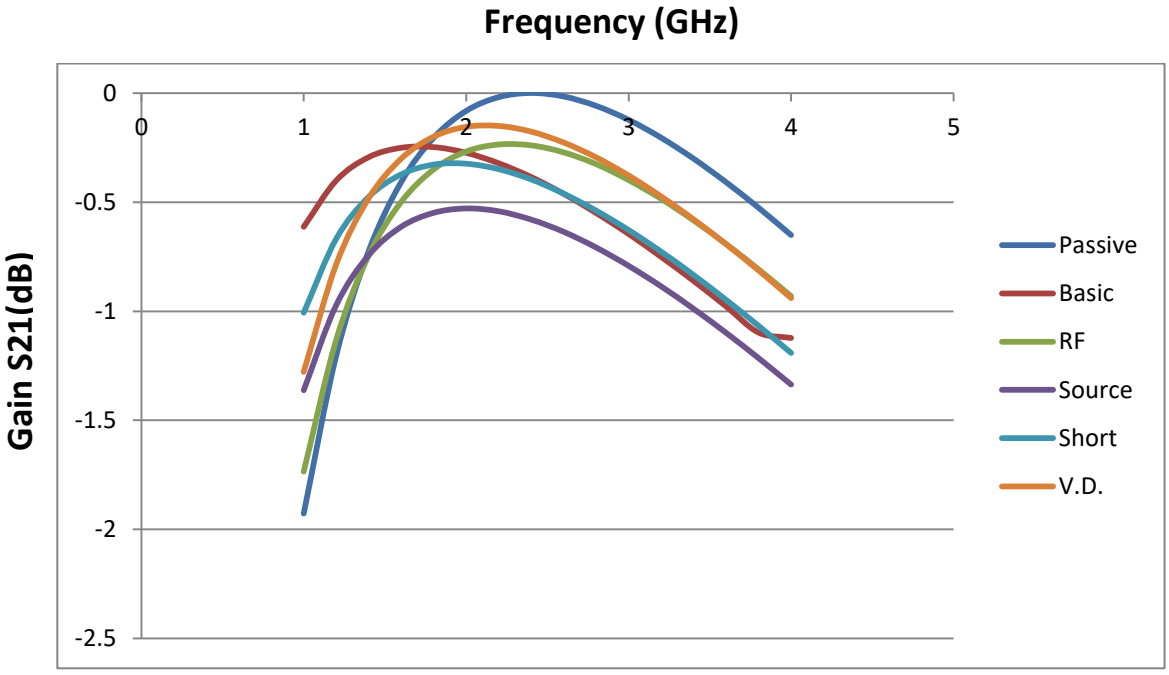
Figure (4-11) Band pass filter with Active Inductor Topologies.

Table (4-11) presents avarious active inductor realization circuit parameters that provide an inductance value of 4.4nH the required for the case under consideration, this design parameters are obtained previously from Genetic Algorithm.

Table (4-11) Design of BPF Active Inductor topologies

Topology	**W_1(µm)**	**W_2(µm)**	**W_3(µm)**	**W_4(µm)**	**W_5(µm)**	**I_1(mA)**	**I_2(mA)**	**R_F(Ω)**
Basic	5.677	5.993	-	-	-	0.227	0.113	-
R_f	6.165	1.981	-	-	-	0.191	0.127	8291
TF1	18.638	14.947	0.997	-	-	0.463	0.1	-
TF2	8.472	5.781	15.947	-	-	0.267	0.1	-
VD	5.102	2.549	1.128	2.867	1.563	0.185	0.392	-

Figure (4-12) presents the ADS simulation results for the active bandpass filter operating at 2.4GHz compared with passive counter part.



Figure(4-12) Comparison between Passive inductor BPF and Active Inductor BPF.

It can be seen from the above figures that active realization of inductor applied in BPF results in an acceptable frequency performance compared with that passive.

Table (4-12) illustrates a comparison between passive and various active structure in terms of center frequency (2.4GHz), simulated gain (S21).

Table (4-12) Comparison between inductance, quality factor and S_{21} of BPF active inductor topologies.

Topologies	**L(nH)**	**Q**	**Midband gain S_{21}(dB)**
Passive	4.4	0.916	0
Basic	4.4	4.756	-0.386
R_f	4.4	12.98	-0.24
TF1	4.4	27.188	-0.58
TF2	4.4	2.77	-0.396
VD	4.4	15.071	-0.157

Table(4-12) summarize the comparison between the previous BPF with active inductor topologies. It is clear from the above table that voltage divider structure provide the nearest performance compared with other realizations.

It may be suitable to compare the quality factor and gain to decide the best topology.

4.9.2 High Pass active filter realization

Another RF application of active inductor is the high pass filter (HPF) application. The HPF is basically pass frequencies above cutoff frequency and reject the frequencies below this cutoff frequency [64].

Ripple is defined as amplitude variation with frequency in the pass band or the repetitive rise and fall of the signal level in the pass band of some types of filters. It is typically expressed in decibels. In some types of filters, the stop bandwidth may also have ripple [64].

Chebyshev (or Tchebyschev) filters have very high selectivity; that is, their attenuation rate or roll-off is much higher than that of the Butterworth filter . The attenuation just outside the pass band is also very high—much higher than the Butterworth. The main issue with the Chebyshev filter is that it has pass band ripple. As with the Butterworth filter, the response is not linear or constant. This may be an issue in some applications.[54]

As a case study a high pass filter realization in passive and active with various active inductor topologies operating at 2.4GHz cutoff frequency is considered

The first step design produce is started from standard filter tables [65]. The passive low pass realization of 3^{rd} order, 1 dB ,Chebychive low pass response is considered, the following normalized parameters for low pass realization are obtained from these filter tables.

L_1=2.0236H, L_2=2.0236H, C=0.9941f, R=1Ω

Then a LPF to HPF transformation is simply obtained by transforming L-to-C and transforming C-to-L

$L = \frac{1}{C} = 1$ H

And C = $\frac{1}{L}$ = 0.49 f

After that a denormalization for frequency from w=1, to 2π×2.4GHz and impedance scaling to 50Ω, the new values are given as :

$L_{New} = \frac{K_m}{K_f} L_{old}$ = 3.337nH, and

$C_{New} = \frac{1}{K_F K_m} C_{old}$ = 0.6555pF

When K_m and K_f are the impedance scale and frequency scale respectively.

Figure(4-13) presents the passive RLC realization of a 3rd order, doubly terminated, HPF chebyshave response, and with its denormalized component values.

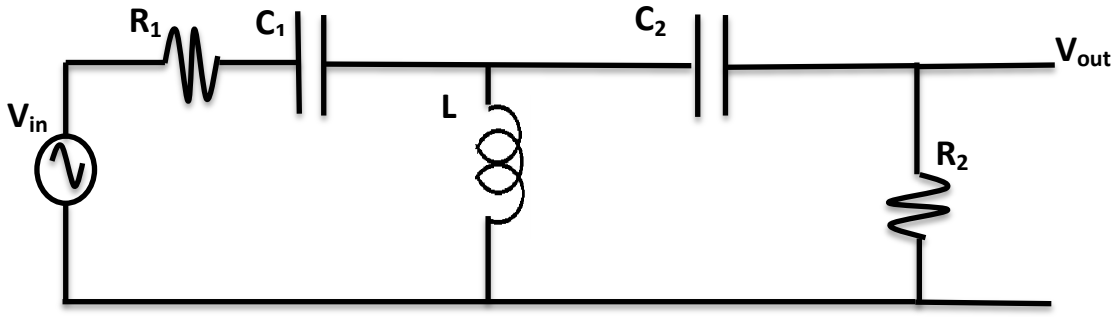


Figure (4-13) High pass filter with passive inductor.

By relacting the passive grounded inductor by its active realization the active HPF realization is obtained as shown in figure (4-14)

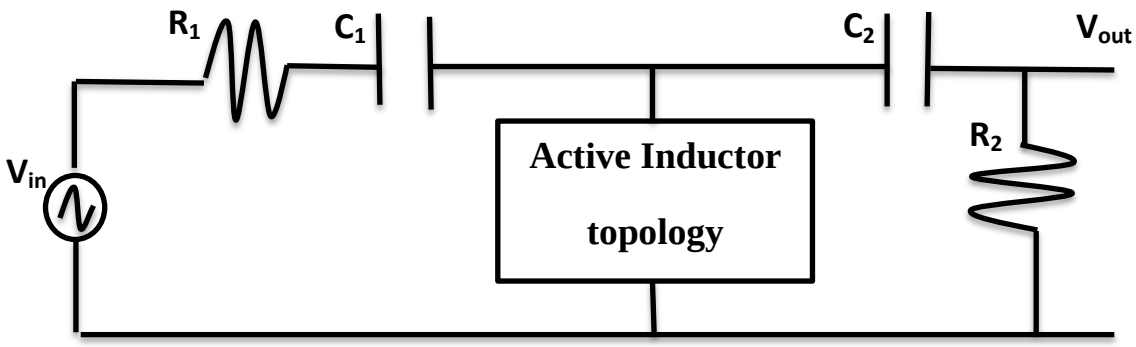


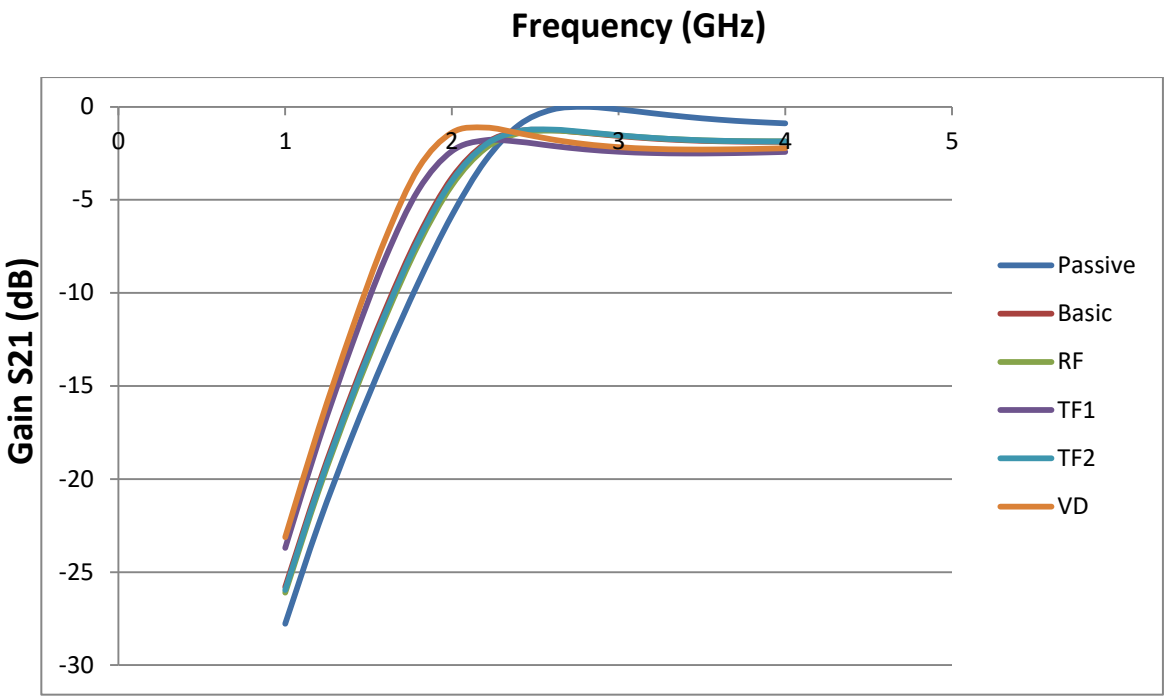
Figure (4-14) High pass filter with Active Inductor.

Table (4-13) presents a various design topologies parameter realization that obtain from genetic algorithm applization for the required inductance vaue of 3.04nH.

Table (4-13) Parameter values for active inductor realization.

Topology	**W_1(µm)**	**W_2(µm)**	**W_3(µm)**	**W_4(µm)**	**W_5(µm)**	**I_1(mA)**	**I_2(mA)**	**R_F(Ω)**
Basic	6.07	2.09	-	-	-	0.262	0.145	-
R_f	6.866	2.687	-	-	-	0.226	0.172	2170
TF1	15.025	4.876	1.493	-	-	0.364	0.136	-
TF2	8.458	6.07	12.04	-	-	0.185	0.437	-
VD	6.841	4.478	1.095	7.065	4.08	0.185	0.427	-

To prove the operation of active realization, an ADS simulation is employed, the simulation result is shown in figure(4-15) compared with that ideal passive counterpart.



Figure(4-15)Comparison between Passive inductor HPF and Active Inductor HPF.

It is clear from the above simulation figures that acceptable similarity between passive and active inductor is obtained.

Again the very small discrepancy between these simulated responses is due to non-ideal behavior of the devices realizing active inductor.

Table(4-14) summarizes the comparison between the passive (ideal) HPF with active inductor topologies. Since the inductance value is designed to be 3.337 nH, it may be suitable to compare between the quality factor and the gain to decide the best topology.

Table (4-14) Comparison between quality factor and Gain of HPF active inductor topologies.

Topologies	**Q**	**Gain (dB)**
Passive	0.916	-0.998
Basic	3.19	-1.306
Rf	5.344	-1.288
TF1	35.821	-1.877
TF2	4.117	-1.298
VD	14.725	-1.415

Chapter 5

Conclusions and Suggestions for Future work

5.1 Conclusion

This study is concerned with the design, simulation and optimization of active inductor CMOS realization for RF filter applications.

Passive and spiral implementations of the RF inductors have many limitations precisely when these RF circuits are designed and realized as CMOS integrated circuits. Typically, standard structure realized active inductors provide a limited inductor value and quality factor. The most important parameters that have to be investigated in this study are the quality factor, the range of inductors value at the specified operating frequency, and the self-resonant frequency.

Five different modified topologies have been designed and optimized to meet the specified requirement and to improve inductor performance. Basic topology, feedback resistor structure, MOS transistor feedback (short circuit) realization, MOS transistor feedback realization (source), and the voltage divider structure were realized, designed, and simulated. A comparison between these topologies is accomplished from point of view of active inductor performance parameters that include the inductance value and the quality factor, as well as the required integrated circuit process such as chip area and power consumption.

Advanced design System (ADS) simulation environment were used to verify the operation of active inductor and to compare between the performance parameters of these topologies.

A genetic algorithm optimization method is applied to improve the performance parameters of active inductor for RF applications that operate at 2.4 GHz frequency. The design performances include inductance value range, quality factor, power consumption, and transistors area were significantly improved. The currents and device widths are chosen as the design variables that formulated the GA chromosome and determine the above performances. Multi-objective fitness functions are developed to obtain the best variables, which are then translated into the best performance parameters. Various fitness function formulations were created and used. When compared to other functions, using a combination of inductance value and quality factor as LQ product in representing the fitness function resulted in a significant improvement in inductance value and quality factor with the least amount of power consumption.

A comparison with other existing methods is presented, demonstrating the superiority of the GA technique over other methods.

Band pass filter and High pass filter are designed and analyzed then optimized using the active inductor design resulted from GA at frequencies of 2.4GHz. The devices and their features used in the designs are based on the 0.18µm RF CMOS TSMC process.

This concludes the following :

1-Using CMOS active inductors in RF circuits provide a small chip area when integrated circuit implementation is required, as well as minimum power consumption needed.

2- A high quality factor, a large inductance, and a high self-resonant frequency are obtained. However passive inductors provide a low quality factor, a small inductance values, and low self-resonant frequency.

3- An improvement of active inductor performance are obtained by applying optimization procedure using MATLAB tool and based Genetic Algorithm (GA) to improve the CMOS active inductor performance.

4- GA was applied to various active inductor topologies to increase the inductance value and the quality factor in terms of LQ product.

5- The GA results obtained resulted in a significant reduction in chip area, power consumption, increase inductance and quality factor compared with existing mathematical methods.

6- ADS simulation was used on the GA resultant design structures to prove and to meet the required design specifications, and to verify the results obtained from GA.

7- The CMOS active inductor structure was used to realize active Band Pass Filter and High Pass Filter operating at 2.4 GHz center frequency and cutoff frequency respectively. The application of these active inductor showed a very near frequency response compared with that ideal passive counterpart.

5.2 Suggestions for future research

1- The complexity of realizing floating inductor that required in Low pass filter or other application may be next considered.

2-The application of active inductor on Low noise amplifier may be considered.

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الخلاصة

دوائر الترددات الراديوية (RF) مثل مكبر الاشارة منخفض الضوضاء(LNA) ومذبذبات التحكم في الجهد(VCO) ومرشحات الترددات الراديوية (RF Filter) تحتاج الى محاثات في تحقيقها.

تطبيقات الغير فعالة واللولبية لها العديد من القيود على وجه التحديد عندما يتم تصميم دوائر التردد الراديوي هذه وتنفيذها كدائرة متكاملة. قد تشمل هذه القيود تأثيرات الضوضاء المتولدة وحجم الرقاقة الكبيرة.

تقدم هذه الدراسة تنفيذ المحاثات المطلوبة في معظم تطبيقات الترددات الراديوية. يعتمد هذا النوع على استخدام تكوين(gyrator-c) المناسب لتصنيع (IC). يتم تقديم العديد من الادراك النشط ل(CMOS) وتنفيذها، وقد يشمل ذلك المحاثة الفعالة الاساسية، والطوبولوجيا تغذية استرجاعية عن طريق مقاومة ، والطوبولوجيا تغذية استرجاعية عن طريق لترانزستور(MOS)، ونوع تقسيم الفولتية. يتم اجراء دراسة مقارنة بين هذه الانواع باستخدام قيم عناصر تصميم الدوائر المختارة المناسبة للحصول على معلمات اداء محث نشط مناسبة اهم الخصائص التي يجب التحقيق منها هي عامل الجودة، مدى قيمة المحرضات بتردد تشغيل معين، تردد الرنين الذاتي، استهلاك الطاقة، ومساحة الرقاقة المطلوبة.

تنشأ صعوبة في التصميم من الناحية التحليلية نظراً لأن معلمات الأداء تتصرف بطريقة مختلفة فيما يتعلق بقيم مكونات التصميم. لذلك هناك حاجة الى تقنية التحسين للتعامل مع هذه المشكلة. يتم استخدام الخوارزمية الجينية (GA) للحصول على معلمات الأداء الأمثل، ويجب الحصول على قيم الحث القصوى، وعامل الجودة الأقصى. والحد الأدنى من استهلاك الطاقة، والحد الادنى من ابعاد الجهاز. يوفر تطبيق (GA) على العديد من طوبولوجيا الحث النشط تحسيناً كبيراً في معلمات الأداء هذه.

تمت المحاكاة باستخدام نظام التصميم المتقدم (ADS) لتحقق من النتائج التي تم الحصول عليها بواسطة الخوارزمية الجينية متعددة الاهداف ومقارنتها بمواصفات التصميم المطلوب.

اقرار المشرف

أشهد بأن هذه الرسالة الموسومة (تصميم المحاثات الفعالة المتكاملة نوع CMOS وتطبيقها في الترددات الراديوية) والمعدة من قبل الطالبة (جوليانا عوني اوراها) تمت تحت اشرافي في جامعة نينوى، وهي جزء من متطلبات نيل درجة الماجستير في الالكترونيك.

التوقيع:

المشرف: أ.م.د. أحمد ذنون يونس

التاريخ:

اقرار المقوم اللغوي

أشهد أن هذه الرسالة الموسومة((تصميم المحاثات الفعالة المتكاملة نوع CMOS وتطبيقها في الترددات الراديوية) تمت مراجعتها من الناحية اللغوية وتصحيح ما ورد فيها من أخطاء لغوية وتعبيرية وبذلك أصبحت الرسالة مؤهلة للمناقشة بقدر تعلق الأمر لسلامة الأسلوب وصحة التعبير.

التوقيع:

المقوم اللغوي: م. محمود احمد محمود

التاريخ:

اقرار رئيس لجنة الدراسات العليا

بناءَ على توصيتي المشرف والمقوم اللغوي ارشح هذه الرسالة للمناقشة.

التوقيع:

أ.د. قيس ذنون نجم

التاريخ:

اقرار رئيس القسم:

بناءَ على توصيات المشرف والمقوم اللغوي ورئيس لجنة الدراسات العليا ارشح هذه الرسالة للمناقشة.

التوقيع:

أ.د. قيس ذنون نجم:

التاريخ:

اقرار لجنة المناقشة

نشهد نحن أعضاء لجنة التقويم والمناقشة الموقعون قد اطلعنا على هذه الرسالة الموسومة (تصميم المحاثات الفعالة المتكاملة نوع CMOS وتطبيقها في الترددات الراديوية) وناقشنا الطالبة (جوليانا عوني اوراها) في محتوياتها وفيما له علاقة بتاريخ 26-4-2023 وقد وجدناها جديرة بنيل شهادة الماجستير علوم في اختصاص هندسة الالكترونيك.

التوقيع: التوقيع:

رئيس اللجنة: أ.م.د. خالد خليل محمد عضو اللجنة: أ.م.د. احمد محمد سلامة

التاريخ: التاريخ:

التوقيع: التوقيع:

عضو اللجنة : أ.م.د. عمر ابراهيم محمد عضو اللجنة (المشرف) : أ.م.د. احمد ذنون يونس

التاريخ: التاريخ:

اقرار مجلس الكلية

اجتمع مجلس كلية هندسة الكترونيات بجلسته ( ) المنعقدة بتاريخ

وقرر المجلس منح شهادة الماجستير علوم اختصاص هندسة الالكترونيك .

التوقيع: التوقيع:

مقرر المجلس : أ.م.د. ضياء محمد علي عميد الكلية: أ.د. خالد خليل محمد

التاريخ: التاريخ:

جامعة نينوى

كلية هندسة الكترونيات

قسم الالكترونيك

تصميم المحاثات الفعالة المتكاملة نوع (CMOS) وتطبيقها في الترددات الراديوية

رسالة مقدمة من قبل

جوليانا عوني اوراها

الى

مجلس كلية هندسة الكترونيات - جامعة نينوى

وهي جزء من متطلبات نيل شهادة الماجستير

في

هندسة الالكترونيك

باشراف

الأستاذ المساعد

الدكتور احمد ذنون يونس

جامعة نينوى

كلية هندسة الكترونيات

قسم الالكترونيك

تصميم المحاثات الفعالة المتكاملة نوع (CMOS) وتطبيقها في الترددات الراديوية

جوليانا عوني اوراها

شهادة الماجستير

هندسة الالكترونيك

باشراف

الأستاذ المساعد

الدكتور احمد ذنون يونس