Ninevah University

College of Electronics

Electronic Department

Design and Optimization of Low Noise Amplifier

Rafal Raed Mahmood Alshaker

A Thesis in

Electronic Engineering

Supervised by

Assistant Professor

Dr. Ahmad T. Younis

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A Thesis Submitted by

Rafal Raed Mahmood Alshaker

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ABSTRACT

Low Noise Amplifier (LNA) represents an important basic building block in most wireless communication systems. The LNA is usually used as a first block in RF receiver system to amplify the very weak incoming signals. As a result, the received signals usually contain noise, therefore, the LNA operation is supposed to suppress and attenuate the noise signals from the received signals as well as the noise generated by the device realizing the amplifier. The traditional design and realization of LNA mostly depend on mathematical equations covering the operation of this amplifier. The design equations provide no space of freedom on design variable, and sometimes require a variable selection random to satisfy the design equations that determine the performance of the LNA. The LNA performance may include noise figure, gain, power consumption, input and output matching, stability and linearity. This study presents an alternative method to a mathematical tradition technique, that is an optimization technique based on the use of Genetic Algorithm (GA). Multi-Objective Genetic Algorithm (MOGA) is applied to improve LNA performance that includes minimizing NF, minimizing power consumption, as well as maximizing gain. In addition, to a procedure is applied to deal with fabrication requirement by reducing the required component values and device dimensions. Significant improvements are obtained in performance parameters while satisfying the specified performance of low noise amplifier required. Two topologies at two operating frequencies of 2.4 GHz and 5 GHz are designed, optimized, and simulated. The two topologies are the single ended low noise amplifier and the differential low noise amplifier structures are designed and realized. The advantages and limitations of each structure are illustrated, and a comparison is made. The

application of MOGA for both structures provide a significant reduction in NF, power consumption, and maximizing the gain. The effect of increasing the operating frequency from 2.4 GHz to 5 GHz is studied and treated, especially the increase in NF. A simulation using Advanced Design System (ADS) is applied to verify the results obtained by genetic algorithm with that specified LNA performance.

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LIST OF ABBREVIATIONS

ABBREVIATIONS	**DESCRIPTION**
1-dB	1-dB Compression Point
ADS	Advanced Design System
BPFs	Band Pass Filters
BSIM	Berkeley Short-channel IGFET Model
CAD	Computer-Aided Design
CMOS	Complementary Metal Oxide Semiconductor
CRT	Current-Reuse Technique
CS	Common-Source
C_S	Capacitor of Source
CS-LNA	Common Source- Low Noise Amplifier
DC	Direct Current
DLNA	Differential Low Noise Amplifier
EA	Evolutionary Algorithm
EDA	Electronic Design Automation
EM	Electromagnetic
FCPCSNIM	Folded Cascade Power Constraint Simultaneous Noise And Input Matching
FDTS	Feasible Design Target Space
FOM	Figure Of Merit
G	Gain
GA	Genetic Algorithm
GPS	Global Positioning System

HPSO	Hybrid Particle Swarm Optimization
IC	Integrated Circuit
IEEE	Institute Of Electrical And Electronics Engineers
IF Amplifier	Intermediate Frequency Amplifier
IP3	Third -Order Intercept Point
KVL	Kirchhoff Voltage Law
LFPSO	Levy Flight Particle Swarm Optimization
LNA	Low Noise Amplifier
MATLAB	Matrix Laboratory
MCDM	Multi-Criteria Decision Making
MMIC	Monolithic Microwave Integrated Circuit
MOGA	Multi-Objective Genetic Algorithm
MOPs	Multi-Objective Optimization Problems
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NF	Noise Figure
NMOS	N-Channel Metal-Oxide Semiconductor
NSGA	Non-Dominated Sorting Genetic Algorithm
OFDM	Orthogonal Frequency Division Multiplexing
OIP3	Third-Order Output-referred Intercept Point
OP-Amp	Operational Amplifier

PCSNIM	Power-Constrained Simultaneous Noise-Input Matching
PSO	Particle Swarm Optimization
RF	Radio Frequency
RFIC	Radio-Frequency Integrated Circuit
SNR	Signal-to-Noise Ratio
SP	Scattering Parameters
TC	Termination Criterion
TSMC	Taiwan Semiconductor Manufacturing Company
UMC	United Microelectronics Corporation
W-CDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
WSM	Weighted Sum Method

LIST OF SYMBOLS

Symbol	DESCRIPTION
C	Correlation Coefficient
C_b	Blocking Capacitor
C_{gd0}	Drain To Source Conductance at Zero V_{DS} Capacitor
C_{gs}	Gate-Source Capacitance
C_{ox}	Capacitance Per Unit Area of the Gate Oxide
F	Noise Factor
f(x)	Cost Function
F_n	The Noise Factor of the n-th Stage
f_r	Resonant Frequency
f_T	Unity Gain Frequency of the MOS
F_{Total}	Total Noise Factor
$_{gd0}$	Drain to Source Conductance at Zero V_{DS}
G_m	Transconductance
g_{m1}	Device Transconductance For MOSFET1
G_n	Gain of the n-th Stage
I_d	Drain Current
i_{in}	Transistor Input Current
i_o	Transistor Output Current
i_d^2	Channel Thermal Noise
k	Stability Factor
L	Channel Length
L_d	Drain Inductance

L_g	Inductance Gate
L_S	Inductance Source Degeneration
P_D	Power Dissipation
Q	Quality Factor
R_1	Resistance of Inductor L_g
R_g	Gate Resistance
R_s	Source Resistance
S_{11}	Input Reflection Coefficient
S_{12}	Reverse Voltage Gain
S_{21}	Forward Voltage Gain
S_{22}	Output Reflection Coefficient
V_T	MOS Transistor Threshold Voltage
W	Width of MOSFET
X_L	Reactance of Inductor
δ	Gate Noise Coefficient
Δf	Band Width
ϵ_o	Dielectric Constant for Free Space
ϵ_s	Dielectric Constant for Silicon
ω_o	Operating Frequency
W_T	Unity Gain Frequency of the MOS
$\mathcal{E}_{ox}$	Permittivity of the Silicon Oxide

CHAPTER 1

Introduction and Literature Review

1.1 Introduction

In wireless communication, the LNA circuit plays an important role, it determines the amplification of the entire system as well as the noise performance. Analog and Radio Frequency RF components comprise the LNA circuit , therefore, a tradeoffs between its performance specifications, i.e. gain, NF, and power consumption is required [1]. With the scaling down of technology, RF circuit design is becoming more difficult, resulting in an increased complexity. Agility and performance are therefore difficult elements in the field of analog circuit design. There have been various attempts to develop design and optimization schemes for RF circuits , these attempts require the experience and knowledge of the designer in order to find an optimal circuit design [2]. Therefore, it seems very appealing to develop reliable automatic tools in RF IC design. These limitations can be solved by employing optimized procedures such as an evolutionary computation and Genetic Algorithms (GA). Genetic Algorithm models the natural evolution process in order to improve the parameters of an issue. Non-gradient-based random search is used in a genetic algorithm for the optimization of complicated processes [3].

1.2 Overview

In Radio Frequency (RF) communication systems that contain a receiver as well as a transmitter, CMOS technology is becoming essential. Low noise amplifiers are generally the first blocks in the receiver chain and those that process the incoming signal first. Because the signal has

undergone significant attenuation, the purpose of the LNA is to amplify it, and at the same time to minimize the noise added by the circuit itself. In the past, the trial and error method was the most common practice where the optimum point of operation was a product of many hours spent tweaking the design and trying to find the best one. The term "optimization" is translated as finding a design that provides a perfect balance in trade-offs such as power consumption, gain, noise figure and other performance parameters. This can be achieved by using a well-defined model of equations, which in combination with a genetic algorithm generates an approximation of an optimized LNA for the fine tuning of the circuit parameters [4] [5]. For their optimization ability, genetic algorithms (GAs) have been well known optimization tool. They are especially suitable for this application as the low noise amplifier problem design can easily be converted into a multi-objective search task [6]. It is possible to model many genuine engineering optimization problems as a multi-objective optimization problem (MOP). These problems actually have multiple goals that conflict with each other, and optimizing a particular solution for a single goal may result in unacceptable results with respect to the other goals. Evolutionary algorithms (EAs) have emerged as flexible and robust meta-heuristic methods to solve problems with optimization, achieving a high level of problem-solving effectiveness across each application domain [7]. The cause for taking multi objective genetic algorithm method to optimize LNA is that RF circuits usually have many of parameters. The reason of applying MOGA due to its low complexity and high efficiency in the selection of its optimization algorithm among the other algorithms [3].

Initially, Genetic Algorithm (GA) was developed to understand the processes of natural systems and design artificial systems which maintain the robustness and adaptability of natural systems [8]. Each unknown design variable in a genetic algorithm is called a gene, design variable produces - chromosome genes, and chromosomes are collected by a population. The idea of the genetic algorithm is to develop the population in each generation. The algorithm creates the individual population generation by using random variables in the present population to become parents and generate the next generation of children [5]. To manipulate the genetic composition of a population, GA uses three basic operators – selection, crossover and mutation. Each person is chosen to achieve his fitness value via an evaluation mechanism [7].

The basic use of genetic algorithms in analog integrated circuit design involves the representation as chromosomes of circuit variables and gene component parameters. The topology is developed using a topology structure which is ready to integrate with the other components. In electronic system design, analog integrated circuit design is very important. These designs may include topology circuit design and design of component values [9].

1.3 Literature Survey

In (1997), Shaeffer and Lee proposed a low-noise CMOS amplifier (LNA) that operates at a frequency of 1.5 GHz implemented in a global positioning system (GPS) receiver and voltage source 1.5 V using 0.6 µm CMOS process. This study also presents noise figure optimization methods, with a detailed discussion of the effects of induced gate noise in MOS devices [10].

In (2001), Andreani and Sjoland presented a technique implemented in the inductive source degeneration topology to substantially reduce the noise of the CMOS low noise amplifier by taking into account the effect of gate induced current noise on noise performance. Therefore, the effectiveness of the inductive source degeneration technique has been established without doubt [11].

In (2002), Goo et al. presented an integrated low noise amplifier in which the source degeneration inductance is adjusted to obtain optimal noise performance at 800-MHz LNA that has been implemented in a standard 0.24μm CMOS technology. This study also features the effect of device geometry on NF [12].

In (2005), Molavi and Hashemi have proposed a wideband CMOS LNA which is an extension to the previous narrowband power-constrained simultaneous noise-input matching (PCSNIM) LNA design technique which is a proposed method. In a 0.18μm CMOS technology, two wide-band single-ended cascode LNAs are designed to operate in the 1.5-2.5 GHz and 3.2-4.8 GHz frequency bands. These LNAs achieved a maximum forward gain based on simulation results [13].

In (2006), Noh et al. have proposed a low noise of 2.14 GHz (LNA) for use in a receiver with a Wide-band Code Division Multiple Access (W-CDMA). The LNA has been implemented in the CMOS 0.18um process of RF. Detailed description of the LNA architecture is presented and analyzed for the type of inductive source degeneration and the differential LNA topology. The circuit complies with the system's requirements [14].

In (2007), Qi and Jie have presented a 1.5V, 0.18μm CMOS low noise amplifiers with differential topology, thus, illustrating the advantages of this topology under a low supply voltage for GPS applications are also discussed in this paper [15].

In (2008), Xuan et al. suggested a differential CMOS LNA of 2.5 GHz used with a wireless RF receiver manufactured with 0.18 μm process CMOS. The differential architecture of two inputs and two outputs can efficiently restrict common mode interference and reduce underlay noise [16].

In (2008), Fan et al. reported noise-reduction methods and differential LNA linearity improvement. A 2.2 GHz inductively degenerated CS-LNA was produced using TSMC 0.35 μm CMOS technology. An inductor is added to the drain of the main transistor to reduce the noise contribution. It can reduce noise, enhance linearity, and increase the voltage gain of the LNA [17].

In (2009), Gorissen et al. proposed study of the performance of neural networks in relation to other methods of modeling. A high-dimensional, parameterized low noise amplifier RF circuit block is the case study under consideration [18].

In (2009), Radic et al. have presented a current-reuse technique using the same process such as a low noise amplifier working at the frequency 2.4 GHz to explain the impact of combining inductances on NF and gain in this work, it has been very seriously dealt with by including inductances effects in each one of them [19].

In (2009), Wang et al. have presented a minimum noise and maximum gain differential LNA for the range of frequencies between 3.3 GHz - 3.8 GHz. In this research, a noise reduction and increase gain were achieved by using differential and cascade circuit with effective balun [20].

In (2009), Chang et al. presented a fully integrated 5GHz low voltage and low power LNA using forward bias technology of current reuse through 0.18μm technology [21].

In (2010), Nor et al. have discussed the different topologies of low noise amplifiers such as current-reuse technique (CRT), power constraint simultaneous noise and input matching (PCSNIM) , and Folded Cascade (FC) PCSNIM [22].

In (2010), Muhamad and Nardin presented the design for Low Noise Amplifier (LNA) using 0.18μm technology and it based on W-CDMA standard application. The LNA function is to amplify extremely low noise signal without adding noise and also preserving required signal to noise ratio of the system at extremely low power level [23].

In (2012), Behzad et al. have presented a precise method for determining the device sizes in RF circuit based on a genetic algorithm (GA). HSPICE RF simulation is used to evaluate the fitness of the circuit specifications. Simulation results confirm the GA's effectiveness for reducing the sizes of the devices and optimization in LNA [3].

In (2012), Samir Barra et al. proposed Multi-Objective Genetic Algorithm (MOGA) methodology based on front Pareto to optimize the operational amplifier. The simulation results certify the efficiency of MOGA in

determining the device sizes in an analog circuit and mixed CMOS-based circuit applications [6].

In (2013), Vural et al. have presented optimization methods for sizing the differential amplifier with current mirror load. The aim is to minimize the transistor area of MOS using three evolutionary algorithms, differential evolution, artificial bee colony algorithm, and harmony search. The results of the simulation show that the proposed methods not only meet design specifications, but also achieve the design objective in a shorter computational time compared to previous methods, and enhance certain design specifications [24].

In (2014), Bhale and Dalal have proposed Low Noise Amplifier with standard United Microelectronics Corporation (UMC) 0.18 μm CMOS technology for Ultra-Wide-Band (UWB) applications. The Elitist Non-Dominated Sorting Genetic Algorithm (NSGA-II) was used in the proposed LNA design to obtain the optimum values of components. The Cadence Spectre-RF simulator was used to simulate the design [25].

In (2014), Chin et al. have proposed Genetic Algorithm (GA) to optimize multiple input variables in order to attain the required circuit design outcomes. GA is shown to be capable of optimizing both single objective Op-Amp and multi-objective LNA from the results of a single objective design study. The developed multi- objective GA optimizer is further compared to Gradient and Quasi-Newton 's ADS built-in optimizers [26].

In (2014), Kalentyev et al. have proposed an advanced synthesis based on GAs for design automation of linear and low noise microwave amplifiers. This allows the selection of the best transistor types (sizes) and DC biases,

together with the automatic generation of amplifier schematics directly from the performance requirements. The design of a 2-10 GHz single-stage MMIC LNA is shown as an example [27].

In (2017), Papadimitriou et al. have introduced a multi-objective radio frequency (RF) low-noise amplifier (LNA) optimization methodology using the MOS transistor analytical model in combination with genetic computation [28].

In (2017), Singh et al. have presented a new automated design methodology of designing a differential low-noise -amplifier with current mirror load. The heuristic optimization algorithm inspired by nature has the capacity to give a reasonable approximate solution. To verify the intended automated design methodology using the UMC 0.18 μm process, the MATLAB and CADENCE tool are linked. In order to check its efficiency in speed, time and robustness have been compared with previous design methodology [29].

In (2017), Joshi et al. have proposed a metaheuristic to optimize a low noise amplifier based on the hybrid technique of particle swarm optimization and simulated annealing scheme with Lévy flight (HPSO) [2]

In (2019), Mahesh Mudavath, K. Hari Kishore have presented the differential Low Noise Amplifier for wireless receiver at the frequency of 2.4 GHz. It provides less noise figure, high gain and good reverse isolation as well as good stability. The designed LNA is simulated with a 180 nanometers CMOS process [30].

Recently, in 2020, F. Gunes et al. have proposed a multi-objective optimization issue, a non-dominated genetic sorting algorithm (NSGA)-III is applied to the ultra-low noise amplifier (LNA). Providing a Feasible Design Target Space (FDTS) consisting of all trade-off relations between all the performance ingredients of the transistor to be used in the challenging LNA design [31].

1.4 Aim of Work

The aim of this project involves the implementation of Multi-Objective Genetic Algorithm in designing and realization different topologies of LNA. The following points summarize the main objectives of the current study:

1. Mathematical analysis for different topologies of LNA single-ended LNA and differential LNA at 2.4 GHz and 5 GHz.
2. Optimization using Multi-Objective Genetic Algorithm (MOGA) toolbox using in MATLAB to improve performance parameters noise figure, gain and power consumption.
3. Multi-Objective Genetic Algorithm (MOGA) is applied to minimize source inductor L_S and minimize gate inductor L_g to improve the fabrication requirement.
4. ADS simulation is used to verify mathematical and optimized results obtained with that specified.
5. Comparison is made between the techniques and topologies of LNA to find the advantage and limitation for each method.

1.5 Thesis Organization

The thesis is divided into five chapters. Chapter two presents a theoretical background for low noise amplifier and genetic algorithm method.
chapter three involves design and optimization of the single ended low noise amplifier at two different frequencies 2.4 GHz and 5 GHz.
chapter four design and optimization of differential low noise amplifier at two different frequencies 2.4 GHz and 5 GHz.
chapter five includes conclusions and suggestions for future researches.

CHAPTER 2

Theoretical Background

2.1 Introduction:

This chapter presents a theoretical background on LNA design, analysis and topologies. In addition, an introductory and illustration of optimization technique applied to improve LNA, Genetic Algorithm (GA) method are explained.

2.2 Fundamentals of LNA

Electronic transmitter and receiver circuits in communication systems transmit information to and from a certain communication medium. The receiver side presents challenges that are not present for the transmitter, or are greatly relaxed. This is mainly due to the nature of the communication channel, which results in the receiver input having a minimum detectable signal that can be as weak as a μ Volts. Such a signal must be accommodated by the receiver in order to ensure a reliable quality of the information transfer. The receiver ability to detect a weak input signal (i.e. its sensitivity) is fundamentally limited by the electrical noise at the receiver input [32].

As shown in Figure (2-1), a typical RF receiver will passes the received antenna signal first to the band pass filter (BPF) and then to the LNA. Usually, the signal that goes into the LNA is very weak and mixed with noise.

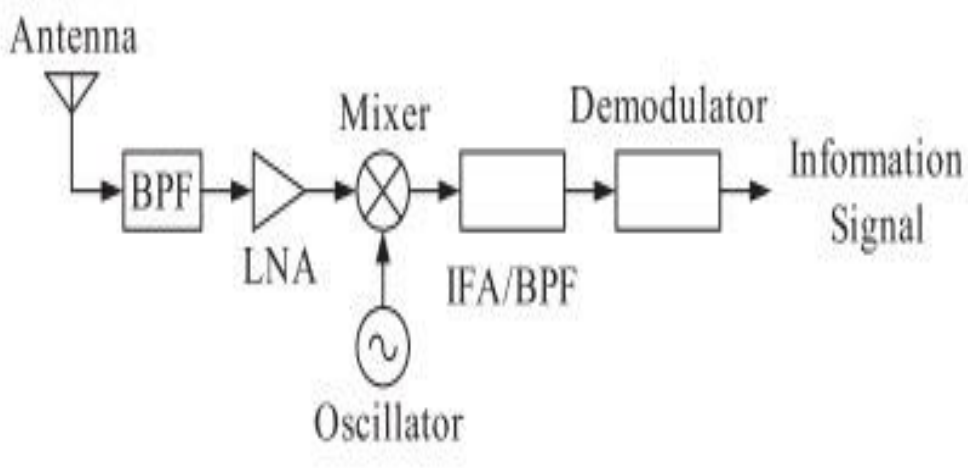


Figure (2-1): Block Diagram of a Typical RF Receiver

Per Frris' formula given in equation (2-1) for noise figure (NF), the receiver in the first few stages will dominate its overall NF.

$$\mathbf{F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots G_n}} \qquad \textbf{(2-1)}$$

Where G_n is the gain of the n-th stage, F_n is the noise factor of the n-th stage.Therefore, LNA plays an important role in amplifying the received signal while suppressing noise by an LNA gain factor for the subsequent stages. The noise generated by the LNA itself, however, is added directly into the signal received. It is therefore necessary for an LNA to increase the desired signal power while adding as little noise and distortion as

possible, enabling the retrieval of the information signal in the receiver at subsequent stages [33].

This leads to a particular situation: the noise figure of the cascaded system will be determined primarily by the noise figure of the first stage of the amplifier. Thus, the noise figure is mostly determined by the LNA in the receiver, which illustrates the significance of the concept for low-noise research. In addition, if a LNA is to be multi-stage amplifier, the first stage noise figure will be the dominant one [34].

2.2.1 LNA Performance Parameters

As the first step in the process when realizing a LNA, it is important to decide the specified performances. This is performed in a number of different parameters as follows [35].

1. Noise Figure (NF)

The fundamental parameter of noise performance is the Noise Factor (F), which is defined as the ratio of total output noise performance to output noise due to input source. The Noise Factor is called the Noise Figure (NF) when expressed in decibels. The Signal-to- Noise Ratio (SNR), which is the ratio of signal power and noise power, is another related and sometime mentioned in RF applications. Noise figure is commonly used to define the extra noise a circuit or system generates. Noise factor at the input to signal to noise power ratio at the output is defined as the ratio of the signal to noise power [36].

$$\boldsymbol{NF = 10\,log(F) = 10\,log\frac{SNR_{IN}}{SNR_{OUT}}} \qquad \textbf{(2-2)}$$

$$F = \frac{Total\ Output\ Noise\ Power}{Output\ Noise\ Power\ by\ Source\ Impedance} \quad \textbf{(2-3)}$$

Thus, the low-noise amplifier noise figure basically determines the sensitivity of the receiver. The LNA must therefore be designed to have as low as possible NF and maximum gain. The RF receiver sensitivity is defined as the minimum signal level that can be detected by the system with an appropriate signal-to- noise ratio [37].

Generally, noise in electronic circuits refers to small changes in current and voltage generated in electronic devices due to the fact that the electrical charge is not continuous, but rather is carried in discrete quantities and called process noise. The types of noise associated with electronic circuits are:

Thermal noise is the most widely used, the noise level depends only upon the temperature and the value of the resistance. Short noise is related with the leakage current of the drain-source diodes. The flicker noise so-called 1/f noise (also classified as pink noise). It should be noted that in MOSFETs, the surface conduction mechanism has the greatest contribution to flicker noise. Another kind of noise is called Burst noise (Popcorn noise), this type is made by changes between several distinct voltage or current stages [33].

Generation-recombination noise, that is the product of statistical generation and recombination of charge carriers.

Avalanche noise is a form of noise that doesn't happen in most circuits, but can happen when PN junctions are run near or at the point of avalanche breakdown, Measurement noise is the noise that generated by the unit

under test such as ammeter, voltmeter, oscilloscope, and spectrum analyzer is amplified to a suitable level - the gain of the amplifier must be known [34].

2. Gain

The LNA gain is its ability to amplify the input signal amplitude or power. It is defined as the ratio between the output and the input signal, and is often defined as decibels [36].

$$\textbf{Voltage Gain} = 10 \log \frac{\frac{v_{out}^2}{R_{out}}}{\frac{v_{in}^2}{R_{in}}} = 20 \log \frac{v_{out}}{v_{in}} \qquad \textbf{(2-4)}$$

Power gain is a measure of an LNA ability to amplify signal power measured by the ratio of the signal output to signal input power. Power gain is usually defined in terms of decibel (dB) on a logarithmic scale [33]. The gain of the LNA must be large enough to minimize the noise contribution of stages later as shown in equation (2-1), specifically the downconversion mixer(s). However, the choice of high gain leads to a compromise between the noise figure NF and the receiver linearity as greater gain makes the nonlinearity of the subsequent stages more pronounced. The LNA drives the mixer directly in modern RF communication system, with no impedance matching between them. Thus, performing the chain calculations in terms of voltage gain, rather than power gain, of the LNA is more meaningful and simpler. In the case of a 50 Ω matched LNA input and output impedance, however, voltage and power gain are the same [5].

3. Power Dissipation

With technology scaling down the need for Integrated Circuits (IC) that consume less power becomes more significant. However, since the supply voltage is reduced, the available voltage may become too small. However, when the power is of primary interest, e.g. in portable devices, power dissipation should be considered strongly during the design process, the LNA consumes only a small fraction of the total receiver power. For LNA design, circuit designers should consider power dissipation along with figures of merit (FOM), such as noise, linearity, gain and trade-offs among them [5].

4. Linearity

In a wireless receiver, the linearity of low-noise-amplifiers (LNA) is the most important for reducing inter-modulation distortion. It is worth optimizing for linearity at every stage in the chain. Linear operation is crucial, especially if the input signal is weak in close proximity with a strong interference signal. This is because unwanted distortion of inter-modulation, such as blocking and cross modulation, is possible in such a scenario, the two LNA parameters that characterize its linearity are the Third-Order Intercept (IP3) and the 1-dB compression point (P_{1dB}) [38],[39]. 1-dB compression is referred to the input power that induces a 1 dB reduction in linear gain due to system saturation. IP3 is referred to the input power at which the amplitude of the third-order intermodulation (IM3) term equals the amplitude of the linear fundamental term. Linearity is also an important limitation with design [33]. The third order intercept point IP3 has emerged as an important parameter in the design of LNA. Increasing the current density or current drawn by LNA is the easiest way

to improve the IP3 efficiency for a given frequency. If the current drawn is less important than IP3 performance, then with the usual slight increase in gain and NF, it can be increased. Thus, it can achieve an important improvement by considering a trade-off in between current draw and NF [40].

5. Input Matching

Usually, LNA is inserted between the antenna and the demodulation circuit with minimal possible loss of insertion. The only way to accomplish this is the need for careful matching of impedance, that is, controlling the amplifier input and output impedances as seen by the source and the load. Matching a general amplifier is typically done to ensure maximum transmission of power occurs between the amplifier and the load. Matching in LNAs also helps to reduce power loss and degradation in SNR (or the noise figure). In LNA design, this is called simultaneous power and noise matching due to the requirement to reduce the minimum detectable signal level [34].

6. Scattering Parameters

The design of analog LNA starts by considering it as two-port network. The two-port network is used to determine gain, noise figure, linearity, and stability [4]. S-parameters play an important role in RF communication systems design, since conventional open and short circuit measurements are no longer available at radio frequencies because of the inductance of the cable, a short circuit at radio frequencies acts differently from an open circuit, which has capacitive conduct. As a result, using standard h- and z-parameters is challenging. Furthermore, calculation of incident and reflected wave strength in a two-port network for RF blocks is of concern. These two-port network parameters are better defined using S-parameters [41]. S-parameters are the best way of describing those two-port network parameters. The scattering parameters, or S-parameters, relate incident voltages and reflected waves through the scattering matrix, at n-ports. The two-port network shown Figure (2-2) can be described as:

$$\begin{bmatrix} V_1^- \\ \dots \\ V_n^- \end{bmatrix} = \begin{bmatrix} S_{11} & \dots & S_{1n} \\ \dots & & \dots \\ S_{n1} & \dots & S_{nn} \end{bmatrix} \begin{bmatrix} V_1^+ \\ \dots \\ V_n^+ \end{bmatrix} \qquad \textbf{(2-5)}$$

Where V_i is the voltage amplitude at port i , positive and negative sign signal are related to the incident and reflected waves respectively. Through the following equation, a specific S-parameter can be determined:

$$S_{ij} = \frac{V_i^-}{V_j^+} \qquad \textbf{(2-6)}$$

This means that the S-parameter S_{ij} can be determined as the ratio between the reflected wave voltage at port i and the incident wave at port j when the

other ports are switched off with the corresponding load to avoid reflections.

- S_{11}- Input reflection coefficient
- S_{12}- Reverse voltage gain
- S_{21}- Forward voltage gain
- S_{22}- Output reflection coefficient

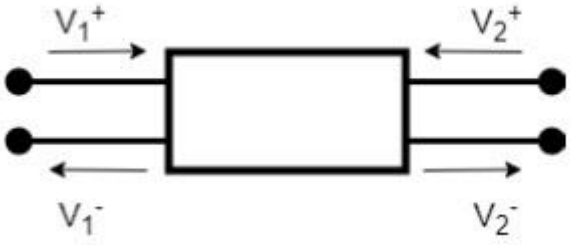


Figure (2-2): Incident and Reflected Waves in a Two-Port Network [42]

In the LNA design, the S-parameters are very important because of the need for input matching associated with the return loss indicating a fraction of the incident power reflected back to the source. The loss of the input return is represented by the following equation:

$$\boldsymbol{R_L = -20\,log\,(|S_{11}|)} \qquad \textbf{(2-7)}$$

Where designers aim to have a return loss of at least 10dB, implying a maximum of 10 percent of the power reflected back to the source [42].

7. Stability

The circuit might become unstable for certain combinations of source and load impedances when feedback paths from the output to the input exist. A LNA design is normally stable which may oscillate at the extremes of the variations in production or voltage, and may be at unexpectedly high or low frequencies. Factor for stability is given by:

$$K = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{21}||S_{12}|} \quad \textbf{(2-8)}$$

$$\Delta = S_{11}\,S_{22} - S_{12}\,S_{21} \quad \textbf{(2-9)}$$

Where K >1, Δ < 1, that circuit is stable unconditionally. A LNA design is a multi-dimensional problem of optimization, there are many trade-offs involved because the optimization of each individual specification does not arrive at the same solution for sizing or biasing. This requires the designer to consider what is the best combination of performance specifications for the LNA intended use [39].

8. Quality Factor

The quality factor (Q) is a parameter of the rate of loss of energy in the entire network or in single inductor or capacitor. The quality factor is defined on two factors, one is circuit damping performance Q means get bigger, the resonator becomes less damped, and the other depends on the frequency ratio to resonator bandwidth [34].

$$Q = \frac{f_r}{\Delta f} \quad \textbf{(2-10)}$$

Where f_r is the resonant frequency and Δf is the bandwidth. Other common definitions of Q are given in equations below[43]:

$$Q = 2\pi * \frac{Energy\ stored}{Energy\ dissipated\ per\ cycle} \quad \textbf{(2-11)}$$

$$Q_L = \frac{X_l}{R} = \frac{\omega L}{R} \quad \textbf{(2-12)}$$

X_L represents reactance of inductor, while R represents the total inductor equivalent resistance.

2.2.2 Mathematical Analysis of LNA:

Determining the minimum noise figure is a common and well-understood procedure in the design of low noise amplifiers. A small-signal amplifier model is typically assumed initially, an expression for F is formed, and differentiation leads to a unique source impedance that optimizes noise performance. The device geometry is flexible in an integrated circuit environment and can be incorporated into the optimization process. Thus, it starts by specifying a desired design parameter, such as gain or power consumption, under perfect matching input conditions. Then, through the optimization procedure, it determines the appropriate small signal model posteriori. By analyzing the circuit in Figure (2-3), the noise figure of the LNA can be calculated.

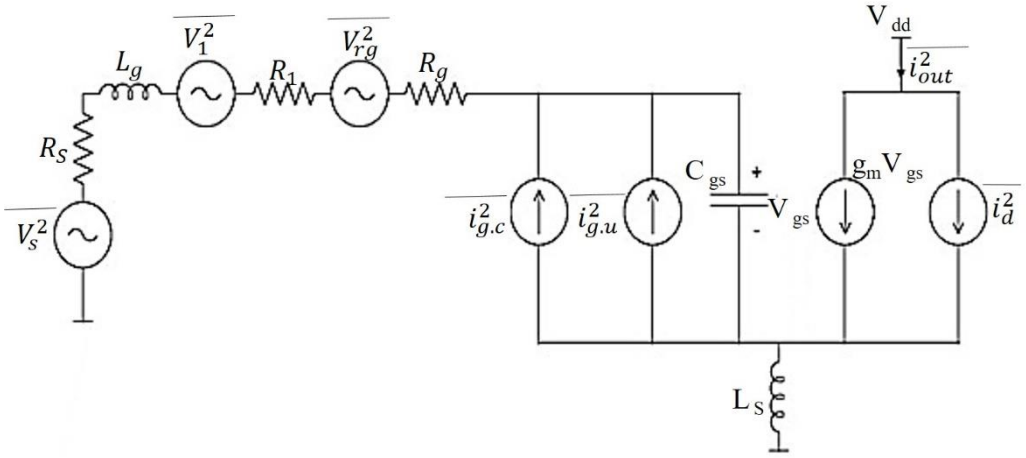


Figure (2-3): Equivalent Circuit for Input Stage for Noise Calculation [44].

Where R_l describes the resistance of inductor L_g , R_g is the NMOS device's gate resistance , i_d^2 defines the device's channel thermal noise.

The Q and Ls can be independently determined in the device geometry producing optimized results, noise performance with excellent input match [44].

There are two approaches to this problem of optimization that merit particular attention. The former takes on a fixed transconductance G_m for the amplifier. The second assumption is a fixed consumption of power. The expression for F may be given as:

$$\boldsymbol{F = 1 + \frac{R_1}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\frac{\chi}{Q_s}\left(\frac{\omega_o}{\omega_T}\right)} \qquad \textbf{(2-13)}$$

Where γ represents coefficient of channel thermal noise , $\alpha = \frac{g_m}{g_{d0}}$, R_S is the resistance of source , g_{d0} is the drain-source conductance at zero drain source bias voltage; ω can be expressed as ω =2*π*f , f is the operating frequency. To illustrate the second approach, the expression for F in Equation (2-13) can be rewritten to make its dependence on Power Dissipation P_D explicit. But, making dependency on G_m explicit is non-trivial. Fortunately, the constant G_m condition is equivalent to the constant $\boldsymbol{\omega_T}$ condition

$$\boldsymbol{G_m = g_{m1}Q_{in} = \frac{g_{m1}}{w_0 C_{gs}(R_S+\omega_\tau L_S)} = \frac{\omega_\tau}{w_0 R_S(1+\frac{\omega_\tau L_S}{R_S})} = \frac{\omega_\tau}{2w_0 R_S}} \quad \textbf{(2-14)}$$

By reformulating F in terms of ρ and P_D to facilitate both optimizations in order to maintain a fixed $\boldsymbol{\omega}$.

2.2.2.1 Fixed Gm Optimization

In order to set the transconductance value, G_m, is only needed to assign a constant value to ρ.

$$\omega_\tau \approx \frac{g_m}{C_{gs}} = \frac{g_m}{\frac{2}{3} W L C_{ox}} = \frac{3}{2} \frac{\alpha \mu_{eff} (v_{gs} - v_T)}{L^2} = \frac{3 \alpha \rho v_{sat}}{L} \qquad \textbf{(2-15)}$$

C_{ox} is the gate per unit area capacitance of transistor, μ_{eff} represents the field-limited mobility of electron, V_{gs} represents gate to source voltage ,V_T is threshold voltage, Vsat is the velocity of saturation, and ϵ_{sat} velocity saturation field strength is defined as the lateral electric field for which mobility flows to half of its low field value. When $\rho = \frac{\delta \alpha}{5 \gamma}$, the parameters for ρ are depend on the technology, but typically γ is set between 2 - 3 (normally 2), δ is set to 2 - 3 times the value of γ (normally 4), α is assumed to be 0.8 -1 (taken to be 0.9)"[45].

The suitable value of Gm is easily determined by replacing it with the expression previously found in (2-14). The G_m relationship with ρ is given by:

$$G_m = \frac{3 v_{sat}}{2 \omega_0 R_S L} \frac{\rho(1+\frac{\rho}{2})}{(1+\rho)^2} \qquad \textbf{(2-16)}$$

Once ρ is determined, the noise factor can be minimized by taking[44]:

$$\frac{\partial P(\rho, P_D)}{\partial P_D} = 0 \qquad \textbf{(2-17)}$$

Which results, after certain algebraic manipulations:

$$P_{D_{opt,G_m}} = P_0 \sqrt{\frac{P3(\rho)}{P1(\rho)}} = P_0 \frac{\rho^2}{1+\rho} \left(1 + \frac{5\gamma}{\delta \alpha^2}\right)^{-1/2} \qquad \textbf{(2-18)}$$

This expression gives the power dissipation under the assumption of matched input impedance which yields the best noise performance for a given G_m. However, the Q_L is:

$$Q_L = \frac{P_0}{P_D} \frac{\rho^2}{1+\rho} \qquad \textbf{(2-19)}$$

By comparing equations (2-18) and (2-19), it can be seen that the optimum quality factor can be obtained when:

$$\boldsymbol{Q_L = Q_{L_{opt,G_m}} = 1 + \sqrt{\frac{5\gamma}{\delta\alpha^2}} \geq 1.87} \qquad \textbf{(2-20)}$$

Therefore, at some specific input, the best noise performance for a given transconductance is achieved. Note that the 1.87 value is only valid value for devices with long channels. The optimum Q_L is to be somewhat larger for short channel lengths, where $\alpha < 1$ is used. By replacing equation (2-20) with equation (2-13), it can be determined that the minimum noise factor (inductor neglect and gate losses) is:

$$\boldsymbol{F_{min,Gm} = 1 + \sqrt{\frac{4}{5}\delta\gamma}\left(\frac{\omega_0}{\omega_\tau}\right)\left\{|C| + \sqrt{1 + \frac{5\gamma}{\delta\alpha^2}}\right\} \geq 1 + 1.33\left(\frac{\omega_0}{\omega_\tau}\right)} \qquad \textbf{(2-21)}$$

2.2.2.2 Fixed P_D Optimization

An alternative optimization method fixes the power dissipation and adjusts to find the minimum amount of noise. The phrase for $P(\rho, P_D)$ is very complicated in ρ for the optimal point to yield a closed form solution. However, a simplifying assumption can be adopted and its validity can be checked by graphical comparison. If assume that this is ρ <<1, it is then possible to simplify $P(\rho, P_D)$:

$$\boldsymbol{P(\rho, P_D) \approx \frac{\frac{P_D}{P_0}\left(1+\frac{\delta}{5\gamma}\right)+2C\sqrt{\frac{\delta}{5\gamma}}\rho^2+\frac{P_0}{P_D}\frac{\delta}{5\gamma}\rho^4}{\rho^3}} \qquad \textbf{(2-22)}$$

This term is minimized for a fixed expression when:

$$\boldsymbol{\frac{\partial P(\rho,P_D)}{\partial \rho} = 0} \qquad \textbf{(2-23)}$$

Solving this equation, on the assumption that ρ <<1 is:

$$\boldsymbol{\rho^2}_{\boldsymbol{opt,P_D}} = \frac{\boldsymbol{P_D}}{\boldsymbol{P_0}} \boldsymbol{|C|}\sqrt{\frac{\boldsymbol{5\gamma}}{\boldsymbol{\delta}}}\left[\boldsymbol{1} + \sqrt{\boldsymbol{1} + \frac{\boldsymbol{3}}{\boldsymbol{|C|^2}}\left(\boldsymbol{1} + \frac{\boldsymbol{\delta}}{\boldsymbol{5\gamma}}\right)}\right] \qquad \textbf{(2-24)}$$

By comparing (2-24) with (2-20), it is evident that the value for ρ is equivalent to the optimum Q_L of:

$$\boldsymbol{Q_{L_{opt,P_D}}} = \boldsymbol{|C|}\sqrt{\frac{\boldsymbol{5\gamma}}{\boldsymbol{\delta}}}\left[\boldsymbol{1} + \sqrt{\boldsymbol{1} + \frac{\boldsymbol{3}}{\boldsymbol{|C|^2}}\left(\boldsymbol{1} + \frac{\boldsymbol{\delta}}{\boldsymbol{5\gamma}}\right)} \approx \boldsymbol{3.9}\right. \qquad \textbf{(2-25)}$$

It is clear, that the optimum Q_L for dissipation of fixed power is larger than the optimum Q_L for a fixed Gm. From these analogies:

$$\boldsymbol{F\_(min, P_D)} \approx \boldsymbol{1 + 2.4\frac{\gamma}{\alpha}\left(\frac{\omega_0}{\omega_\tau}\right) \geq 1 + 1.62\left(\frac{\omega_0}{\omega_\tau}\right)} \qquad \textbf{(2-26)}$$

The value of 1.62 is valid only at the long-channel limit; for short-channel devices in velocity saturation, the value will be somewhat larger [46] .

2.2.3 Basic Low Noise Amplifier Realization and Topologies

There are different low noise amplifier topologies that can be used to meet the main requirement. Each topology has its advantages and limitations, which gives the analog designer various solutions in accordance with the application specifications. The basic topologies may include the single ended low noise amplifier and differential low noise amplifier[5].

The CMOS technology realization of LNA becomes an attractive method due to its simplicity in operation and in fabrication as monolithic IC. There are several basic realizations for single ended narrow band low noise amplifier low-power , low-voltage design such as resistive common source termination, common gate, shunt series common source feedback, inductive common source degeneration , and cascode source degeneration as shown in Figure (2-4) [47].

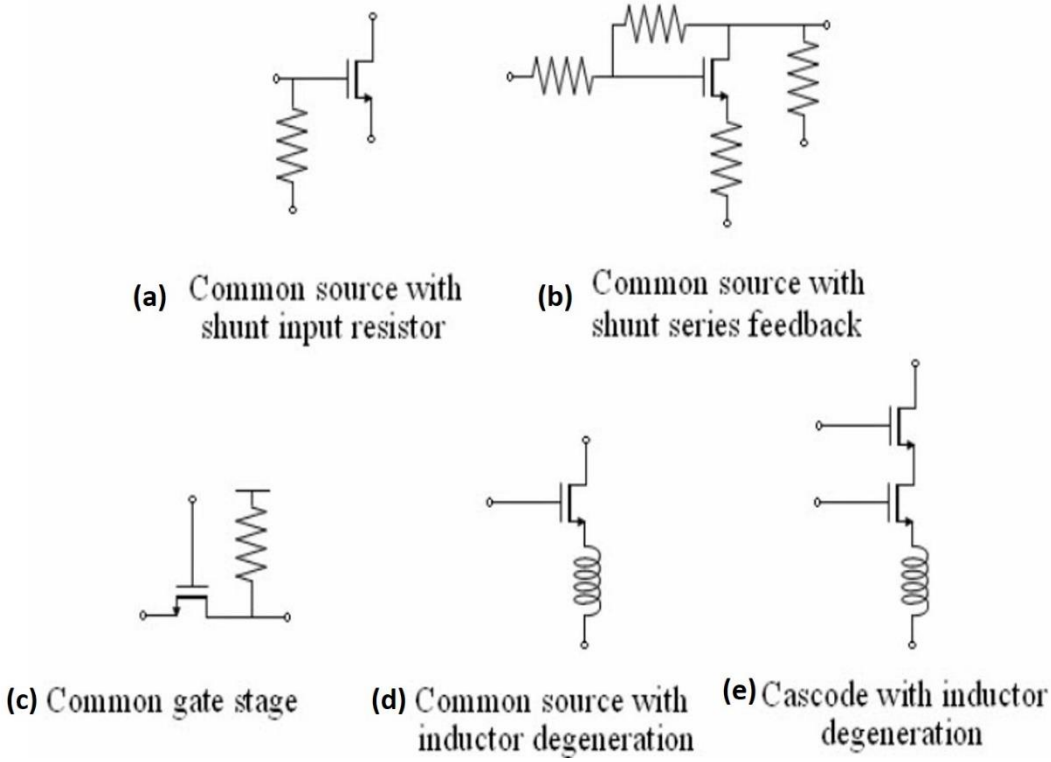


Figure (2-4): LNA Topologies

A. Common Source (CS) with Inductive Degeneration

Due to its advantages such as low noise figure of input matching, high gain and low power consumption, the inductively degenerated LNA is the dominant topology for narrow-band systems [48]. Figure (2-5) presents common source inductive degeneration single ended LNA, the input inductor is L_g, the source inducer is L_S, and the inductive load is represented by $j\boldsymbol{\omega}L$ [4]. In order to establish the necessary purely resistive input, L_g and L_s are used to provide inductance to counteract the capacitance of C_{gs}. It is a narrow band because, due to the resonant nature of the reactive matching network, the impedance matching is only established within a very narrow frequency range [35][49].

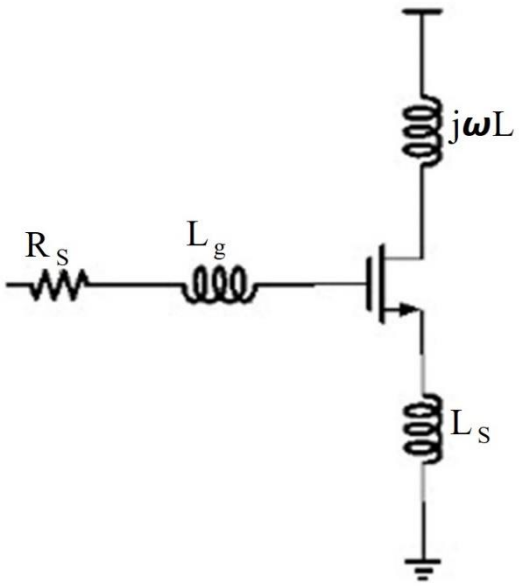


Figure (2-5): Common Source of Inductive Degeneration [4]

Consider the LNA 's small-signal model as shown in Figure (2-6) where i_{in} is the transistor input current, i_o is the current output of the transistor, g_m

is the transductance of the input transistor, and C_{gs} is the gate-to-source capacitance ; therefore, according to the KVL rule, the input voltage can be derived from the small-signal model [4]:

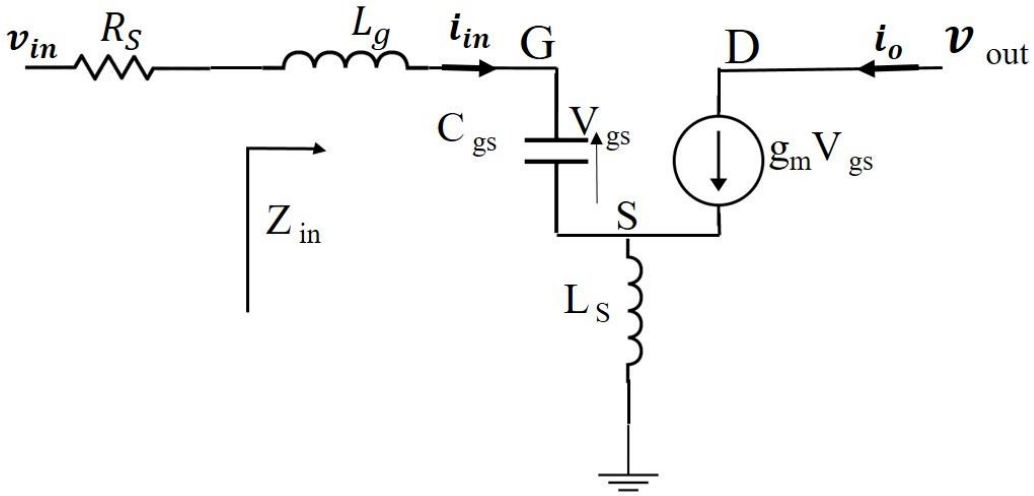


Figure (2-6): Small Signal Model of LNA

$$v_{in} = i_{in}(j\omega L_g + j\omega L_S) + i_{in}\left(\frac{1}{j\omega c}\right) + i_o(j\omega L_S) \qquad (2\text{-}27)$$

The current output is:

$$i_o = g_m v_{gs} = g_m i_{in} * \left(\frac{1}{j\omega C_{gs}}\right) \qquad (2\text{-}28)$$

so

$$v_{in} = i_{in}(j\omega(L_g + L_S)) + i_{in}\left(\frac{1}{j\omega C_{gs}}\right) + \frac{g_m L_S}{C_{gs}} \qquad (2\text{-}29)$$

Impedance is then derived at the input port as:

$$Z_{in} = j\omega(L_S + L_g) + \frac{1}{j\omega\, C_{gs}} + (\frac{g_{m1}}{C_{gs}})L_S \qquad (2\text{-}30)$$

The following equality should be used for matching the parasitic capacitor:

$$\omega_0(L_S + L_g) = \frac{1}{\omega_0 C_{gs}} \quad \textbf{(2-31)}$$

Since the load is usually having a resistance of 50 Ω, it is possible to calculate the inductor value from the following expression:

$$R_S = \frac{g_m}{C_{gs}} L_S = 50\,\Omega \quad (2\text{-}32)$$

The 50 Ω resistor R_S is connected at the input of LNA terminal, and thus, provide a matching input. At the resonant frequency, the inductance at the gate of NMOS removes the gate to source capacitance C_{gs} of M1, and therefore making the NMOS input impedance real i.e., only input resistance R_{IN} [45].

This topology provides control over the real part of the input impedance without passing the noise of the material resistors in the circuit. Cascoding improves the insulation of input-output as there is no direct connection from output to input [50] .

Noise is mainly due to the contribution of drain noise, gate noise and noise are due to the correlation between the gate and drain noise. Considering the series resistance of the inductors used in the LNA, an additional term should be added. The noise of the degeneration inducer from series resistance is negligible. Gate noise is the biggest of all contributors to noise. This is because the gate noise current is highly impeded by the resonance of the network matching the input[51]. Inductive source degenerated LNA topology is frequently used due to its low noise amplifier and sufficient gain [41].

B. Design of the Transistors

To calculate the size of the transistors, the thickness of the gate-oxide t_{ox} must be known, and the following parameters should be calculated:ε_0 the permittivity of the free space, ε_s the relative permittivity of the material, and ε_{ox} the permittivity of the silicon dioxide [4].

$$\varepsilon_{ox} = \varepsilon_0 * \varepsilon_s \quad \textbf{(2-33)}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad \textbf{(2-34)}$$

Where C_{OX} is the capacitance of gate oxides, μ_n is the mobility of carriers.

$$W_{M1} = \frac{1}{3\omega_0 L C_{ox} R_S} \quad \textbf{(2-35)}$$

Thus, the capacitance gate to source can be calculated by [4]:

$$C_{gs} = \frac{2}{3} W_{M1} L C_{ox} \quad \textbf{(2-36)}$$

$$g_m = \sqrt{2 \mu_n C_{ox} \frac{W_{M1}}{L} I_{DM1}} \quad \textbf{(2-37)}$$

$$w_T = \frac{g_m}{C_{gs}} \quad \textbf{(2-38)}$$

$$L_S = \frac{R_S}{w_T} \quad \textbf{(2-39)}$$

$$(L_S + L_g) = \frac{1}{\omega_0{}^2 C_{gs}} \quad \textbf{(2-40)}$$

$$L_d = \frac{1}{\omega_0{}^2 C_L} \quad \textbf{(2-41)}$$

C. Cascode LNA

Cascode LNA promises high performance, good noise, low power consumption, and high reverse insulation [52][53][54]. As a result, the cascode stage has superior performance in noise. Unfortunately, at very high frequencies, excellent noise and gain performances are no longer valid. This is due to the parasitic admission to the drain-source common node, which increases with increasing frequency [55][56]. Due to the lower impedance in the upper transistor source, its drain noise appears in the output [57][17]. Like a CS stage, the cascode stage is suitable for applications with a narrowband, however, feedback techniques enable multi-band and wide-band applications to use the cascode stage[58][59]. One of the most widely used techniques for reducing the effect of this capacitance in CMOS RF LNAs is cascode configuration. Cascode amplifier is a two-stage circuit consisting of an amplifier for transconductance followed by a buffer amplifier. The word "cascode" had its origin in the phrase "cascade to cathode." This circuit has many advantages over the single stage amplifier. This may include input output isolation, better gain, greater bandwidth, higher input impedance, higher output impedance, and good stability [51].

As shown in Figure (2-7) the M_2 cascoding transistor helps to reduce the interaction between the tuned output and the tuned input. The RF input is connected by the coupling capacitance C_s to the amplifier gate. Output Inductor L_d resonates with output load to maximize output transmission and resonance frequency gains. The width of the cascoded transistor must be measured in order to reduce and increase the parasite source capacity of M_2 by compensating a common source (both are consequence of a wider M_2). Cascode transistor helps reduce the effect of S_{21} and C_{gd1} Miller. R_{bias} is large enough to be ignored by its equivalent current noise [46].

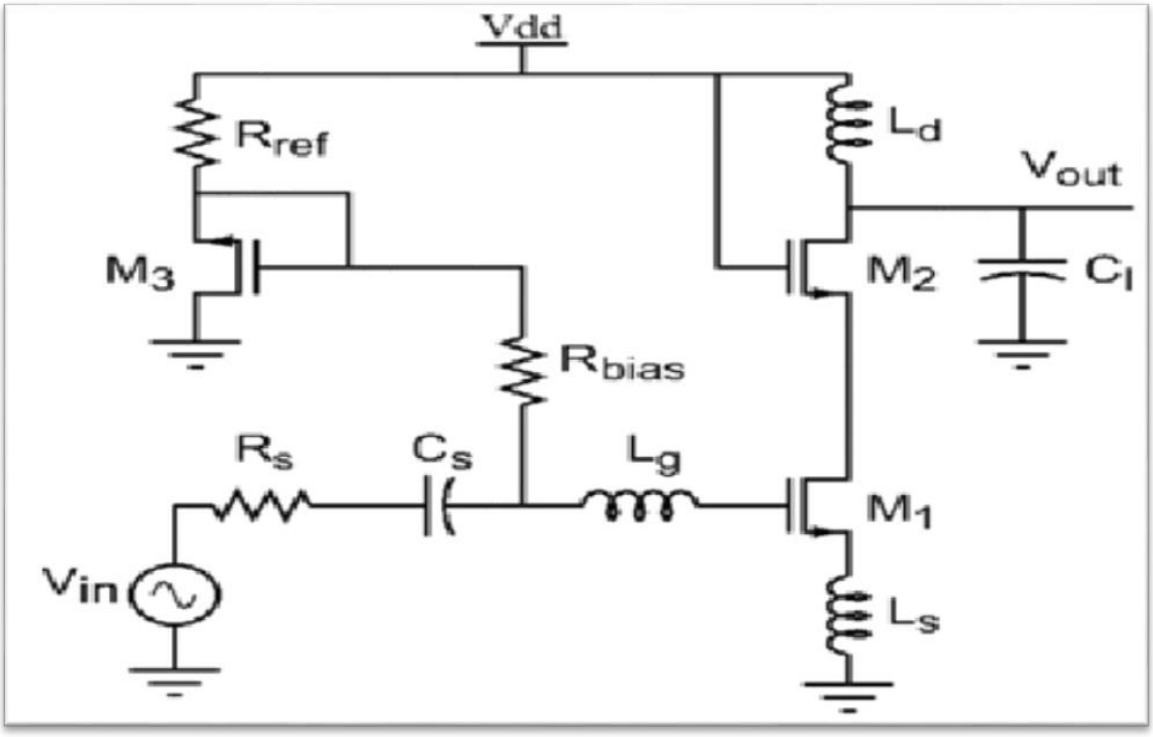


Figure (2-7): Cascode Source Degenerated LNA Topology [60]

In order to ensure that the input impedance is purely resistive at resonance frequency, the inductor L_g is necessary [50].Transistors M_1 and M_3 that form the current mirror are aware of the biasing circuit. The width of the

transistor M_3 is generally kept at a small fraction of the width of the transistor M_1 in order to achieve the lowest overhead power of the bias circuit [60].

D. Differential LNA Topology

The differential topology represents a single-ended structure in a symmetrical form. Thus, a differential structure can first be realized by the design of single ended structure and symmetry on both sides [44][50].

Using single-ended signaling LNA designs typically result in smaller chip sizes than those with differential signals. Single-ended signaling, however, suffers from parasitic ground inductance, which will usually cause considerable degradation in an LNA 's performance. The main advantage of differential stage is the reduction of distortion of the second order and dismiss common-mode noise. Differential LNA topologies as shown in Figure (2-8), are thus almost immune to problems of stability or degradation of performance caused by parasitic feedback loops. In addition, DLNA output is desired when connecting to mixer cells [6].

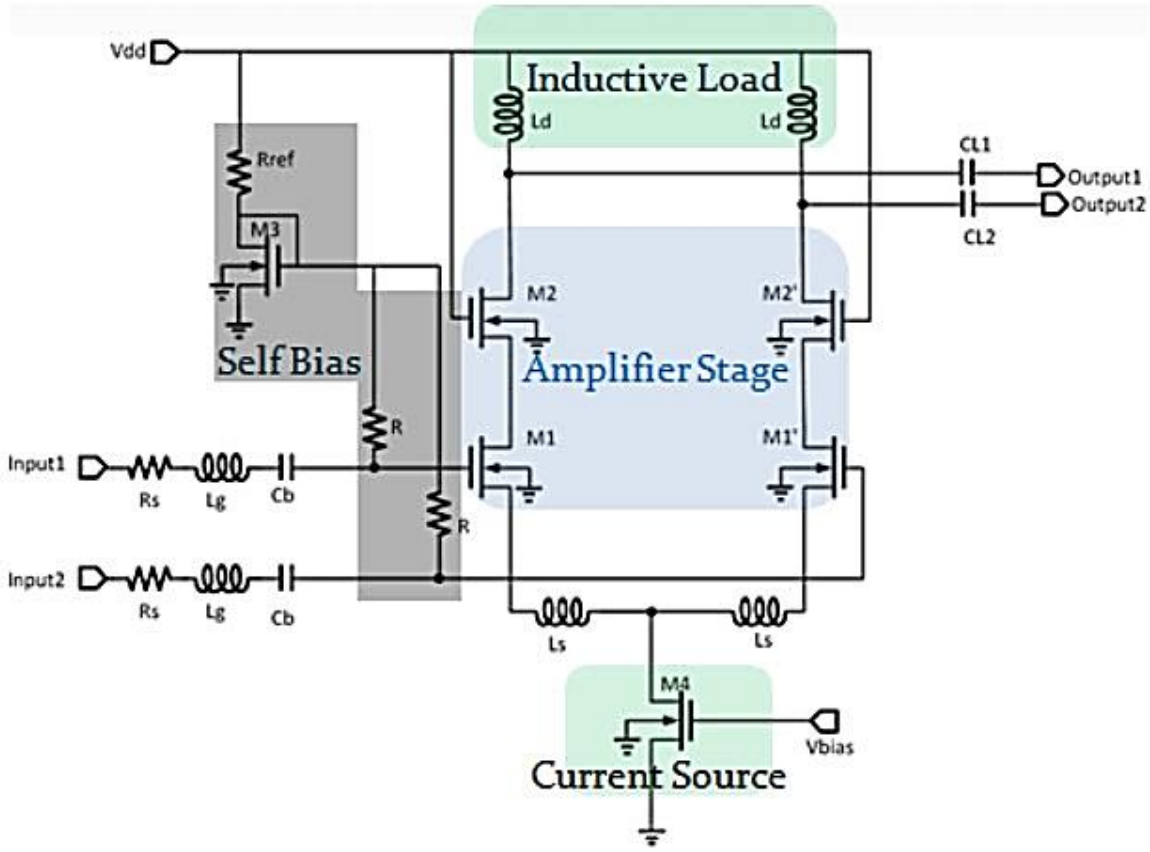


Figure (2-8): Differential LNA Topology [4]

Generally, a 50 Ω input impedance is set in the single stage design by making g_m= 20 and the virtual ground degenerative inductor (L_S). The current source is connected to the negative supply set in the differential type of LNA to give twice the current flowing one of the LNA sections.

The use of an 'ideal' balun (balanced to unbalanced) transformer is not to provide a differential signal for each LNA input. Furthermore, another balun is used at the amplifier output to re-combine the signal to simulate the voltage gain [11][20]. As shown in Figure (2-8), the main transistors are M_1 and M_1 which represent the input of differential LNA, while the cascading transistors are M_2 and M_2 that are needed to decrease the interaction of the tuned input with the tuned output ,to minimize the amount of the C_{gd} of M_1 , and to enhance the gain. . To maintain the symmetry, the

width of the M_1, M_1, M_2, and M_2 transistors is kept to be the same. C_b , C_{L1} ,and C_{L2} are the blocking capacitors. Transistor M_3 is used for biasing, and it also forms a current mirror with the M_1. The width of the bias transistor M_3 is adjusted to be the one-tenth of the main transistor to provide the correct biasing current. The source inductor or the degenerated inductor (L_s, L_s), and gate inductor (L_g and L_g) play an important role in trying to obtain the frequency of resonances. Thus, the values of these inductors are adjusted to provide the resonant frequency the device has to operate at. Two drain inductors L_d are applied to match the output impedance [4] [40] [41]. However, differential LNA has higher noise factor than its one-ended counterpart for equal power consumption. In addition, it requires more silicon area of single ended counterpart, twice [6].

2.2.4 Comparison Between Single-Ended and Differential Structures

The main reason for using a differential topology is the rejection of the common mode, noise appears in common-mode on the power supply lines and is not seen at the output. This greatly reduces possible digital switching noise problems when integrating both RF, analog and digital base band on the same chip. In addition, the even harmonics appear as common mode, and are similarly eliminated. Some blocking signal that has a second-harmonic in the signal band is disarmed in this way. The main disadvantage of differential topologies is that they demand more or less twice the power for equal performance. Obviously this trade-off should be considered separately for each application.

Gain, noise, linearity, power consumption, stability, and input matching are the main specifications for characterizing the performance of any

integrated LNA. These specifications depend on the topology of the circuits. Since narrow-band applications are the focus of this study, a common-source LNA seems to be a good choice. However, this topology suffers from the poor insulation between input and output, due to the parasitic capacitance gate-to-drain C_{gd}, significantly increases the chance of instability [61].

.

2.3 Optimization Techniques

Optimization problems are formulated by incorporating various factors, objective functions, and constraint functions. In general, these problems can be solved by either conventional optimization technique, or by heuristic methods [2]. Optimization is the process of improving and obtaining the best solution of any case problem or process. An engineer or scientist stirs up a new idea and that idea is improved by optimization. Optimization involves testing variations on an initial concept and using the information gained to improve the idea. Computer is the perfect tool for optimization as long as the idea or variable that influences the idea can be entered in electronic format [62].

2.3.1 Genetic Algorithm

A Genetic Algorithm GA is a method based on natural selection, which is drives biological evolution, and belongs to the larger class of evolutionary algorithms for solving optimization problems. The genetic algorithm can be used to solve a variety of optimization problems that are not appropriate for standard optimization algorithms, including problems where discontinuous, non-differentiable, stochastic, or highly non-linear objective functions are involved.

The genetic algorithm is an optimization and search technique based on the genetic and natural selection principles. A GA allows a population composed of many individuals to evolve to a state that maximizes "fitness" under specified selection rules (i.e. minimizes the cost function). The method was developed by John Holland (1975) during the 1960s and 1970s and finally popularized by one of his students, David Goldberg, who for his dissertation was able to solve a difficult problem involving control of

gas-pipeline transmission (Goldberg, 1989). Holland's original work has been summed up in his book. He was the first to try using his schema theorem to develop a theoretical basis for GAs. De Jong 's work (1975) demonstrated the GA 's utility for function optimization and made the first concerted effort to find optimized GA parameters with its successful applications and excellent book (1989) Goldberg probably contributed the most fuel to the GA fire. Several versions of evolutionary programming have been tried since then with varying degrees of success.

2.3.2 Advantages of a GA

- Optimizes with discrete or continuous variables.
- Doesn't need derivative information.
- Searches at the same time from a wide sampling of the cost surface.
- Deals with a significant number of variables.
- Is suitable for parallel PCs.
- Optimizes variables that have extremely complex cost surfaces (they can leap from a minimum local level).
- Gives a list of optimal variables and not just a single solution.
- Can encode the variables so that the encoded variables are optimized.
- Works with data generated numerically, experimental data, or analytical functions.

These advantages are fascinating and produce stunning results when traditional approaches to optimization fail miserably [62].

Genetic algorithms have many attributes which make them good choices when solving very complicated problems. The Algorithm 's simplicity and robustness made it popular among developers.

2.3.3 GA Concepts

This section includes several concepts of genetic algorithms and formulation of them in MOGA-Spice.

- **Chromosomes**

The concept of the chromosome is central to all genetic algorithms. The chromosome contains all the necessary information to describe an individual Chromosomes consist of DNA in nature. A long binary or string is used on a computer. Chromosomes consist of genes that can be optimized for different characteristics and can be of any length depending on the number of parameters to optimize [63]. The GA Toolbox supports binary, integer and floats representation of Chromosomes [64].

- **Design Variables**

The design variables are called the parameters chosen to describe a system design. Selecting the set of design variables may be the first and significant step in the formulation of an optimization procedure. The choice of the design variables is entirely determined by the designer to add flexibility to the procedure. It may be important to have more variables than necessary. These variables are represented by numerical value so that they are eliminated from problem formulation. It is usually better to have independent design variables, so that any of these can be altered without any need to alter any of the others [65].

- **Fitness Function**

Also referred to as the evaluation function, the genetic algorithm component rates a possible solution by calculating how good they are in relation to the current problem area [66].

- **Design Constraints**

All restrictions that are placed on a design are called constraints collectively. Most designs require that certain functions be greater or less than a given value. They also have conditions imposed on them by some variables. These conditions are translated into problems as constraints which the design solution must satisfy [65] [67].

- **Linear/Nonlinear Constraints**

Linear constraints are called constraint functions that only have first order terms of the design variables. If the limit has at least one term with an order greater than one, it is called a non-linear restriction [65].

- **Feasibility**

A feasible solution is called the problem solution that satisfies all constraints. Obviously, the optimum solution is a feasible solution. An infeasible solution is called a solution which violates at least one constraint [68][69].

2.3.4 Description of GA Toolbox

As shown in Figure (2-9), the GA procedure flow chart provided by MATLAB environment has four primary modules. The optimization problem definition module, the module for setting variables, the initial population module generation, and the module for evolution. By exchanging information that allows the operation of the algorithm, these modules interact with each other. There are a number of subroutines with particular tasks inside each module. Different operators available in the GA toolbox can execute each of these subroutines. In this way, according to the way the operators are set by the user, the GA algorithm can be configured differently[70].

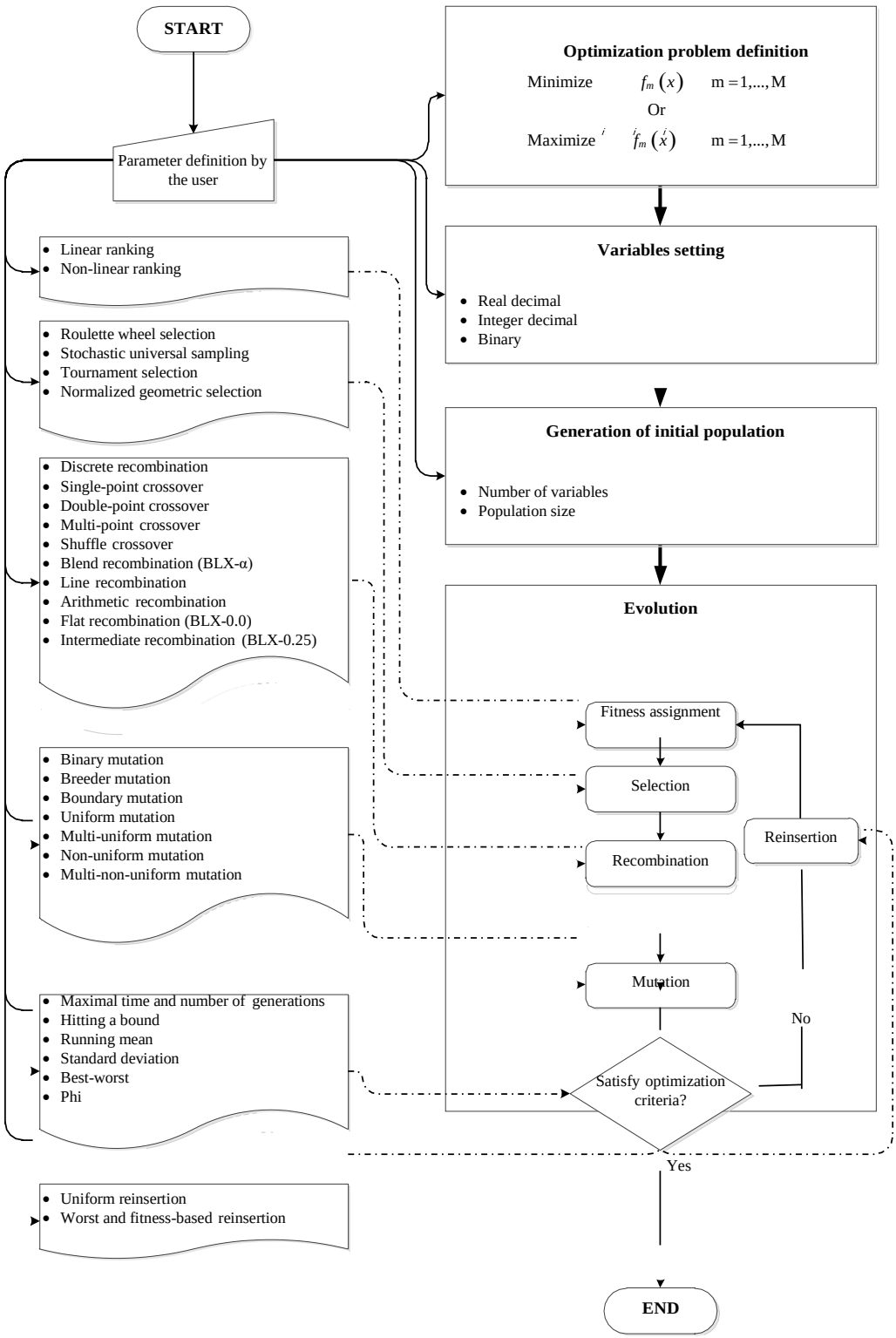


Figure (2-9): Operational Structure of the GA tool box [70].

2.3.5 Operational Structure of the GA Toolbox

The operational structure of the GA toolbox can be described as follows:

A. Problem Definition Module

Before the optimization algorithm is executed, it is necessary to characterize the problem of optimization, which is defined as:

Minimize $f_m(x)$ $m=1, 2\ldots.M$

The algorithm introduced in the GA toolbox, by definition, minimizes the objective function, the user can solve a maximization, however,

Max $f_m(x)=-(\min f_m(x))$ [70][71].

B. Variable Setting Module

After the optimization problem is established, it is necessary to define the variable type and the representation of the variables that the algorithm uses. GAs can operate with real variables or with codified variables directly. Thus, there will be a need for coding / decoding to pass from the actual workspace to the GA workspace, depending on the type of variable defined by the problem and the type of representation used by the GA.

C. Generation of Initial Population Module

The initial population must be firstly created in the GA, this is executed by generating the required number of individual using a random number generator that distributes numbers in the range of desire uniformly.

D. Evolution Module

This process applies the operators of evolution to the Population of individuals; the following subroutines are included:

1) Selection

Constitutes the first operator in the process of evolution. Its function is to distinguish between individuals on the basis of their fitness and, in particular, to allow the better individuals in the next generation to undergo variation and create offspring. The algorithm creates a mating pool (an intermediate population) to reserve the individuals chosen for breeding in order to do this.

2) Recombination

No new individuals are generated by the selection operator, but multiple copies of the fittest ones are generated instead. Therefore, to generate new people and thus to diversify the population (exploration process), it is necessary to apply the recombination operator. The recombination operator produces new chromosomes which have some parts of the genetic material of both parents [64].

Probabilistically, it is usually applied according to a crossover / recombination rate, which typically varies from 0.5 to 1.0 [72].

3) Mutation

The recursive application of recombination and selection operators can contribute to the loss of genetic information that is crucially significant. It is therefore necessary to use an operator that promotes population diversity (exploration process) so as not to be trapped in a local optimum. This is achieved through the mutation operator which alters the genetic information of the people in the population randomly. A mutation rate controls the mutation process [70].

4) Termination

A Termination Criterion (TC) is a requirement that has been adopted to determine the conclusion of a run. Until a given TC is true, the GA will run, deciding the end of the optimization process. This criterion prevents the optimization algorithm from being terminated prematurely as well as from further unnecessary computation. The choice of TC depends on the configuration of the GA and the characteristics of the assessed objective function [73].

5) Reinsertion

If the criterion of termination is not met, the population will undergo a new evolutionary process. Therefore, the new individuals produced in the original population need to be included. The simplest criterion is to create and replace the entire population with an equal number of children and parents. However, a different number of children than the original population size can be generated and, in this situation, rules need to be laid down to define which parents are to be replaced [70].

E. Constraint Handling

There is a benefit to Evolutionary Algorithms EA in dealing with optimization problems which are restricted because they can preserve a population of individuals, either feasible or infeasible, that can encourage development in different feasible regions, identify new feasible regions or approach the optimum from different directions [74].

CHAPTER 3

Design and Optimization of Single Ended LNA

3.1 Introduction:

This chapter presents an optimum design using multi-objective genetic algorithm for single ended low noise amplifier structure. The design is performed at two different frequencies: 2.4 GHz and 5 GHz. Figure (3-1) illustrates the topology of the low noise amplifier single-ended cascode with inductive source degeneration. Inductive source degeneration, represented by an inductor L_S connected to the transistor source MOSFET1, is used in this structure. A proper selection of L_S determines and controls the real part of input impedance. MOSFET2 Transistor (M2) has the function of minimizing the effect of tuned output with tuned input. MOSFET Transistor (M1) and MOSFET Transistor (M3) that form the current mirror are aware of the biasing circuit. The width of the MOSFET transistor (M3) is generally kept at a small fraction of the width of the MOSFET transistor (M1) in order to obtain the minimum overhead power of the bias circuit. To maximize the transfer of output power, the output inductor L4 is introduced to resonate with the output load. The design and optimization are carried out at two different frequencies: 2.4 and 5 GHz to show the effect of increasing frequency on amplifier performance.

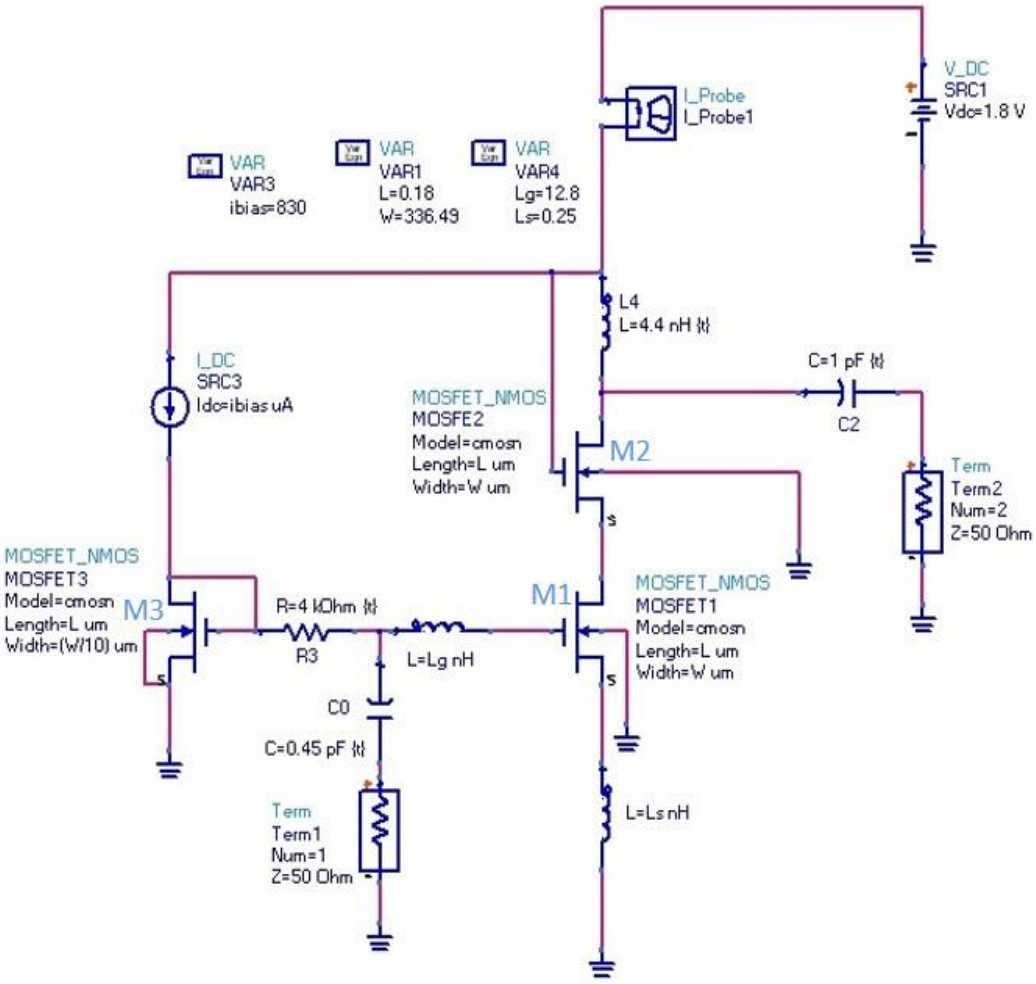


Figure (3-1): Single Ended LNA Topology Simulation Using ADS

3.2 Single Ended LNA at 2.4 GHz

A narrow band (LNA) is presented in this section for Bluetooth application at 2.4 GHz. Bluetooth system is primarily used in narrow bands wireless communication with high-performance receiver design using RFIC to enhance Bluetooth system performance. LNA is the most essential block for the complete receiver design. The higher gain of the first stage of the receiver relaxes the subsequent stages noise performance requirements [39].

3.3 Mathematical Results of Single Ended LNA at 2.4 GHz

The LNA design must meet the most important parameter values of the specified performance requirements [75]. Below is an overview of the design of the low noise amplifier steps. These could include the widths of MOSFET transistors W1, W2, and W3 and the values of inductors as degenerated inductance L_S, gate inductance L_g, drain inductance L_d, as well as the values of coupling capacitance (capacitance at load C_2, capacitance at input C_0) and the biasing current I_d. A small signal simplified equivalent circuit is shown in Figure (3-2). The derived input impedance of the single-ended low noise amplifier is given as [76] :

$$\mathbf{Z_{in} = R_g + \left(\frac{g_{m1}}{C_{gs1}}\right) L_S + j(\omega L_s - \frac{1}{\omega\, C_{gs1}})} \qquad \textbf{(3-1)}$$

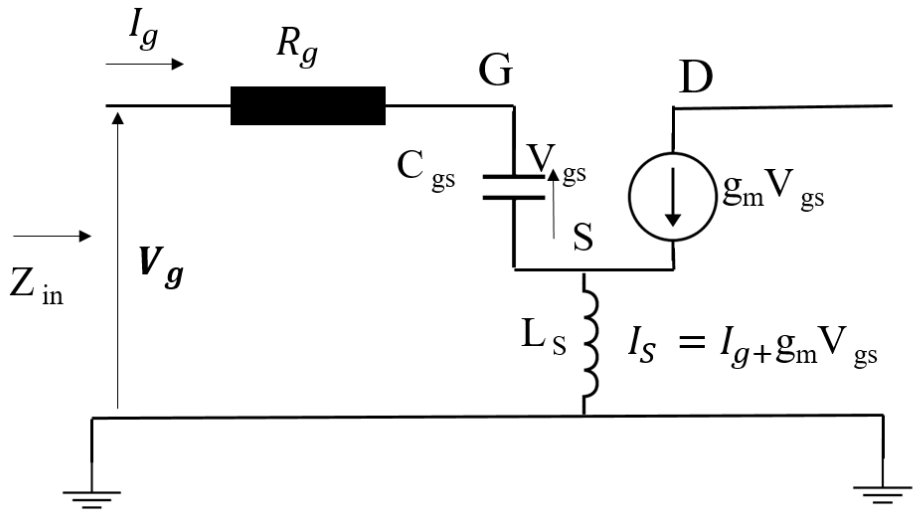


Figure (3-2): New Equivalent Model of MOSFET with Source De-Generation Added .

The above equation can be written as follow:

$$\boldsymbol{Z_{in} = R_g + R_a + j(X_{Ls} - X_{cgs1})} \qquad \textbf{(3-2)}$$

where

$$\boldsymbol{R_a = \left(\frac{g_{m1}}{C_{gs1}}\right) L_S} \quad \textbf{(3-3)}$$

Consequently, the impedance with no feedback from the MOSFET will be:

$$\boldsymbol{Z_{in} = R_g - j\, X_{Cgs1} \rightarrow Z_{in} = -j(X_{Cgs1})} \quad \textbf{(3-4)}$$

The $\boldsymbol{R_a + jX_{Ls}}$ term is added to the original input impedance when adding series feedback.

In addition, another inductor is added with the gate L_g in series that is chosen to resonate with the C_{gs} Capacitor. The value of L_g caused to cancel C_{gs} then achieved $Z_{in} = \left(\frac{g_{m1}}{C_{gs1}}\right) L_S$, $Z_{in} = 50\Omega$ the value of I_d is selected in most LNA designs and the values of g_m and C_{gs} are then obtained to give the Rin required. Assuming the case of using a process of 0.18 μm, for the operating frequency of 2.4 GHz and given process parameter [45][76].

μ_0=293.168 $m^2/_{V.S}$,C_{ox}=8.221 $* 10^{-15} F/\mu m^2$,ε_0=8.854*10^{-12},ε_r=3.9 for Sio2 , V_{DD}=1.8 V , I_d =5 mA

- The device width of transistor MOSFET1 (M1) and MOSFET2 (M2) are determined by [46]:

$$\boldsymbol{W_1 = \frac{3}{2* C_{ox} * L_1 * Q_{opt} * w_0 * R}} \textbf{ = 336.49 μm} \quad \textbf{(3-5)}$$

- The Gate to source capacitor C_{gs} is calculated as:

$$\boldsymbol{C_{gs} = \frac{2}{3} * C_{ox} * W_1 * L_1 = 0.34\ PF} \quad \textbf{(3-6)}$$

- Trans-conductance (g_{m1}) of MOSFET1 (M1) is given as :

$$g_{m1} = \sqrt{2 * \mu_n * C_{ox} * \frac{W}{L} I_d} = 67.93 \text{ ms} \quad (3\text{-}7)$$

- Therefore the transistor unity gain frequency W_T is:

$$W_T = \frac{g_m}{C_{gs}} = 199.8 \text{ Grps} \quad (3\text{-}8)$$

- The values of L_s , L_g , and L_d are obtained as follows:

$$L_S = \frac{R_S}{W_T} = 0.25\, nH \quad (3\text{-}9)$$

$$\text{And } L_g = \frac{1}{W_0^{\,2} * C_{gs}} - Ls = 12.8 \text{ nH} \quad (3\text{-}10)$$

$$\text{And } L_d = \frac{1}{W_0^{\,2} * C_L} = 4.4 \text{ nH} \quad (3\text{-}11)$$

- Then the voltage gain can be determined as [77] :

$$A_V = 20\, log \left(\frac{1}{50 * C_{gs} * W_0}\right) = 11.86 \text{ dB} \quad (3\text{-}12)$$

- The minimum noise figure is given as:

$$NF = \left(1 + 1.62 * \frac{w_0}{W_T}\right) = 1.122 \quad (3\text{-}13)$$

- The power dissipation is then calculated to be:

$$P_D = V_{DD} * I_d = 9 \text{ mW} \quad (3\text{-}14)$$

The design component values of LNA that obtained mathematically is simulated using a simulator of the ADS Advanced Design System RF circuit using the BSIM3 model parameters of the 0.18 μm CMOS process.

The single ended LNA is powered by a 1.8 V power supply and consumes 9 mw of power .Noise figure (NF) obtained is 1.39 dB as shown, Figure (3-3), Figure (3-4), and Figure (3-5) show accomplished power gain (S_{21}) and input reflection coefficient (S_{11}) simulated results respectively. By simulated the design variables that obtained mathematically using the Agilent Advanced Design System (ADS) simulator also there is a small discrepancy between the calculation and the simulation results (which can be derived from the lumped capacitor tolerance and the manufacturing of the circuit).

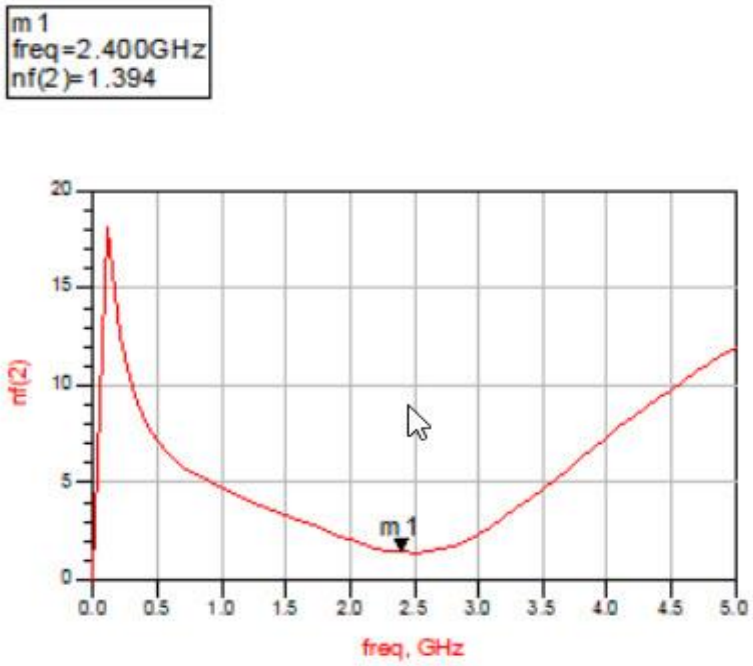


Figure (3-3): Mathematical NF for 2.4 GHz Single Ended LNA

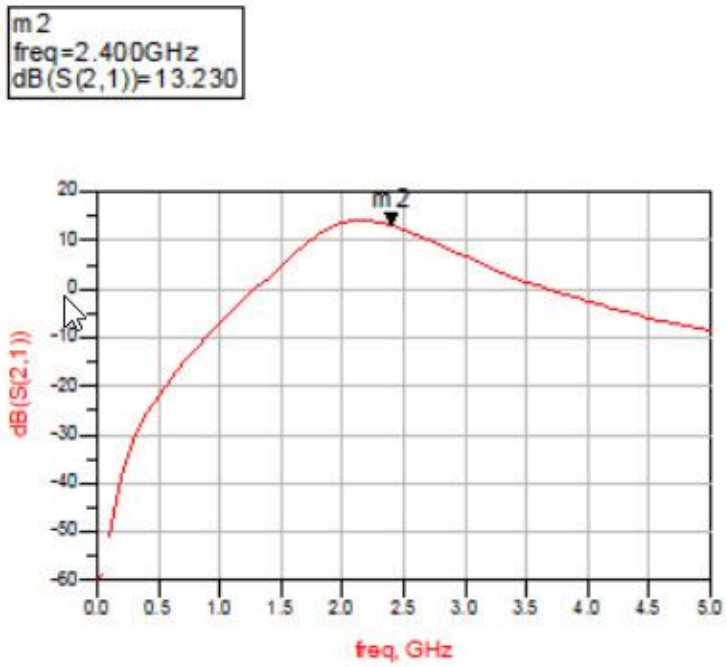


Figure (3-4): Mathematical Power Gain for 2.4 GHz Single Ended LNA

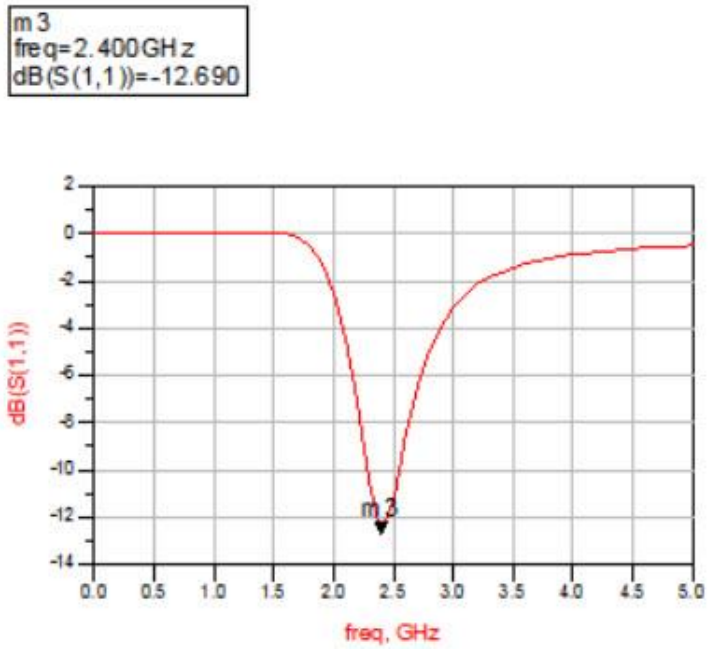


Figure (3-5): Mathematical Input Return Loss S_{11} for 2.4 GHz Single Ended LNA

3.3.1 Optimization Results for Single Ended LNA at 2.4 GHz:

Due to the complex mathematical model of MOSFET, it is very difficult and impossible task to find manual optimal design variables value in nanometer design. To overcome this complexity and time-consuming task, optimization algorithm is widely used to find the optimum value of design variables [39]. The multi-objective optimization method is needed because of usually existing numerous parameters for RF circuits. Together they are opposed, and designers need to tradeoff between such goals as gain, power consumption, noise figure (NF) and so on. Among the other algorithms, the basis for choosing MOGA is the low complexity and high efficiency of its optimization algorithm [3].

3.3.1.1 Optimization for Power Consumption, Noise Figure and Maximization Gain

In design a LNA a tradeoff between minimization power consumption, minimization noise figure, and maximization gain is achieved using Multi-Objective Genetic Algorithm (MOGA). This technique has shown good results in solving complex multi-objective optimization problems, and has been able to discover various solutions to the Pareto front with little computational effort [70]. Figure (3-6) illustrates the procedure steps for MOGA toolbox optimization method using MATLAB language.

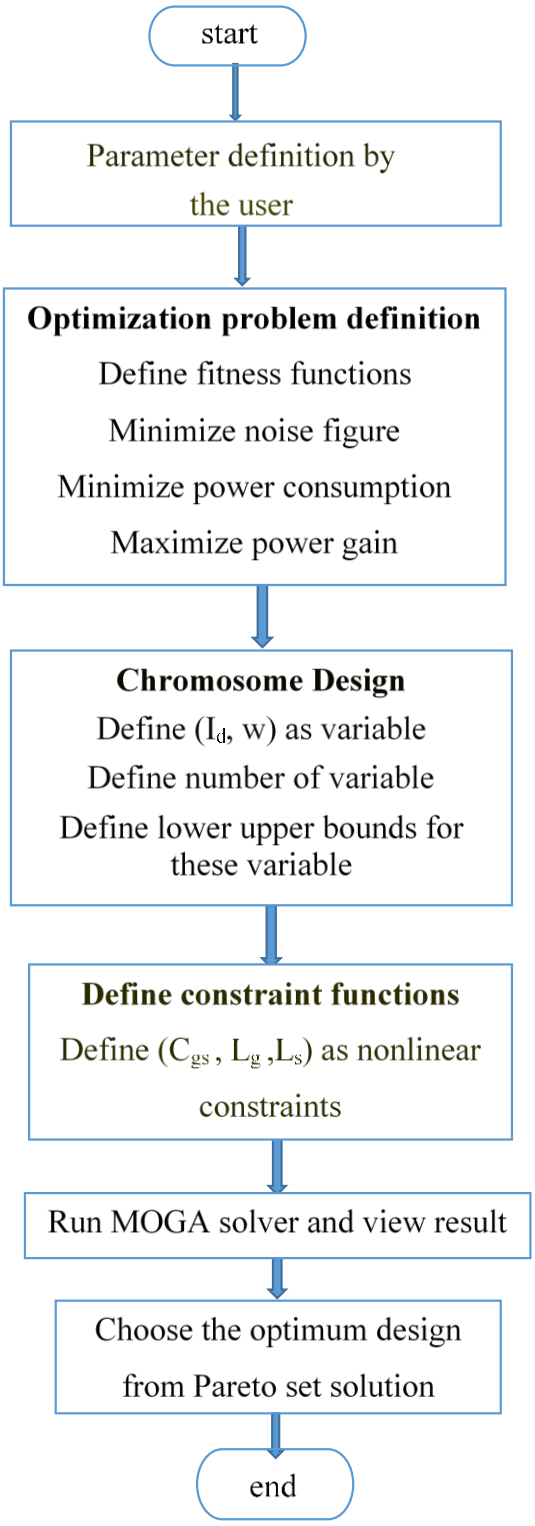


Figure (3-6): Flowchart of Genetic Algorithm Procedure Based on MATLAB

The GA chromosome cells are formed by two real values that correspond to the designed variables (I_d, width W_1) which there Constraints are listed in Table (3-1).

Table (3-1): Design Variables and Constraints Limit Using MOGA

Variables name	**Constraints values**
W_1	10 to 700 µm
I_d	1 to 7 mA

In other hand , (L_S, L_g, C_{gs}) are used as nonlinear constraint functions to obtain minimization for power consumption and noise figure, maximization gain, and to satisfy the required specifications and performances that illustrate in Table (3-2) and Table (3-3) respectively.

Table (3-2): Constraints Limit Using MOGA

Parameter	**Constraints values**
L_S	0.1 to 10 nH
L_g	1 to 50 nH
C_{gs}	0.05 to 10 pF

Table (3-3): LNA Specifications Design Target for 0.18µm CMOS Process

Parameter	**Value**
Frequency (GHz)	2.4
Supply Voltage(V)	1.8
S_{22}(dB)	< -10
S_{11}(dB)	< -10
S_{21} (dB)	> 10
Noise Figure(dB)	< 3
Power consumption(mW)	< 15
Source/load Impedance (Ω)	50

The performances specifications of low noise amplifier are employed in the MOGA optimization toolbox of MATLAB. Some of them considered to formulate the proposed fitness functions and others used as constraints. These specifications are summarized in Table (3-4).

Table (3-4): Design Constraints and Specifications for Low Noise Amplifier

Specifications/Constraints	**Type**	**Equation**
Noise Figure	Fitness Function	(3-13)
Gain	Fitness Function	(3-12)
Power Dissipation	Fitness Function	(3-14)
Gate to Cource Capacitor C_{gs}	Constraint	(3-6)
L_s Degeneration Inductor	Constraint	(3-9)
L_g Inductance at The Gate	Constraint	(3-10)

The health of each chromosome represents the efficiency of each design. Fitness is one of the most important characteristics of the multi-objective genetic algorithm. The reliability of a MOGA depends directly on the fitness function definition. The fitness function has an added philosophy, and the goal of the genetic algorithm is to maximize or minimize the fitness function.

The multi-objective problem of optimization can be identified as:

Minimize/Maximize $F(x)=f_1(x), f_2(x), f_3(x)\ldots\ldots f_N(x)$

When, $f_1(x), f_2(x), f_3(x)$ The fitness functions ,N the number of fitness functions. The fitness functions can be a minimization or maximization form.

The fitness function can be formulated as:

$$\boldsymbol{fitness = \sum_{i=1}^{N} w_i * f_i} \qquad \textbf{(3-15)}$$

where w_i represents the weight factors and f_i represents the performance metrics (e.g. noise figure, power consumption, gain, or matching in the case of the LNA). The weight factors are optional used to enhance the algorithm to produce a result that favors performance metrics over others. This approach is helpful when dealings occur in the design and certain results are preferred over others.

This fitness function can be applied in MATLAB as follows:

$\boldsymbol{f_1 = NF = \left(1 + 1.62 * \frac{w_0}{W_T}\right)}$ **minimization noise figure**

NF= (1+1.62*(2*pi*f_o)/$\left(\frac{sqrt\left(2*\mu o*\boldsymbol{C_{ox}}*\left(\frac{W*10^{-6}}{0.18*10^{-6}}\right)*(I_d*10^{-3})\right)}{\left(\frac{2}{3}\right)*(W*0.18*1e-12)*\boldsymbol{C_{ox}}}\right)$) **(3-16)**

$\boldsymbol{f_2 = A_V = -(20\ log\ \left(\frac{1}{50*C_{gs}*W_0}\right))}$ **maximization gain**

$$= -(\mathbf{20}\ \boldsymbol{log}\frac{\mathbf{1}}{\mathbf{50}*\left(\frac{1}{sqrt((Ls+Lg)*\left(\frac{2}{3}\right)*(W*0.18*1e-12)*C_{ox}}\right)*\left(\frac{2}{3}\right)*(W*0.18*1e-12)*C_{ox}})$$

(3-17)

$\boldsymbol{f_3 = P_D = V_{DD} * I_d}$ **minimization power dissipation**

=1.8*I_d*10^-3 **(3-18)**

When W represent the width of transistor and I_d represent the current of drain.

3.3.2 Development of Multi-Criteria Decision Making

After run the solver, results view as set of Pareto solutions. Since the Pareto set solution involves different specifications with different units, a normalized and weighted methods are used to select the optimum solution. This technique includes two main procedures:

1. Weighted Sum Method (WSM)

Due to the reality that it follows an intuitive process, the WSM is the simplest method available. The hypothesis of additive utility is applied in the context of this method, which implies that the overall value of each alternative is equivalent to the total sum of the products. WSM is easily applicable in issues with the ranges of the same units across criteria; however, when the ranges of the units vary, for example, when qualitative and quantitative attributes are used, the problem becomes difficult to deal

with as the above-mentioned hypothesis is violated, and therefore standardization schemes should be used. Because of the simple nature of the method, it is common practice to use WSM along with other methods[78].

2. Linear Normalization

Linear normalization is a subset of methods based on linear ratios that apply a comparison ratio between the value of alternatives and the best solution obtained. The method simply uses the ratio of attribute values relative to each criterion's maximum attribute value (x_j).

as presented in:

$$\boldsymbol{r_{ij} = \frac{X_{ij}}{X_j^{max}} \quad i = 1, 2, \dots \dots n \ ; j = 1, 2, , \dots \dots m;}$$

$$\boldsymbol{for\ maximization}\ \textbf{(3-19)}$$

$$\boldsymbol{r_{ij} = 1 - \frac{X_{ij}}{X_j^{max}} \quad i = 1, 2, \dots \dots n \ ; j = 1, 2, , \dots \dots m;}$$

$$\boldsymbol{for\ minimization}\ \textbf{(3-20)}$$

Figure (3-7) illustrates the steps that used in MATLAB to select the optimum solution from Pareto set solution.

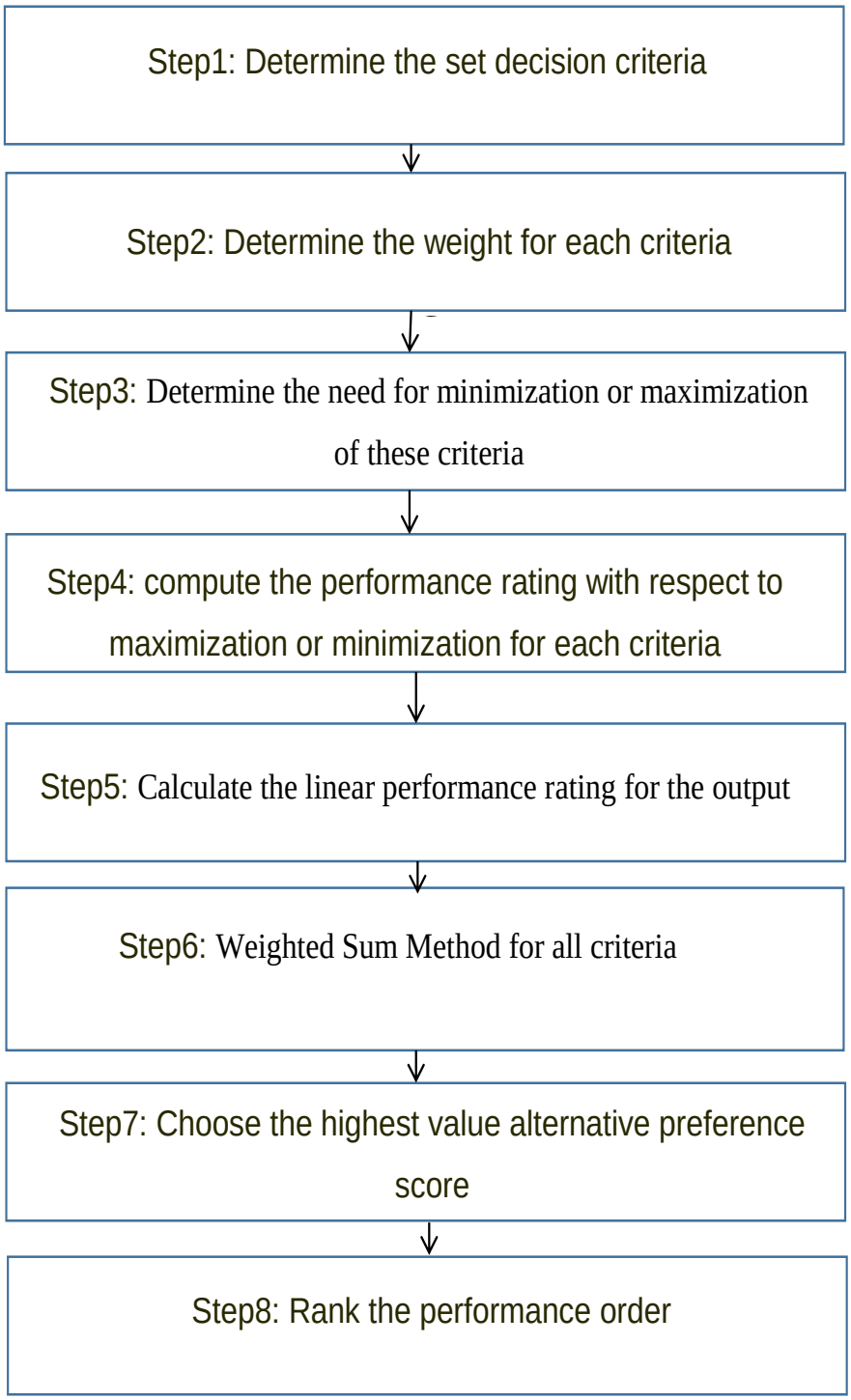


Figure (3-7): Flow Chart of Selection for Optimum Parameter Values

Table (3-5) illustrates the Pareto range of solutions. To choose the optimum design from the Pareto set solution, a MATLAB code is provided for implementation of the described Multi-Criteria Decision Making MCDM methods using normalization techniques and weight assignments.

Table (3-5): Pareto Set Solution for Optimization NF ,Gain, P for Single Ended LNA at 2.4 GHz

INDEX	NF(dB)	Gain (dB)	Power Consumption(watt)	Width (W_1) µm	I_d (mA)	WSM
1	1.05255	23.58313	0.012581	86.87224	6.989564	0.6427
2	1.090434	23.59922	0.00424	86.71141	2.355788	0.7169
3	1.152442	21.96925	0.0018	104.6104	1.0002	0.8532
4	1.062613	23.50381	0.008944	87.66918	4.968677	0.6563
5	1.08479	23.22392	0.005037	90.54015	2.798187	0.6935
6	1.15347	21.85402	0.0018	106.0074	1.000025	0.8516
7	1.060358	22.86044	0.010364	94.40938	5.75786	0.6405
8	1.127381	23.14797	0.002251	91.33533	1.250688	0.8142
9	1.120628	22.67148	0.002652	96.48581	1.473282	0.7736
10	1.102491	22.58162	0.003712	97.48912	2.062085	0.719
11	1.10899	23.05715	0.003107	92.29532	1.726333	0.7516
12	1.086412	23.466	0.004716	88.0516	2.620032	0.7035
13	1.05255	23.58313	0.012581	86.87224	6.989564	0.6427
14	1.112305	23.35134	0.002829	89.22162	1.571795	0.7716
15	1.057161	22.88535	0.011523	94.13911	6.401676	0.6365
16	1.146228	22.11111	0.001925	102.9158	1.069399	0.8371
17	1.144344	22.26013	0.001942	101.1651	1.078833	0.837
18	1.095789	23.57422	0.00379	86.96141	2.105788	0.7303

Figure (3-8) illustrates score histogram which plots the score diversity for each objective .

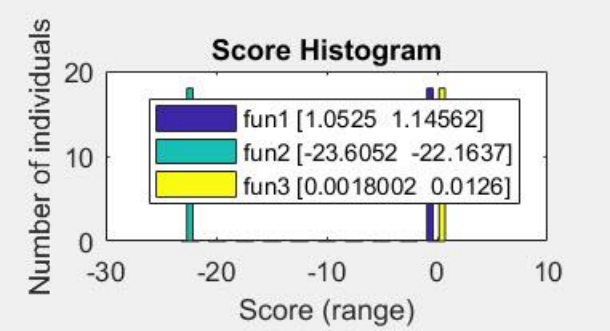


Figure (3-8): Score Histogram for MOGA

Simulation is performed using the design variables that obtained from the Pareto optimization by the Agilent Advanced Design System (ADS) simulation environment supplied by Keysight Technologies is employed in the simulation purposes.

Also, there is a small discrepancy between the calculation and the simulation (which can be derived from the lumped capacitor tolerance and the manufacturing of the circuit).

Figures (3-9), (3-10), and (3-11) show that using MOGA succeeded to obtain best values for system parameters that used to achieve best performance. Figure (3-9) shows low noise figure (NF) of 1.497 is achieved at 2.4 GHz. The forward power gain (S_{21}) is 20.5 dB at 2.4 GHz as shown in Figure (3-10) , when the input return loss (S_{11}) is -15.9 dB at 2.4 GHz as shown in Figure (3-11) that represents a good input match.

These figures clearly show that the proposed MOGA has demonstrated its ability to tune the design variables properly that used to produce satisfactory results.

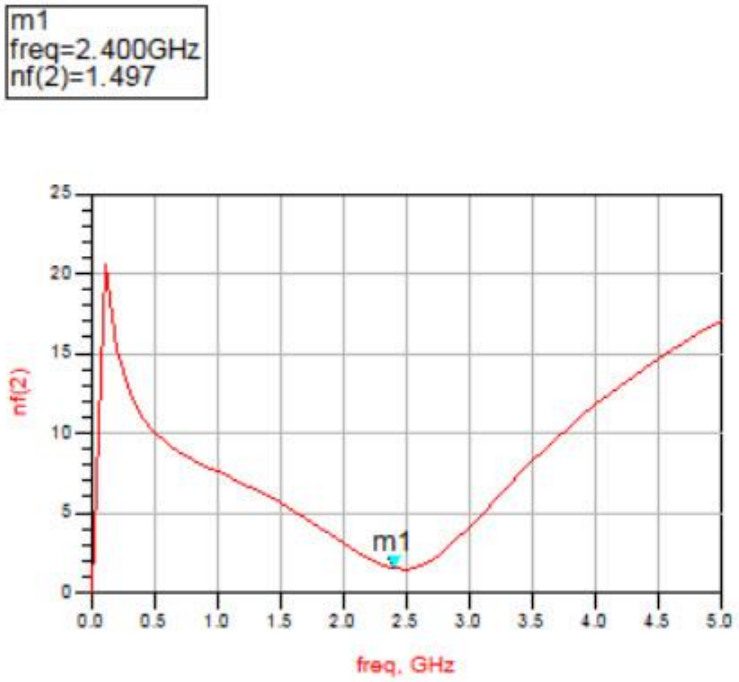


Figure (3-9): NF Optimized Result for 2.4 GHz Single Ended LNA

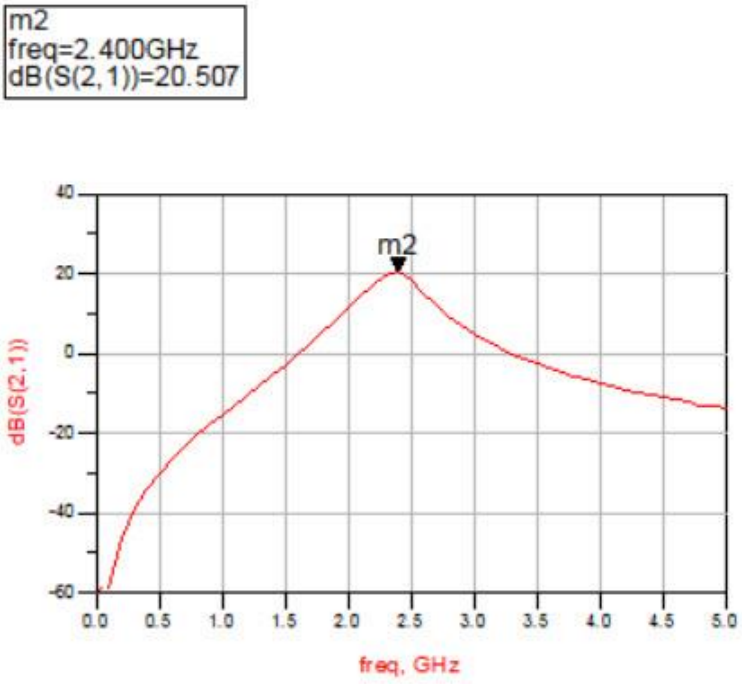


Figure (3-10): Power Gain Optimized Result for 2.4 GHz Single Ended LNA

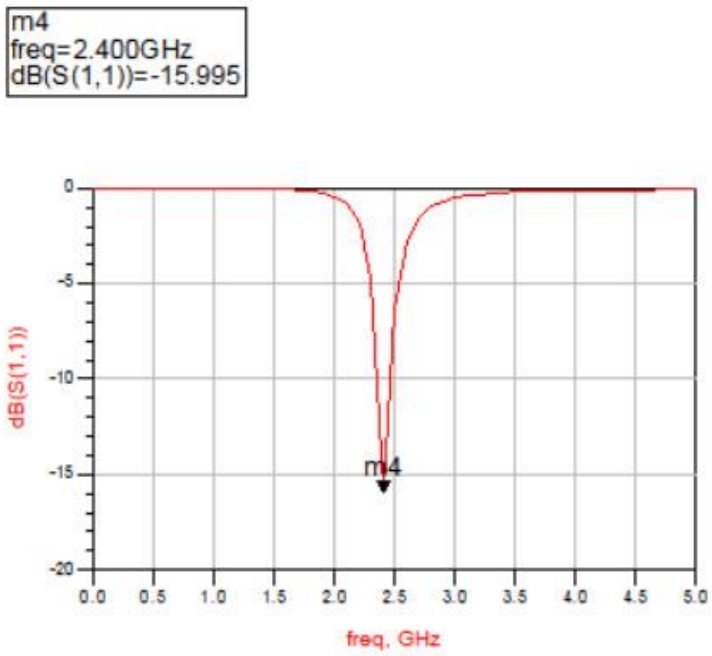


Figure (3-11): The Input Return Loss S_{11} Optimized Result for 2.4 GHz Single Ended LNA

Table (3-6) illustrates a comparison between the mathematical and optimized analysis based on MOGA optimization method for 2.4 GHz LNA.

Table (3-6): Comparison Between Mathematical and Optimized Results for Single Ended LNA at 2.4 GHz

Design Parameters and Performance	**Single Ended Low Noise Amplifier**	
	Mathematical	**Optimized using GA**
Width W_1(µm)	336.49	104.6104
$\boldsymbol{I_d}$(mA)	5	1.0002
C_{gs}(PF)	0.34	0.10572
L_S(nH)	0.25	0.312
L_g(nH)	12.8	41.28
$\boldsymbol{L_d}$(nH)	4.4	7.4
NF(dB)	1.3	1.49
Power Consumption(mw)	9	1.8
Gain(dB)	13.2	20.5

It can be shown from this table that a significant improvement is obtained in transistor dimension when the width of transistor (W) resulted to be 104µm after optimization when I_d become 1.0002 mA with low power consumption P=1.8(mw), and amplifier gain increased to 20.5(dB).

However, it can be seen that this improvement is price for increasing the noise figure, and this is the concept of tradeoff between variables.

3.3.3 Minimization of Inductive Source Degeneration and Gate Inductance at 2.4 GHz

It is well established that one of important parameter of analog integrated circuit design is to minimize the chip area required for fabrication and power consumption [79].

For better NF, added source degeneration can also bring the match needed for good return losses closer to the match. However, adding source feedback trades off gain with IP3 and P1dB performance, also trades off linearity and stability particularly at higher frequencies. Stability improves with source degeneration at the lower frequencies of the cellular bands, while stability decreases at frequencies greater than around 5 GHz as degeneration increases. The difference between linearity and stability must therefore be investigated across a full range of frequencies.

Small inductance changes have been added to the source of an LNA. Gain, NF and stability can have large impacts. As inductance increases, at the expense of gain, stability increases. Also, NF can improve. Continued inductance increases, however, can soon lead to degraded gain and NF. In the LNA transistor, at the expense of the current draw, device size can be increased to improve linearity. Increasing current density can improve gain and NF in the LNA device, but it is again at the expense of current drawing. This inductor's value is fairly arbitrary, but is ultimately limited to the maximum inductance size permitted by the technology, which is generally about 10 nH [40].

It is worth considering that the design of performance parameters using analytical solutions may take too much time and may not lead to desired specifications. Therefore, MOGA is used to search for optimal design variables that deliver optimal results.

The design variables that used are Id and width W_1 , the chromosome is designed to contain these variables as shown in Table (3-7).

Table (3-7): Design Variables and Constraints Limit Using MOGA

Variables name	**Range of values**
W_1	10 to 300 µm
I_d	1 to 5 mA

In other hand, NF, gain, power consumption, and C_{gs} , which are employed as nonlinear constraint functions, are used to obtain minimization for L_S and L_g and to satisfy the required specifications and performance. The limit of this constraints are illustrated in Table (3-8).

Table (3-8): Constraints Limit Using MOGA

Performance parameters	**Range of values**
NF	<3dB
Gain	>15dB
Power Consumption	<20mw
Gate to Source Capacitor C_{gs}	0.2 to 10 pF

Table (3-9) illustrates the performances specifications of low noise amplifier required. The specifications are employed in the MOGA optimization toolbox of MATLAB, some of them are used to formulate the fitness functions and others are used as constraints.

Table (3-9): Design Constraints and Specifications for LNA

Specifications/Constraints	**Type**	**Equation**
Noise Figure	Constraint	(3-13)
Gain	Constraint	(3-12)
Power Dissipation	Constraint	(3-14)
Gate to Source Capacitor C_{gs}	Constraint	(3-6)
$\boldsymbol{L_s}$ Degeneration Inductor	Fitness Function	(3-9)
$\boldsymbol{L_g}$ Inductance At The Gate	Fitness Function	(3-10)

The Table (3-10) illustrates the Pareto range of solutions. To choose the optimum design from the Pareto set solution, a MATLAB code is provided for implementation of the described Multi-Criteria Decision Making (MCDM) methods, using linear normalization techniques and Weighted Sum Model (WSM) assignments.

Since the Pareto set solution involves different specifications with different units, a normalized and weighted methods are used to select the optimum solution. The highlighted values in Table (3-10) are the best solution which considered for the design.

Table (3-10):Pareto Set Optimum Solution Optimization L_S and L_g

INDEX	L_S(H)	L_g(H)	Width(µm)	I_d (mA)	WSM
1	4.66E-10	1.82E-08	233.3686	1.00009	0.704936
2	1.91E-10	2.20E-08	196.0572	4.99999	0.913636
3	1.92E-10	2.18E-08	197.9381	4.98349	0.914827
4	2.02E-10	2.01E-08	214.8261	4.880023	0.925509
5	1.95E-10	2.14E-08	201.6782	4.959898	0.914977
6	2.59E-10	1.85E-08	232.1488	3.231746	0.860618
7	2.09E-10	1.88E-08	228.9191	4.856667	0.94098
8	2.06E-10	1.91E-08	225.896	4.955105	0.940032
9	2.87E-10	1.84E-08	233.1469	2.626667	0.827318
10	2.04E-10	1.94E-08	221.6637	4.977221	0.937209
11	4.66E-10	1.82E-08	233.3686	1.00009	0.704936
12	1.94E-10	2.14E-08	201.1961	4.982662	0.917502
13	1.96E-10	2.09E-08	206.0574	4.976747	0.922652
14	3.63E-10	1.83E-08	232.71	1.64356	0.760353
15	1.94E-10	2.17E-08	198.6988	4.927822	0.911623
16	2.03E-10	2.00E-08	215.8289	4.897016	0.925443
17	2.18E-10	1.86E-08	231.3483	4.536328	0.927321
18	4.66E-10	1.82E-08	233.3646	1.00009	0.704936

Figure (3-12) illustrates score histogram, which plots the score diversity for each objective, fun1 for minimization L_S and fun 2 for minimization gate inductance L_g.

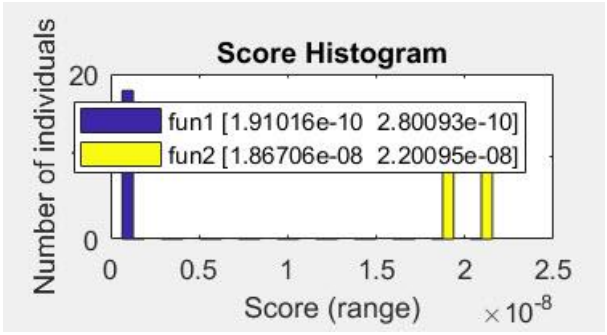


Figure (3-12): Score Histogram for L_S and L_g

From the Pareto front shown in Figure (3-13), an initial set of 18 acceptable responses was chosen, all satisfying the desired constraints.

The final set includes several candidates that allow the designer to select the appropriate answers.

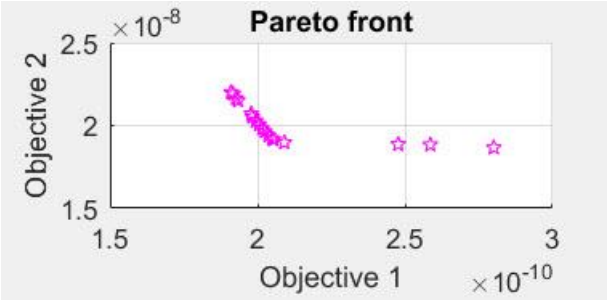


Figure (3-13) :Pareto Front of MOGA

The noise performance of the LNA that is presented in Figure (3-14) is the most striking result of these plots. NF of 1.68 dB value considers a suitable result for the majority of applications. In addition, the high gain value of 17.34 dB as seen in Figure (3-15) is another significant result.

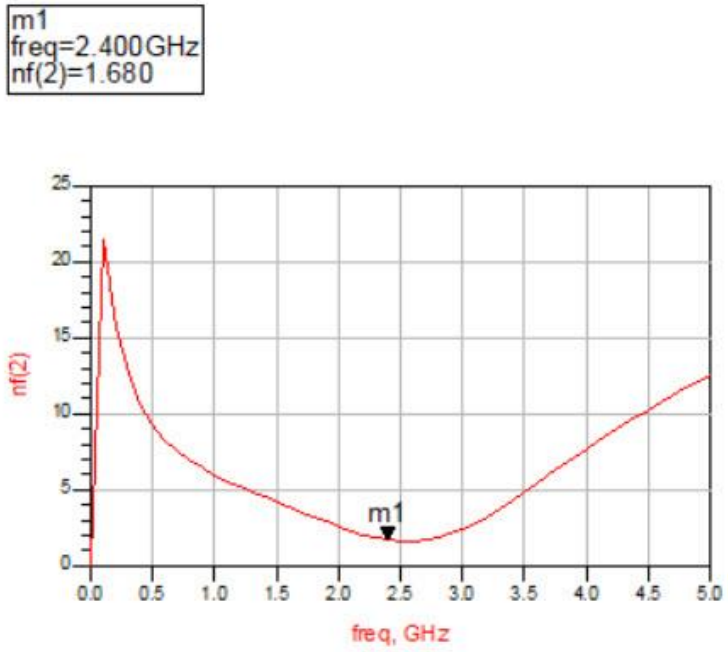


Figure (3-14): NF Based on Optimized (L_S and L_g) at 2.4 GHz Single Ended LNA

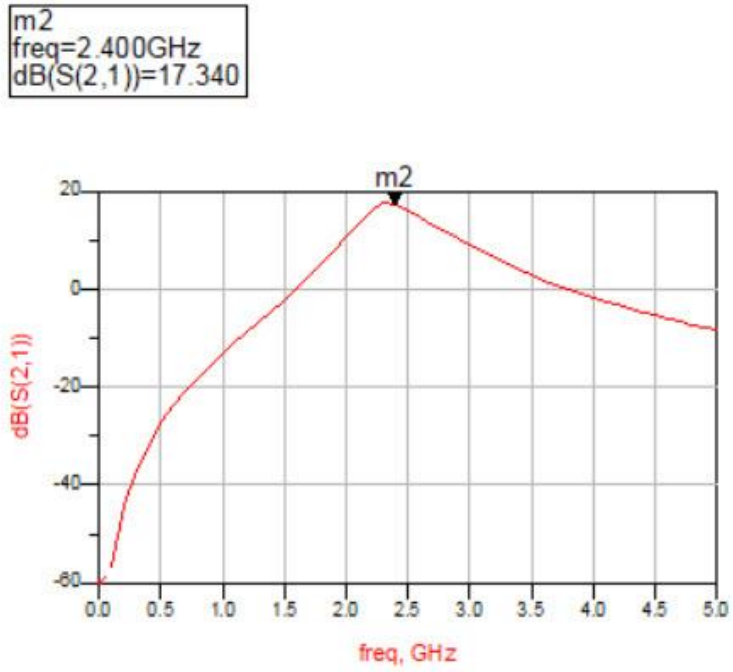


Figure (3-15): S_{21} Based on Optimized (L_S and L_g) at 2.4 GHz Single Ended LNA

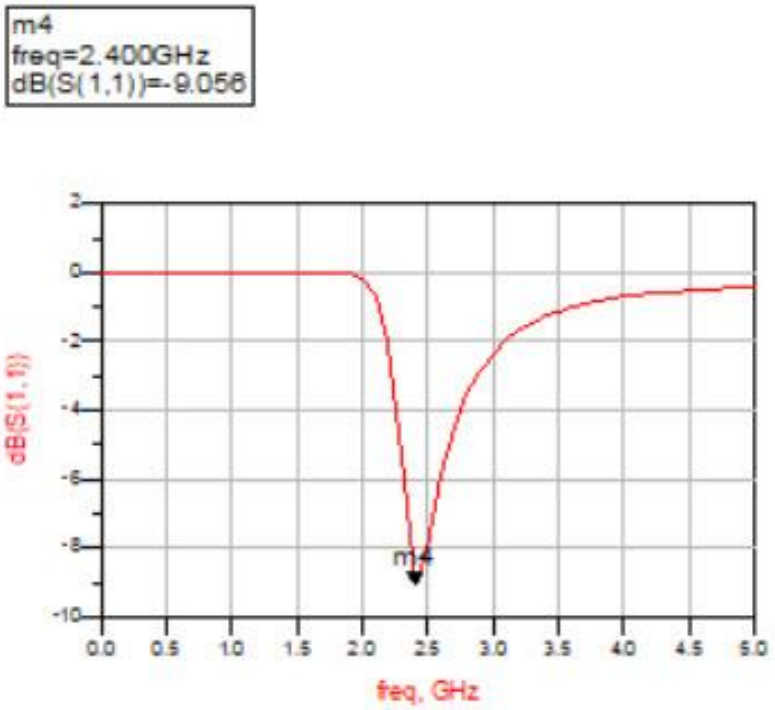


Figure (3-16): S_{11} Based on Optimized (L_S and L_g) at 2.4 GHz Single Ended LNA

3.4 Comparison Between Analytical and Optimized Results Using MOGA for 2.4 GHz Single Ended LNA

This section presents the results of comparisons between the analytical method and those produced by the MOGA. The main purpose of applying MOGA is to comply the obtained results with the design specifications desired. The comparison is performed using two ways, the first way is by using noise figure, power consumption, and gain as fitness functions, and other specifications as constraints. While the second way for optimization LNA using source inductor L_S and gate inductor L_g as fitness functions while noise figure, power consumption and gain using as constraints.

Table (3-11) shows a comparison results between the analytical and optimized output using MOGA optimization technique for 2.4 GHz LNA system. This table reveals that there is a considerable improvement in the performance parameters of the LNA is achieved by using MOGA tuning approach.

Table (3-11): Comparison Between Analytical and MOGA Results for Single Ended LNA at 2.4 GHz

Design and performance parameters	**Single Ended Low Noise Amplifier at 2.4GHz**		
	Mathematical	**Optimized using MOGA(NF,G,P)**	**Optimized using MOGA (L_S , L_g)**
Width W_1(µm)	336.49	104.6104	228.9
$\boldsymbol{I_d}$(mA)	5	1.0002	4.87
C_{gs}(PF)	0.34	0.10572	0.231
L_S(nH)	0.25	0.312	0.209
L_g(nH)	12.8	41.28	18.8
$\boldsymbol{L_d}$(nH)	4.4	7.4	4.3
NF(dB)	1.3	1.49	1.68
Power Consumption(mw)	9	1.8	8.766
Gain(dB)	13.2	20.5	17.3

It can be seen from the above table that there is a significant improvement in the performance parameters of the LNA system is achieved using MOGA tuning method when the fitness function is formed based on NF , gain , power consumption , L_g , and L_S.

3.5 LNA Design and Optimization at 5 GHz

A 5 GHz single ended low noise amplifier is used for the WLAN (Wireless Local Area Network). With the CMOS and the latest double gate MOSFET technology, it can use this technology to design RF CMOS.

Currently, wireless applications are growing substantially in the 2.4/5 GHz frequency range because they are relatively economical and have the potential for on-chip system integration [80].

3.5.1 Mathematical Results for Single Ended LNA at 5 GHz

The analytical results are repeated for 5 GHz and can be simulated as follows in Table (3-12).

Table (3-12) : Analytical Results for Single Ended LNA at 5 GHz

Design parameters and performance	**Mathematical**
Width W_1(µm)	161.522
$\boldsymbol{I_d}$(mA)	5
C_{gs}(PF)	0.16
$\boldsymbol{g_m}$	47.07
L_S(nH)	0.17
L_g(nH)	6.33
$\boldsymbol{L_d}$(nH)	2.04
NF(dB)	1.37
Power Consumption(mw)	9
Gain(dB)	12.03

The results obtained from analytical method are applied for simulation. The simulator results for NF, power gain , and S_{11} are shown in Figure (3-17) , Figure (3-18) , and Figure (3-19) .

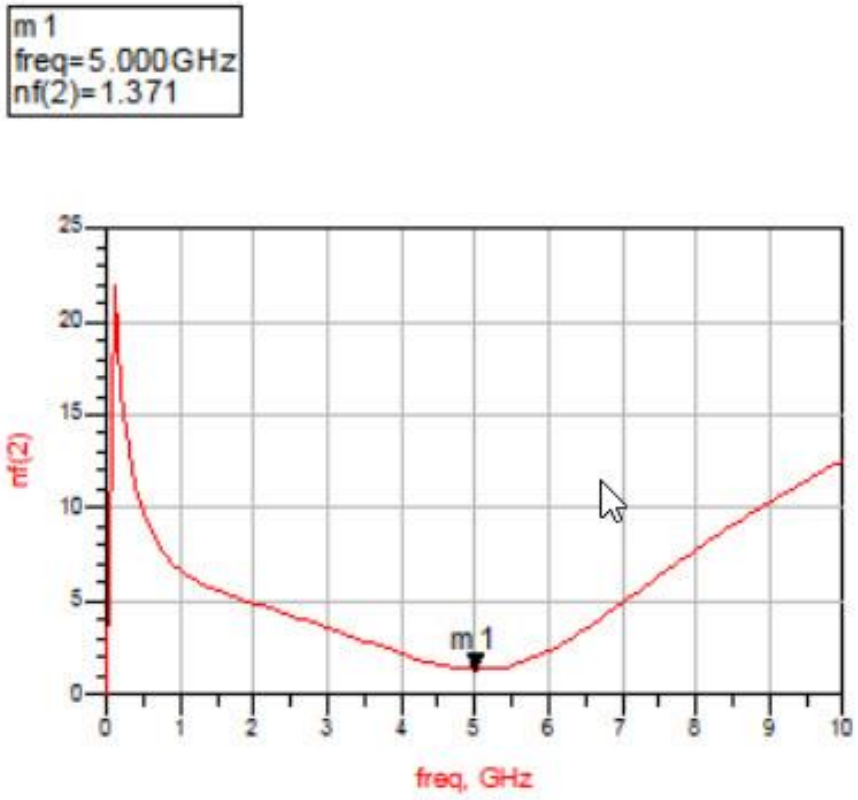


Figure (3-17): Mathematical NF Result for 5 GHz Single Ended LNA

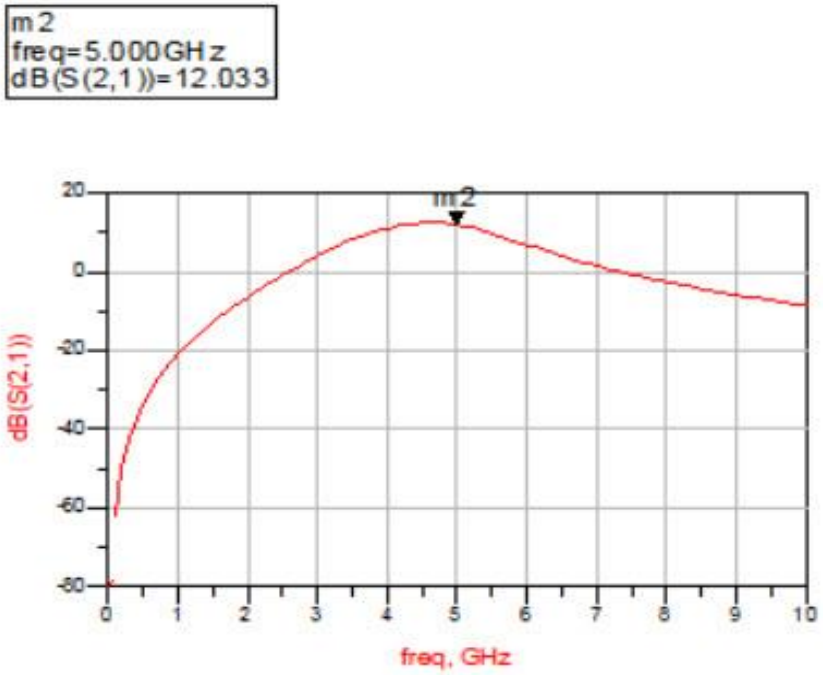


Figure (3-18): Mathematical Power Gain Result for 5 GHz Single Ended LNA

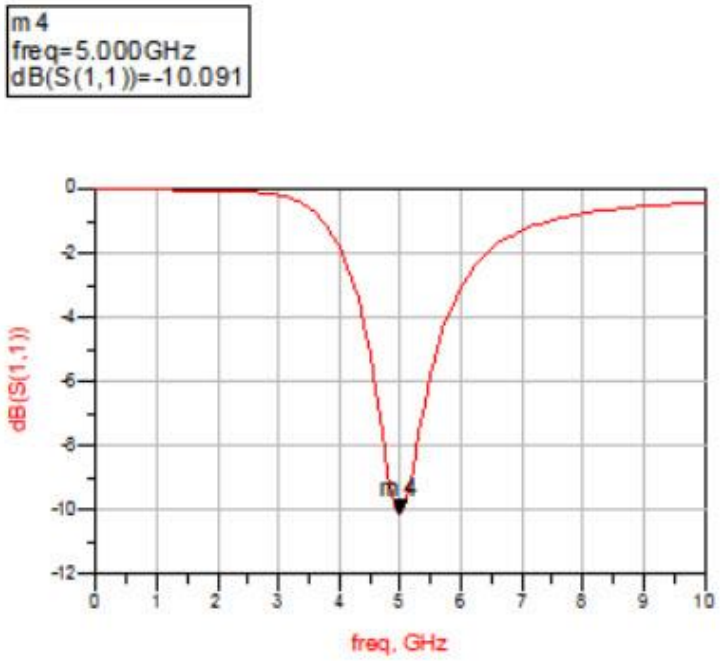


Figure (3-19): Mathematical Input Return Loss Result for 5 GHz Single Ended LNA

3.5.2 Optimization Results for Single Ended LNA at 5 GHz

A method of circuit optimization is presented using the meta-heuristic multi objective genetic algorithm to optimize a low noise amplifier operating at 5 GHz. The MOGA principle is applied as a required specification are needed to improve NF, gain and power consumption.

In order to optimize noise figure, gain and power consumption, the multi objective genetic algorithm of the MATLAB toolbox optimization technique is implemented for low noise amplifier design at 5 GHz. Direct equations for the noise figure, gain and power consumption calculated for inductive source degeneration cascode LNA were used. As discussed in previous section, the MATLAB m file is modified and the fitness functions and constraint functions are replaced with the equations. Also the design variables width w, and drain current Id have been added with their limit that actually evaluates all these equations. There are many candidates in the final Pareto set which allow the designer to choose the answers that are required.

3.5.2.1 Optimization for Power Consumption, Noise Figure, and Gain for LNA at 5 GHz

To obtain high gain for LNA, the trans-conductance, g_m, of the device MOSFET1(M1) is very significant. However, the transistor width depends on this g_m. It is also necessary to maintain the g_m/I_d ratio to meet the optimum LNA gain. Therefore, to give sufficient gain and minimum noise figure, the width of the transistor needs to be selected or optimized as shown in Figure (3-20). The normalization and Weighted Sum Method (WSM) is applied as illustrated previously. It presents a set of solution as well as the optimum solution to be selected with value of 59.69 μm.

Table (3-13): Pareto Set Solution for Optimization NF ,Gain , P for Single Ended LNA at 5 GHz.

INDEX	NF(dB)	Gain (dB)	Power Consumption(watt)	Width (µm)	I_d (mA)	WSM	L_S (H)
1	1.10178	19.8076	0.01079	64.4022	5.9955	0.5974	1E-10
2	1.31579	15.6923	0.0018	103.434	1.00023	0.7472	3.1E-10
3	1.31579	15.6923	0.0018	103.434	1.00023	0.7472	3.1E-10
4	1.17772	21.9919	0.00275	50.0824	1.52911	0.7515	1.7E-10
5	1.29366	16.9546	0.0018	89.4435	1.00023	0.7672	2.9E-10
6	1.11028	24.0216	0.00566	39.6457	3.14354	0.6932	1.1E-10
7	1.27068	18.3646	0.0018	76.0412	1.00086	0.7893	2.7E-10
8	1.11786	23.3207	0.00537	42.9777	2.98388	0.6875	1.2E-10
9	1.10178	19.8076	0.01079	64.4022	5.9955	0.5974	1E-10
10	1.25803	19.1888	0.0018	69.1573	1.00166	0.802	2.5E-10
11	1.30398	16.3543	0.0018	95.8432	1.00023	0.7577	3E-10

12	1.27954	17.8061	0.0018	81.0909	1.00073	0.7805	2.7E-10
13	1.19392	21.0246	0.00258	55.9819	1.43563	0.7484	1.9E-10
14	1.23279	20.4669	0.00191	59.6942	1.06226	0.8062	2.3E-10
15	1.10426	22.2839	0.00773	48.4265	4.296	0.6475	1E-10
16	1.1384	23.6035	0.00377	41.6011	2.09449	0.7284	1.4E-10
17	1.28279	17.6091	0.0018	82.9517	1.00028	0.7776	2.8E-10
18	1.15486	22.7404	0.00333	45.9474	1.8476	0.7326	1.5E-10

It can be seen from Figure (3-21) that the noise figure increases with increasing L_S. The optimal L_S value is therefore optimized to be 0.23 nH at a minimum noise figure. The effect of a source inductor variation on power consumption is shown in Figure (3-22), whereby the value of source degeneration inductor increases; power dispersion decreases but the inductor cannot be bulky for RF design. For a low noise amplifier design, there is usually uses tradeoff between power dissipation, gain and noise figure. In LNA design, it usually needs a tradeoff in improving performance parameters. Figure(3-23) presents a 3-dimention relationship between gain , noise figure , and power consumption. It can be seen from this figure that achieving an improvement any parameter must be in the expense of other parameters that can be noted through decreasing the gain with the increase in the value of the source inductance degenerated. Thus Ls = 0.23 nH is chosen for a further optimized value that provides the best compromise between gain and noise figure.

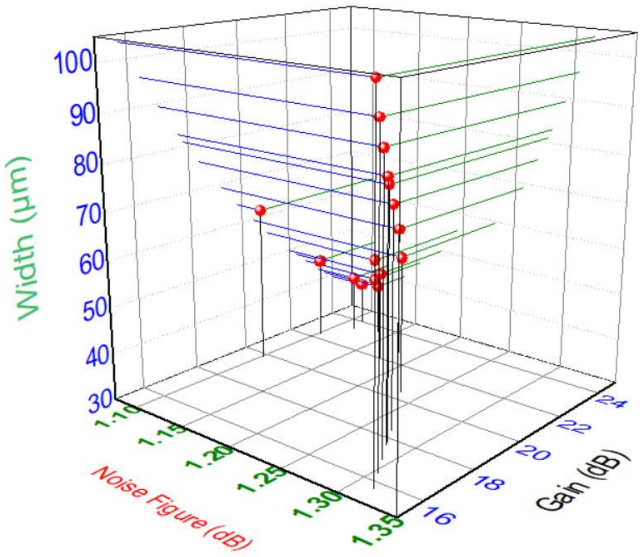


Figure (3-20): Three Dimensional Relationship Between NF , G and W

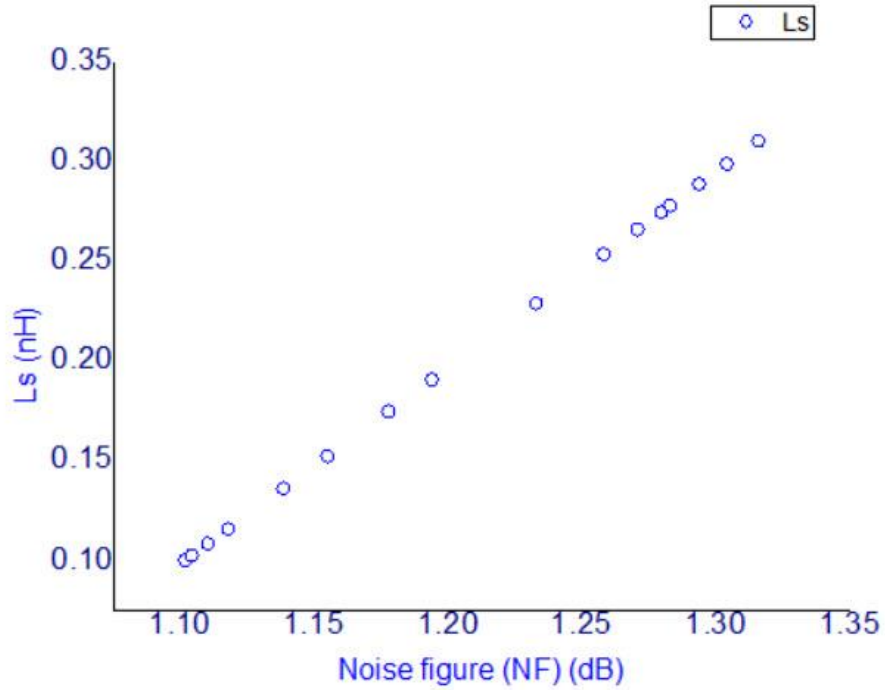


Figure (3-21): L_S versus NF

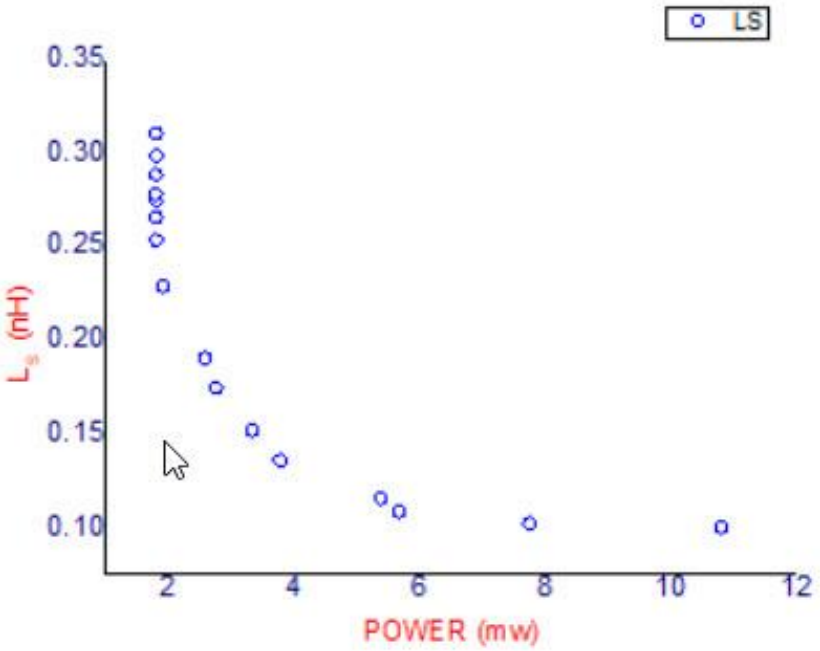
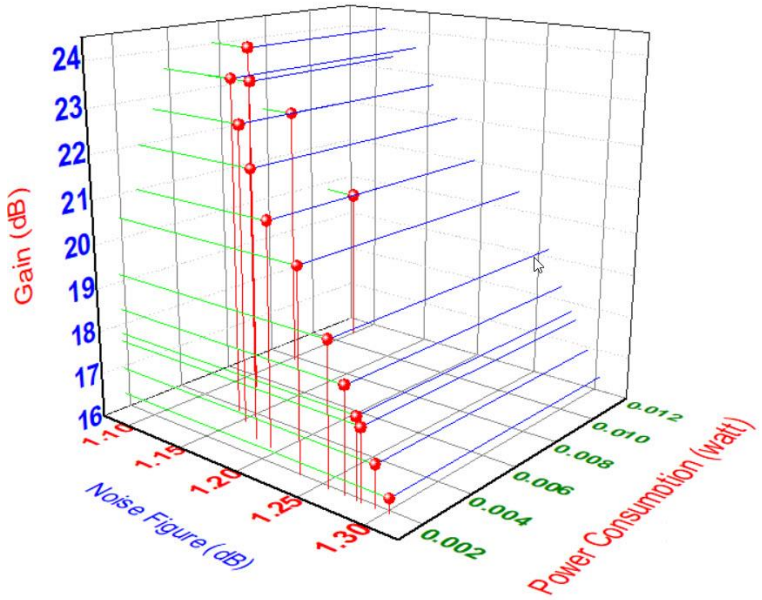


Figure (3-22): L_S versus Power Consumption



Figure(3-23): Three Dimensional Relationship Between Power , NF and Gain

After running MOGA using MATLAB toolbox, there are a lot of candidates which allow the designer to choose the answers required to specify the design requirements. For CMOS Low Noise Amplifier design for 0.18 μm technology, these design parameters which have been chosen as the optimal solution are used. The design is finally simulated with the tool ADS Advanced Design System. The analysis of S- parameters will provide the power gain and noise figure parameters. The most striking result is the noise performance of the LNA shown in Figure (3-24) . For the majority of applications, the 1.3 dB value is a sufficient result. Another worthwhile result, as shown in Figure (3-25) , is the high gain value of 20.44 dB, when the input return loss (S_{11}) =-12.79 dB as shown in Figure (3-26) that represents a good input match.

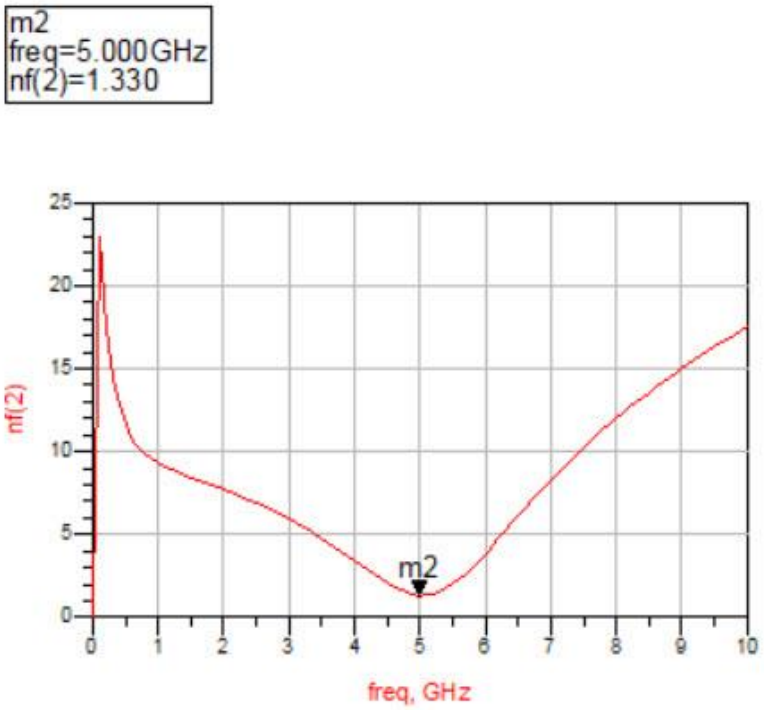


Figure (3-24): Optimized NF Result for 5 GHz Single Ended LNA

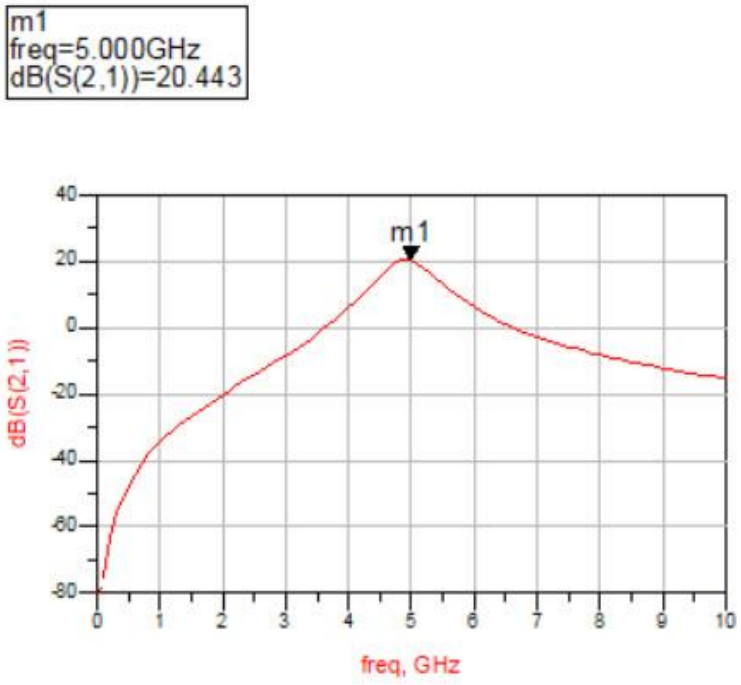


Figure (3-25): Optimized Power Gain Result for 5 GHz Single Ended LNA

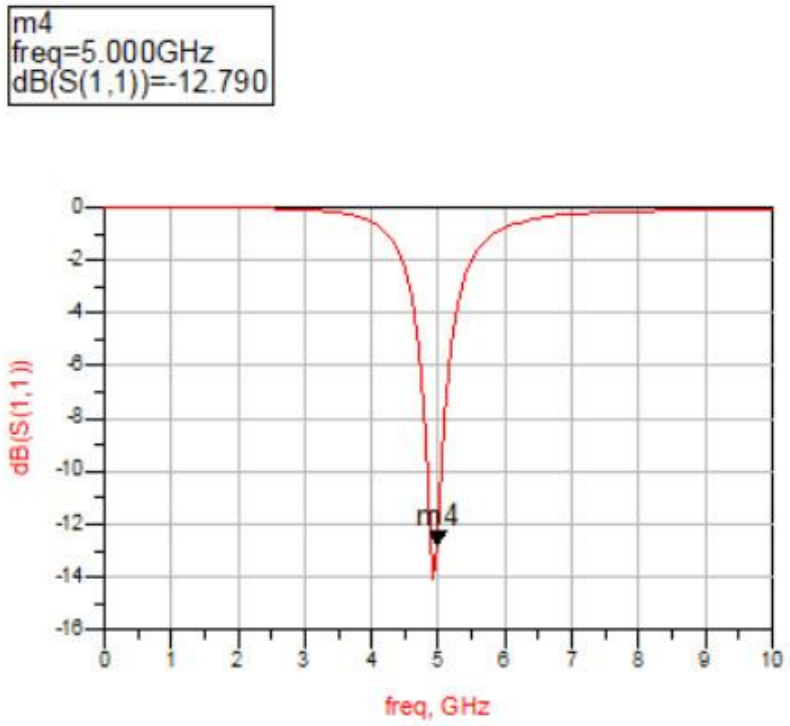


Figure (3-26): Optimized Input Return Loss Result for 5 GHz Single Ended LNA

Consequently, based on the obtained results, it can be say that the optimization method can be adopted to design an optimum amplifier.

Finally, the LNA's power consumption is 1.8 mw. The maximum power voltage is allowed at 1.8 V and the current consumption is 1.06 mA in the process.

3.5.2.2 Optimization of L_S and L_g for 5 GHz Single Ended LNA - MOGA

Optimization of inductor values L_S and L_g is achieved using Pareto set solution that obtained from implementing MOGA. The same concept of optimization previously presented can be extended to the design of LNAs

at 5 GHz. The design variables of MOGA are selected to be the width of transistor MOSFET1 W_1, and current drain I_d. Then, these variables are introduced to formulate the chromosome that containing two variables representing the genes as earlier reported and shown in Table (3-14).

Table (3-14): Design Variables and Range of Limit Using MOGA to Optimize L_S and L_g

Variables name	**Range of values**
W_1	10 to 300 µm
I_d	1 to 5 mA

The L_S and L_g parameters are used to formulate the proposed fitness functions of 5 GHz LNA system, which should be minimized in order to meet the desired system performance. While NF, gain, power consumption, and C_{gs} are used as nonlinear constraint functions. The limit of this constraints is illustrated in Table (3-15).

Table (3-15):Constraints Limit Using MOGA

Performance parameters	**Range of values**
NF	<3 dB
Gain	>15 dB
Power Consumption	<20 mw
C_{gs}	(0.1 to 10) pF

Figure (3-27) illustrates a histogram showing the score variety for every objective (fitness function) fun1 for minimization L_S , and fun 2 for minimization gate induction L_g .

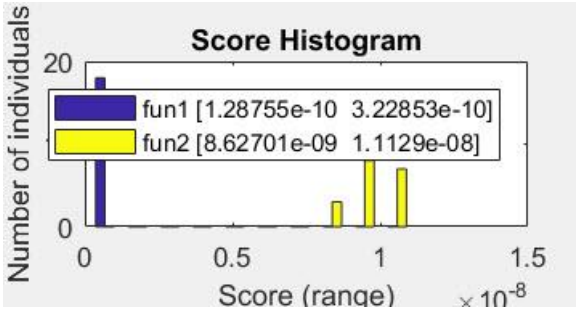


Figure (3-27) : Score Histogram

Figure (3-28) illustrates the relationship between objective 1 (L_S) and objective 2 (L_g) . This figure reveals a visualization about selection optimum value of fitness (objective) functions and relationship between them.

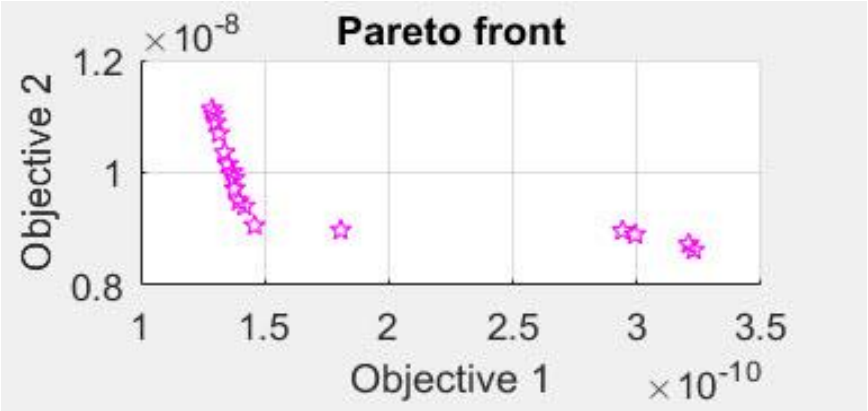


Figure (3-28):Pareto Front

Applying MOGA allows the designer to determine an optimum design parameter from Pareto set solutions that illustrated in Table (3-16) for LNA and subsequently affixes the recommended design parameters.

Table (3-16) :Pareto Set Optimum Solution for Optimization L_S and L_g for LNA at 5 GHz

INDEX	L_S(H)	L_g(H)	Width(µm)	I_d (mA)	WSM
1	3.22E-10	8.63E-09	112.00922	1.0033501	0.69972151
2	1.29E-10	1.11E-08	89.0542444	4.99969698	0.88764767
3	1.43E-10	9.00E-09	109.698879	4.98561872	0.92942719
4	2.84E-10	8.72E-09	111.340746	1.2870455	0.72158606
5	1.39E-10	9.59E-09	103.069542	4.97519244	0.91357073
6	1.37E-10	9.95E-09	99.3936428	4.94772339	0.90439743
7	1.35E-10	1.01E-08	97.8642667	4.99559939	0.90351813
8	2.12E-10	8.81E-09	111.063082	2.30533995	0.7934264
9	1.33E-10	1.04E-08	95.1171398	4.97766436	0.89728395
10	3.22E-10	8.63E-09	112.00922	1.0033501	0.69972151
11	1.63E-10	8.85E-09	111.272433	3.89535924	0.88247336
12	1.31E-10	1.09E-08	91.1919176	4.98072592	0.89029488
13	1.32E-10	1.06E-08	93.4087141	4.98375643	0.8943877
14	1.30E-10	1.10E-08	90.1339006	4.94619704	0.88678526
15	1.42E-10	9.15E-09	107.939963	4.94854237	0.9235466
16	1.29E-10	1.11E-08	89.0542444	4.99969698	0.88764767
17	1.38E-10	9.75E-09	101.38608	4.93381744	0.90797688
18	1.40E-10	9.51E-09	103.912135	4.94424966	0.91402895

A practical IC fabrication of this LNA requires minimum chip area. This concept is satisfied using this technique as shown from above table and as indicated L_S=0.14 nH and L_g=9.00 nH are significantly decreased.

However, the LNA designed using optimum parameters that obtained based on MOGA for particular bias 1.8 V, W_1= 109.69 µm and I_d=4.98 mA, will be optimized in terms of the noise figure NF=1.72 dB as shown in Figure (3-29). The low noise amplifier has a satisfactory amount of gain S_{21}=16.3 dB as shown in Figure (3-30), while input return loss S_{11} = -15.053 dB as shown in Figure (3-31) that represents a good input match.

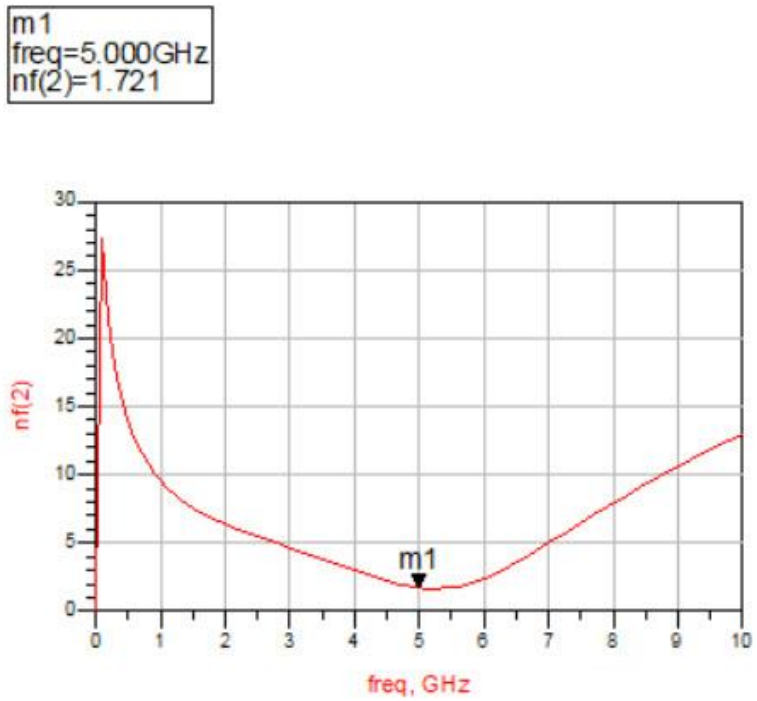


Figure (3-29): NF Based on Optimized (L_S and L_g) at 5 GHz Single Ended LNA

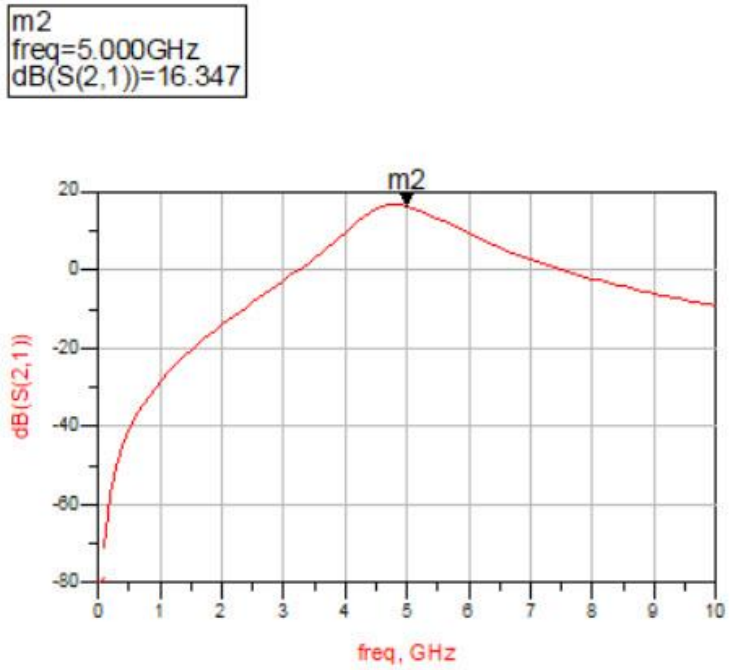


Figure (3-30): S_{21} Based on Optimized (L_S and L_g) at 5 GHz Single Ended LNA

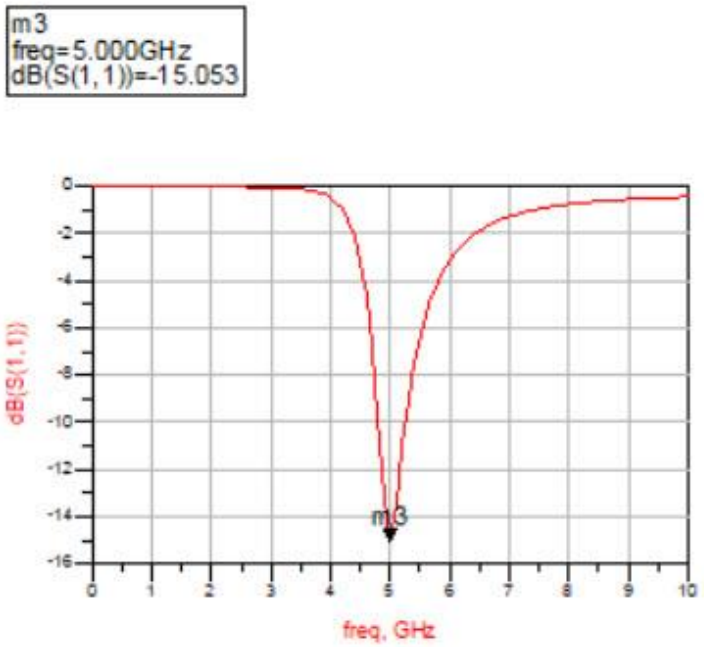


Figure (3-31): S_{11} Based on Optimized (L_S and L_g) at 5 GHz Single Ended LNA

Therefore, according to these results, it can be safely assumed that our methods using MOGA has produced an optimum design.

3.6 Comparison Between Analytical and Optimized Results Using MOGA for 5 GHz Single Ended LNA

Table (3-17**)** illustrates a comparison between the mathematical analysis method based on design equations and optimization analysis using MOGA method for LNA at 5 GHz.

Table (3-17): Comparison Between Mathematical and Optimized Results for Single Ended LNA at 5 GHz

Design and Performance Parameters	**Single Ended Low Noise Amplifier at 5 GHz**		
	Mathematical	**Optimized using MOGA(NF,G,P)**	**Optimized using MOGA (L_S , L_g)**
Width W_1(µm)	161.522	59.69	109.6
$\boldsymbol{I_d}$(mA)	5	1.06	4.9
C_{gs}(PF)	0.16	0.06	0.11
L_S(nH)	0.17	0.228	0.143
L_g(nH)	6.33	16.5	9
$\boldsymbol{L_d}$(nH)	2.04	4.49	2.46
NF(dB)	1.37	1.33	1.72
Power consumption(mw)	9	1.8	8.82
Gain(dB)	12.03	20.44	16.3

The table shows clearly that our design methodology has proven its ability to produce satisfactory results, with outstanding noise performance, adequate gain, and good matching input and output.

CHAPTER 4

Design and Optimization of Differential Low Noise Amplifier

4.1 Introduction:

The design methodology and optimization applied previously on single ended structure is used in this chapter to design and optimize differential structure [5].

DLNAs are designed and analyzed, then optimized using MOGA at frequencies of 2.4 GHz and 5 GHz. The devices and their features used in the designs are based on the 0.18-µm RF CMOS TSMC process. Performance analysis is performed using Agilent's Advanced Design System (ADS) tools for Electronic Design Automation (EDA) [80].

4.2 Differential Low Noise Amplifier

As previously illustrated, the single-end LNA consumes low power and required low chip area. Differential topology is used because of the following significant advantages. Firstly, noise is a critical factor for low-noise amplifiers, it is most popular because common-mode noise can be rejected. In theory, two sides of the circuit are close, so it is possible to view common-mode noise on each side as equal. Secondly, that is better linearity performance for the differential mode amplifier. Since the circuit is symmetrical, and it is able to eliminate even-order distortions, that increases the amplifier linearity [81].

However, DLNA consumes more power comparing to single ended counter point. Figure (4-1) represents the DLNA topology[50].

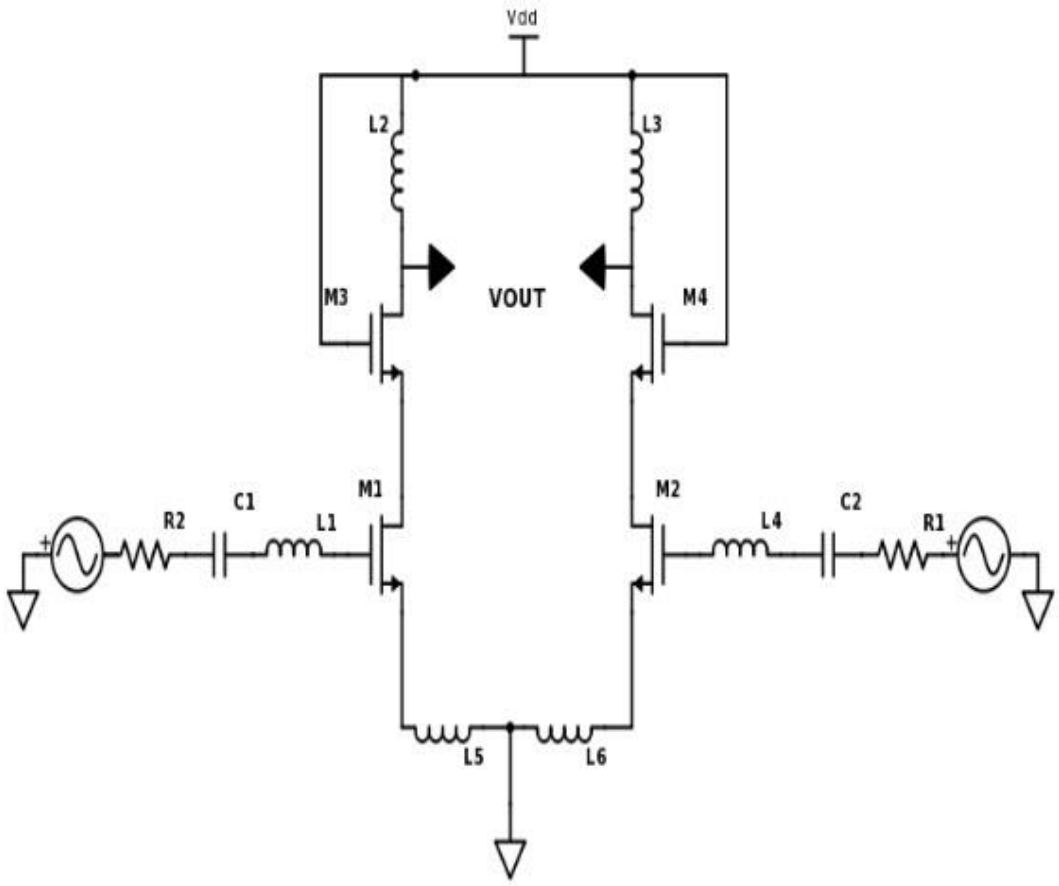


Figure (4-1) : DLNA Structure

4.3 Mathematical Results of 2.4 GHz DLNA

The steps taken to design the DLNA are identical that of the single-ended LNA. Since it includes two single-ended configurations that are connected back to back. The gain and noise figure and power consumption can be calculated and validated using ADS simulator [80].

- Voltage Gain

$$A_V = \frac{g_m}{C_{gs}\, w_0} \qquad (4\text{-}1)$$

- The minimum noise figure

$$\boldsymbol{NF = \left(1 + 2.4 * \frac{w_0}{W_T}\right)} \qquad \textbf{(4-2)}$$

- The power dissipation

$$\boldsymbol{P_D = 2 * I_d * V_{DD}} \qquad \textbf{(4-3)}$$

Table (4-1) illustrates the analytical results obtained using the above mathematical equations.

Table (4-1): Mathematical Results for DLNA Simulated at 2.4 GHz

Design parameters and performance	**Mathematical**
Width W_1(µm)	336.7
$\boldsymbol{I_d}$(mA)	5
C_{gs}(PF)	0.34
$\boldsymbol{g_m}$	67.93
L_S(nH)	0.25
L_g(nH)	12.8
$\boldsymbol{L_d}$(nH)	4.33
NF(dB)	1.5
Power Consumption(mw)	18
Gain(dB)	12.5

Figure (4-2) variation of NF based on frequency for DLNA. It can be seen from the figure that the lowest NF is achieved at frequency 2.4 GHz. Presents the lowest noise figure simulated result for the DLNA designs. The noise figure is around 1.5 dB as low as for single-end design, but due

to two signal paths, it costs higher power consumption about 18 mw based on equation.

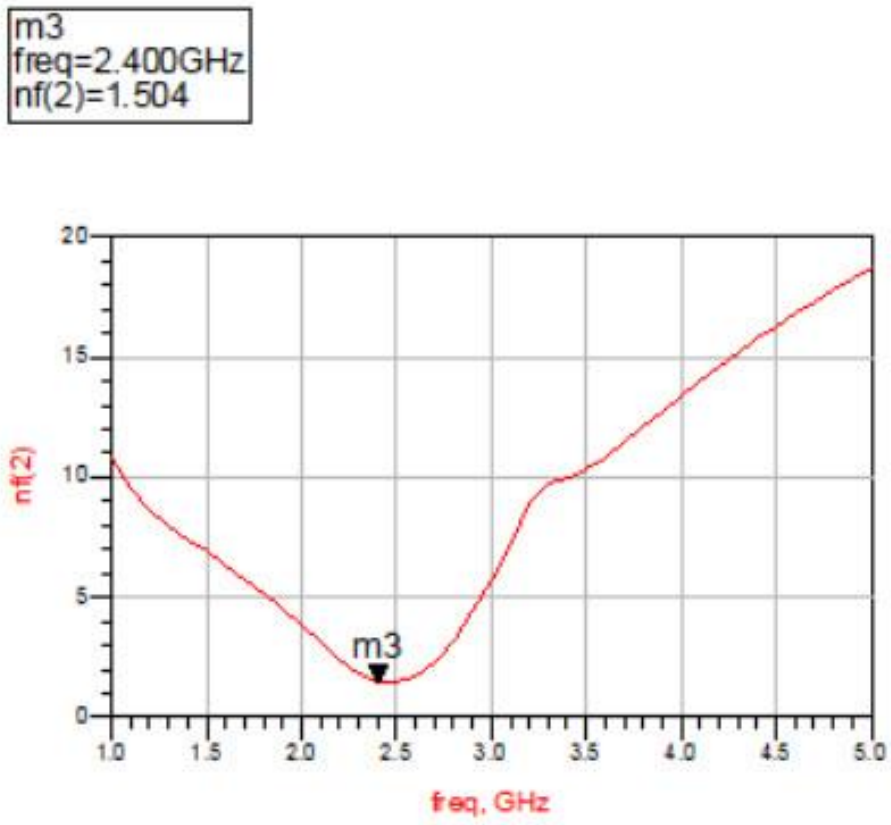


Figure (4-2): Mathematical NF result for 2.4 GHz DLNA

The power gain value of S_{21} is equal to 12.5 dB as shown in Figure (4-3). Typically, the gain requirement is in the range of 20 dB at 2.4 GHz frequency. The gain limit is satisfied by DLNA, but the value is still less. To sort out this problem, the designed system is optimized using GA. Figure (4-4) shows the input reflection coefficients S_{11}=-7.5 dB for matching between input and output S_{11} should be less than -10 dB.

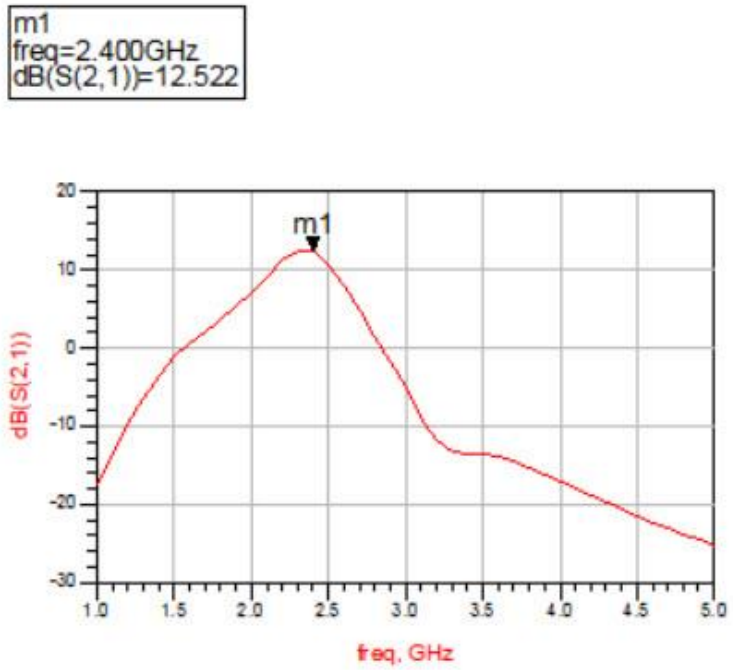


Figure (4-3): Mathematical Power Gain Result for 2.4 GHz DLNA

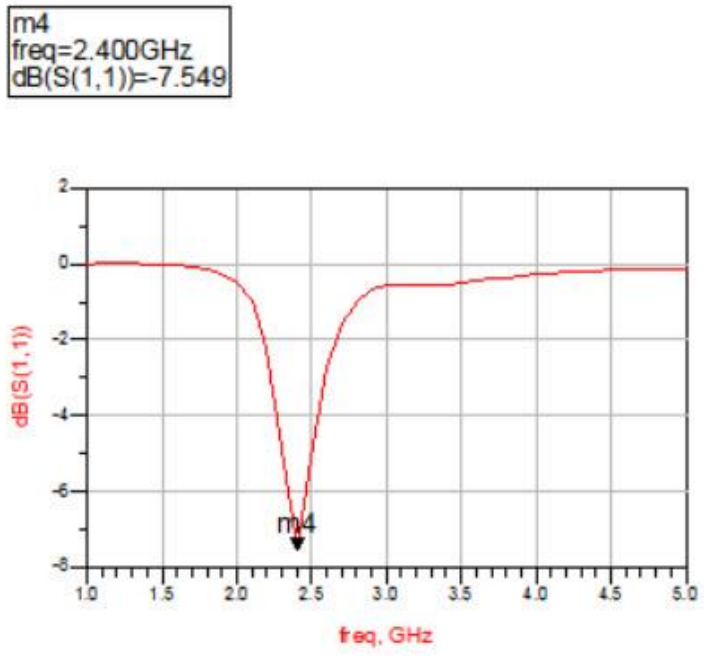


Figure (4-4): Mathematical Input Reflection Coefficients (S_{11}) Result for 2.4 GHz DLNA

4.4 Optimized 2.4 GHz DLNA Based on MOGA

The design of 2.4 GHz DLNA is presented in this section, the optimization of system parameters is achieved using MOGA.

4.4.1 Minimization for Power Consumption, Noise Figure and Maximization Gain

Design of DLNA topology involves selection best values for noise figure, power consumption, and gain that can lead to achieve the desired or required circuit performance specifications.

In this realization, the MOGA tries to optimize the values of the fitness through tradeoff between minimization the power consumption and noise figure and maximization gain.

The power consumed in the DLNA is significantly important because its value is twice of the single ended LNA, since the current flow is twice the of the single ended LNA. The chromosomes are generated randomly. The width of MOSFET1 W_1 and drain current I_d are the design variables that formulate the chromosome.

The optimal values of performance parameters obtained by MOGA are given in Table (4-2).

Table (4-2): Pareto Set Solution for Optimization NF ,Gain, P for DLNA at 2.4 GHz

INDEX	NF(dB)	Gain(dB)	Power Consumption(watt)	Width (µm)	I_d (mA)	WSM
1	1.1021	27.424	0.015	89.053	4.1667	0.7459
2	1.1021	27.424	0.015	89.053	4.1667	0.7459
3	1.1915	21.962	0.0044	91.718	1.2198	0.8471
4	1.2125	21.056	0.0036	92.637	1.0001	0.8914
5	1.1879	22.128	0.0045	90.916	1.2563	0.844
6	1.2125	21.056	0.0036	92.637	1.0001	0.8914
7	1.1136	26.5	0.0122	89.469	3.3834	0.7496
8	1.1412	24.606	0.0081	92.008	2.2497	0.7684
9	1.1998	21.594	0.0041	92.354	1.1286	0.8605
10	1.181	22.449	0.0048	90.466	1.346	0.8331
11	1.1376	24.829	0.0085	91.947	2.3665	0.7651
12	1.1074	26.983	0.0139	91.092	3.8502	0.7453
13	1.122	25.878	0.0109	92.098	3.0182	0.7513
14	1.1047	27.204	0.0143	89.605	3.9851	0.7464
15	1.1284	25.43	0.0098	91.872	2.7155	0.7564
16	1.1691	23.044	0.0056	91.864	1.5675	0.8078
17	1.1622	23.403	0.0061	90.943	1.6856	0.7965
18	1.1168	26.255	0.0116	90.17	3.2231	0.7508

Best values for performance parameter can be obtained using MOGA approach which are listed in Table (4-2), and after implementing these values in ADS. Figure (4-5) shows an improvement in NF is achieved due to using DLNA which added a minimum noise. The NF provides a very good power gain (S_{21}) as shown in Figure (4-6), while Figure (4-7) illustrates the response of input reflection coefficients S_{11}.

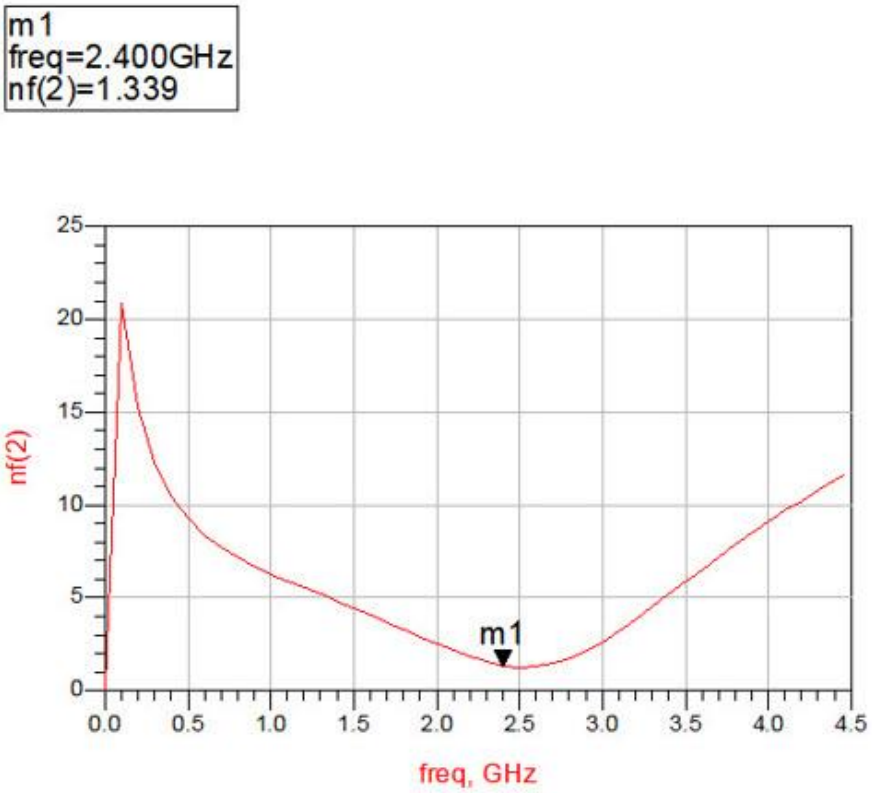


Figure (4-5): Optimized NF Result for 2.4 GHz DLNA

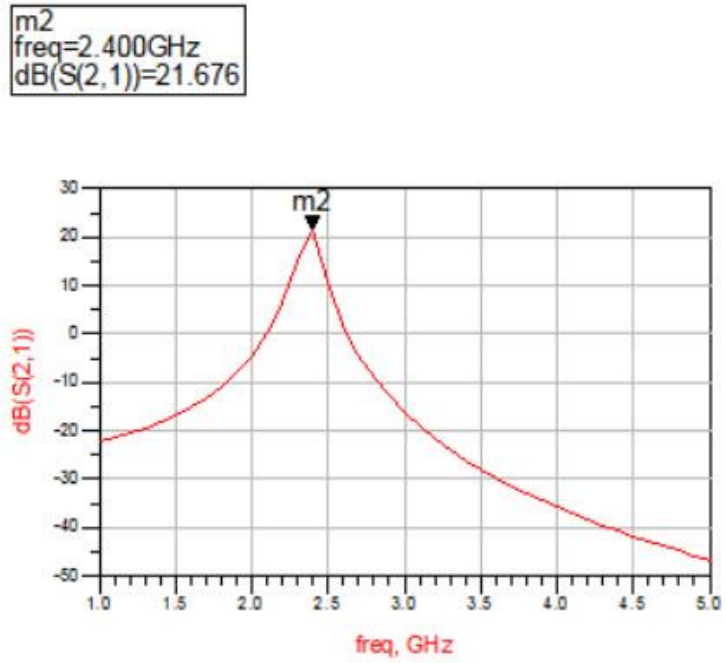


Figure (4-6): Optimized S_{21} Result for 2.4 GHz DLNA

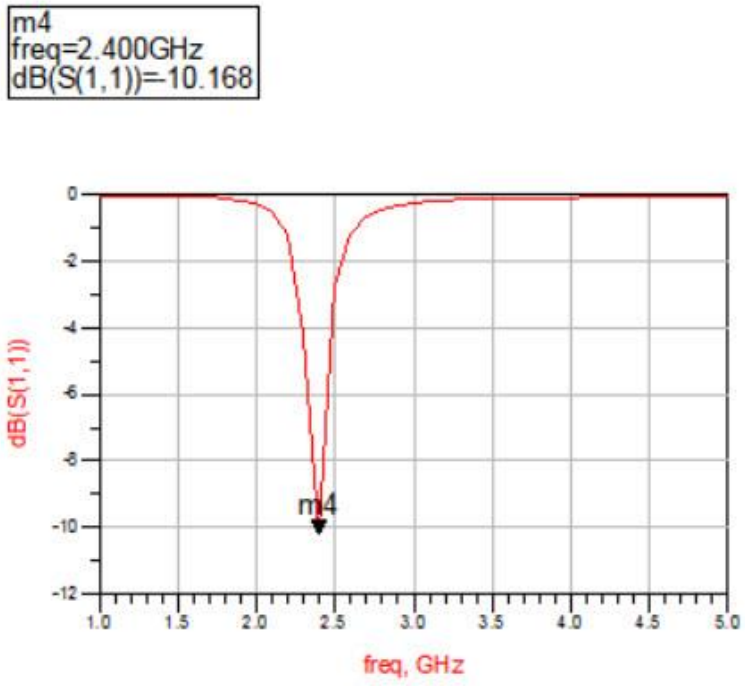


Figure (4-7): Optimized S_{11} Result for 2.4 GHz DLNA

Figure (4-8) shows variation of NF, gain, and power consumption obtained from Pareto set solution.

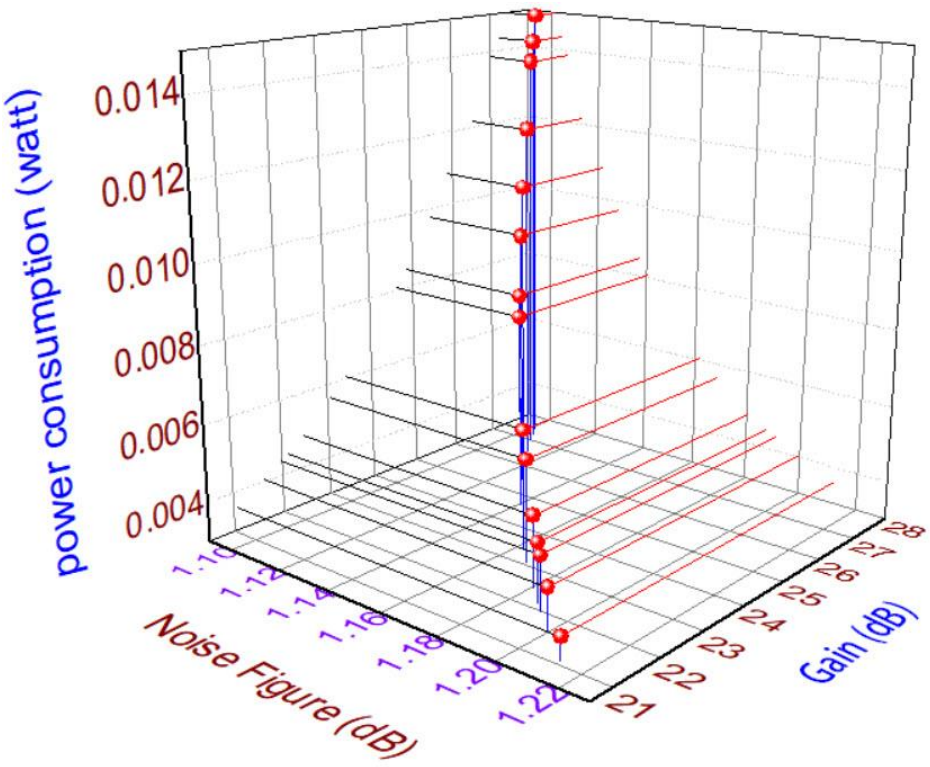


Figure (4-8): Three Dimensional Relationship Between NF, Gain ,Power Consumption for DLNA at 2.4 GHz

It is obvious from the above figure that it is impossible to improve all performance parameters. Therefore, tradeoff method is needed to concentrate on specified performance parameter.

Table (4-3) illustrates a comparison between the mathematical and Optimized result based on MOGA for 2.4 GHz DLNA system.

Table (4-3):Comparison Between Mathematical and Optimized Results for DLNA at 2.4 GHz.

Design Parameters and Performance	**Differential Low Noise Amplifier at 2.4 GHz**	
	Mathematical	**Optimized using GA**
Width W_1(µm)	336.7	92.637
$\boldsymbol{I_d}$ (mA)	5	1
C_{gs}(PF)	0.34	0.0936
$\boldsymbol{g_m}$	67.93	15.9
L_S(nH)	0.25	0.29
L_g(nH)	12.8	46.67
$\boldsymbol{L_d}$**(** nH**)**	4.33	4.2
NF(dB)	1.5	1.3
Power Consumption(mw)	18	3.6
Gain(dB)	12.5	21.67

The design of LNA using differential low noise amplifier extends the complexity of the realized structure. However, the quality of design choice is achieved with several goals such as gain, NF, power compression.

4.4.2 Optimization of L_S and L_g for 2.4 GHz DLNA

The gate inductor L_g and the source inductor L_S or the degenerated inductor plays a critical role in obtaining the resonance frequency. Therefore, the values of these inductors are optimized so that they produce the resonant frequency at which the design has to operate. The implementing MOGA results a Pareto set solution as shown in Table (4-4) for DLNA topology. The application of WSM procedure after that is to select the optimum solution among the Pareto set. The obtained results include source inductor that minimized to 0.2 nH, and the gate inductor which is minimized to 20.9 nH. The width of transistor W_1=206.2496135 µm when the current I_d = 4.809501957 mA.

Table (4-4):Pareto Set Optimum Solution for Optimization L_S and L_g for DLNA at 2.4 GHz

INDEX	L_S(H)	L_g(H)	Width(µm)	I_d (mA)	WSM
1	1.29E-10	4.82E-08	90.01555482	4.999083148	0.716733846
2	1.29E-10	4.82E-08	90.01555482	4.999083148	0.716733846
3	1.82E-10	2.51E-08	171.9932242	4.84711275	0.772173759
4	1.54E-10	3.52E-08	123.1119337	4.819790411	0.716727731
5	1.56E-10	3.34E-08	129.5800287	4.933166922	0.726593018
6	1.78E-10	2.61E-08	165.7985862	4.864397843	0.764269976
7	1.36E-10	4.44E-08	97.65138892	4.905878061	0.710764937
8	1.33E-10	4.55E-08	95.27384209	4.99381016	0.715199515
9	1.31E-10	4.82E-08	90.08020241	4.852628503	0.709343543
10	1.62E-10	3.22E-08	134.3798095	4.763989327	0.723794059
11	1.65E-10	3.00E-08	144.4787785	4.951531095	0.741626005
12	1.49E-10	3.71E-08	116.8614333	4.893728222	0.715924345
13	1.32E-10	4.66E-08	93.20812644	4.992333826	0.715484063
14	1.38E-10	4.30E-08	100.9229712	4.90228323	0.71074016
15	1.48E-10	3.78E-08	114.5350706	4.896247728	0.714782451
16	1.71E-10	2.79E-08	154.9000795	4.95284897	0.753622442
17	2.00E-10	2.09E-08	206.2496135	4.809501957	0.823994089
18	1.39E-10	4.16E-08	104.1808413	4.99775689	0.715710349

Figure (4-9) shows the simulated result of noise figure (NF) which is equal to 1.52 dB . Figure (4-6) depicts power gain (S_{21}) of 18.1 dB. Figure (4-11) shows the simulated result of the input return loss (S_{11}) which is equal to -20.1dB at 2.4 GHz.

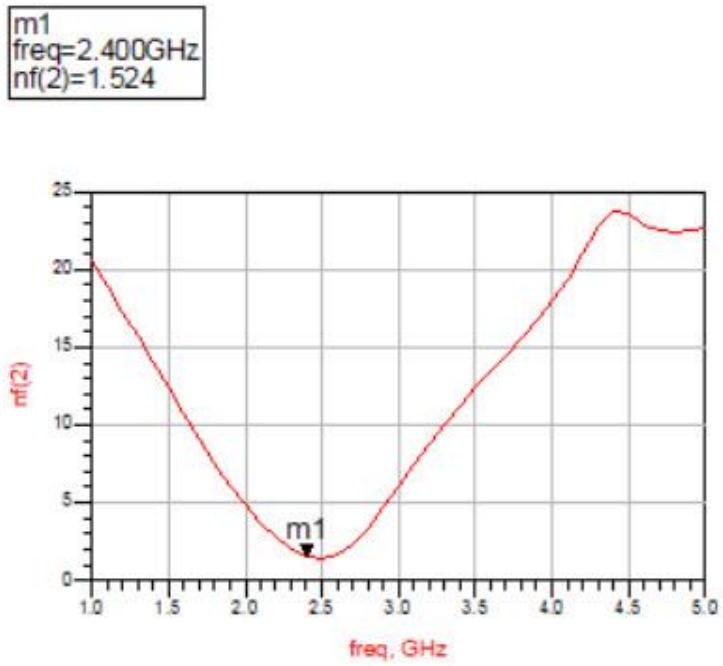


Figure (4-9): NF Based on Optimized (L_S and L_g) at 2.4 GHz DLNA

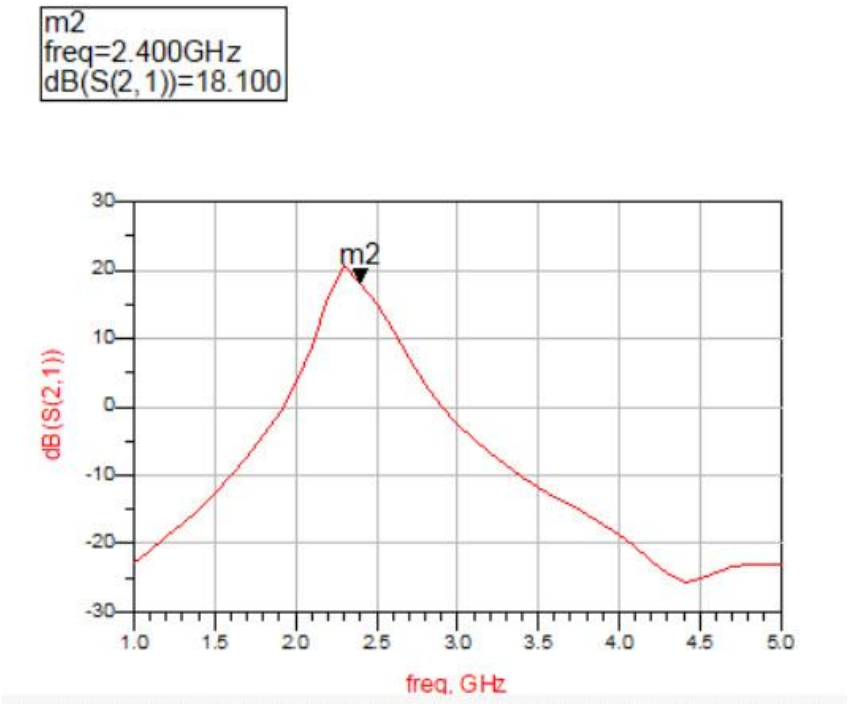


Figure (4-10): S_{21} Based on Optimized (L_S and L_g) at 2.4 GHz DLNA

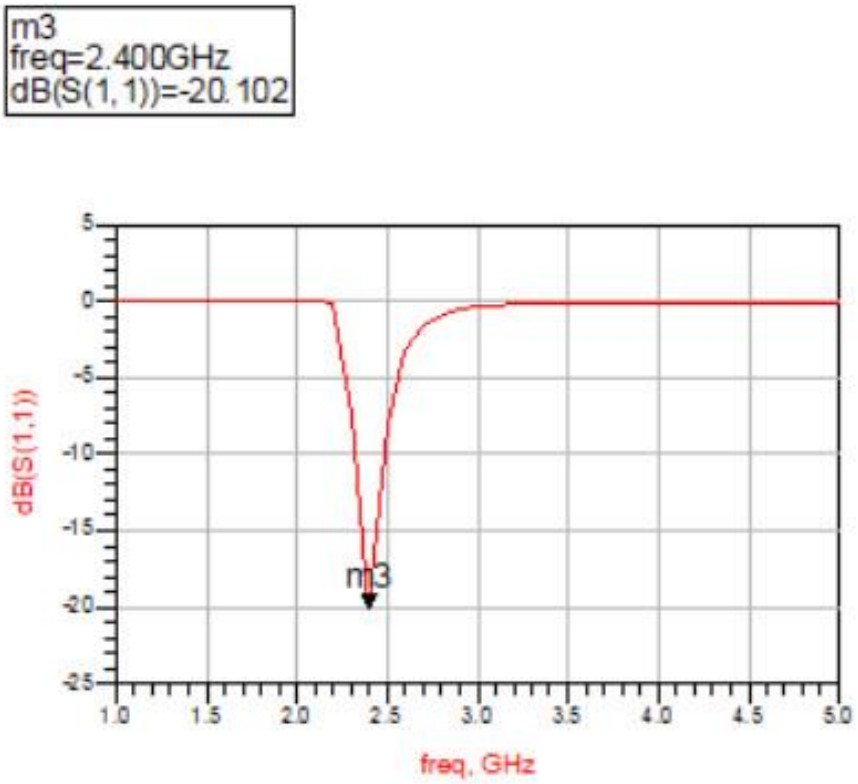


Figure (4-11): S_{11} Based on Optimized (L_S and L_g) at 2.4 GHz DLNA

4.5 Comparison Between Analytical and Optimized Results Using MOGA for 2.4 GHz DLNA

Table (4-5) illustrates a comparison between the mathematical analysis method based on design equations and the optimized results using multi-objective genetic algorithm method at frequency 2.4 GHz.

Table (4-5): Comparison Between Design Techniques for DLNA at 2.4 GHz .

Design Parameters and Performance	**Differential Low Noise Amplifier at 2.4 GHz**		
	Mathematical	**Optimization (NF ,Gain ,P)**	**Optimized using MOGA (L_S , L_g)**
Width W_1(µm)	336.7	92.637	206.2
$\boldsymbol{I_d}$ (mA)	5	1	4.80
C_{gs}(PF)	0.34	0.0936	0.208
$\boldsymbol{g_m}$	67.93	15.9	52.1
L_S(nH)	0.25	0.29	0.20
L_g(nH)	12.8	46.67	20.9
NF(dB)	1.5	1.3	1.524
Power consumption(mw)	18	3.6	17.28
Gain(dB)	12.5	21.67	18.1
S_{11}(dB)	-7.5	-10.168	-20.102

It is clear from the above table that a significant reduction in L_S and L_g values, that is important in realizing LNA practically. However, the expense of this improvement is clear on NF, gain and power consumption.

4.6 Design and Optimization of 5 GHz DLNA

Wireless applications in the 5 GHz frequency are currently receiving greater attention because they are relatively economical and have potential for on-chip system integration. IEEE 802.11a / b / g is a promising market standard for portable / wireless communications devices such as cell phones, WLANs, RFICs, global positioning systems and so on. The IEEE 802.11a standard is based purely on the modulation technology of orthogonal frequency division multiplexing (OFDM) in the 5 GHz frequency range, and it is compatible with data rates up to 54 Mbps. It provides almost four to five times the data rate, and has 10 times the overall system capacity currently available in wireless IEEE 802.11b [80] [82].

4.6.1 Mathematical Results for 5 GHz DLNA

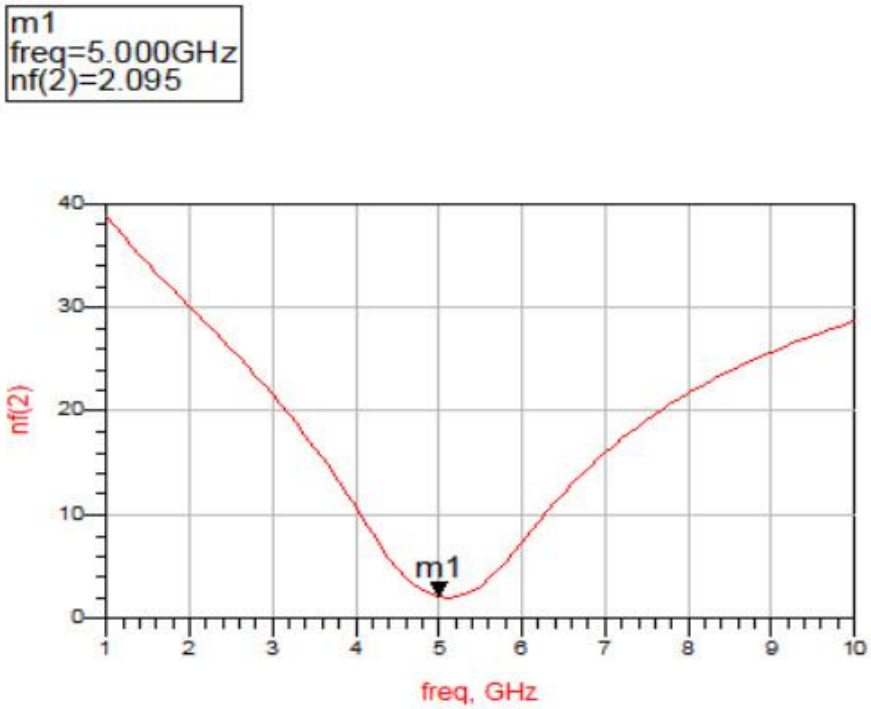
The same procedure applied previously for 2.4 GHz is performed for 5 GHz. The channel length is fixed at 180 nm and mathematical analysis is used to find other parameters, so that the design parameters of the DLNA circuit are analyzed with respect to the operating frequency of 5 GHz.

Table (4-6) presents the mathematical design parameter values in addition to the resulted performance parameters value that include NF, gain and power consumption.

Table (4-6): Mathematical Results for Simulated 5 GHz DLNA

Design Parameters and Performance	**Mathematical**
Width W_1(µm)	161.522
$\boldsymbol{I_d}$(mA)	5
C_{gs}(PF)	0.16
$\boldsymbol{g_m}$	47.07
L_S(nH)	0.17
L_g(nH)	6.33
$\boldsymbol{L_d}$(nH)	2.04
NF(dB)	2.09
Power Consumption(mw)	18
Gain(dB)	12.76

The simulation for NF, gain and input reflection coefficients (S_{11}) results are illustrated in Figure(4-12) , Figure (4-13) and Figure (4-14) respectively.



Figure(4-12): Mathematical NF Result for 5 GHz DLNA

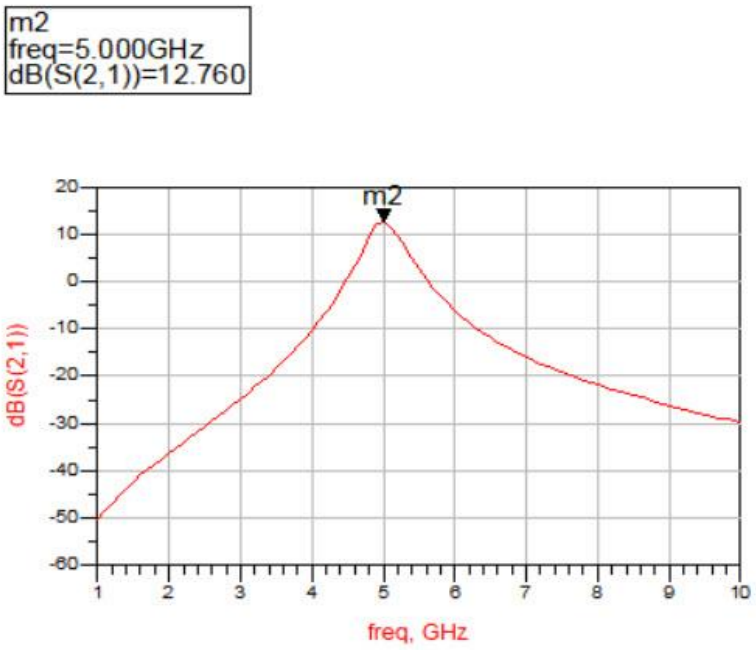


Figure (4-13): Mathematical Power Gain Result for 5 GHz DLNA

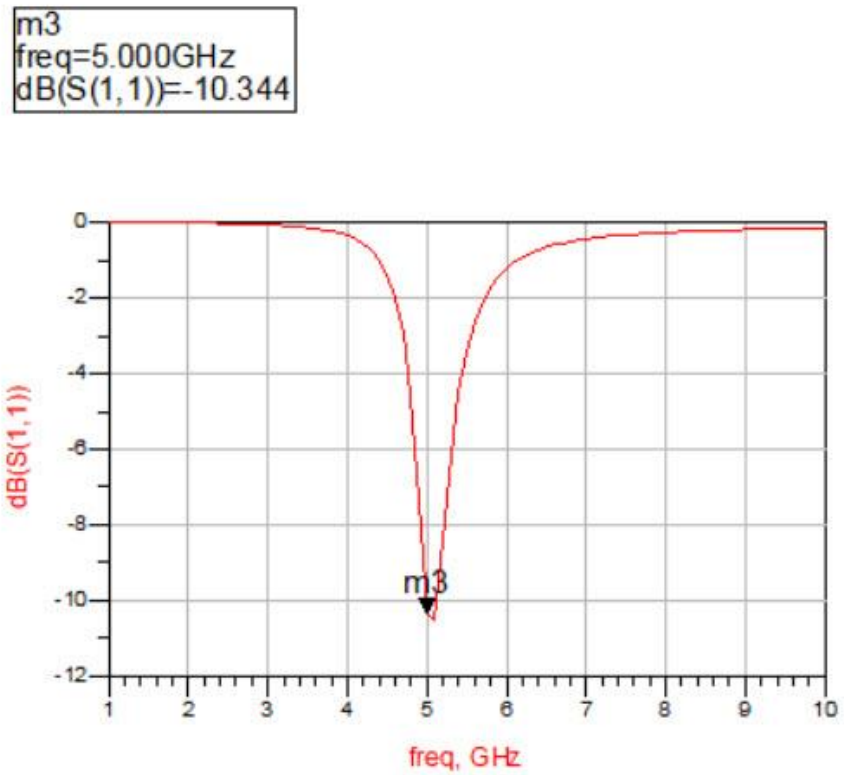


Figure (4-14): Mathematical Input Reflection Coefficients Result for 5 GHz DLNA

4.7 Optimized 5 GHz DLNA

An optimization method can be a sufficient solution to reduce the difficulties of mathematical analytics and to match the specific performance of DLNA at 5 GHz. A multi-objective genetic algorithm as a search algorithm is used to solve and improve certain system requirements in two ways, as described in these two sections.

4.7.1 Minimization for Power Consumption, Noise Figure and Maximization Gain

This optimization process requires splitting performance specifications for DLNA into fitness function, constraints and design variables as mention previously. Noise figure, power consumption, and gain are needed as fitness functions, while inductive source L_S and inductive gate L_g and source gate capacitor C_{gs} are condensed as constraint functions, where drain current I_d and width of MOSFET1 W_1 applied as the design variables. After processing the MOGA using MATLAB optimization toolbox, the Pareto set solution is resulted as shown in the Table (4-7), then to select the optimum design from this set of solution , normalization and weighted sum approach with the same weight for each fitness are used .

Table (4-7):Pareto Set Optimum Solution for Optimization Gain ,Power Consumption and NF for DLNA at 5 GHz.

INDEX	NF(dB)	Gain (dB)	Power Consumption(watt)	Width (µm)	I_d (mA)	WSM
1	1.519935	13.28525	0.0036	127.7227	1.000016	0.797184
2	1.388592	15.81434	0.004931	97.72114	1.369735	0.770607
3	1.462615	14.29983	0.003677	103.2847	1.021485	0.815907
4	1.194165	21.84081	0.018	89.05831	4.999991	0.732601
5	1.227108	20.47958	0.013279	89.88695	3.688656	0.726584
6	1.311234	17.74249	0.008199	104.2325	2.27754	0.719996
7	1.243751	19.86531	0.011892	92.72829	3.303367	0.723412
8	1.348973	16.74838	0.005869	93.79701	1.630199	0.754415
9	1.217732	20.84577	0.01477	91.89171	4.102678	0.725552
10	1.314499	17.65185	0.007101	92.17551	1.972486	0.740473
11	1.256051	19.43771	0.010741	92.41549	2.983524	0.724568
12	1.43409	17.85263	0.003601	89.05269	1.000286	0.882392
13	1.496619	13.68376	0.003602	116.5852	1.000537	0.807162
14	1.208692	21.2141	0.016306	93.19862	4.529326	0.725965
15	1.294365	18.2265	0.008481	96.44899	2.355923	0.726463
16	1.519935	13.28525	0.0036	127.7227	1.000016	0.797184
17	1.19417	21.84058	0.017999	89.0588	4.999747	0.732599
18	1.369072	16.26199	0.005534	98.93166	1.537263	0.755021

Hence, the MOGA-based design procedure is effective to obtain the optimal parameters value of design that appear in satisfaction of both constraints and objective functions of the DLNA.

Figure (4-15) shows that the improvement in the noise figure and gain is at the expense of the power consumed. The DLNA gain should be high in order to suppress the noise of the later front-end stages. DLNA is unable to amplify the incoming weak signal to an optimum level if the gain is too small.

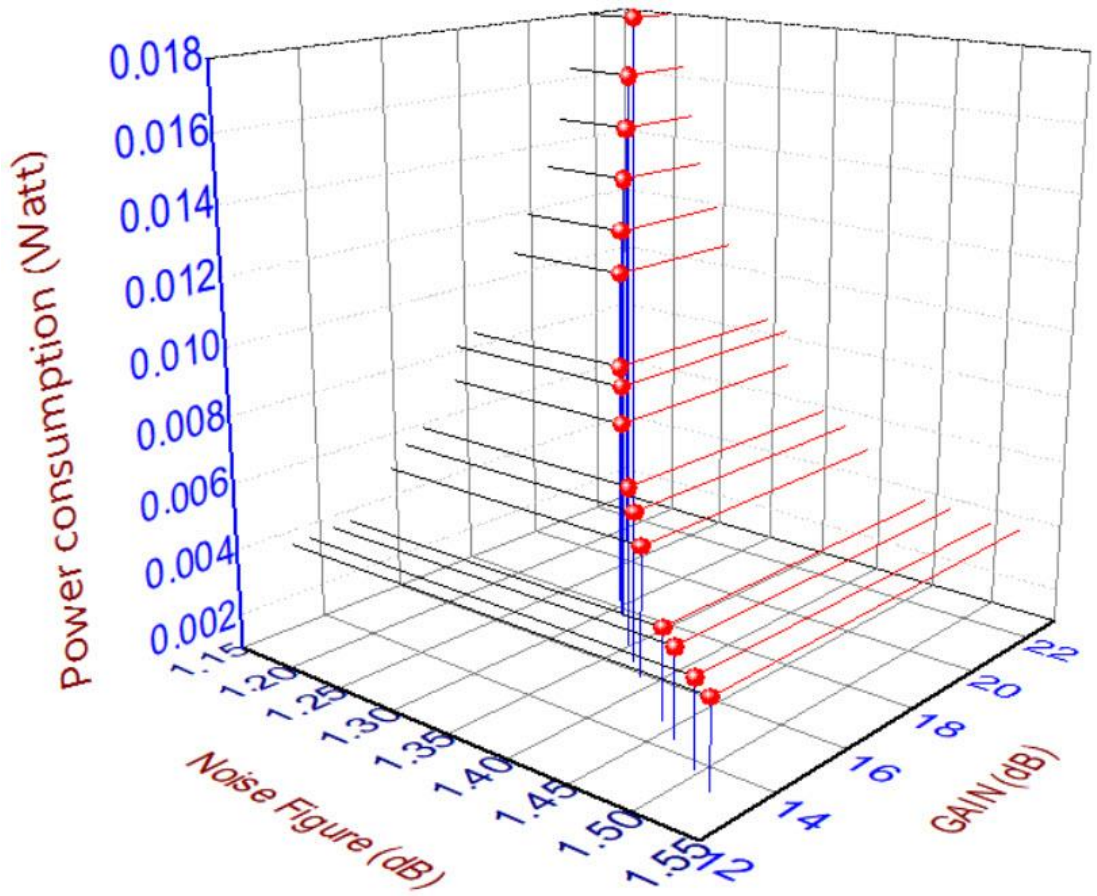


Figure (4-15): Three Dimensional Relationship Between NF, Gain and Power Consumption for 5 GHz DLNA

In general, in other stages of the receiver, such as the mixer, IF amplifier, etc, the noise figure of the LNA should remain below 5 dB to avoid causing noise problems. Figure (4-16) shows the optimized NF =1.6 dB.

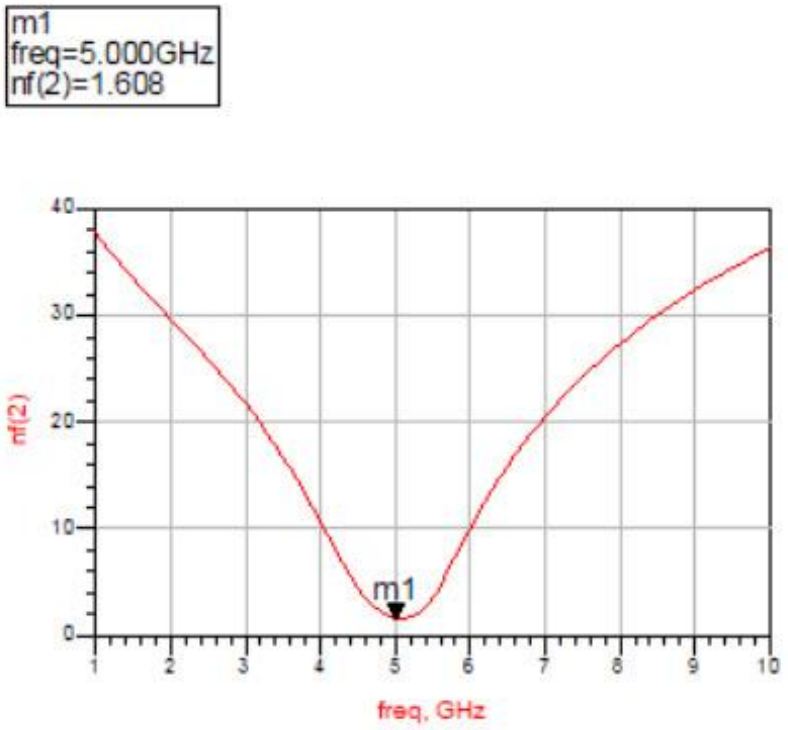


Figure (4-16): Optimized NF Result for 5 GHz DLNA

Figure (4-17) shows the optimized power gain response for DLNA based on MOGA tuning method . It is obvious from the figure that the gain S_{21} is 18.64 dB which is considered a sufficient to enhance any weak signal.

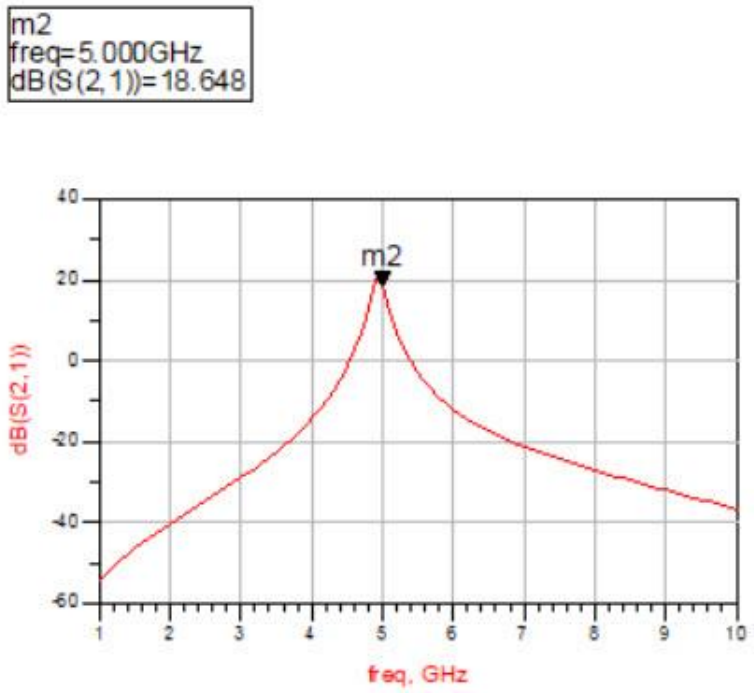
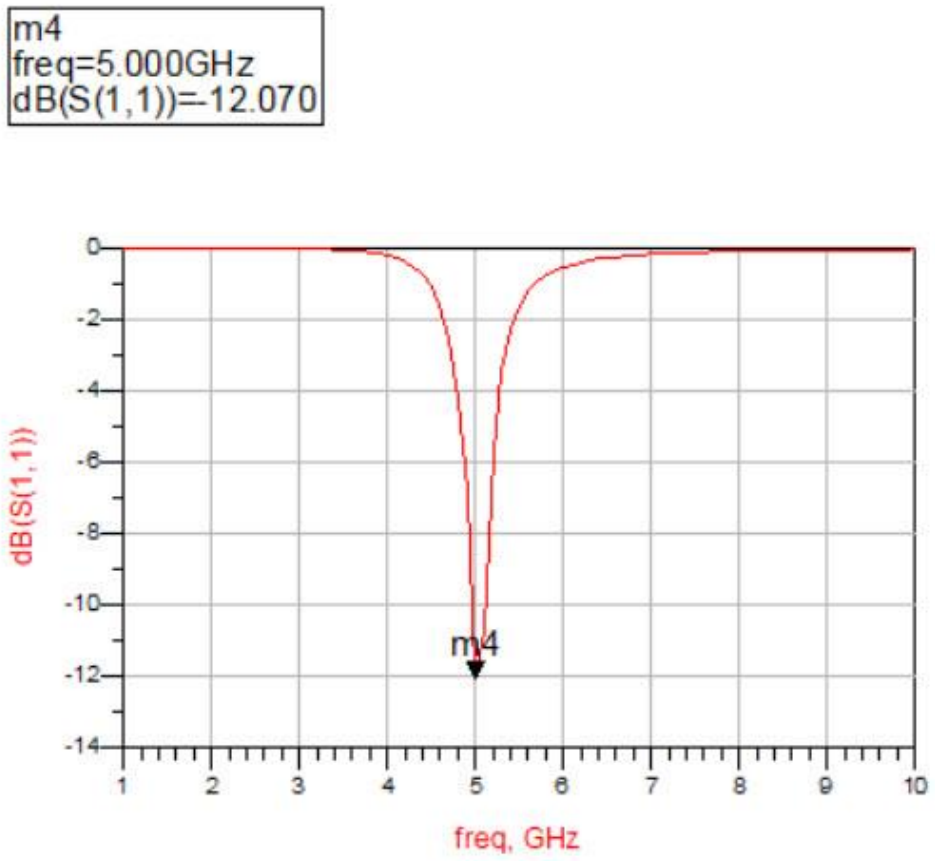


Figure (4-17): Optimized Power Gain Result for 5 GHz DLNA

Figure(4-18) present input impedance matching for DLNA based on MOGA. The simulation output provides the matching value of the input as S_{11}=-12.07 dB that meets the LNA matching constraint requirements of S_{11} <-10 dB at 5 GHz.



Figure(4-18): Optimized The Input Reflection Coefficients (S_{11}) Result for 5 GHz DLNA

4.7.2 Reduction of Inductive Source Degeneration and Inductive Gate DLNA

More compact inductive designs would have significantly reduced the chip area by reducing the values of L_S and L_g at the cost of a slightly more noise figure increase [83].

Table (4-8) illustrates Pareto set solution that L_S and L_g are considered as objective functions

Table (4-8):Pareto Set Optimum Solution for Optimization L_S and L_g for DLNA at 5 GHz

INDEX	L_S(H)	L_g(H)	Width(µm)	I_d (mA)	WSM
1	1.36E-10	1.01E-08	98.2369469	4.97618914	0.80226441
2	1.37E-10	9.84E-09	100.465626	4.95485572	0.80312282
3	1.68E-10	6.84E-09	143.15308	4.73639264	0.85825881
4	1.51E-10	8.08E-09	121.839159	4.98587915	0.83086361
5	3.51E-10	6.36E-09	149.463612	1.12898111	0.6879194
6	1.84E-10	6.65E-09	146.664405	4.02937688	0.83621258
7	1.47E-10	8.52E-09	115.69271	4.96972055	0.82124473
8	1.40E-10	9.45E-09	104.54173	4.95776499	0.80719647
9	1.63E-10	7.05E-09	138.952125	4.88436512	0.85605827
10	1.54E-10	7.77E-09	126.459106	4.93486099	0.835997
11	1.35E-10	1.03E-08	96.5291709	4.96424492	0.80037039
12	1.45E-10	8.79E-09	112.164596	4.93175119	0.81485738
13	2.47E-10	6.53E-09	147.877429	2.2561763	0.75360391
14	1.60E-10	7.27E-09	134.854438	4.8943656	0.8488494
15	1.42E-10	9.17E-09	107.635386	4.97712989	0.811458
16	1.49E-10	8.33E-09	118.178651	4.95723578	0.8241883
17	1.32E-10	1.06E-08	93.4782017	4.99871448	0.80003757
18	1.32E-10	1.06E-08	93.4782017	4.99871448	0.80003757

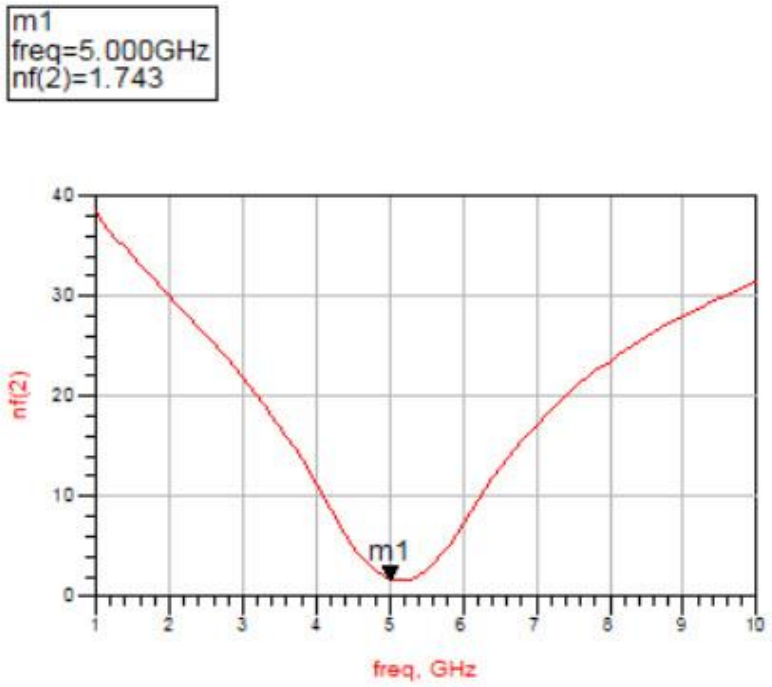


Figure (4-19): NF Based on Optimized (L_S and L_g) at 5 GHz DLNA

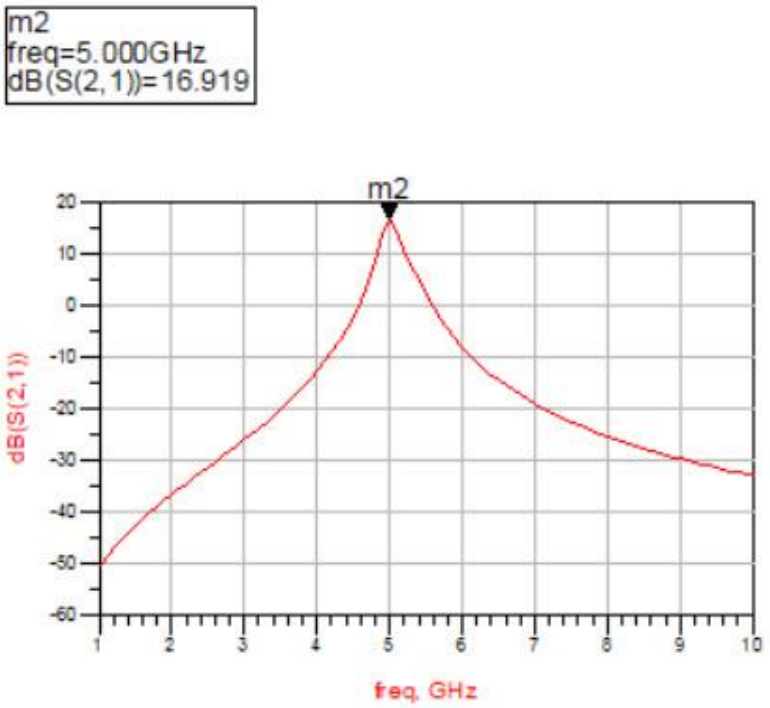


Figure (4-20): S_{21} Based on Optimized (L_S and L_g) at 5 GHz DLNA

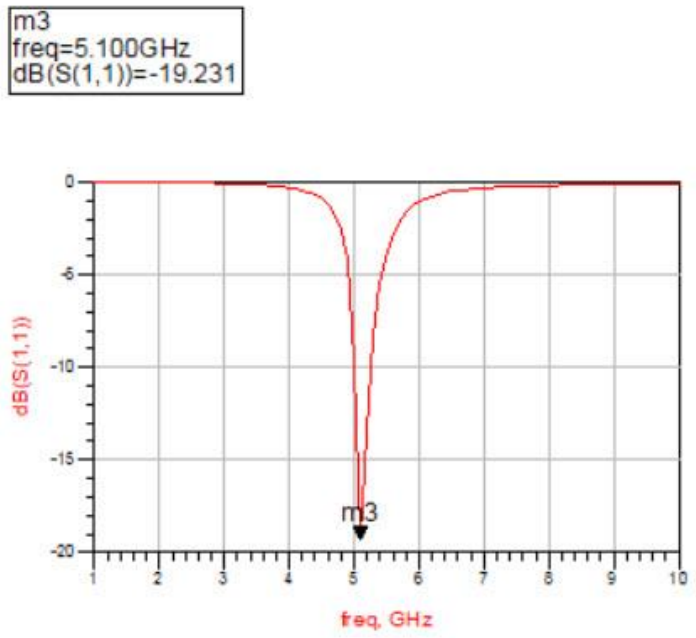


Figure (4-21): S_{11} Based on Optimized (L_S and L_g) at 5 GHz DLNA

4.8 Comparison Between Analytical and Optimized Results Using MOGA for 5 GHz DLNA

Table (4-9): Comparison Between Design Techniques for DLNA at 5 GHz

Design Parameters and Performance	**Mathematical**	**Optimization (NF ,Gain ,P)**	**Optimization (L_S ,L_g)**
Width W_1(µm)	161	89	143.153
$\boldsymbol{I_d}$ (mA)	5	1	4.736
C_{gs}(PF)	0.16	0.0899	0.144
L_S(nH)	0.17	0.287	0.16
L_g(nH)	6.33	10.97	6.8
NF(dB)	2.09	1.6	1.74
Power Consumption(mw)	18	3.6	17.04
Gain(dB)	12.76	18.648	16.919
S_{11}(dB)	-10.3	-13.5	-19.2

It can be seen from the above table that if the design procedure may operates and involves the improvement gain, noise figure, and power set of specification or can the algorithm will concentrates on fabrication requirements that determined by device dimension, L_S and L_g.

CHAPTER 5

Conclusions and Suggestions for Future Research

5.1 Conclusions:

This thesis presented an optimization technique for the design of Low Noise Amplifier (LNA) with an improved performance using the Multi-Objective Genetic Algorithms (MOGA) concept.

Two different LNA topologies have been designed and optimized to meet the specified requirement and improved performance. LNAs with two different operating frequencies at 2.4 GHz and 5 GHz are considered in design LNA and simulated. The single ended and differential low noise amplifier with inductive source degeneration were designed and optimized to obtain the optimum design parameter values. All the design topologies were simulated using Advanced Design System (ADS), based TSMC CMOS 180 nm process. MOGA optimization toolbox of MATLAB 2017a has been developed and implemented to improve the performance parameters of LNA. The improvement includes minimization noise figure and power consumption, maximization gain and reduce the area involved by the inductors $L_{S,}$ L_g.

The contribution of this research:

1. Optimization procedure is realized using MATLAB language and based Multi-Objective Genetic Algorithm (MOGA).
2. The first strategy of optimization is concentrated on minimizing NF, power consumption and maximizing gain and satisfying the required specification.

3. The second strategy considered minimization chip area by reducing the value of degeneration inductance L_S and gate inductance L_g.
4. Two different design topologies were used, the single ended and differential stage. Both structures were designed, optimized and simulated at two different frequencies at 2.4 GHz and 5 GHz to illustrate the behavior and the variation of performance when the frequency increased.
5. A comparison between the MOGA with existing mathematical techniques illustrates that MOGA results give a significant reduction in power consumption and noise figure and enhance the gain to maximum value.
6. A Weighted Sum Method (WSM) is realized after performance parameter normalization, and MATLAB code was implemented to select the appropriate gen –variables from a Pareto set of solutions.

5.2 Suggestions for Future Research

- To study and design reconfigurable LNA's at mm Wave frequencies by indirectly matching higher -Q-factor inductors using EM simulators.
- To carry out post-layout simulations, design and carry out our LNA design experimental measurements.
- To optimize the balance between performance measurements such as noise factor, gain and linearity. By increasing the current drainage, linearity performance can be further improved. However, the power consumption will be increased at the same time. The compensation can be adjusted to suit a specific application.

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الخلاصة

يمثل مكبر الإشارة منخفض الضوضاء (LNA) لبنة أساسية مهمة في معظم أنظمة الاتصالات اللاسلكية ويعد الكتلة الاولى في نظام مستقبل الترددات الراديوية حيث يستخدم لتكبير الإشارات المستلمة الضعيفة جدًا. وبسبب احتوائها على ضوضاء، يكون من المفترض أن يقمع ويوهن المكبر منخفض الضوضاء (LNA) إشارات الضوضاء المستلمة وكذلك الضوضاء الناتجة عن الجهاز الذي يحقق المكبر .يعتمد التصميم التقليدي لـ LNA وتحقيقه في الغالب على معادلات رياضية تغطي تشغيل هذا المكبر .لا توفر معادلات التصميم مساحة من الحرية للعمل على اختيار متغيرات التصميم، وتتطلب أحياناً اختياراً عشوائياً لمتغيرات التصميم، وذلك لتلبية معادلات التصميم التي تحدد أداء مكبر الإشارة منخفض الضوضاء (LNA). ويشتمل الأداء الامثل لمكبر الإشارة منخفض الضوضاء (LNA) على عدة عوامل ، منها عامل شكل الضوضاء (NF) ، والكسب (G)، واستهلاك الطاقة ، ومطابقة المدخلات والمخرجات، وإلاستقرارية ، والخطية .تقدم هذه الدراسة طريقة بديلة للتقنيات الرياضية التقليدية، والتي تعتمد على استخدام الخوارزمية الجينية (GA)في التحسين وتوخي الامثلية .

طُبقت الخوارزمية الجينية متعددة الاهداف (MOGA) لتحسين أداءLNA ، والذي يتضمن تقليل NFوتقليل استهلاك الطاقة، وتعظيم الكسب. بالإضافة إلى هذا الإجراء، تُطبق الخوارزمية الجينية متعددة الاهداف للتعامل مع متطلبات التصنيع من خلال تقليل قيم المكونات المطلوبة وأبعاد الجهاز. تم الحصول على تحسن كبير في عوامل الأداء مع تلبية متطلبات الأداء المحدد لمكبر الضوضاء المنخفض. تم تصميم وتحسين ومحاكاة اثنين من اشكال مكبر الإشارة منخفضة الضوضاء بترددي تشغيل 2.4 GHz و5 GHz. تم تحقيق مكبرات الإشارة منخفضة الضوضاء أحادية الطرف وهياكل المكبرات التفاضلية منخفضة الضوضاء. تم توضيح مزايا وقيود كل هيكل وتم إجراء مقارنة بين النتائج في جميع الحالات. يوفر تطبيق الخوارزمية الجينية متعددة الأهداف MOGA لكلا الشكلين انخفاضًا كبيرًا في NF واستهلاك الطاقة وتعظيم الكسب. تمت دراسة تأثير زيادة تردد التشغيل من 2.4 GHz إلى 5 GHz. ومعالجته لاسيما الزيادة في NF . تمت المحاكاة باستخدام نظام التصميم المتقدم (ADS) للتحقق من النتائج التي تم الحصول عليها بواسطة الخوارزمية الجينية متعددة الاهداف ومقارنتها مع متطلبات أداء LNA المحدده.

بسم الله الرحمن الرحيم

﴿ يُؤْتِي الْحِكْمَةَ مَن يَشَاءُ ۚ وَمَن يُؤْتَ الْحِكْمَةَ فَقَدْ أُوتِيَ
خَيْرًا كَثِيرًا ۗ وَمَا يَذَّكَّرُ إِلَّا أُولُو الْأَلْبَابِ ﴾

صدق الله العظيم

جـامعـة نينوى
كلية هندسة الالكترونيات
قسم الالكترونيك

التصميم الأمثل لمكبر الإشارة منخفض الضوضاء

رفل رائد محمود الشاكر

رسالة في هندسة الإلكترونيك

(الالكترونيك)

بإشراف

الاستاذ المساعد

الدكتور أحمد ذنون يونس

1442 هـ 2021 م

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رسالة تقدمت بها

رفل رائد محمود الشاكر

إلى

مجلس كلية هندسة الالكترونيات –جامعة نينوى

وهي جزء من متطلبات نيل شهادة الماجستير

علوم في هندسة الالكترونيك

(الالكترونيك)

بإشراف

الأستاذ المساعد

الدكتور أحمد ذنون يونس

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