Ninevah University

College of Electronics

Electronic Department

Comparative Control Study of Multilevel Inverter Using Less Switching Devices

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A Thesis in

Electronic Engineering

Supervised by

Dr. Harith Ahmad Mohammed Al-Badrani

2022 A.D. **1444 A.H.**

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As a Partial Fulfillment of the Requirements

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بِسْمِ اللَّهِ الرَّحْمَٰنِ الرَّحِيمِ

﴿يَرْفَعِ اللَّهُ الَّذِينَ آمَنُوا مِنْكُمْ وَالَّذِينَ أُوتُوا الْعِلْمَ دَرَجَاتٍ وَاللَّهُ بِمَا تَعْمَلُونَ خَبِيرٌ﴾

صَدَقَ اللهُ العَظيم

المجادلة: 11

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Layth

Dedication

This work is intended for:

For the sake of Allah, my Creator and Master and to my great teacher and messenger Muhammad (May God bless him and grant him peace)

To My father (may God have mercy on him) and my mother

To my brothers Azzam, Mohanad, Mahmood and my sister Zina

Layth

ABSTRACT

DC to AC inverter has become an interesting topic as renewable energy sources which are increasingly used and invested in as a competitive energy source. In this research, effective methods for converting DC voltage into a sinusoidal signal AC are presented. The main objective is to develop a highly efficient inverter which is produced a sinusoidal AC signal that is as pure as possible. For this purpose, a 27-level cascaded inverter is designed and simulated using MATLAB Simulink. The inverter design includes three H-Bridges connected in series, with each bridge connected to a separate DC voltage source. As a result, this design requires three asynchronous DC voltage sources with a ratio of 1:3:9 to obtain a 27-level (-13 to 13) inverter.

In addition, various modulation methods applicable to the cascaded inverter are investigated, such as a selective harmonic, nearest level, and SPWM. The simulation results of these three modulation methods show that the nearest level method has a lower THD value (i.e., 2.95 %) when no filter is used, On the other hand, SPWM achieves the lowest THD value (i.e., 0.56 %) when the filter is used. As a result, these two methods are practically demonstrated for hardware design.

The hardware design consists of the following steps. First, a programmable micro controller used as micro controller unit. A complex programmable logic device is used as a lookup table to reduce the micro controller unit tasks and thus minimize the programming code. Second, drivers used for optical isolation to isolate the micro controller unit, which operates at low voltages, whereas the HBs, which require high voltages. Since the driver requires high voltage, a separate power supply

is developed to power the isolator driver. The CHBs stage includes three HBs connected to switch the polarity of the corresponding DC source and then build up an AC waveform. Each HB consists of four semiconductor switches. Since the Silicon Carbide SiC-MOSFET has high input impedance, high switching frequency and high-power handling capability, it is used as a switch. Also, a filter is used to smooth the generated signal for enhancing the THD. The signals generated in the hardware have the same THD as the simulation results of the counterpart. The inverter was tested with a range of loads and the efficiency was changed. However, it maintained a value of more than 90%.

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LIST OF ABBREVIATIONS

ACHBMLI	Asymmetrical CHBMLI
ADC	Analog to Digital Converter
CHB	Cascaded H-bridge
CHBMLI	Cascaded H-Bridge Multi-Level Inverter
CPLD	Complex Programmable Logic Device
DSP	Digital Signal Processing
FC	Flying Capacitor
GA	Generic Algorithm
IGCT	Integrated Gate-Commutated Thyristors
GPIO	General-Purpose Input/Output
GTO	Gate-Turn-Off
IGBT	Insulated-Gate Bipolar Transistors
KSPS	Kilo Samples Per Second
L	Number of Levels
MCU	Micro Controller Unit
MFCI	Multilevel Flying Capacitor Inverter
NPC	Neutral-Point-Clamped
NR	Newton Raphson
PUC	Packed U-Cell
PWM	Pulse Width Modulation
SCSS	Series Connected Switched Sources
SHE	Selective Harmonic Elimination
SiC	Silicon Carbide
SPWM	Sinusoidal Pulse Width Modulation
SSPS	Switched Series/Parallel Sources
THD	Total Harmonic Distortion
USP	Universal Serial Port
VHDL	VHSIC Hardware Description Language
VHSIC	Very High-Speed Integrated Circuit

LIST OF SYMBOLS

V_{ci}	Voltage of the i-th capacitor
V_{dcN}	The N-th DC voltage source
V_{max}	Maximum voltage
V_{inv}	Inverter output voltage
V_p	The peak voltage
$V_{R.M.S}$	The root mean square of the voltage
f_{sw}	Switching frequency
Q_{rated}	The total reactive power absorbed by the capacitor
f_{Load}	The generated frequency
V_{Load}	The voltage of the generated waveform
N_{PRI}	Turns number of the primary transformer coil
V_{IN}	The input voltage
B_{MAX}	Maximum flux density

CHAPTER ONE

Introduction and Literature Review

1.1 Introduction

DC to AC power inverters have attracted the interest of researchers and industrial manufacturers in the last decades [1]. When talking about inverters, one must think about renewable energies, because they play an important role in renewable energy generation.

However, the importance of inverters for industrial application is shown when they are used to control the pumps of inlet flow in chemical factories, fans in the cement industry, and electric trains by adjusting the frequency and magnitude resulting in motor speed control [2][3]. This type of control is better than the traditional mechanical gear transformation in terms of efficiency and accuracy [4]-[7]. The demand for such inverters prompted electronics manufacturers to develop high-power and medium-voltage drivers such as 4500-V Gate-Turn-Off (GTO) thyristors, high-power Insulated-Gate Bipolar Transistors (IGBTs) and Integrated Gate-Commutated Thyristors (IGCTs) [3][8]. Until the late 1990s, the main consumers of medium power drivers were industry and transportation [9].

The exponential increase in solar energy at the beginning of this century results in high power and high voltage inverters required to fully utilize this enormous energy. As a result, the two and three level inverters with medium voltage drivers used in the industry are not sufficient. On

the other hand, high voltage semiconductor electronics are very expensive [1].

Multilevel inverters are a solution for handling high power using medium voltage drivers. Wide variety of applications start to adopt inverters, and each of them has its own needs in addition to the development in the semiconductor industry.

1.2 Literature Review

A DC to AC inverter went through several stages of development. Two main reasons are behind this modification process of inverter performance. First, the demand for inverters with higher power and better performance to meet application requirements. Second, semiconductor manufacturers are producing higher power devices that are capable of handling higher power, shorter switching time, and lower power consumption. For instance, Silicon Carbide (SiC) technology is receiving increased attention as new technique of semiconductor manufacturing because of its exceptional material properties. For example, it has high electric breakdown field, high thermal conductivity and high saturated electron drift velocity. These properties are optimal for power device manufacturing [10].

There are several topologies that have been proposed and used in some applications. However, in the following subsections, some of the known inverters are presented and explained in more detail.

The full bridge (H-bridge) inverter is a two-level and the simplest form of inverter that has a DC voltage source as input and four transistors as switches. Each two diagonal switches are controlled together. It is a very simple inverter that only switches the polarity of the DC source around the load frequently.

This topology is simple and uses only a few transistors switched at low frequency, the same frequency as the desired generated signal. However, it produces a square wave that has a very high Total Harmonic Distortion (THD). THD means power consumption and heating up the load, especially inductive loads such as motors. As a result, it was not suitable for higher power or inductive loads. This limitation led researchers to develop a new design suitable for industrial use [1]. However, the H-bridge is used in various topologies and could be considered as a cornerstone for other inverters development.

Sinusoidal pulse width modulation method is implemented by increasing the switching of the two-level inverter with higher frequency with different duty cycles. The width of the pulse is proportional to the corresponding amplitude of the desired output signal in the time axis, i.e., sine wave [11]. The generated output signal is then fed to a lowpass filter to smooth the signal. This reduces the THD and increases power efficiency. However, a higher switching frequency also means higher switching losses.

The beginning of the use of inverters was for industrial applications, such as motors requiring medium power. For such applications, two levels inverters with medium power semiconductors were satisfactory. However, higher-power applications began to appear, such as renewable energy sources. This led to the need for higher power semiconductors to realise high-power inverters. Researchers focused on increasing the power of the semiconductor to then increase the power of the inverters.

In the 1970s [12], there were two main approaches for inverter implementation: current source inverters and voltage source inverters. As

a result, some manufacturers made efforts to improve the current capacity of semiconductors to achieve the current source inverter. Other researchers worked to improve the voltage of semiconductors to develop voltage source inverters [13].

In 1981, AKIRA NABAE et la [14] demonstrated for the first time the Neutral-Point-Clamped PWM inverter (NPC), which is also called diode-clamped inverter. The new topology obtains three levels by adding zero-voltage. By adding capacitors in series to the topology, the source voltage is divided into equal voltages, providing multiple DC levels of voltage. This addition of capacitors improves the inverter in to two ways. First, each semiconductor switch now provides only half of the total power. In other words, the total power of the inverter can be doubled by using semiconductor switches with the same characteristics. Second, the levels are increased, which help to suppress the THD.

Theoretically, multiple layers can be added to this topology. However, this reduces the overall reliability of the system, increases the number of diodes, and makes it difficult to maintain the neutral point at zero voltage. The idea of adding multilevel for higher power inverters has been developed [15][16].

The advantages of this topology are: Reduction of THD, requires a relatively simple control circuit to switch the transistors, and requires only one DC source. However, this topology also has some disadvantages: it requires a high number of semiconductor components, low modularity, and it is difficult to maintain the voltage balance of the two diodes.

Flying Capacitor (FC) or capacitor clamping, as alternatively known. It was proposed in 1992 by Meynard et al [17]. FC multilevel inverter is

similar in structure to NPC, except that the diodes are replaced by capacitors.

FC inverter has the following advantages: This type allows both active and reactive power flow control. Also, THD decreases as the number of levels increases. It also has high modularity and requires only one DC source.

On the other hand, there are some disadvantages of this type of inverter. First, the capacitors are bulky and more expensive compared to the diodes. Also, the efficiency of transferring active power is poor, and a complex control circuit is required to drive the transistors [18]. FC is usually used with AC motors and active filters.

The main disadvantage of the above inverters, which use a DC voltage source, is the limitation of levels. As a result, they are not suitable for higher voltages because the use of capacitors as voltage dividers to obtain multiple DC sources reduces the reliability of the system with multiple levels. As a result, dedicated DC sources could solve this problem as in Cascaded H-bridge (CHB) inverters.

The CHB multilevel inverter was introduced by [17]. It is implemented by connecting the outputs of several classical H-Bridge inverters in series. Each single H-Bridge inverter has its own DC supply. As a result, CHB requires *m* separated DC sources, where *m* is the level order. This topology is theoretically capable of supplying an infinite number of levels. As a result, power and voltage are scalable over a wide range.

The main disadvantage of the CHB is the need for multiple DC sources. However, this drawback could be reduced if the applications are

those that have multiple DC sources, such as PV panel array or electric vehicle that have a number of batteries and can be grouped as needed.

CHB has many properties that make it more practical for a wide range of applications. First, DC voltage sources can be set to specific values and then manipulated, resulting in a wide range of output signals that can be achieved with a minimal number of levels. Second, low switching frequency, resulting in lower losses and longer transistor lifetime.

In addition, the CHB has high modularity and fewer semiconductor components. Furthermore, it is fault tolerant, and if any H-bridge is damaged, it can be easily replaced. On the other hand, this type has the following disadvantages. First, it needs several separated DC voltage sources, which makes it inappropriate for some applications. Second, it requires complex switching control.

Since the voltage sources are fully isolated, different modulation methods can be implemented with cascaded H-bridge, resulting in different topologies, of which the following are some.

Switched Series/Parallel Sources (SSPS) Multilevel Inverter topology is proposed by Hinago et, al [19]. It consists of two main levels. The first is the DC level generator. The controller switches the transistors to set the output of this stage to a specific DC voltage. The output of the first stage then powers the second stage, which generates the AC voltage by switching the polarity.

This topology has many advantages. It works with asymmetric configuration. Moreover, Switched Series/Parallel Sources (SSPS) generate wide range of levels with a smaller number of switches than conventional multilevel inverters. In addition, multiple sources in

different configurations can be flexibly connected to meet application requirements. SSPS is used in a wide range of applications. For example, for electric vehicles [20].

The T-Inverter is a single-phase five-level inverter proposed by Gerardo Ceglia et al [21]. It requires two identical voltage sources. The T-Inverter reduces the number of semiconductors devises as well as the switching frequency. Furthermore, it has a simpler configuration than its counterparts with the same levels. As a result, its power consumption is about 40% lower [22].

It has an H-bridge with bidirectional auxiliary switch to generate the DC levels out if the DC suppliers. However, it does not support asymmetric source configuration [21].

The Nilkar inverter topology is proposed by Nilkar et la. [23]. It uses two identical DC voltage sources and four semiconductor switches to produce stepped DC levels. The H-bridge stage switches the polarity of the stepped DC levels and generates an AC voltage signal.

T-type topology produces a lower THD waveform. In addition, capacitors can be used as voltage source. As a result, it is prepared for various medium and high voltage applications in industry as well as photovoltaic applications.

This topology was proposed by Khosroshahi in [24] as a novel inverter. It consists of two main parts, a step or level generator consisting of two DC voltage sources as well as unidirectional along with bidirectional switches. The second part is similar to the previous ones which is H-bridge that changes the polarity of the DC level around the load.

Reversing Voltage (RV) topology was introduced by Najafi et al [25] [26], similar to the previous ones, RV also consists of two stages. The first stage (level-generation) has three identical DC sources and six semiconductor switches. The output of this stage is always a positive DC voltage.

However, the rule of the H-bridge in the second stage is to switch the polarity around the load so that the AC waveform is generated. This topology is scalable, so it can be extended to any number of levels by repeating the middle voltage source and the appropriate transistors. It can also be used for three-phase systems.

Series Connected Switched Sources (SCSS) topology, semiconductor switches are used to connect DC sources in series. In this way, a multilevel is created. On the other hand, the H-bridge synthesizes the AC signal [27] [28]. The DC sources are asymmetric, each source has a calculated value to reduce the number of switches. However, the semiconductors used are not identical, as some require high power and others do not. This could be the biggest drawback. Also, since the configuration of the DC side of the inverter is constantly changing, load sharing cannot be achieved.

Packed U-Cell (PUC) Topology was introduced by Youssef et al. in [29]-[33] as a new class topology consisting of ten power switches and four DC sources. The switches and the dc sources are interconnected in the form of a U-cell. Each U-cell has one source and two transistors.

This topology has the distinct advantage of switching switches that deliver higher power at a lower frequency and vice-versa. This reduces the load on the switches, extends their service lifetime and reduces switching losses.

Al-Badrani et la. In [34]-[36] designed two-level SiC-based inverter that generates nearly sinusoidal waveform to feed a three-phase induction motor controller. It controls the machine by measuring the voltage at the load terminals to then estimates the flux for each phase.

1.3 Objective of the Thesis

The main objective of this research is to develop and implement an inverter from DC to AC, which could contribute positively to renewable energy generation. This main objective could be achieved through the following steps:

1. Studying and investigating the existing topologies used in terms of power losses, THD and other parameters.
2. Discussing the performance of the inverters and their advantages and disadvantages, as well as the applicable applications for each one individually.
3. Designing and analyse multilevel cascaded H-bridge inverter and finding out the optimum level order in terms of minimum switches devices, power efficiency, harmonics elimination and circuit complexity.
4. Studying and investigating the optimum voltage and power of each source feeding the corresponding H-bridge inverters.
5. Designing and investigate the driver that drives the cascaded inverters using Digital Signal Processing (DSP) to optimally control and switch the transistors.
6. Phasing adjustable to be synchronized with the gride and thus work simultaneously with the gride.

1.4 Thesis Outline

This thesis is divided into five chapters,

Chapter One includes introduction and literature review of previous works is introduced in chapter one.

Chapter Two introduces the theoretical background of the system that includes the working principle of well-known inverter topologies. In addition, used modulation methods are introduced.

Chapter Three demonstrates the simulation of the design and investigates and compare the simulation results.

Chapter Four presents the hardware design of the inverter including the controller, driver and the power supply circuits. In addition, the experimental and real time results of the inverter are demonstrated and investigated.

Chapter Five concludes the research as well as gives some suggestions for future work that could extend this work.

CHAPTER TWO

THEORETICAL BACKGROUND

2.1 Introduction

In this chapter, the theoretical background of the inversion process is presented. There are a variety of inverter topologies. Each of them has a different configuration, such as the electronic circuit diagram of the inverter as well as the type of DC power supply feeding the inverter and the method of modulation. Changing any of these parts will result in a change in the behaviour of the inverter. In the next subsections, the inverter topologies and their operating principles are presented as well as the semiconductors technique that used as switches. In addition, modulation methods for controlling the switching operations are presented and studied.

2.2 Multilevel Inverter Topologies

Inverting DC to AC is not new and is used in several basic applications such as radio tuning, which is called an oscillator. However, the technical term inverter is used for inverting the voltage from DC to AC to power a device. There are a variety of loads that require an AC voltage power. As a result, a wide range of inverters has been developed, e.g., a simple load with low voltage can be operated with a two levels inverter. On the other hand, higher and more complicated applications require a high-power inverter that is instantly controllable. This led to the beginning of improving the efficiency of controllable power supplies in a cost-effective way to meet the increasing demand for power. This goal could be achieved either by designing a power semiconductor device with capacity up to 6500V, which is very expensive [37]. Or, one could

design a multilevel inverter using existing medium voltage semiconductors.

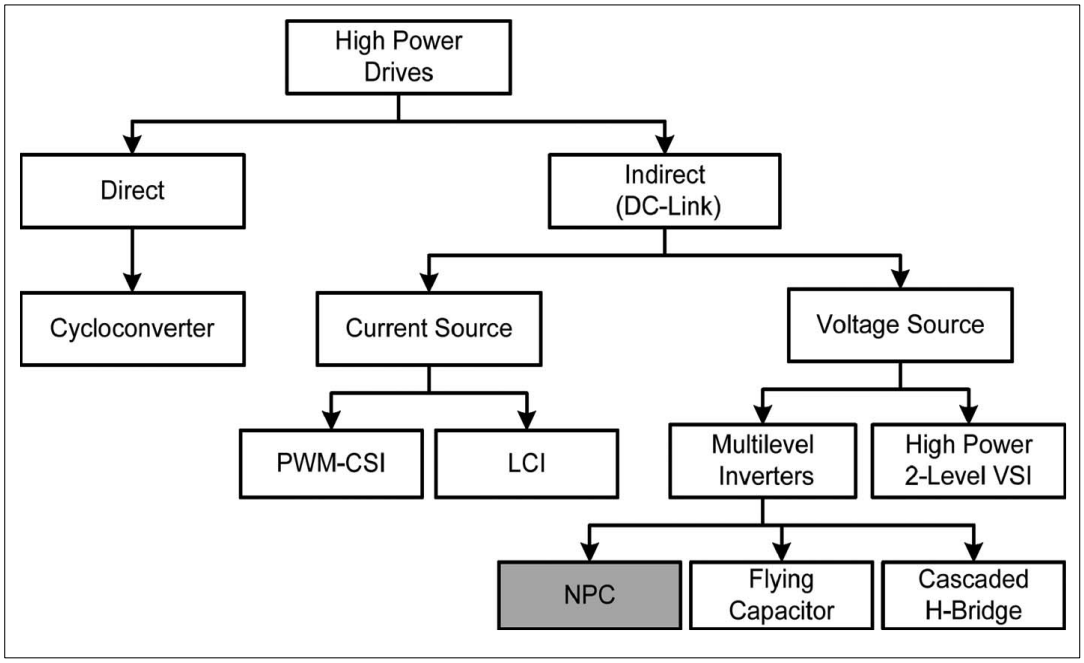

Figure 2.1 Families of High-Power Converters [38]

For the above reasons, multilevel inverters have become an important research topic to improve the generated AC signal and meet the application requirements. As a result, several topologies have been proposed as shown in Figure (2.1). Each of these topologies is optimal for certain type of loads and applications.

However, three of these topologies are examined in the following subsections: Neutral Point Clamped (NPC) multilevel topology, Multilevel Flying Capacitor Inverter (MFCI) topology, and Cascaded H-Bridge Multi-Level Inverter (CHBMLI) topology. These topologies were selected because they are widely used in the industry [39]. However, CHBMLI is more suitable than the others for the following reasons: It has a higher number of levels and lower voltage stress. In addition, it is flexible in terms of expanding the number of levels and maintenance

[40]. For these reasons, CHBMLI topology is used in the experiments and therefore it is intensively studied.

Figure (2.2) shows and compares the output of different level inverters. It can be clearly seen that a higher level has better performance and less distortion.

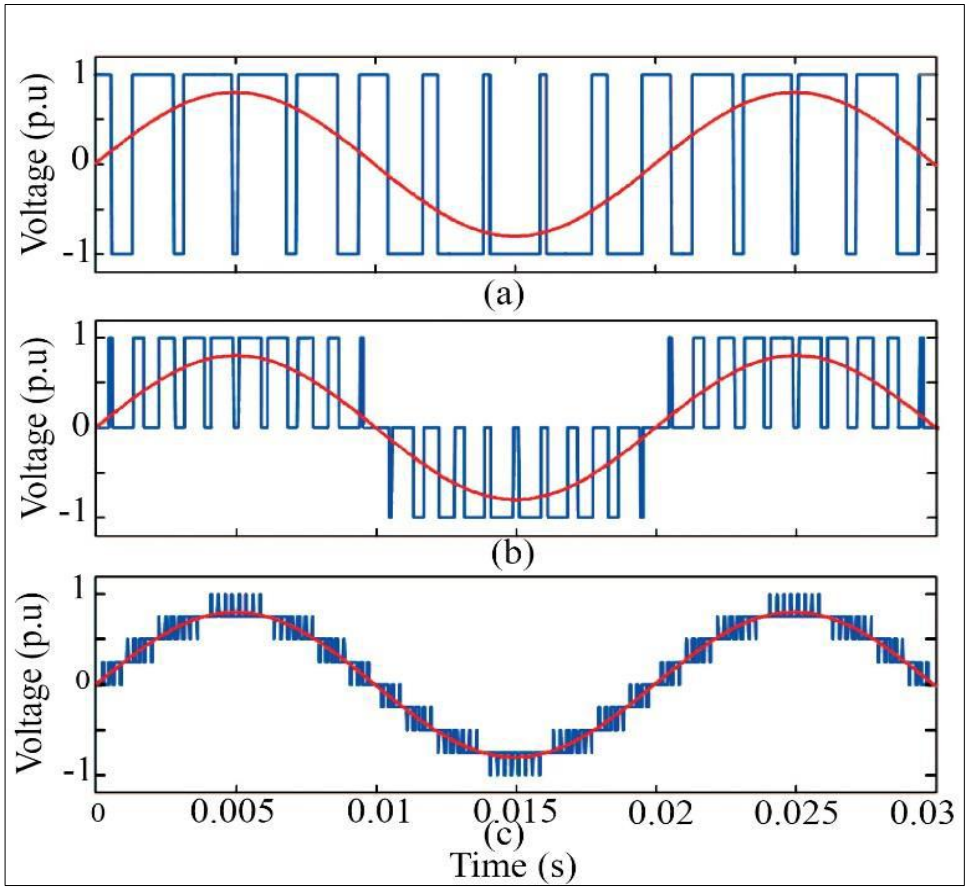

Figure 2.2The Output Phase Voltage for (a): Two-level Inverter, (b): Three-level Inverter, (c) Nine-level Inverter [12]

2.2.1 Neutral Point Clamped (NPC) Multilevel Topology

This topology is a three-level inverter derived from a two-level inverter. This change is made by adding two switches for each phase. In addition, two series-connected capacitors are added in parallel with the DC voltage source and diodes are used to limit the DC bus voltages as shown in Figure (2.3).

The two capacitors C1 and C2 act as voltage dividers; the point where the two capacitors are connected is the neutral point (P). The neutral point is considered as the third level of the DC source. In addition, the clamping diode suppresses the voltage load across the switches and reduces it to half. NPC is very popular because of its wide range of applications, including medium voltage high power controllable speed motors, interfacing the DC and AC power transmission lines.

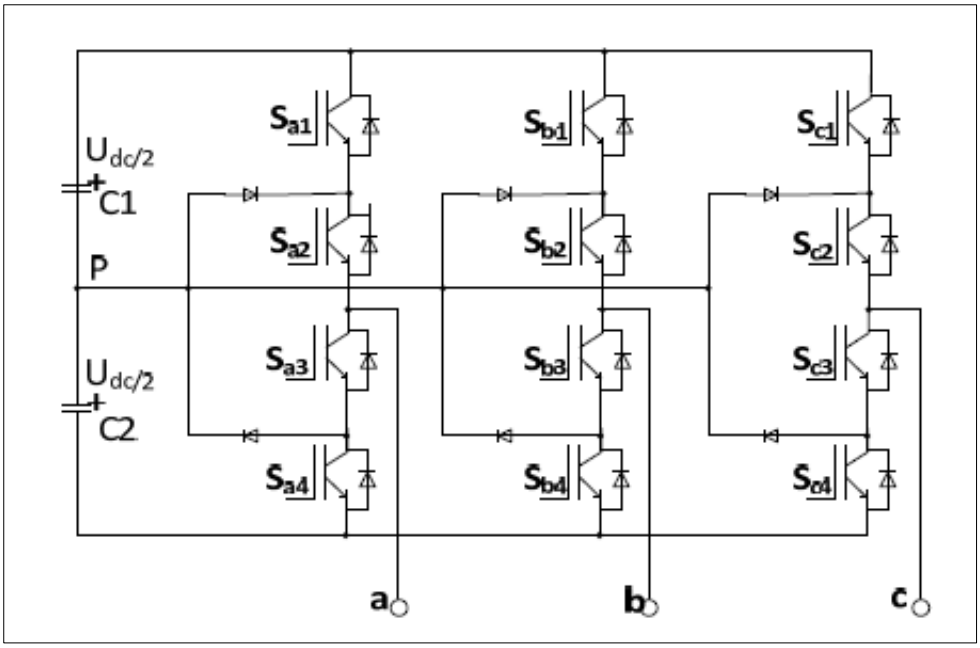

Figure 2.3 NPC Three Level Inverter Topology [41]

Theoretically, NPC can be extended to more than three levels by adding more capacitors and switches. For each phase, an N-number of levels NPC, the number of capacitors (C), which does not affect by the number of phases, diodes (D), and switches (S) are given by the following equations (2.1), (2.2), and (2.3), respectively.

$$C = N - 1 \quad \ldots\ldots\ldots\ldots \quad (2.1)$$

$$D = 2[N - 2] \quad \ldots\ldots\ldots \quad (2.2)$$

$$S = 2[N - 1] \quad \ldots\ldots\ldots \quad (2.3)$$

Even though increasing the levels does not require a massive increase in the number of semiconductor devices such as diodes, more than three levels NPC are practically not used because of the difficulty of maintaining a uniform voltage across the capacitors. This is the major limitation of using higher order NPC inverters.

However, several studies focus on the voltage balance, which should look like the following equation (2.4).

$$V_{ci} = \frac{V_{DC}}{(N - 1)} \quad \ldots\ldots\ldots \quad (2.4)$$

Where V_{ci} represents the voltage across each capacitor

Because of the neutral points (inner DC-link points) are connected to the inverter, circulation of current through these points, which maintain the voltage balance across the capacitors. This balance depends on the current flow through the neutral points. The current in turn is subjected to the modulation method. As a result, the modulation method used to control the switching is an important factor in maintaining the equilibrium processes.

However, there are other ways to improve this balance, some are hardware implemented such as back-to-back operations or additional circuits while others are software methods, for instance, open loop techniques method that analyse the unbalance problem considering the specific modulation strategy used in each case, and then propose certain arrangements over the modulation strategy to keep the balance. However, shortage of feedback resulting in close loop techniques has higher

performance. Figure (2.4) shows the headlines of some capacitor balance methods. In addition to the voltage balance, which is a challenge at higher levels, the complexity of the modulation also increases drastically

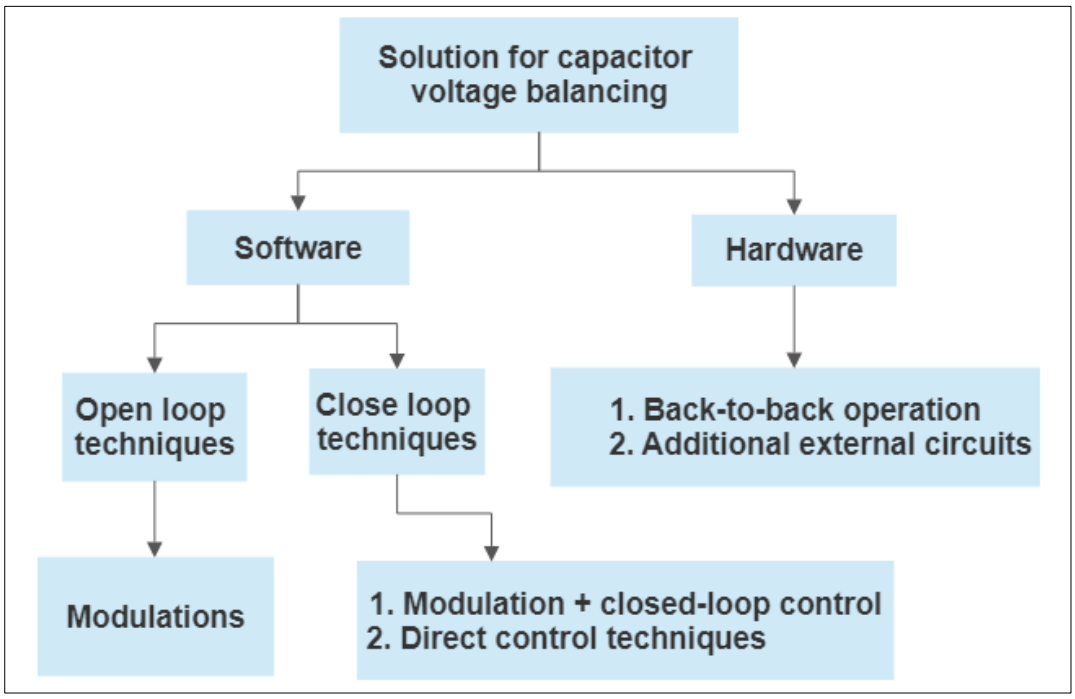

Figure 2.4 Classification of the Solutions for DC-link Capacitor Voltage Balancing in NPC Topology [42]

2.2.2 Multilevel Flying Capacitor Inverter (MFCI) Topology

The MFCI topology, like the NPC, requires only one DC source. However, MFCI uses capacitors rather than diodes. The term (flying or floating) is included in the name of this topology because these capacitors are not directly connected to the electrodes of the DC power [43] as shown in Figure (2.5).

This topology is composed of cells, each cell consisting of two switches and their flying capacitor. The cells are like shells, for example cell number one acts like a skin for the other cells inside.

Each cell is capable of generating a level, therefore multiple levels can be generated just from one DC source. However, increasing the levels leads to an increase in the size of the semiconductor devices. For instance, for L level inverter, the number of switches (S) and capacitors (C) can be given in equations (2.5) and (2.6), respectively, which depend on the number of cells (K), where K = L-1.

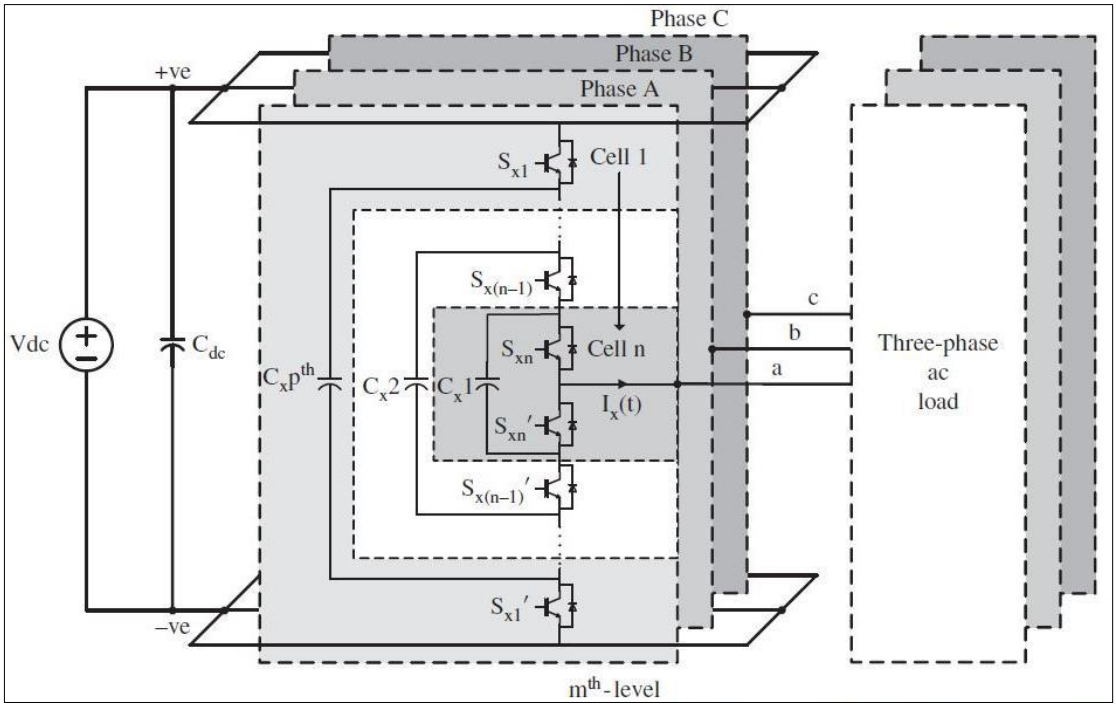

Figure 2.5 Three-Phase n-cell Multilevel Flying Capacitor Inverter [44].

$$S = K * 2 \quad \ldots\ldots\ldots\ldots \quad (2.5)$$

$$C = K - 1 \quad \ldots\ldots\ldots\ldots \quad (2.6)$$

In higher level inverters, the number of capacitors increases. Such an increase results in a high current flow that could puncture and damage the semiconductors during start up, so they must be charged before the inverter is started. In addition, these capacitors are passive elements and store electrical energy that distorts the output voltage. Furthermore,

MFCI has the same disadvantage as the NPC in terms of capacitor voltage balance. Moreover, each capacitor is charged by the load current, which changes its voltage. This voltage changes of the capacitor must remain within the allowable range.

These drawbacks limit the use of MFCI to low levels, high speed drives and requires low current ripple applications. As a result, the capacitance of the capacitors used is inversely proportional to the switching frequency [45].

2.2.3 Cascaded H-Bridge Multi-Level Inverter (CHBMLI) Topology

H-Bridge (HB) is a simple three-level inverter that uses four switches. It is used by most inverters as an alternating part to switch the polarity of the DC source around the load. However, series-connected HBs results in a new multilevel inverter, as shown in Figure (2.6) for single phase inverter. However, three phase inverter can be achieved by connecting three CHBMLI in (Y) shape.

This topology requires a separate DC voltage source for each HB cell, and this DC supply cannot be shared with any other cell, whether in the same phase or in other phases. The total output signal is the sum of the outputs of the HB cells. As a result, increasing the number of HB cells means higher level inverter and therefore a better output signal and lower THD. As a result, the output filter is reduced. Each HB cell in CHBMLI generates ($+V_{DC}$, 0, $-V_{DC}$), where V_{DC} refers to the value of the DC voltage source of the corresponding HB cell. The output value is the sum of the outputs of the HBs.

However, there are two types of CHBMLI [46], symmetrical and asymmetrical. In the symmetrical type, all DC power sources are identical for all HB. In the asymmetrical type, DC voltage sources are

used with different voltages in the ratio of 1:2 (binary) or 1:3 (trinary). In the following, description of each type:

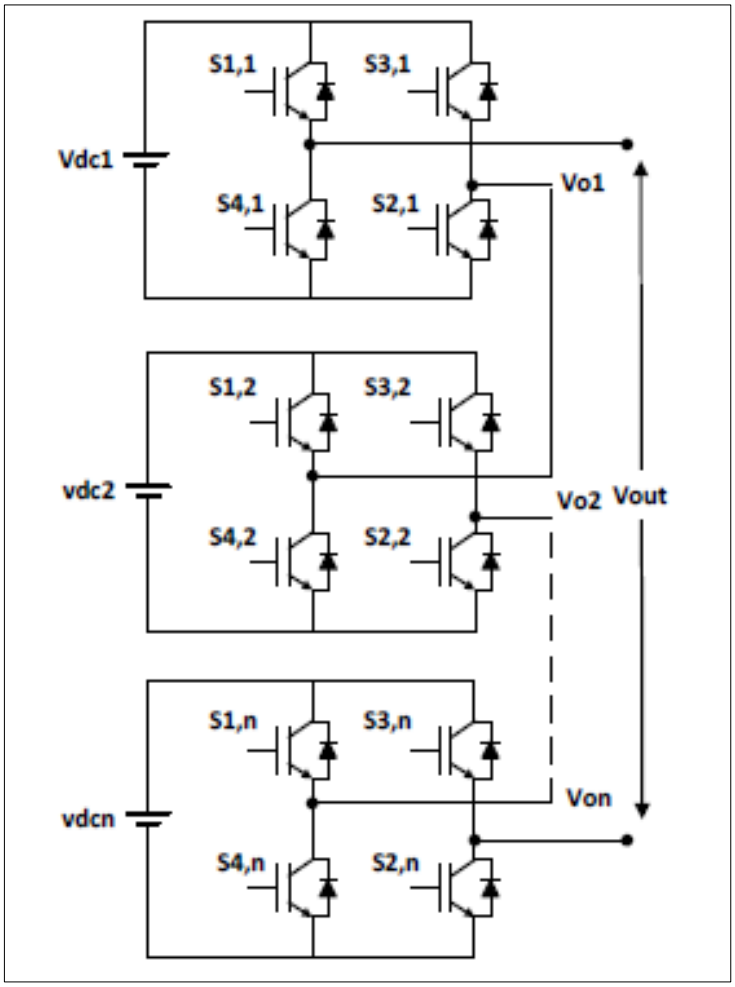

Figure 2.6 Cascaded H-bridge Multilevel Inverter (CHBMLI) [47]

A. Symmetrical CHBMLI

The symmetrical configuration uses an identical DC voltage source for each cell, i.e., ($V_{dc1} = V_{dc2} = \ldots = V_{dcN}$), where N is the number of HB cells. Since each individual cell is capable of producing ($+V_{DC}$, 0 or $-V_{DC}$) and the total output is the accumulation of the outputs of these cells, the number of levels (L) can be calculated using equation (2.7) [48].

$$L = 2N + 1 \quad \ldots\ldots\ldots\ldots \quad (2.7)$$

Since each HB cell has four switches, the total number of switches (S) used in CHBMLI is four times the number of cells in equation (2.8) and the maximum achievable output voltage in equation (2.9)

$$S = 4 * N \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (2.8)$$

$$V_{max} = N * V_{dc} \quad \ldots\ldots\ldots\ldots \quad (2.9)$$

According to the above explanations, two symmetrical HB are required for the generation of five levels ($+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$,).

B. Asymmetrical CHBMLI

The Asymmetrical CHBMLI (ACHBMLI), on the other hand, requires unequal DC voltage sources. As a result, this type is able to generate more levels with fewer switches compared to the symmetrical type [49]. However, they are not selected randomly, but in a ratio of either 1:2 (binary), for instance, (V_{dc}, $2V_{dc}$, $4V_{dc}$, …, 2^{N-1} V_{dc}) or 1:3 (trinary), e.g.,, (V_{dc}, $3V_{dc}$, $9V_{dc}$, …, 3^{N-1} V_{dc}).

Trinary ACHBMLI outperforms its binary counterpart in terms of the number of levels generated. For example, with two HB cells and two (V and 2V) power supplies, the binary ACHBMLI can generate seven levels (+3V to -3V), as shown in table (2.1).

Table 2.1 Output Levels Generated from Two (Binary Ratio) Voltage Sources

Source_1 (1V)	+ V	0	+ V	0	-V	0	-V
Source_2 (2V)	+2V	+2V	0	0	0	-2V	-2V
Total output (V_{out})	+3V	+2V	+V	0	-V	-2V	-3V

On the other hand, trinary ACHBMLI with the same number of switches and HB cells can produce nine levels (+4V to -4V) with these voltage source values (V and 3V) as illustrated in Table (2.2).

Table 2.2 Output Levels Generated from Two (Trinary Ratio) Voltage Sources

Source_1 (1V)	+V	0	- V_{dc}	+V	0	-V	+V	0	-V
Source_2 (3V)	+3V	+3V	+3V	0	0	0	-3V	-3V	-3V
Total output (V_{out})	+4V	+3V	+2V	+V	0	-V	-2V	-3V	-4V

These two examples show that the trinary ACHBMLI provides more levels than other types [50]. As a result, and by using an appropriate modulation method, this could be a promising topology for DC to AC inverters for applications that have multiple DC sources, such as a photovoltaic panel array.

Crucially, however, the load is allocated proportionally to the DC power supply. in addition, switches in the HB cell, which are supplied with a higher voltage, provide higher power than their counterparts in other cells. To solve this problem, switches with higher power capacitance are used. However, this solution can lead to another problem, namely, non-identical switches have different timing characteristics, which is a serious problem at high frequencies [43].

Finally, a comparison of the symmetric, binary asymmetric, and trinary asymmetric is presented in Table (2.3) in the following page.

Table 2.3 Comparison of Multilevel Inverter [51]

	Symmetrical Inverter	Asymmetrical Inverter	
		Binary	Trinary
Number of levels (L)	2N + 1	$2^{(N+1)} - 1$	3^N
Number of DC sources	N	N	N
Number of switches	4N	4N	4N
V_{MAX} (Maximum output voltage)	$N * V_{dc}$	$(2^N - 1) * V_{dc}$	$(3^N - 1) * V_{dc} / 2$

Where N is the number of HB cells

2.3 Semiconductors Switching Devices

The development in semiconductors industry has a significant impact on the growth of power electronics and high-power inverter subsequently. Conventionally, to use a semiconductor switch, a trade of between the power handling and the switching frequency need to be made. For instance, for low power, Si-MOSFET is feasible to run at high frequencies and hence small filter components are needed. on the other hand, Si-IGBT capable of handling high power that but with low frequencies and subsequently, a bulk filter is required [34]. The following points summarize the advantages of the SiC switches [52]-[54]:

- SiC switches have higher thermal conductivity by about three times than its counterparts that made of Si. As a result, the heat resulting from the losses is suppressed.

- SiC devices are capable of operating at high temperature up to 400°C. While their counterparts that made of standard silicon cannot operate when its heat reaches 150°C.
- In terms of current density, SiC has more than double current density than traditional silicon devices. Thus, higher power handling [36].
- They have higher switching, subsequently, operating at higher frequency up to 100 kHz [34].

The above-mentioned features promoted SiC technology to be widely used in different range of power devices and has improved the utility of semiconductors and expanded their applications [36]. Figure (2.7) demonstrates and compares the losses at Si=IGBT and SiC-MOSFET. In terms of efficiency, SiC-MOSFET has higher efficiency in a wide frequency range, as shown in Figure (2.8).

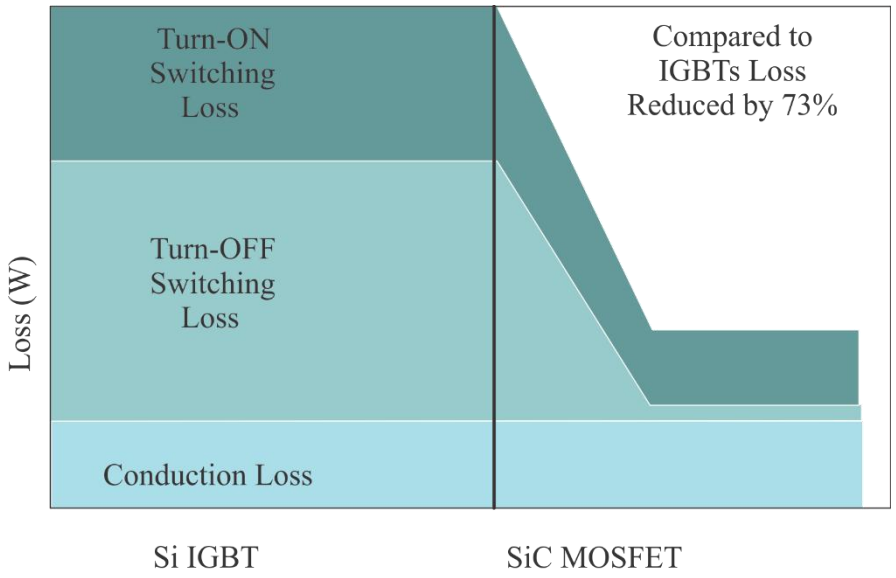

Figure 2.7 Loss Comparison of SiC-MOSFET and Si-IGBT

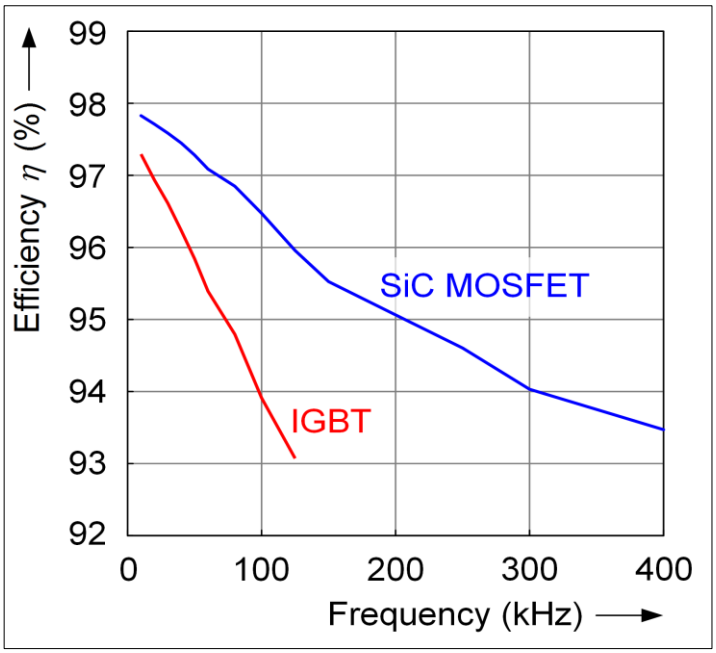

Figure 2.8 Measured Efficiency Over Switching Frequency at Pout = 10kW [36]

2.4 Modulation Methods for Multilevel Inverter

Designing the optimal inverter topology to achieve the best performance in terms of THD and producing a smooth sinusoidal waveform is only half the battle. As a result, the inverter's switches must be controlled and switched at an optimal time to achieve the inverter's perfect performance, which is called the modulation process.

There are several methods of controlling multilevel inverters that have been proposed to fully utilize the inverter circuit and then generate a signal with the required characteristics for a particular application and the DC power source availability [55]. Some applications, such as medical instruments, require a pure sine wave with the lowest possible THD, which requires the use of filters. However, the filter causes power losses. On the other hand, it is more important to preserve the power of DC as long as possible than the waveform, e.g., for satellites and spaceships.

Switching methods can be divided into two mains categories: those that use fundamental frequencies and high frequency modulation. For each classification, there are several techniques, as shown in Figure (2.9). The following subsections present some of the common methods and techniques used in multilevel inverters.

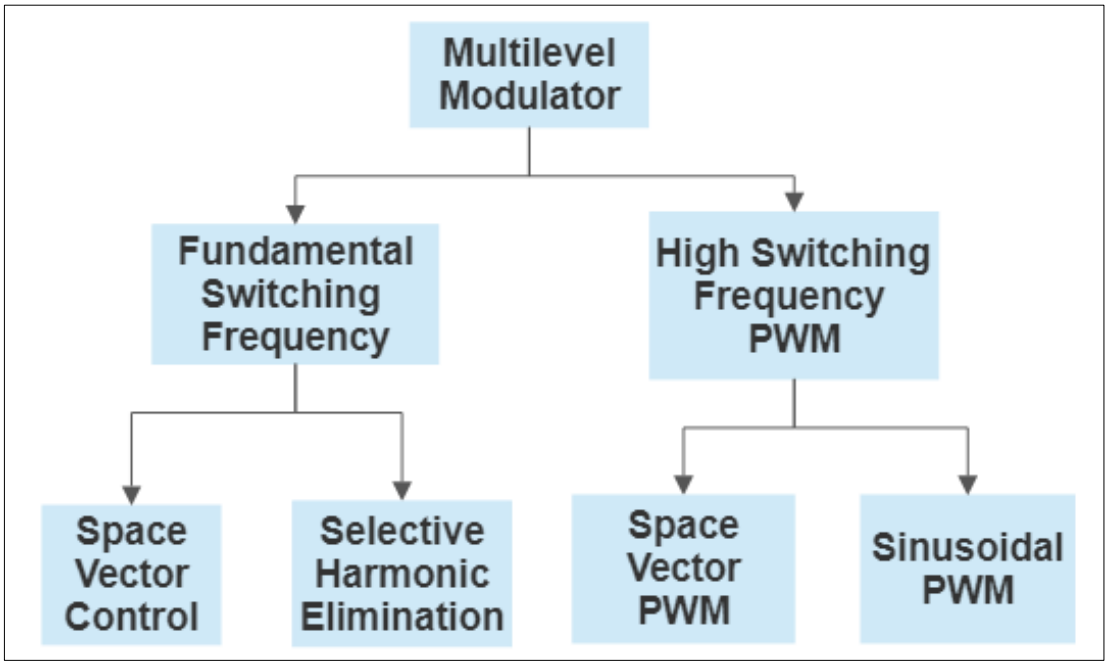

Figure 2.9 Classification of Modulation Methods [56]

2.4.1 Selective Harmonic Elimination (SHE) Modulation

According to Fourie series theory, any periodic signal with frequency (f) is actually a summation of sine and cosine waveforms with frequencies (f, 2f, 3f, …). Exploiting this theory, Patel and Hoft proposed the SHE method in 1973 [57]. This method is actually a function describing the output waveform of a single-phase L-inverter as in equation (2.10).

$$V_{inv}(\omega\tau) = \frac{4V_{dc}}{n\pi} \sum_{n=1,3,5,\ldots}^{\infty} [\cos(n\,\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_k)] * \sin(n\omega\tau) \qquad (2.10)$$

Where: k = (L-1)/2.

θ_1-θ_k are the switching angles in the first quarter waveform at each level. These angels must satisfy the following condition: ($\theta_1 < \theta_2 < \ldots < \theta_k \leq \pi/2$).

The following equations can be used to calculate the switching angles:

$$cos(\theta_1) + cos(\theta_2) + \cdots + cos(\theta_k) = kM \qquad (2.11)$$

$$cos(3\theta_1) + cos(3\theta_2) + \cdots + cos(3\theta_k) = 0 \qquad (2.12)$$

$$cos(5\theta_1) + cos(5\theta_2) + \cdots + cos(5\theta_k) = 0 \qquad (2.13)$$

... ...

$$cos(n\theta_1) + cos(n\theta_2) + \cdots + cos(n\theta_k) = 0 \qquad (2.14)$$

Where M is the value of the basic DC voltage source, (M = the DC voltage source for symmetric, while for asymmetric, M = the lowest value of the DC voltage sources) and n = L – 2.

Solving equations (2.11-14) and determining the optimal switching time (switching angle) of each switch produces a staircase waveform that has no low harmonics. Since all the values of θ must be within the first quarter according to the above condition, these values are used in the second quarter at $\pi - \theta$, and $\pi + \theta$ and $2\pi - \theta$ are used for the third and fourth quarters, respectively, as shown in figure (2.10).

Solving the equations (2.11) to (2.14) and finding values of θ_1-θ_k and then substitute them in equation (2.10). The inverter will then generate a sinusoidal waveform in which lower harmonics are eliminated and thus the harmonic distortion is lower. However, solving these equations is challenging, especially for higher level inverters. There are several methods for solving these equations, such as Generic Algorithm and Newton Raphson.

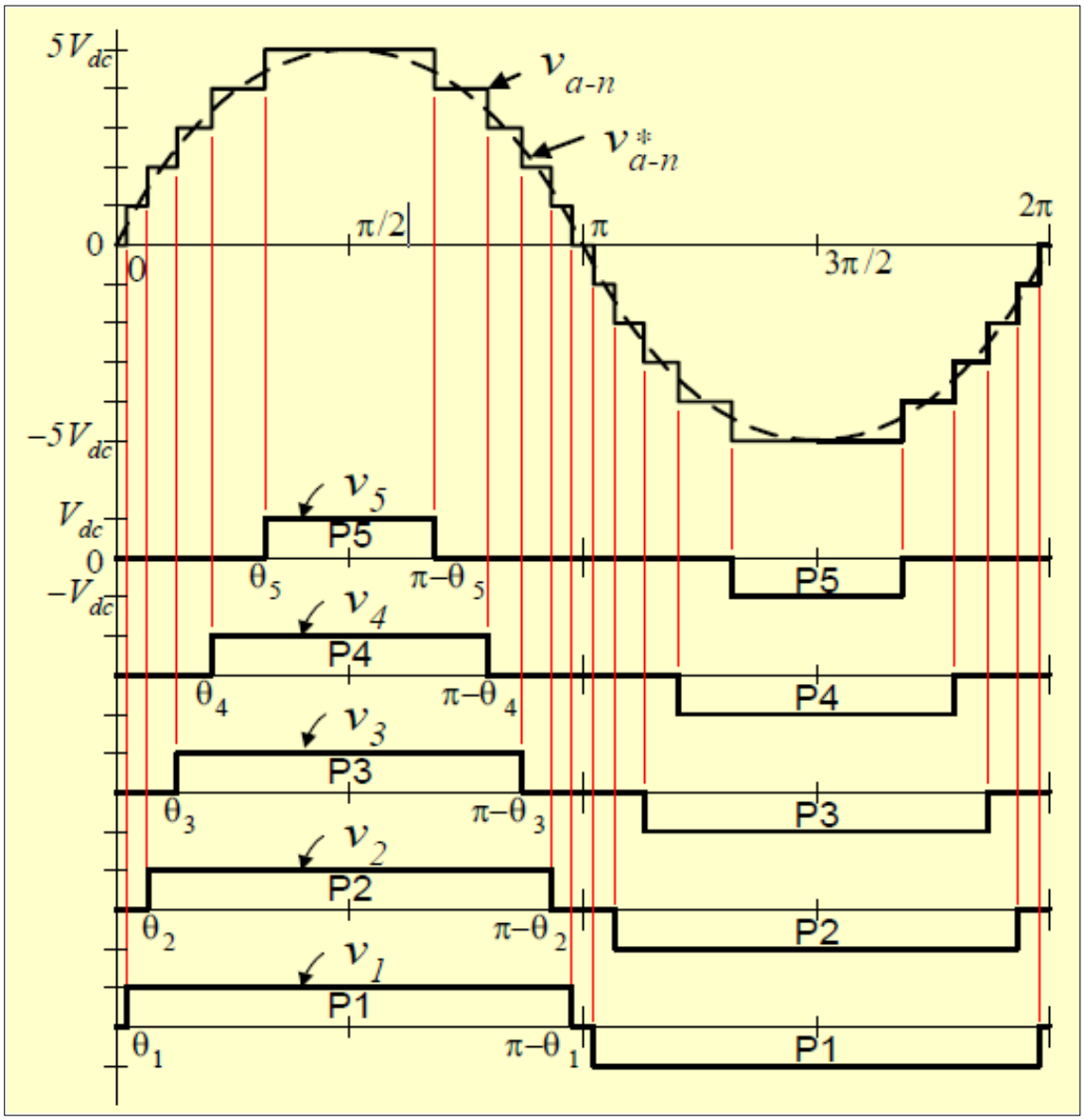

Figure 2.10 Output Waveform of an 11-level Cascade Multilevel Inverter [58]

Where *P* represents the output voltage of each bridge.

A. Newton Raphson (NR) Method

NR method is used to solve the above equations and determine the optimal time for switching. It is one of the fastest iteration algorithms for solving nonlinear sets equations. However, it requires a reasonable estimate of the initial values at the beginning. If the estimate is not reasonable, there may be no solution [59].

The equations above have several variables that must be found. First, these variables are eliminated by replacing multiple equations with only one equation and one variable. NR is used to solve the final equation by assuming the initial value and then finding the next point through the following equation (2.15)

$$x_{n+1} = x_n - \frac{f(x_n)}{f'(x_n)} \qquad (2.15)$$

However, for some equations, it is difficult to drive the equation, and therefore numerical derivation methods are used. Nowadays, MATLAB does most of the work to solve such problems using accurate and fast approaches [60].

B. Genetic Algorithm (GA) Method

GA is a method for random search algorithm that is derived from nature. It is capable of solving linear and convex equations. However, it is more efficient for discrete and nonlinear equations [61].

Since it was derived from nature, it works just like nature. As a result, at the beginning, a group of solutions is proposed either randomly or algorithmically; these solutions are called population, and each of them is called a chromosome. The genetic algorithm is then applied to these

chromosomes, such as crossover and mutation, and thus a new generation is produced. Figure (2.11) illustrates the GA process, where the previous steps are reapplied to approach the solution.

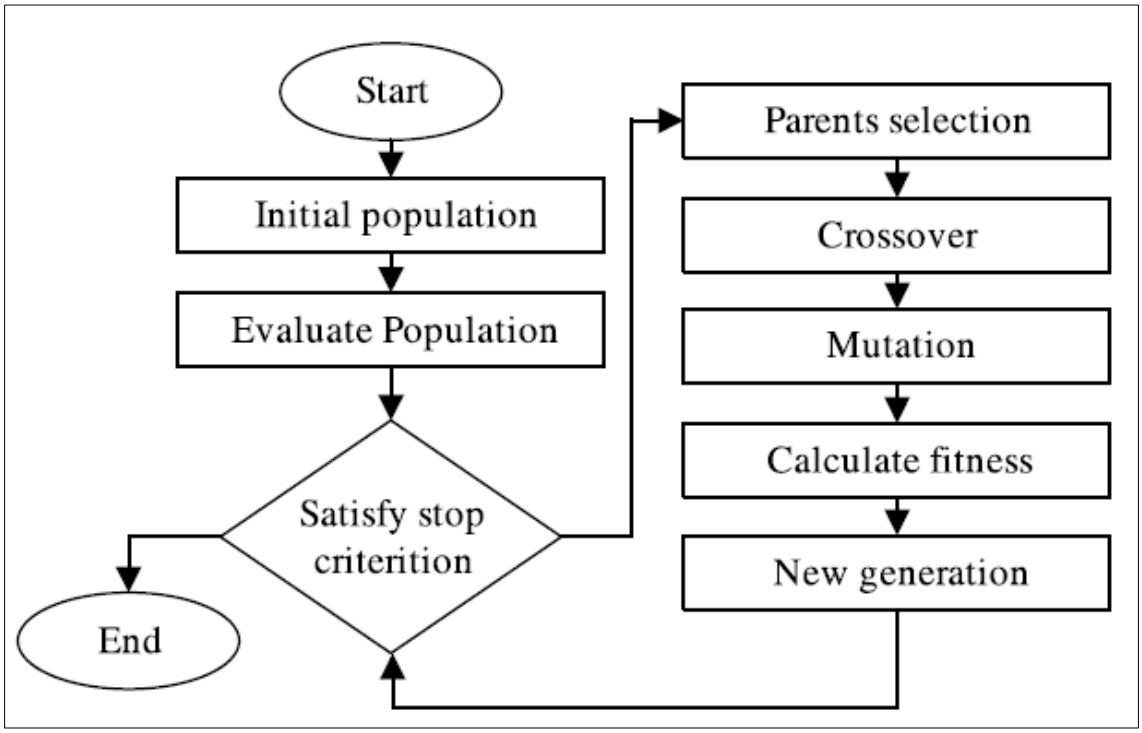

Figure 2.11 GA Flow Chart Process [62]

2.4.2 Sinusoidal Pulse Width Modulation (SPWM)

SPWM is one of the most popular switching control methods for multilevel inverters and is widely used because of the following advantages: It is easy to be implemented, its output signal has lower THD, and switching losses are low.

The main idea of this method is to compare a tringle signal with the ideal sinewave. If the sinewave is larger than the triangle signal, the gating ON and thus the corresponding level is higher. On the other hand, if the sinewave is smaller than the tringle signal, this is an indication of

OFF. However, there are different approaches to the use of PWM and the way tringle signals are used. In the following subsections, some of them are presented [63].

A. Phase Disposition PWM

In this approach, the carrier signals are identical in frequency, amplitude, and phase. However, each one is located at different dc offset level and the number of these carrier signals is (L-1), where L is the number of inverter levels. A sine wave is compared to these carrier signals individually; if the carrier signal is higher, it signals the corresponding switch level by ON, otherwise OFF. Figure (2.12) illustrates this method.

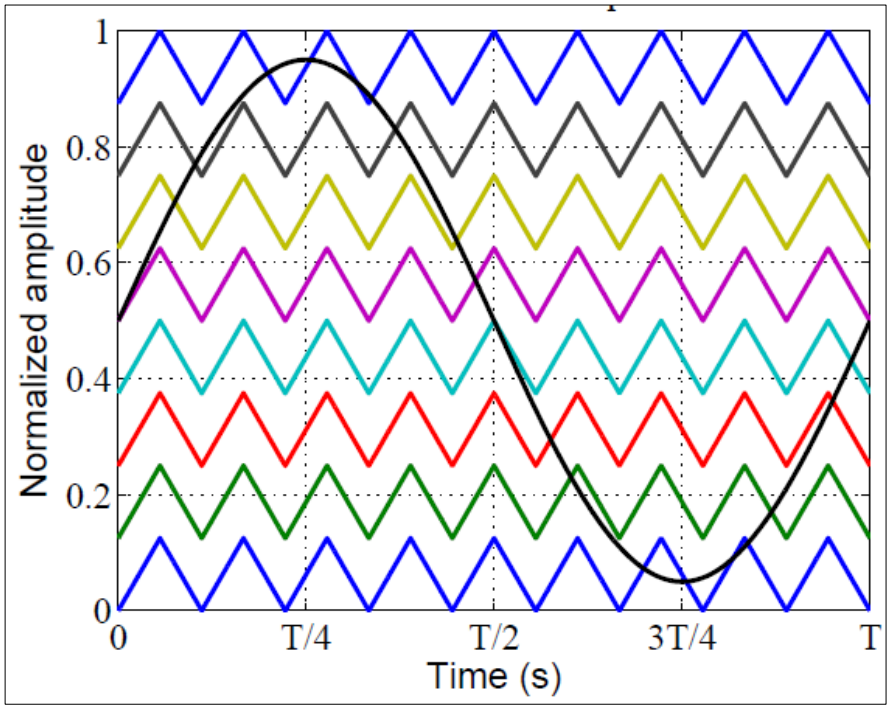

Figure 2.12 Phase Disposition PWM [61]

B. Phase Opposition Disposition PWM

This approach is similar to the previous one, except that the carrier signal is 180º out of phase below the reference neutral voltage line. In

other words, the carrier signals are mirrored about the neutral-voltage axis. Figure (2.13) illustrates this method [61].

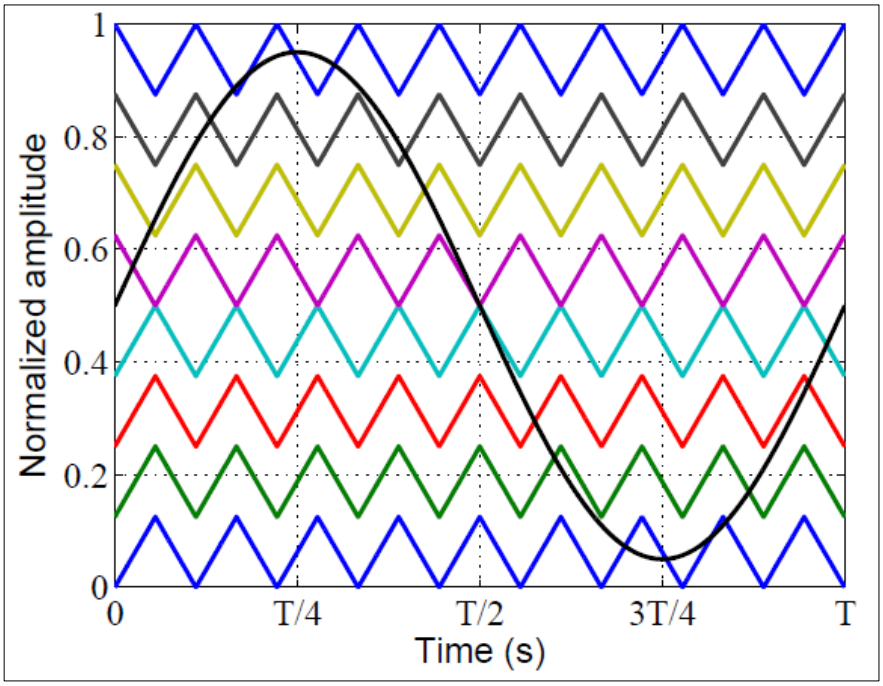

Figure 2.13 Phase Opposition Disposition PWM [61]

C. Alternative Phase Opposition Disposition PWM

In this method, there are multiple carriers that have identical amplitude and frequency, each of which is shifted vertically, similar to the aforementioned methods. The difference, however, is that the waves from each of two adjacent carriers are 180^{o} out of phase. Furthermore, these carriers are mirrored around the neutral-voltage reference axis, as shown in Figure (2.14) [58] and [63].

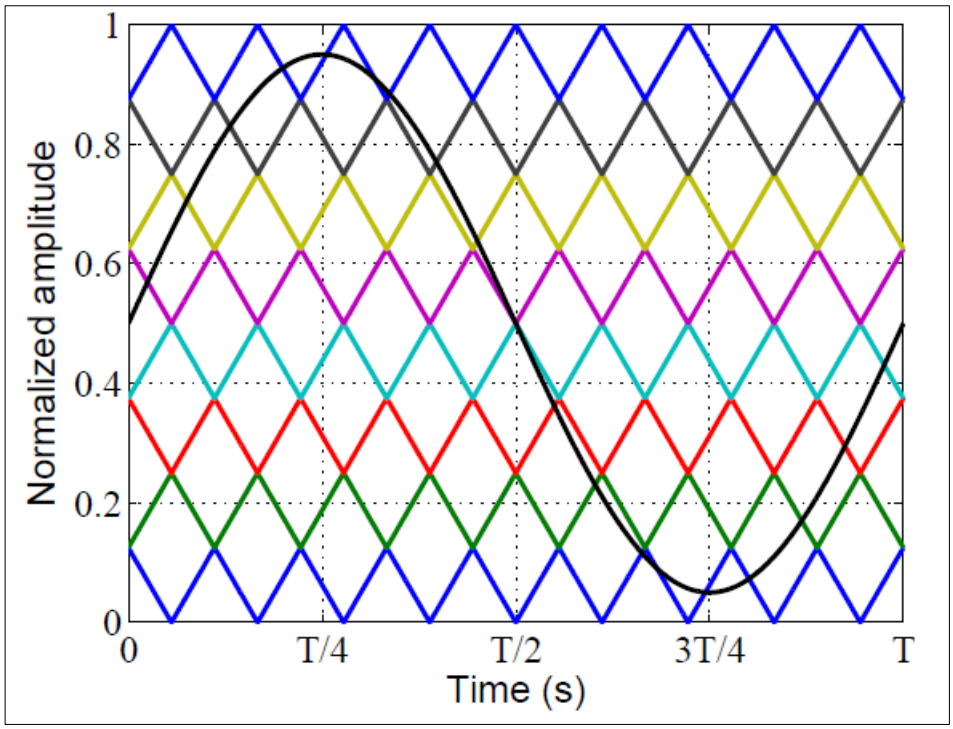

Figure 2.14 Alternative Phase Opposition Disposition PWM [61]

D. Phase Shift PWM

In this method, the carriers have the same amplitude, frequency, and dc level. However, they differ by phase, as shown in figure (2.15). This method is the most common method of PWM used in multilevel inverters because its implementation is simple, it can distribute the load evenly among the DC sources, and it produces a high-quality waveform [61] and [63].

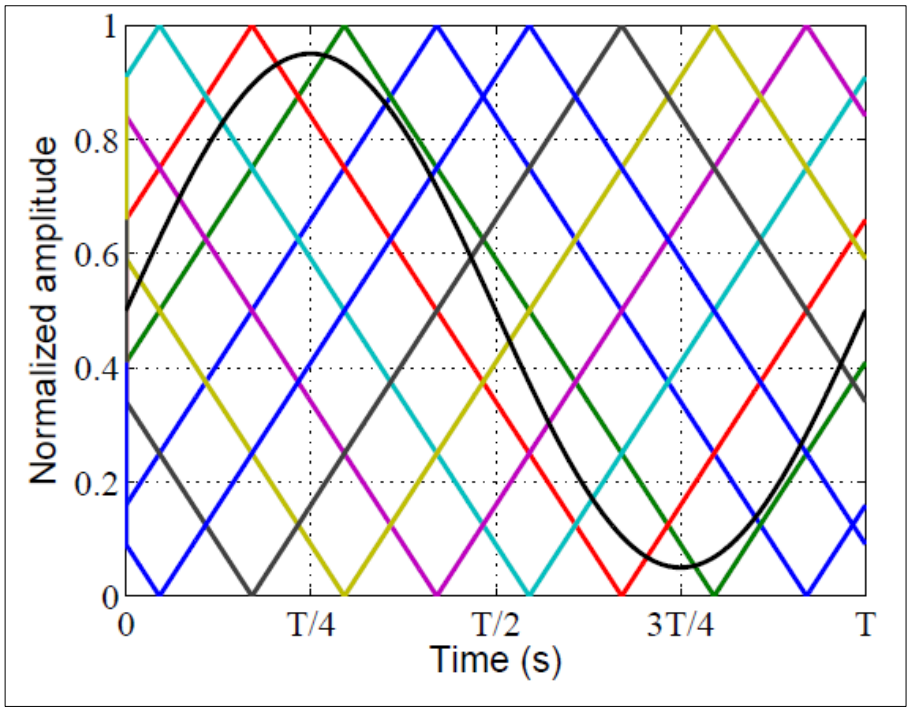

Figure 2.15 Phase Shift PWM [61]

2.4.3 Nearest Level Modulation Method

In this method, the entire range of the output voltage (V peak to peak) is divided into steps corresponding to the number of inverter levels. The instantaneous value of a sine wave is then quantized to the nearest level, as shown in Figure (2.16). Each level has an array of ones and zeros that control the inverter's switches. This technique is simple to implement, has a low switching frequency, and therefore lower switching losses [64].

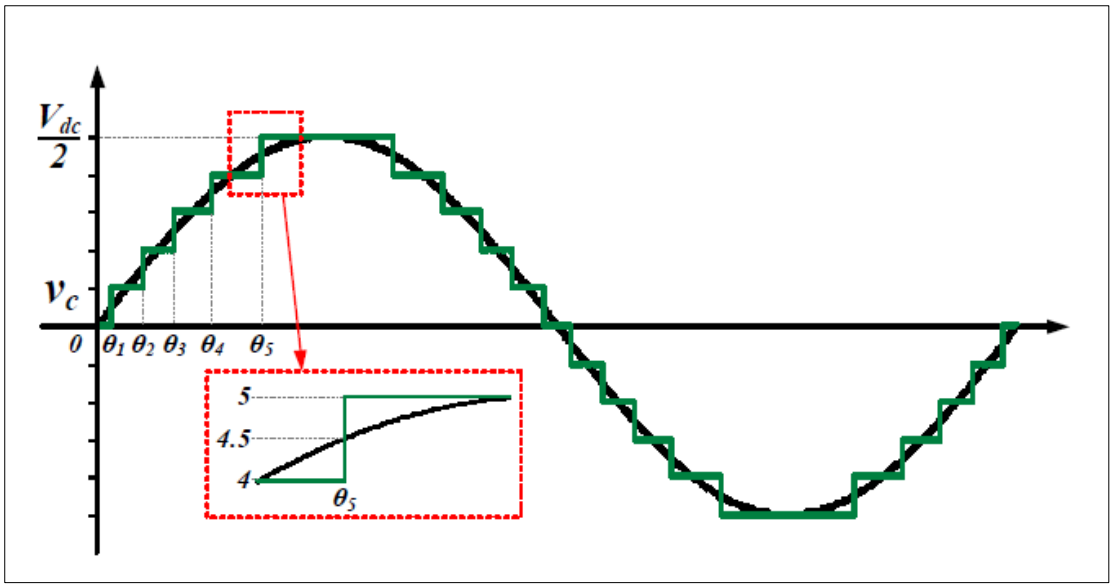

Figure 2.16 Operational Principle of the Nearest Level Modulation [64]

CHAPTER THREE

DESIGN THE INVERTER AND THE SIMULATION RESULTS

3.1 Introduction

This chapter presents a 27-level CHB inverter design and simulation by MATLAB Simulink. Three HBs are used, each powered by a trinary asymmetric DC voltage source in a 1:3 ratio, i.e. (25, 75 and 225 volts). Each HB consists of four MOSFET switches controlled by a control circuit. The control circuit uses Nearest Level, SPWM and SHE modulation methods. The HBs are series-connected and the THD of the generated waveform is measured and compared to the different modulation methods. This process is repeated with inserting a filter between the inverter and the load then, the THD is measured again. System design simulation helps predict the optimal design and modulation method. In the following subsections, the inverter design is explained, the modulation methods used are presented, and a comparison of the final results is made.

3.2 Design of 27 Level Asymmetrical Inverter

MATLAB Simulink was used to design and implement a 27-level inverter that has three CHBs, each with its own DC source. In addition, a switching controller is used to control the inverter using three different methods. In this section, the design of the inverter system as shown in Figure (3.1) is explained in detail.

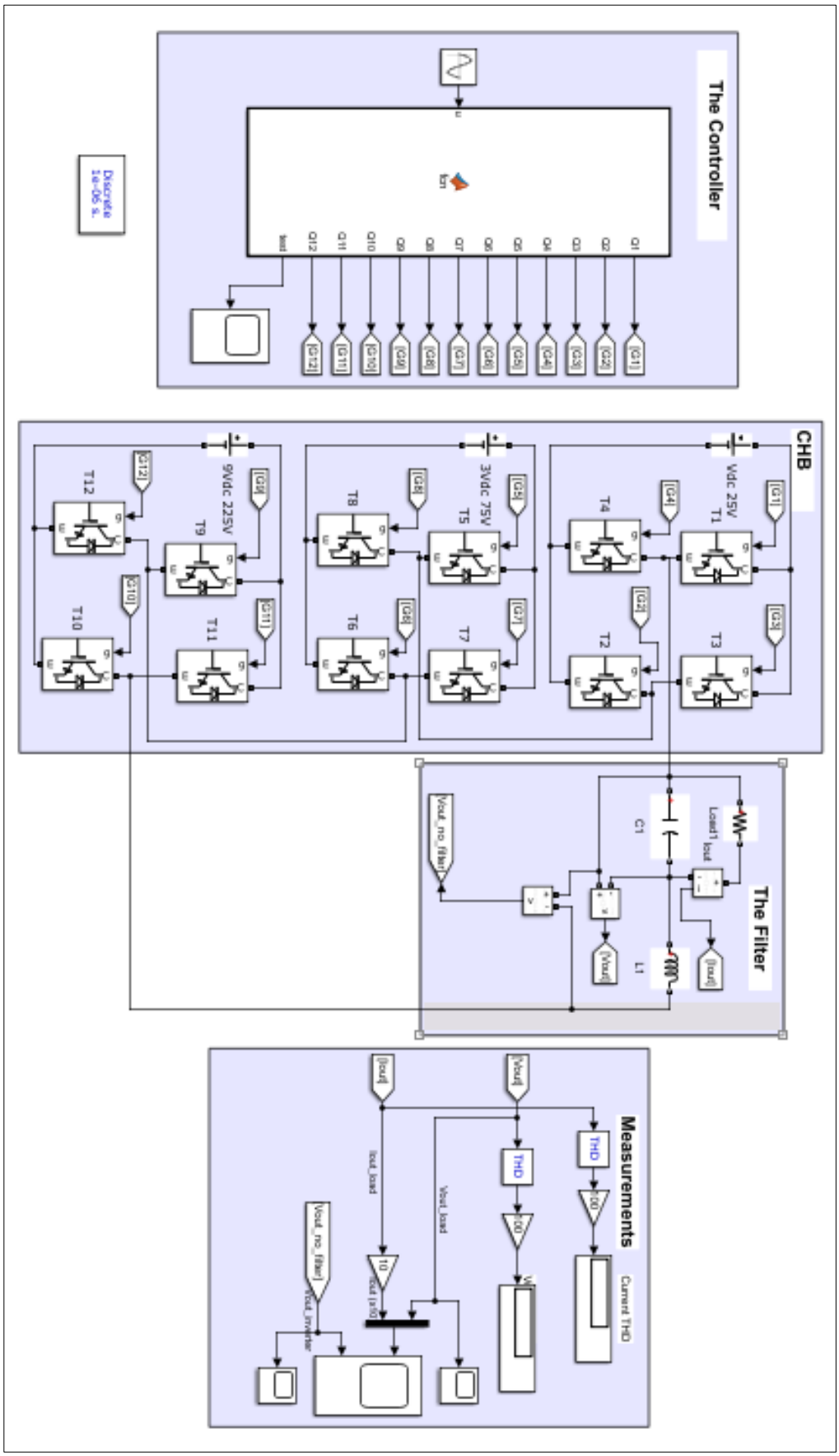

Figure 3.1 Simulink of 27-Level Inverter System

3.2.1 Design of Cascaded H Bridges

The main part of this system consists of three series-connected CHBs. Each of them is composed of four semiconductor switches. The switch used is a MOSFET, which is a power switching device with three terminals: Drain, source, and gate. MOSFETs have a high input impedance and are therefore particularly suitable for switching high power devices.

Regarding power losses from inverters, semiconductor switches are considered the main source of power losses. Semiconductor switches lose power in three ways.

1 Conduction losses: losses during steady-state normal conduction mode.
2 Switching losses: losses caused by transistor transition between on and off states.
3 Internal body diode losses: when the body diode is used for conducting.

Since the system is designed to generate a single-phase 220-volt waveform, the peak voltage ($V_p = V_{R.M.S} * \sqrt{2}$) for 220-volts is ($V_p = 220 * \sqrt{2} = 311$). As a result, the HBs are fed by three asymmetric DC sources, which are (25, 75, and 225V). The addition of these three sources gives a peak voltage of 325-volts. This value must be higher than 311 and can be set to a specific value, i.e., 311, using the modulation index.

3.2.2 Design of The Output Filter

The CHB produces a sinusoidal waveform that has higher harmonics, whereas inductive loads such as motors are designed for a pure

sinusoidal signal. As a result, these harmonics heat up the load and hence reduces the efficiency. Subsequently, they reducing the load lifetime.

As a result, in the simulation, LC filter, as shown in Figure (3.2), is used to suppress the high harmonics and improve the generated waveform. The inductor and capacitor act as energy storage and therefore increase the efficiency of the inverter. In addition, the values of L and C determine the filter performance and the cut-off frequency. As a result, they must be carefully selected to avoid resonant frequencies and achieve optimum performance.

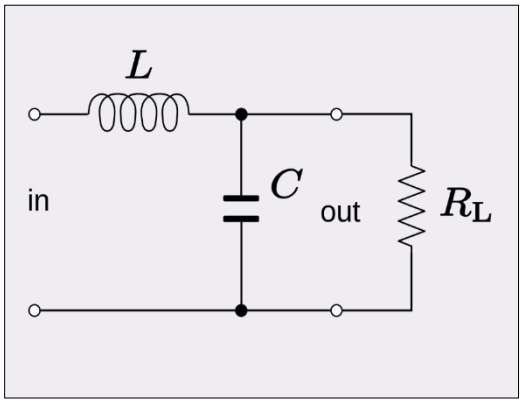

Figure 3.2 Typical Architecture of LC Filter

A. Inductor Design

The value of the inductor is calculated by the following equation (3.1)

$$L = \frac{V_{DC}}{Num\ of\ Levels \times 2 \times f_{sw} \times I\_load\_\max \times ripple\_percentage} \ldots\ldots (3.1)$$

Where:

f_{sw}: the switching frequency.

The ripple- percentage is the inductor ripple current, which should be chosen as 40% of the RMS current of the inverter and is considered in most references [65]-[67].

By substituting the values, L is calculated as follows for SPWM as the switching frequency is 10 kHz

$$L = \frac{325}{13 \times 2 \times 10{,}000 \times 4 \times 0.40} = 781\ \mu H$$

On the other hand, for SHE and Nearest Level Modulation, the value of the value of inductance (L) is calculated as following as the switching frequency is 50 Hz times 54 levels resulting in 2,700 Hz.

$$L = \frac{325}{13 \times 2 \times 2700 \times 4 \times 0.40} = 2.893\ mH$$

From the equation above, it can be noticed that the value of the inductor is large and is inefficient practically.

B. Capacitor Design

To assign the capacitor value, it is calculated by the equation (3.2).

$$C = \frac{\%Q_{rated}}{2\pi \times f_{Load} \times V_{Load}^2} \quad \ldots\ldots\ldots \quad (3.2)$$

Where $\%Q_{rated}$ is the total reactive power absorbed by the capacitor, limited to 5% of the total power for each phase [65]. f_{Load} is the generated frequency, V_{Load} is the voltage of the generated waveform.

$$C = \frac{0.05 \times 1000}{2\pi \times 50 \times (220)^2} = 3.28\,\mu F$$

3.3 Modulation Methods

Developing the inverter topology is only half the battle in producing an acceptable sinusoidal waveform that contains fewer harmonics. The other half of the way is the modulation method. Three modulation methods are applied in this simulation, namely SHE, SPWM, and Nearest level modulation. The methodology of these methods is explained in chapter two.

The simulation was run twice with each modulation method, once with filter and once without filter. Thus, the simulation was run six times and different results were obtained. In the following section, the results are presented.

3.4 Simulation Results

Since three modulation methods are used in this simulation, each with and without filters, therefore, six different results are generated. Each result includes the generated waveform and the measurement of the THD. These results give a prediction of the optimal design to then design and implement the hardware circuit.

3.4.1 Results of The Nearest Level Modulation

Figure (3.3) demonstrates the wave form without filter. On other hand Figure (3.4) shows the effect of adding a filter on the output waveform. The filter effect has a significant impact on the generated signal. For example, the steep edges are smoothed.

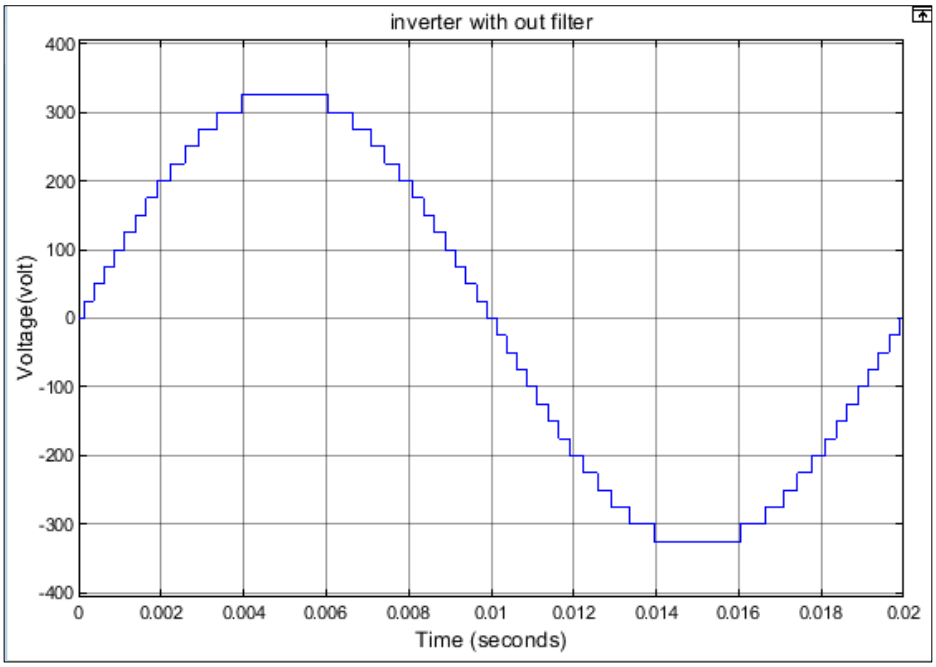

Figure 3.3 The Generated Waveform of Nearest Level without Filter

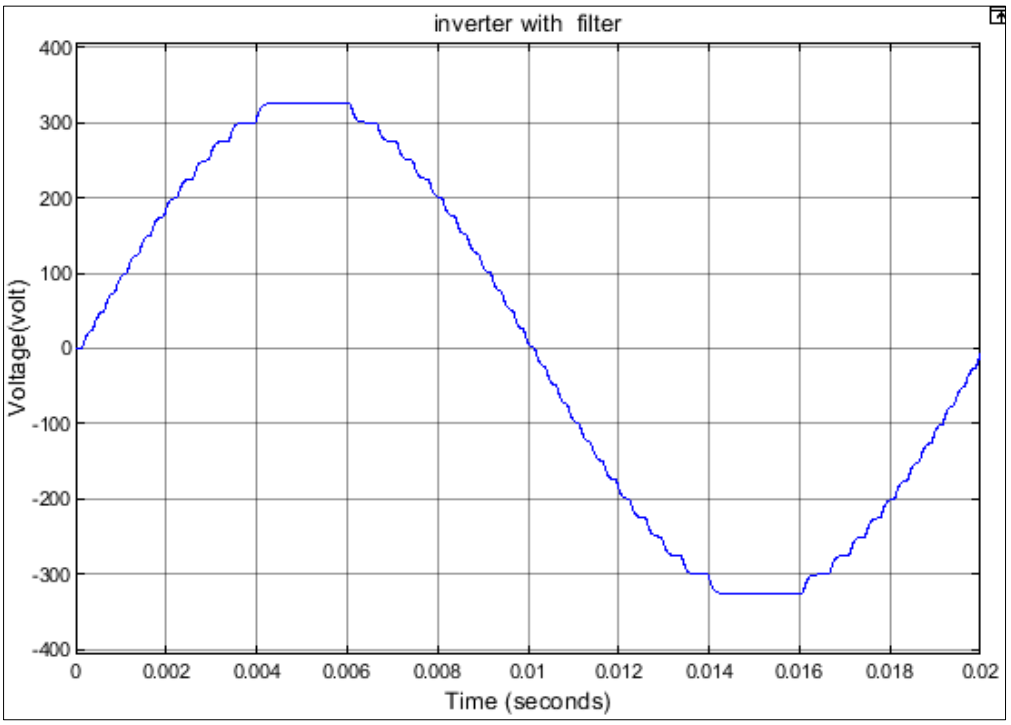

Figure 3.4 The Generated Waveform of Nearest Level with Filter

In terms of THD, Figures (3.5) and (3.6) show that the THD of the generated signals dropped from 2.95% to 1.55% after applying the filter.

It can be noticed that the THD is decreased, this is a reasonable result because of the filter suppressed higher frequencies which are resulting from the switching edges.

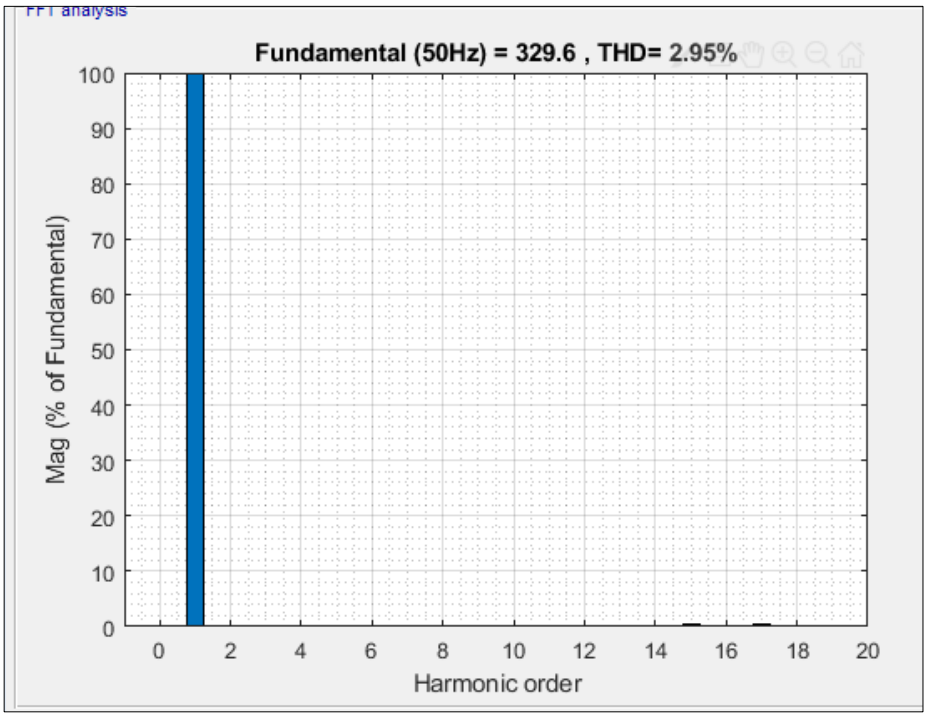

Figure 3.5 THD of the Nearest Level Output Signal without Filter

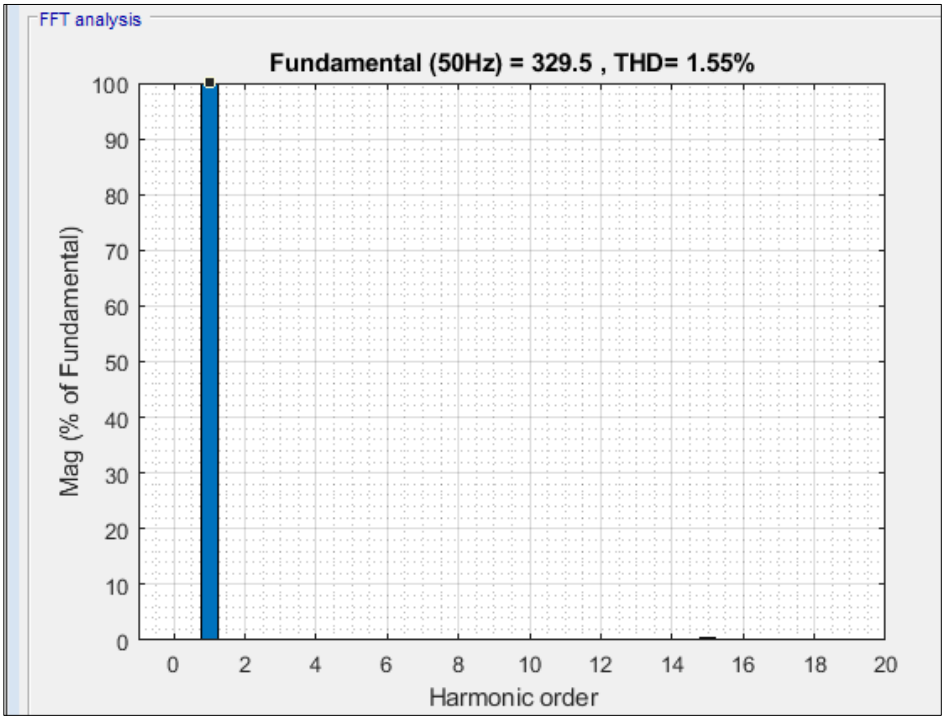

Figure 3.6 THD of The Nearest Level Output Signal with Filter

3.4.2 Results of SPWM

Figures (3.7) and (3.8) show the generated waveform without and with filters, respectively, when SPWM is applied. Since SPWM operates at high frequencies, the generated signal is enhanced using the filter. It is smoothed and the higher frequencies are suppressed. So, it looks like an ideal sinusoidal waveform.

However, the THD calculation determines the actual impact of the filter on system performance. Figures (3.9) and (3.10) show the THD without and with the filter. The THD decreased from 4.29% to 0.56% after the filter was applied. The filter improved the output signal of the SPWM since it operates at high frequencies and higher harmonics are present, which are then removed by the filter.

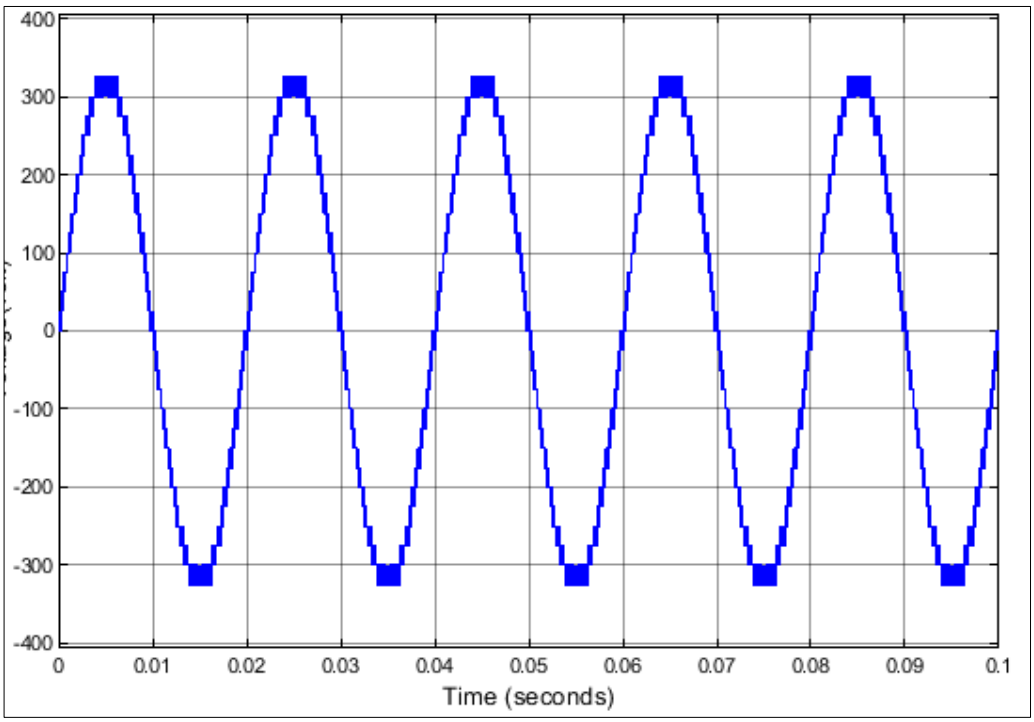

Figure 3.7 The Generated Waveform of SPWM without Filter

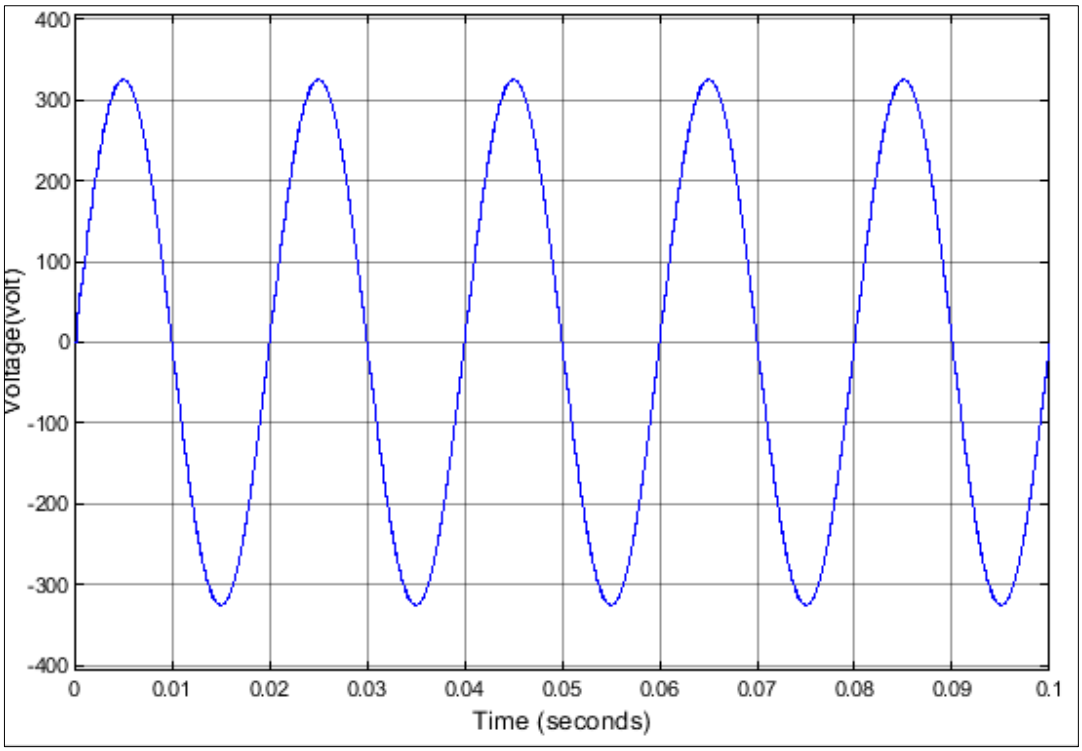

Figure 3.8 The Generated Waveform of SPWM with Filter

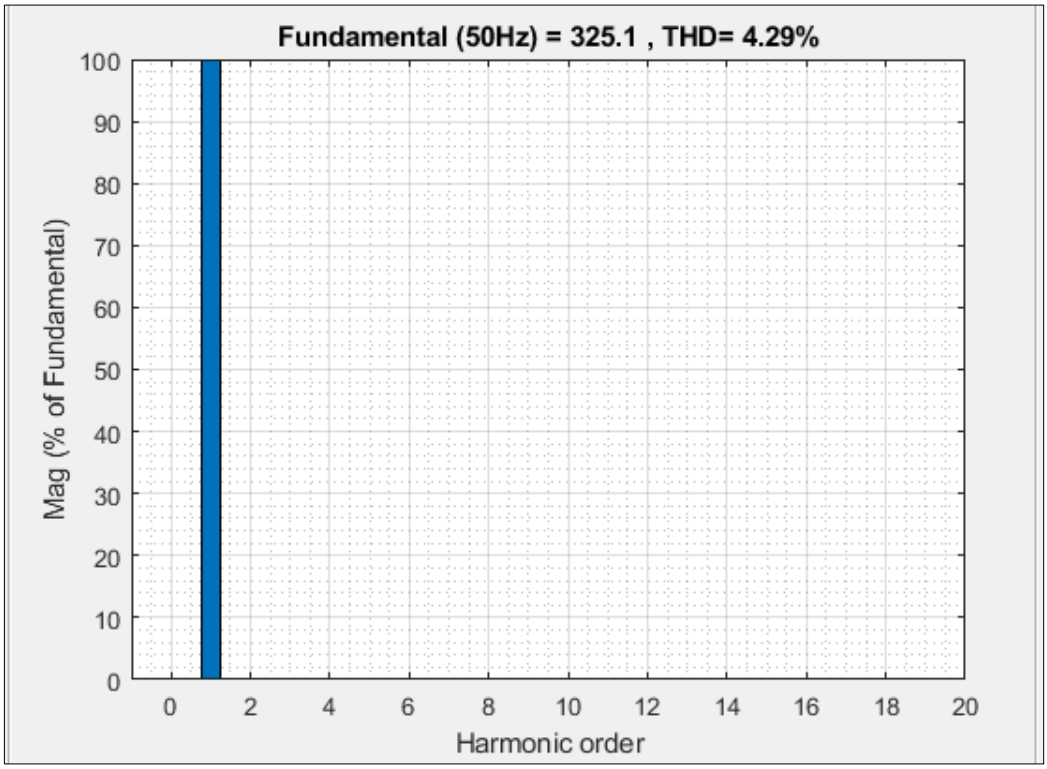

Figure 3.9 THD of the SPWM Output Signal without Filter

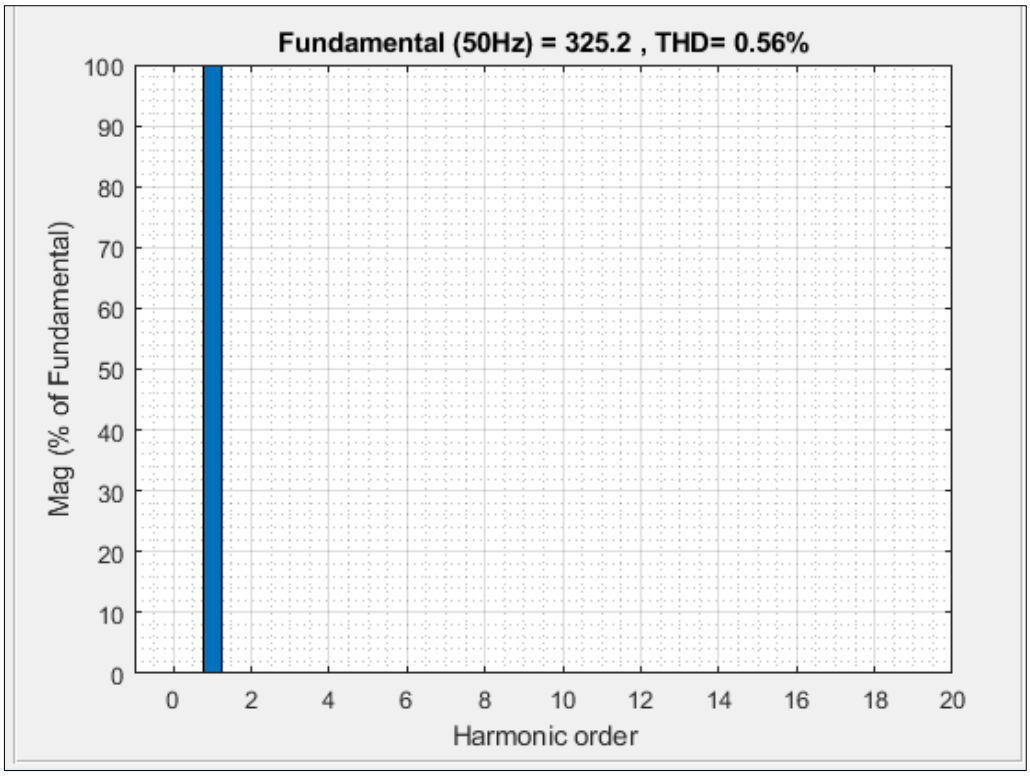

Figure 3.10 THD of the SPWM Output Signal with Filter

3.4.3 Results of Selective Harmonics Modulation

Selective Harmonic uses a certain switching degree depends on the method being used for calculating them. In this research, Newton Raphson method, and by the use of MATLAB, these triggering angles are determined as in the following table.

Table 3.1 switching angles for 27 level SHE inverter

Number of levels	Switching angles in degree
27 level	4.25, 7.27, 11.75, 16.2, 21.35, 27, 31.9, 37.5, 43.79, 49.3, 57.6, 70.2, 89.4

These triggering angels are chosen to eliminate the odd order harmonics from 3 to 25.

This section shows and compares the waveform and THD of the SHE modulation method without and with filter.

Figure (3.11) shows the waveform when no filter is inserted.

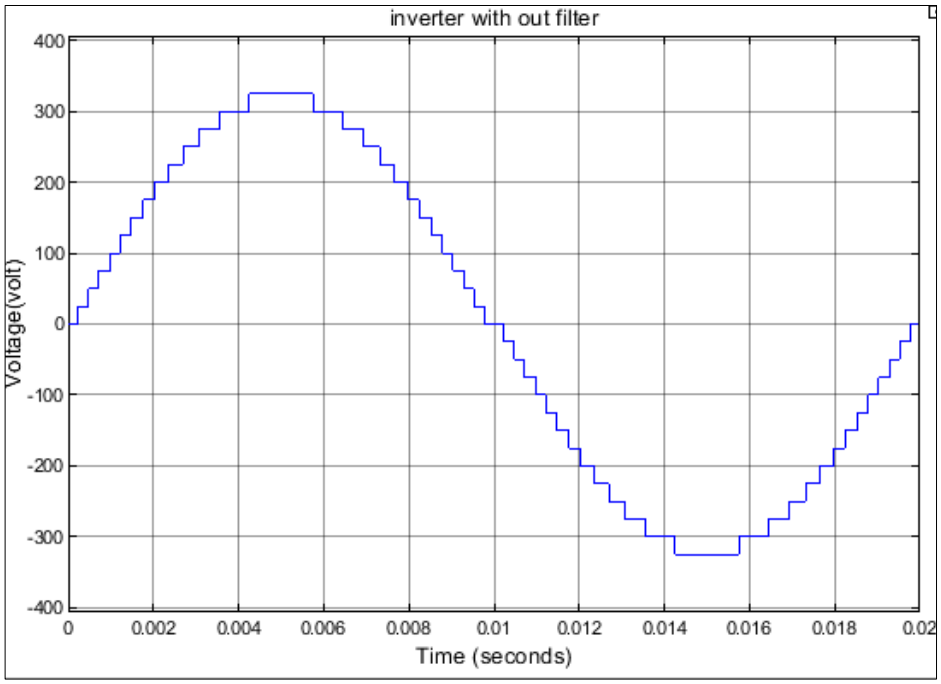

Figure 3.11 The Generated Waveform of SHE without Filter

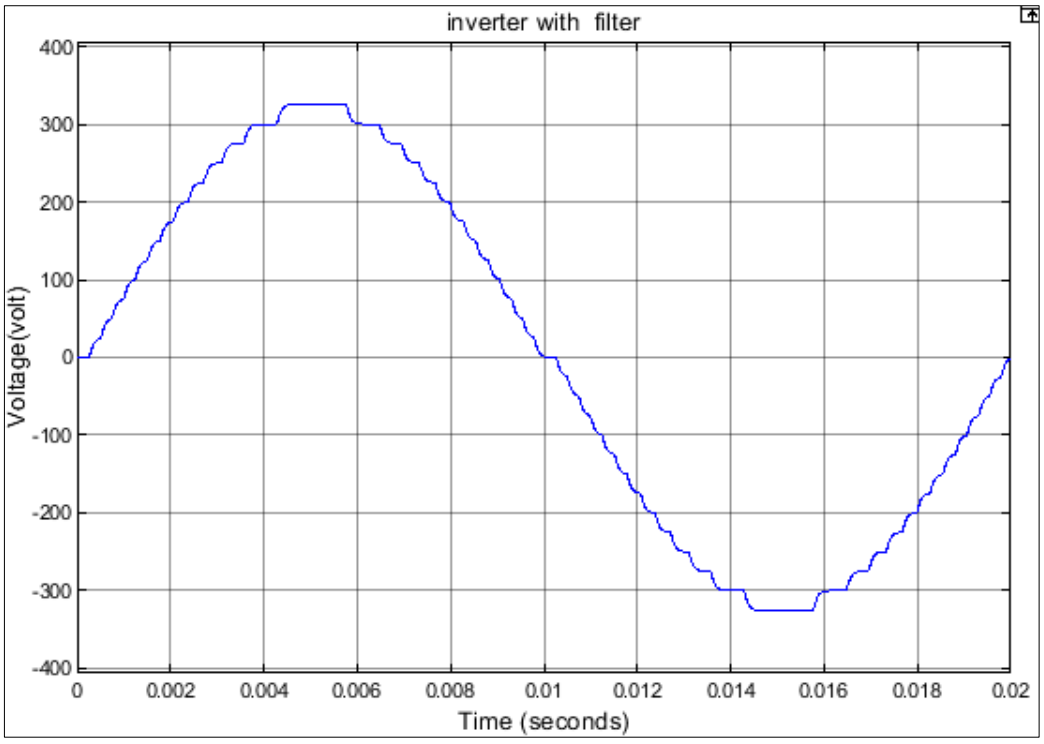

Figure 3.12 The Generated Waveform of SHE with Filter

On the other hand, Figure (3.12) shows the output signal with filter. These two figures show the waveform, and the filter effect is clearly visible. The filter smoothed the signal and removed the steep edges and become more like sinusoidal wave.

In terms of THD, Figures (3.13) and (3.14) show the THD of the output signal without and with filter respectively.

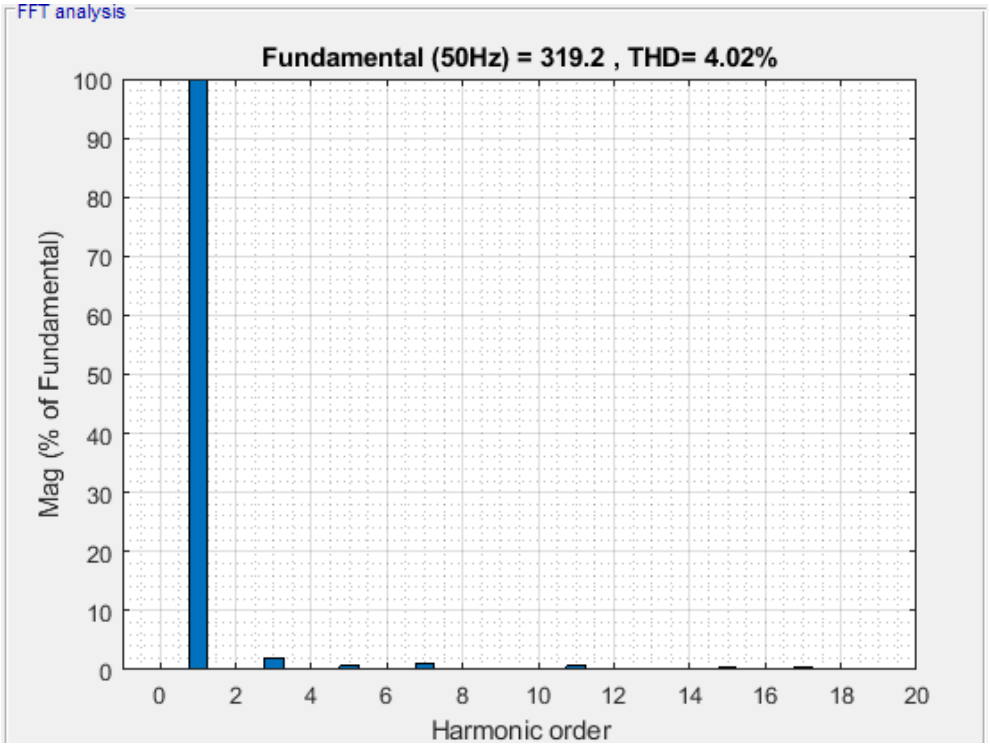

Figure 3.13 THD of the SHE Output Signal without Filter

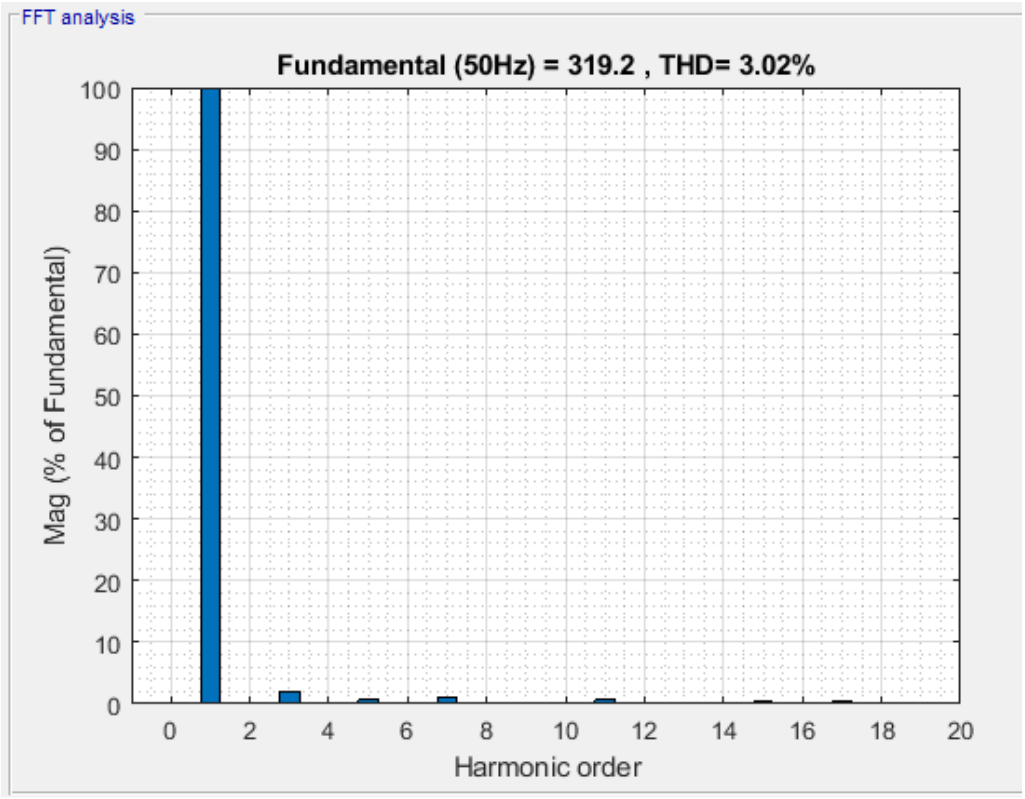

Figure 3.14 THD of the SHE Output Signal with Filter

The output signal has THD = 4.02% when the selective harmonic method is used and no filter is applied as in Figure (3.13). Comparing this Figure with the result in Figure (3.14) where the filter was applied, i.e., THD = 3.02%. These results show that the filter decreased the THD. The decrease in the THD resulting from smoothing the edges.

To summarize the results, Table (3.2) compares the THD of all the above results.

Table 3.2 Compression of the THD Percentage for Different Modulation Techniques and Filter

Modulation methods	THD percentage	
	With filter	Without filter
Nearest level	1.55%	2.95%
SPWM	0.56%	4.29%

SHE	3.04%	4.02%

In summary, the nearest level modulation method shows the lowest THD when no filter is applied, which is 2.95%. However, the SPWM shows the best performance in terms of waveform, which produces an ideal sinusoidal signal, and the THD = 0.56%.

CHAPTER FOUR

Experimental Validation

4.1 Introduction

In this chapter, the hardware design of the 27-level inverter is described and the electronic ICs used are presented. The hardware design can be divided into four main parts. First, the controller part, which includes a Micro Controller Unit (MCU) and a Complex Programmable Logic Device (CPLD). They calculate the required level and duty cycle of the PWM and then switch the transistors in the HBs to the appropriate state. Since the transistors in the HBs are power transistors that require +18 V to turn on and -5 V to turn off, while the controller generates logic levels between 0 and 5 V, a separate driver is required. In addition, a filter is used to smooth the generated sinusoidal signal and suppress the higher harmonics. Finally, voltage and current sensors are developed and used to monitor the inverter performance, and a built-in programming circuit and Universal Serial Port (USP) connector are used to reprogram the inverter and apply a different modulation method easily.

4.2 Experimental Setup

Figure (4.1) illustrates the operation of the inverter, Whereas Figure (4.2) shows the hardware implemented system.

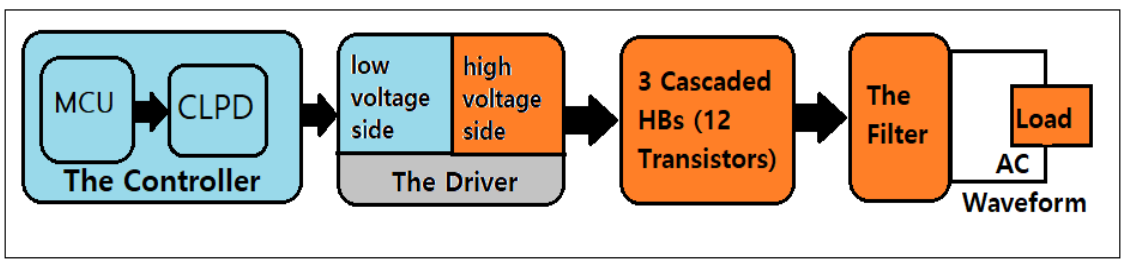

Figure 4.1 The Flow Chart of the Inverter Process

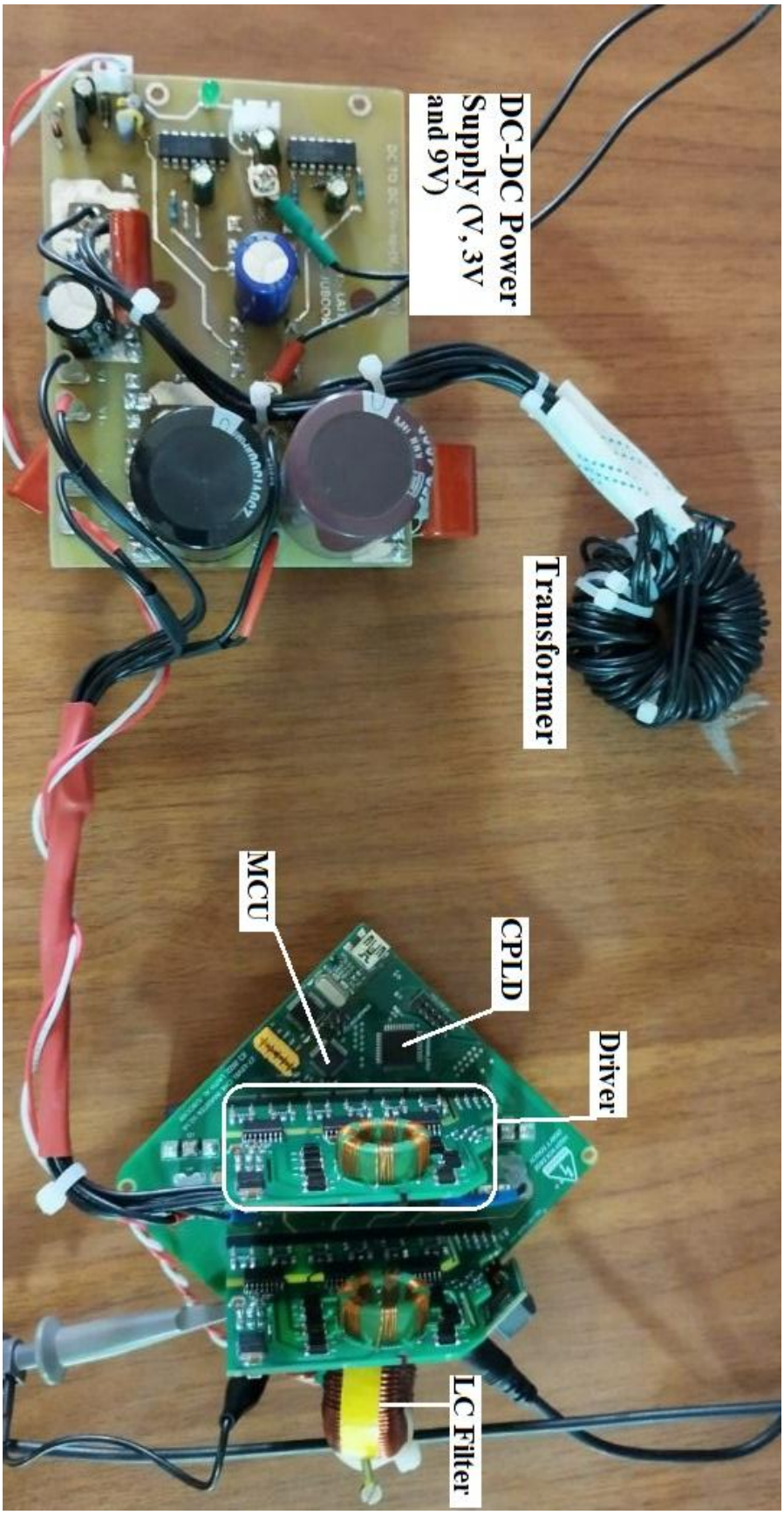

Figure 4.2 The Hardware Implemented System

4.2.1 The Controller

The controller is the main part of the inverter and its task is to control the switching of the 12 semiconductor switches in the HBs. It consists of MCU and CPLD which are presented in the following subsections.

A. The Micro Controller Unit

MCU is the master for the other parts of the inverter. For example, it hosts the modulation method and interprets the modulation method to give signals to other parts. ***STM32F334C8T6*** is used as the MCU in this design. This MC is ARM Cortex M4, 32-bit architecture, it operates at high frequency, up to 72 MHz. It has several built-in functions, such as two 12-bit ADC with fast sampling up to 5 Msps, and high-speed embedded memory, i.e., 64 KB flash memory and 12 KB SRAM. in addition, this microcontroller has three DACs and several timers, such as a high-resolution timer and a general-purpose timer. It supports a number of interfaces, such as SPI, I2C and USART. It also has up to 20 general purpose ports that are used as input/ output controllers [68]. Due to the above-mentioned features, this MC was selected in this design.

Since the MCU is a digital device, it does not have a sinusoidal generator. However, it is possible to stimulates a sine wave by specifying a table of values to be used by a timer, which then generates a sine wave. This wave is used as a reference to apply the modulation method.

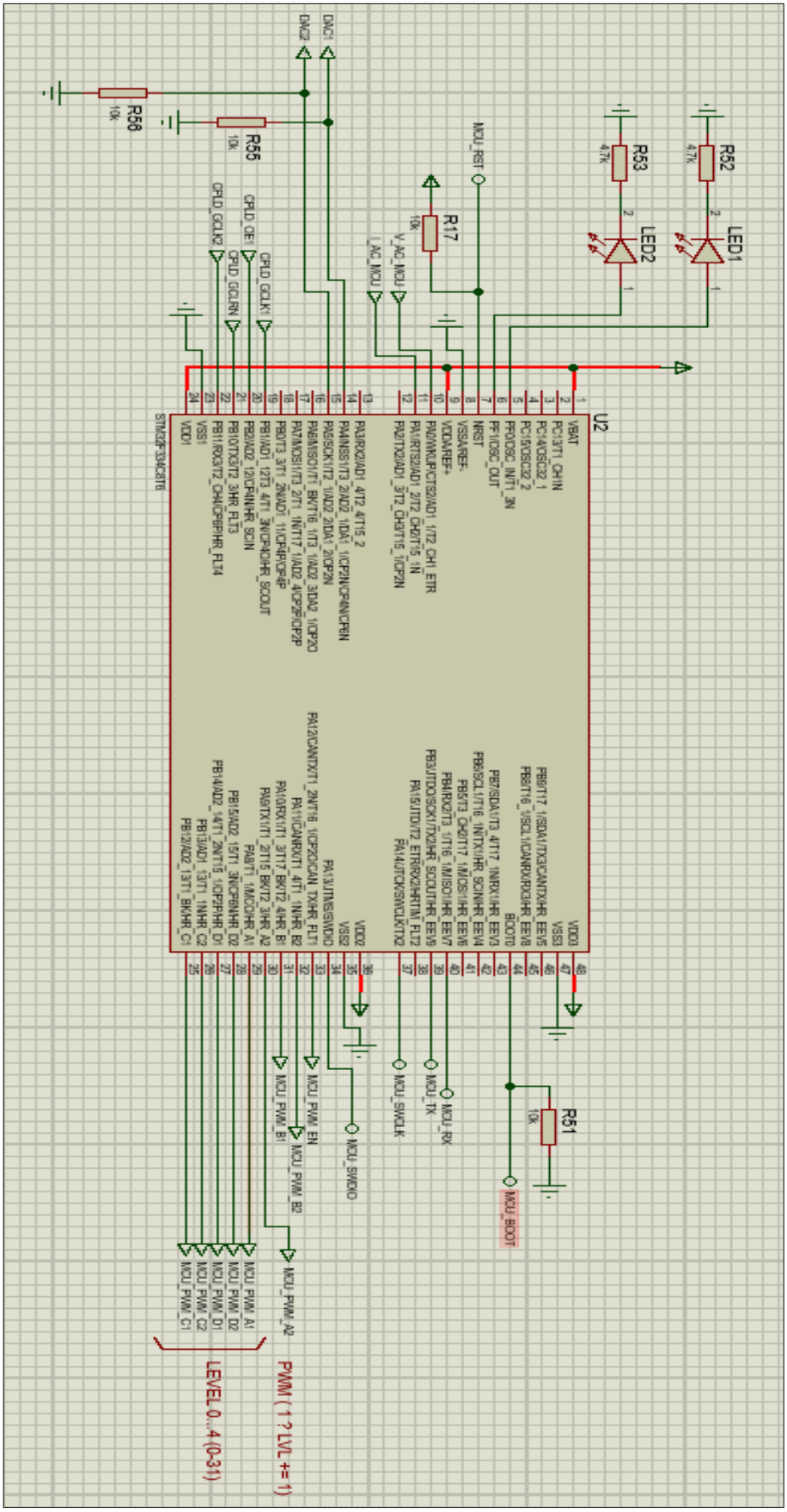

Figure 4.3 STM32F334C8T6 MCU (The Design in the PCB)

In this inverter design, 27 levels are selected by using three cascaded HBs, therefore 12 switches are involved. These switches may be driven at 10 kHz, that is, if the SPWM method is used. In other words, the switches must update their state every 0.1 ms. In addition, the duty cycle of the PWM must be a fraction of the level, resulting in a shorter time for the switches to update. For instance, if the duty cycle is 10%, the HBs must be updated within 0.01 ms. In addition to switching, other sensing functions and calculations also take time. Therefore, direct control of the HBs is not practical and could lead to problems. Subsequently, a CPLD is used to drive the HBs according to a table of values. By adding the CPLD to the system, the number of switching buses is reduced to only 6 (pins 25-30) instead of 12 as shown in Figure (4.3).

B. Complex Programmable Logic Device

CPLD is a logic device that is programmable according to the user's needs. It consists of many microcells, each one of consists of a large number of logic gates. When programming the CPLD, the logical gates are connected together to then perform complex logical operations. In this project, the ***EPM3064A_CPLD*** is used to drive the CHBs. Very High-Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL) is the programming language for CPLD and Quartus 9 software is used to program CPLD through JTAG_ISP port as shown in figure (4.4).

The CPLD has 6 input busses coming from the MCU and 12 output busses to give signals to the driver and then switch the 12 transistors inside the CHBs, as shown in Figure (4.5). Table (4.1) shows the respective switching status for each level, where 1 means ON and 0 means OFF.

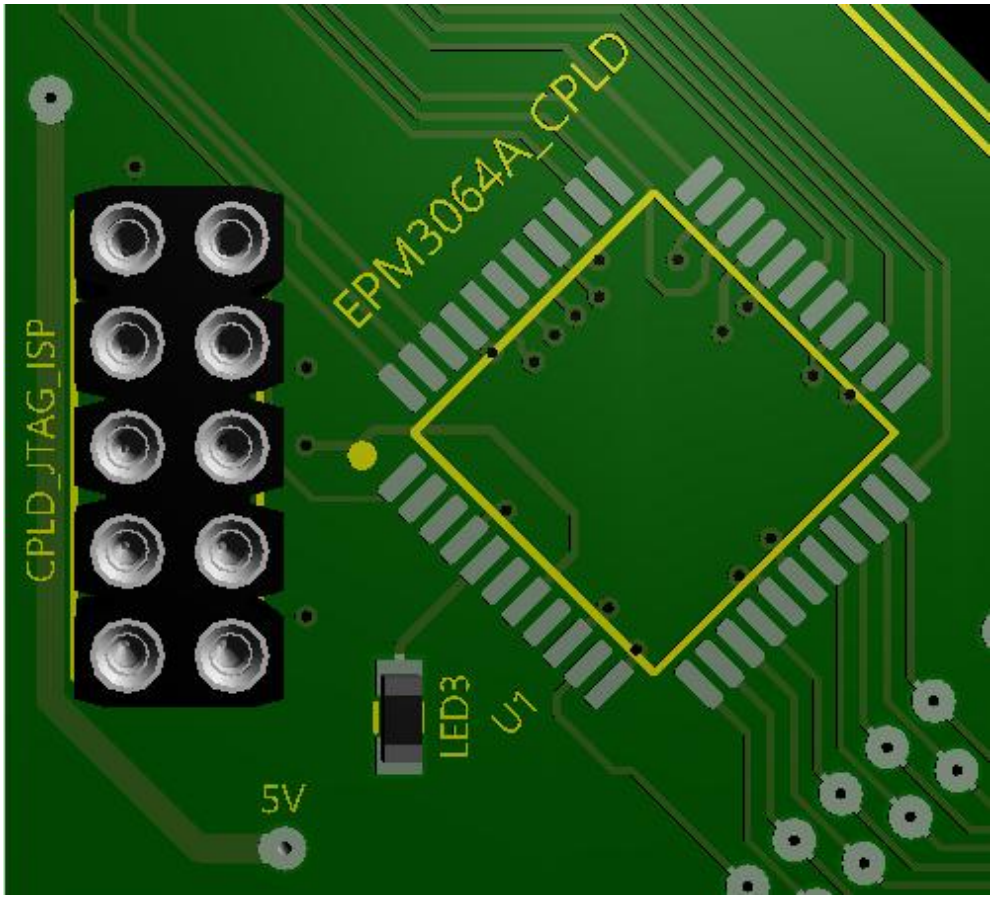

Figure 4.4 CPLD and JTAG_ISP port

27 levels can only be controlled by 5 buses, i.e., (2^5 = 32), while the sixth bus is for the duty cycle percentage of the PWM. It tells the CPLD how long to stay at the base level and how long to jump to an adjacent level to achieve the optimum output level and supress the THD.

Since the CPLD operates at 0 and 3.3 volts, while the SiC MOSFETs used in the CHBs require +18 volts to switch ON and -5 volts to switch OFF [69], a driver is needed to connect the CPLD and power the SiC MOSFETs in the HBs.

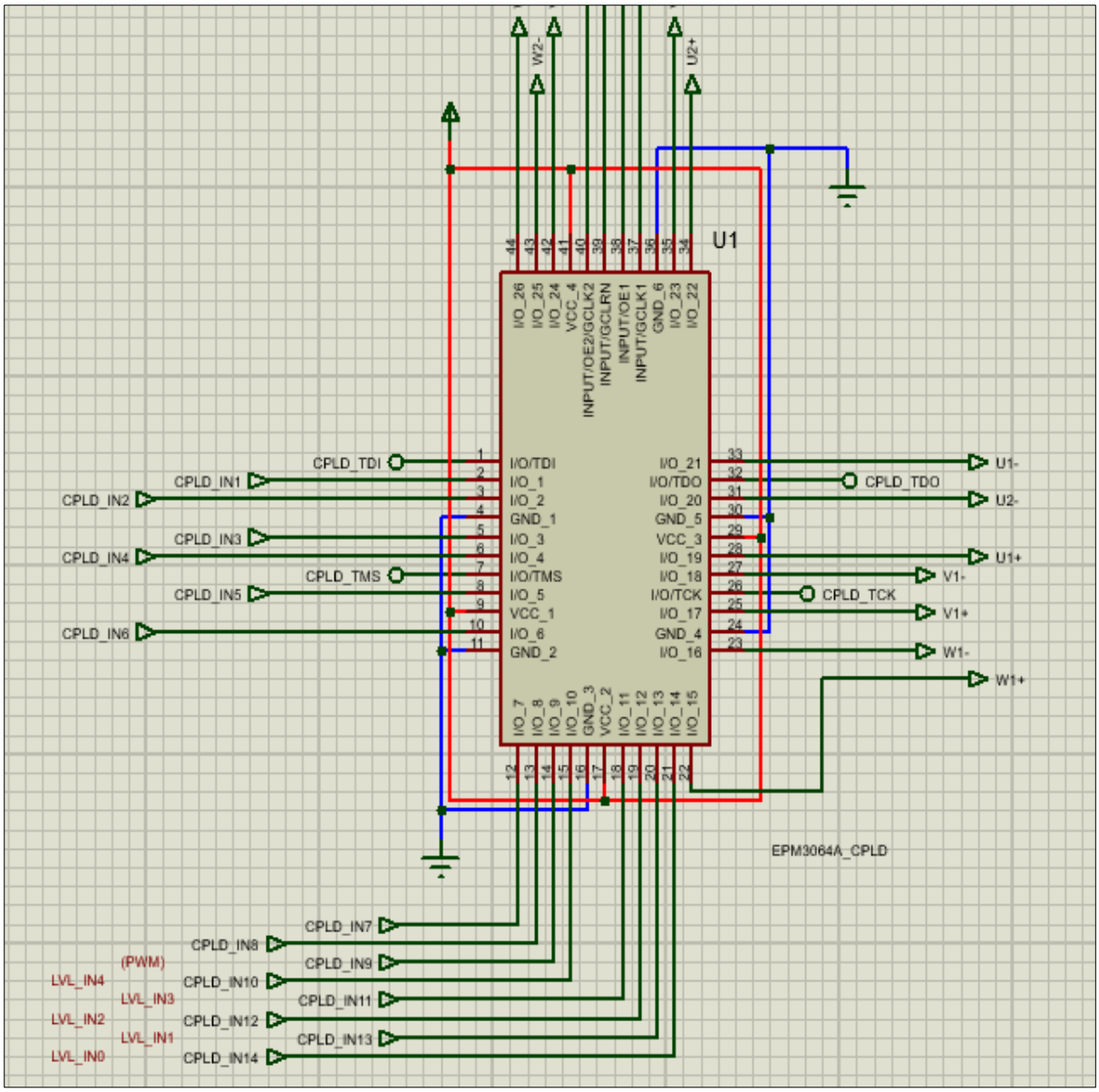

Figure 4.5 EPM3064A_CPLD IC Circuit Connections

Table 4.1 Lookup Table for the Transistors' Status for Each Level

	HB3 (9 V_{DC})				HB2 (3 V_{DC})				HB1 (1 V_{DC})			
Levels	**Q12**	**Q11**	**Q10**	**Q9**	**Q8**	**Q7**	**Q6**	**Q5**	**Q4**	**Q3**	**Q2**	**Q1**
13	0	1	0	1	0	1	0	1	0	1	0	1
12	0	1	0	1	0	1	0	1	0	1	1	1
11	0	1	0	1	0	0	1	1	1	1	0	0
10	0	1	0	1	0	0	1	1	0	1	0	1
9	0	1	0	1	0	0	1	1	0	0	1	1
8	0	0	1	1	1	1	0	0	1	1	0	0
7	0	0	1	1	1	1	0	0	0	1	0	1
6	0	0	1	1	1	1	0	0	0	0	1	1
5	0	0	1	1	0	1	0	1	1	1	0	0
4	0	0	1	1	0	1	0	1	0	1	0	1
3	0	0	1	1	0	1	0	1	0	0	1	1
2	0	0	1	1	0	0	1	1	1	1	0	0
1	0	0	1	1	0	0	1	1	0	1	0	1
0	0	0	1	1	0	0	1	1	0	0	1	1
-1	1	1	0	0	1	1	0	0	0	1	0	1
-2	1	1	0	0	1	1	0	0	0	0	1	1
-3	1	1	0	0	0	1	0	1	1	1	0	0
-4	1	1	0	0	0	1	0	1	0	1	0	1
-5	1	1	0	0	0	1	0	1	0	0	1	1
-6	1	1	0	0	0	0	1	1	1	1	0	0
-7	1	1	0	0	0	0	1	1	0	1	0	1
-8	1	1	0	0	0	0	1	1	0	0	1	1
-9	0	1	0	1	1	1	0	0	1	1	0	0
-10	0	1	0	1	1	1	0	0	0	1	0	1
-11	0	1	0	1	1	1	0	0	0	0	1	1
-12	0	1	0	1	0	1	0	1	1	1	0	0
-13	0	1	0	1	0	1	0	1	0	1	0	1

4.3 The Driver

As shown in Figure (4.1), the driver interfaces the controller with the CHBs and isolates them based on their different logic levels. The logic of the controller is 0 and 3.3 V, while the CHBs are -5 V and +18 V for zero and one, respectively. The practical implementation of the deriver involves two main steps, the first being the development of the driver itself. Second, the deriver's power supply must be designed with the appropriate voltage levels, i.e., -5 V and +18 V.

4.3.1 Driver Designing

Since the inverter has 12 switches, 12 drivers are needed. However, the drivers are divided into two groups to reduce the density of the board. As a result, two identical boards are used as drivers, each controlling 6 switches. In this design, the ***UCC21520DWR*** IC is selected, which is an Isolated Dual-Channel Gate Driver. Figure (4.6) illustrates the block diagram of the isolated driver.

The diagram shows that the two channels are completely isolated and each channel has its own power supply. The left side is for input and setting the dead time. This side is called the low voltage side because its logic levels are 0 and 3.3 V. In addition, the dead time is set by connecting a resistor to avoid time overlaps that cause interference during switching. On the other hand, a high voltage is used, i.e., VDD and VSS are connected to +18 V and -5 V, respectively. As a result, the output of this IC is connected to the gate of the semiconductor switches. Figure (4.7) shows the design of the isolated double channel with the Proteus software.

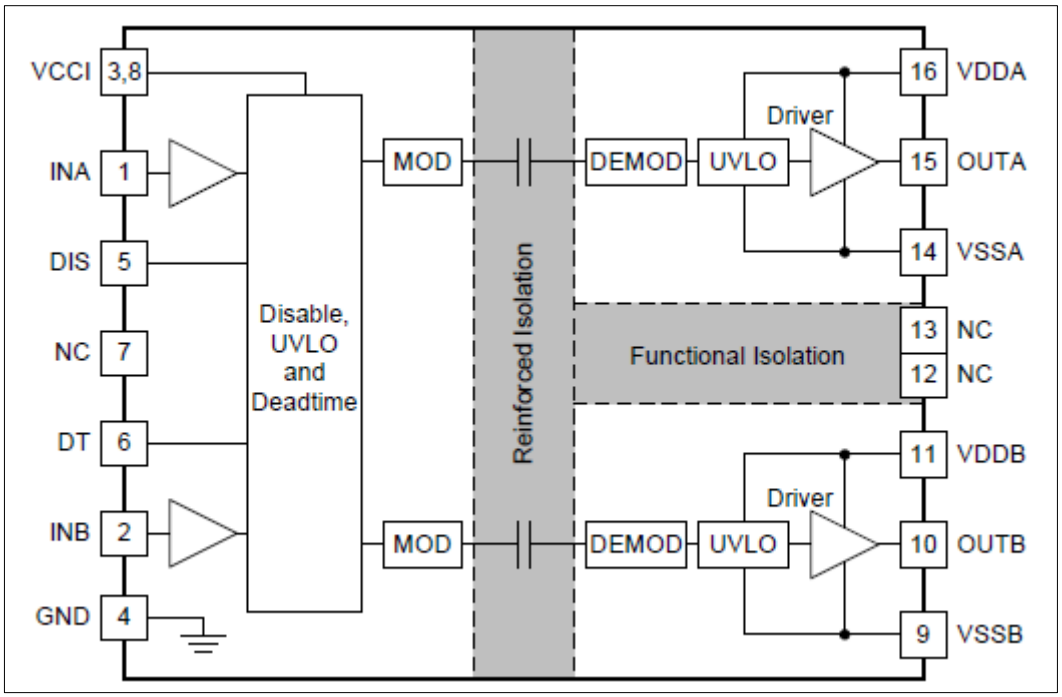

Figure 4.6 The Block Diagram of UCC21520DWR IC

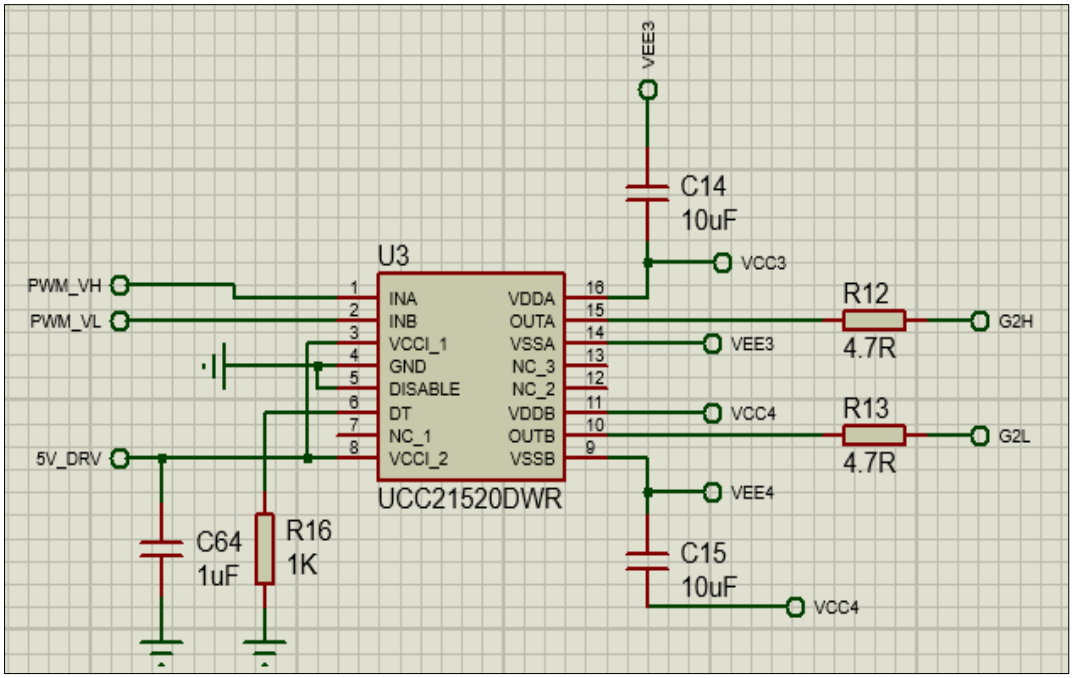

Figure 4.7 Design of the Isolated Dual Channels UCC21520DWR IC using Proteus Software

4.3.2 Driver Power Supply

As mentioned earlier, two driver broads were designed so that each board contains 6 isolated power supplies with voltages of +18 V and -5 V. This process includes three stages as shown in Figure (4.8). Half bridge driver circuit responsible for generating the appropriate frequency for the half bridge circuit. The half ridge driver IR21531S IC is selected and set to 50 kHz. The generated signal drives the half bridge circuit.

The half bridge circuit consists of two capacitors that act as voltage dividers. Since the half bridge circuit is connected to the 24-volt DC source, it generates 12 V, which is connected to the primary side of the high-frequency transformer. On the other hand, the absolute voltage difference is 23 V, i.e., (18-(-5) = 23). As a result, the transformation ratio must be 1:2. To calculate the number of turns in the primary coil (N_{PRI}), equation (4.1) is applied [65].

$$N_{PRI} = \frac{10^8 \times V_{IN}}{4 \times f_{SW} \times B_{MAX} \times A_C} \ldots\ldots\ldots\ldots \quad (4.1)$$

Where: V_{IN}: input voltage (12 V)

f_{SW}: the switching frequency i.e., 50 kHz

B_{MAX}: maximum flux density i.e., 2000 (from datasheet)

A_C: effective cross-sectional area of the core 0.8 cm^2 (from datasheet)

N_{PRI} = 3.75, since the number of turns away from any limitation such as power saturation. The primary coil consists of 5 turns, while the other 6 secondary coils consist of 10 turns. The polarity of the secondary coils is reversed so that the load is evenly distributed.

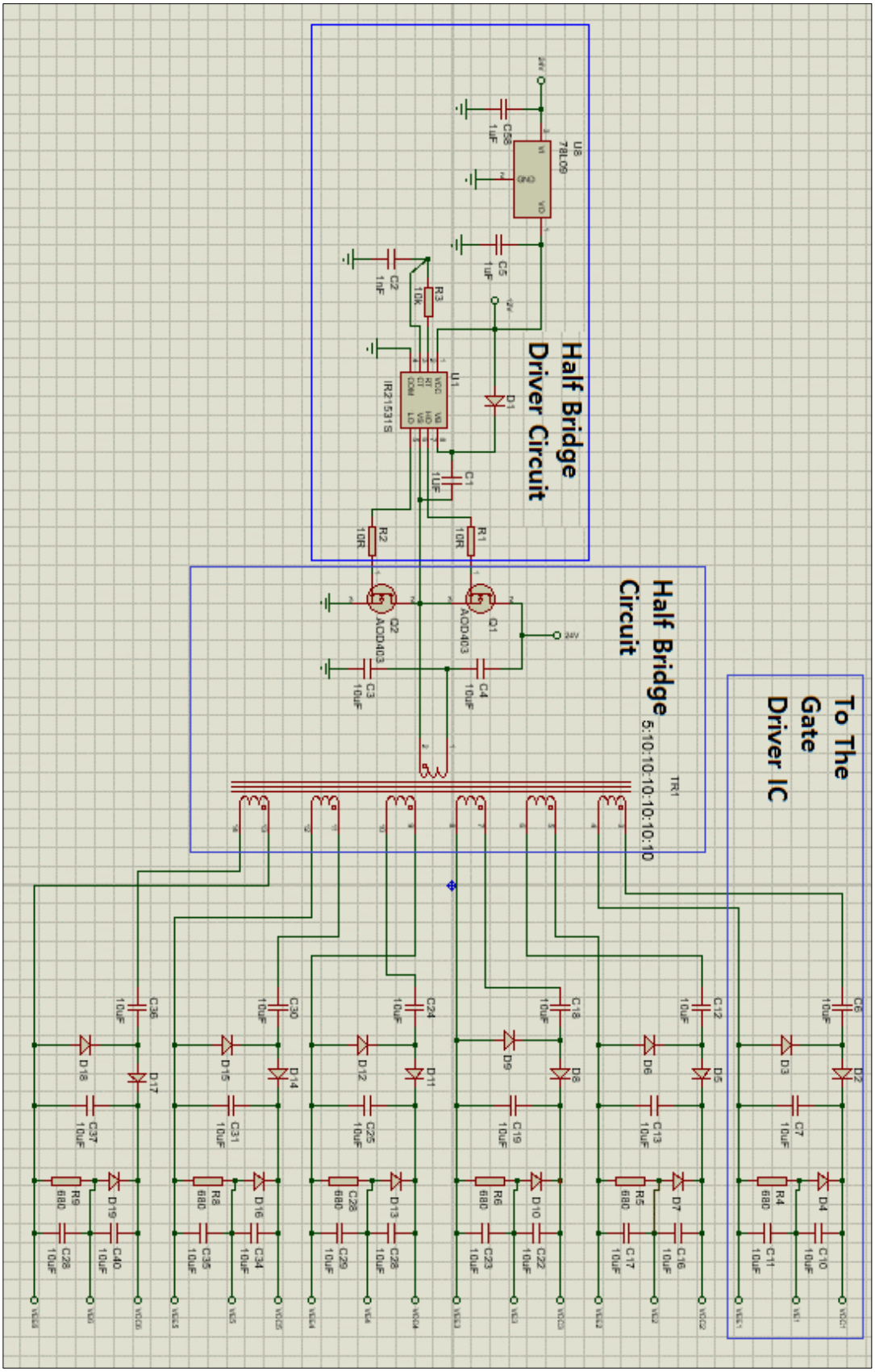

Figure 4.8 Stages of Generating +18, -5 Volt to Drive the Gate

The half bridge circuit is connected to a voltage doubler network rectifier to convert AC to DC. This circuit has three output terminals, as shown in Figure (4.8). a Zener diode is connected in series with a resistor, in addition to two voltage stability capacitors that act as voltage dividers. When the centre capacitor is connected to ground, the other two terminals represent +18 V and -5 Vs, which are used to drive the SiC-MOSFETs of the CHBs. Figure (4.9) shows the manufactured board of the driver power supply.

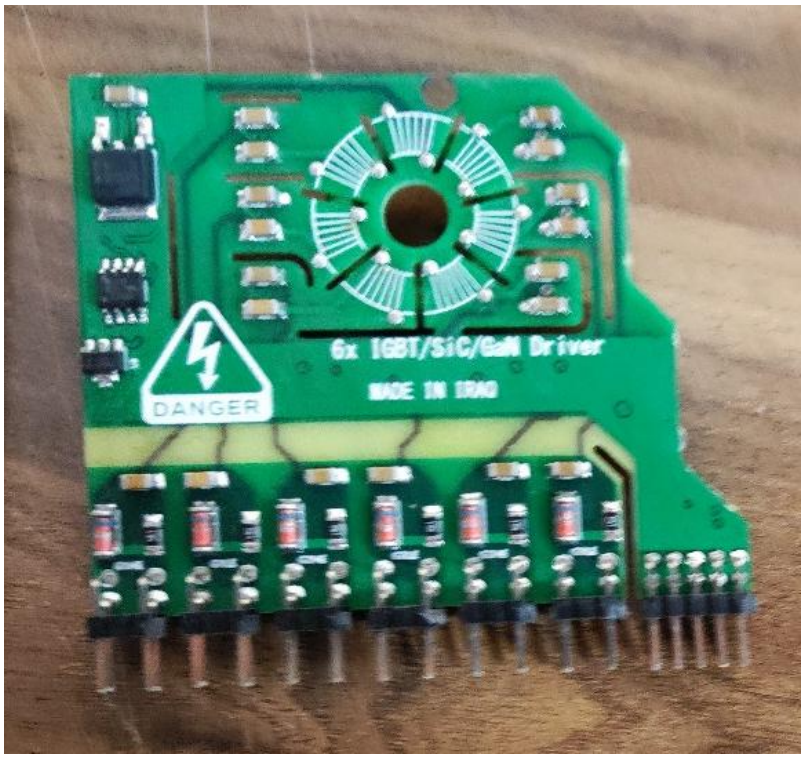

Figure 4.9 The Driver Power Supply Board

4.4 Cascaded H-Bridge Design

The theoretical background of the cascaded H-Bridge is presented in the previous sections. However, in this section, the practical implementation of the CHBs is presented and the properties of the electronic IC are used. In the hardware design of this project, SiC-MOSFETs are used instead of Si devices because they have lower losses

and switch faster [35] and [36]. In this project, the SCTW40N120G2VAG SiC-MOSFET is used as the semiconductor switch. The device has low ON-resistance in addition to high switching performance. Moreover, switching losses is almost constant regardless the junction temperature [69]. Figure (4.10) shows the actual board of the CHBs.

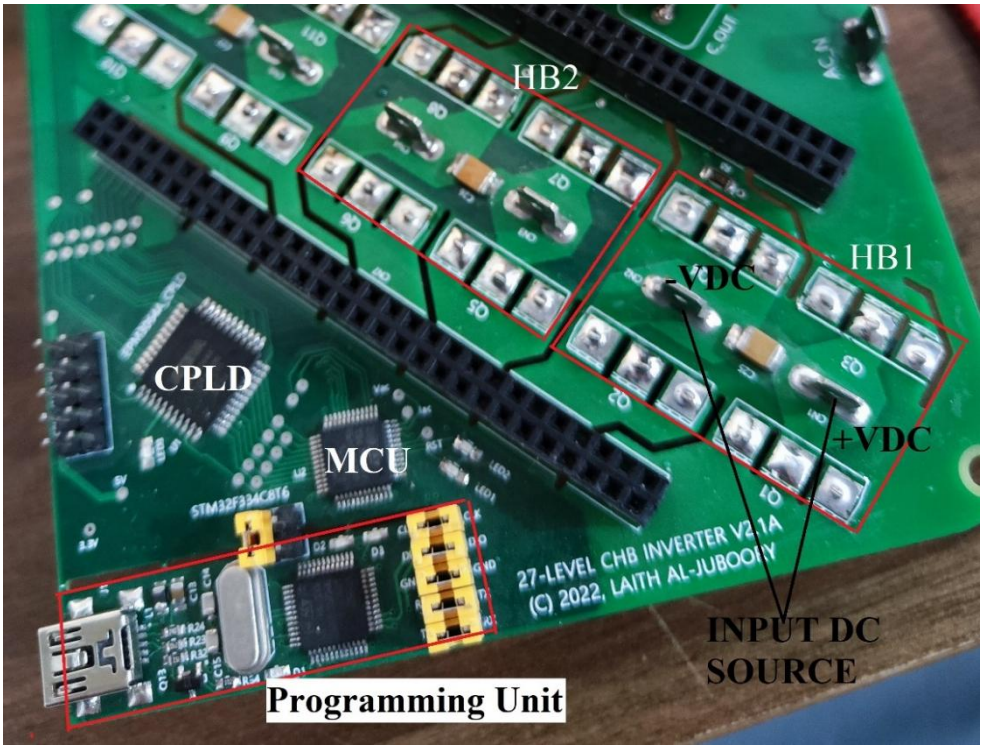

Figure 4.10 The Actual Design of the Main Board (MCU, CPLD and CHBs)

4.5 Current Measurement Circuit

For reliable inversion and to protect the circuit from overload, current measurement is set at the output. The ACS733KLATR-20AB IC is used to measure the current. This IC has four pins for current input and another four are for output. The other pins are used to set the IC, while the FAULT pin indicates whether the current has exceeded the limit. It operates at a very high bandwidth, i.e., 1 MHz [70]. Figure (4.11) illustrates the functional block diagram of the current sensor. The fault

pin is used as a breaker for the MCU when the current exceeds the limit. In addition, this sensor is able to detect the direction of the current, which is very convenient especially for grid-connected inverters. Figure (4.12) shows the schematic structure of the current sensor.

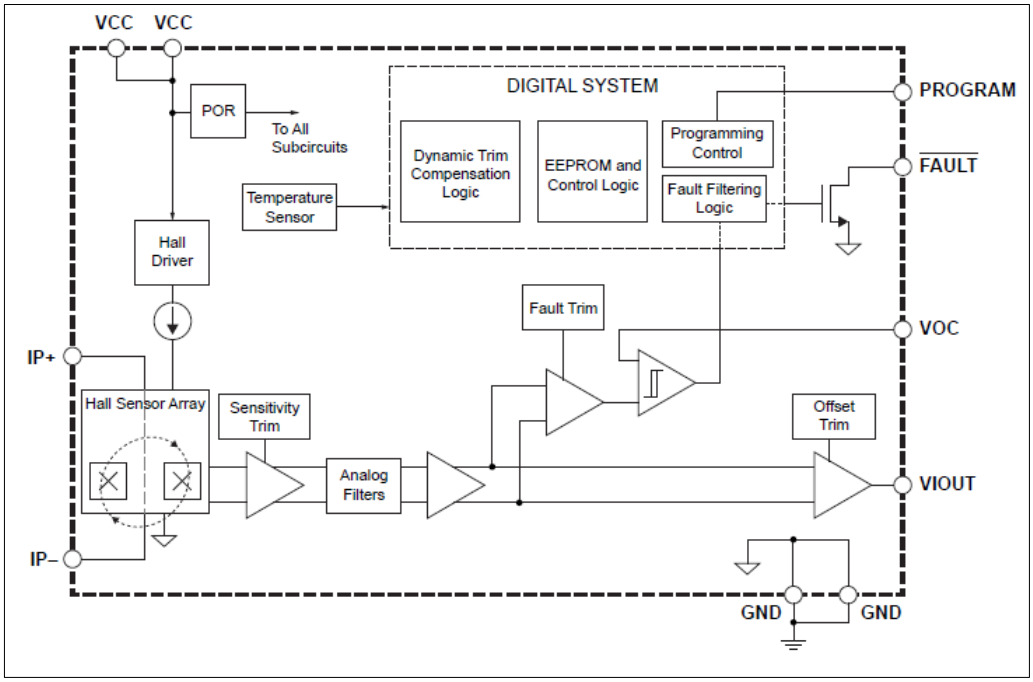

Figure 4.11 Functional Block Diagram of ACS733KLATR-20AB IC [67]

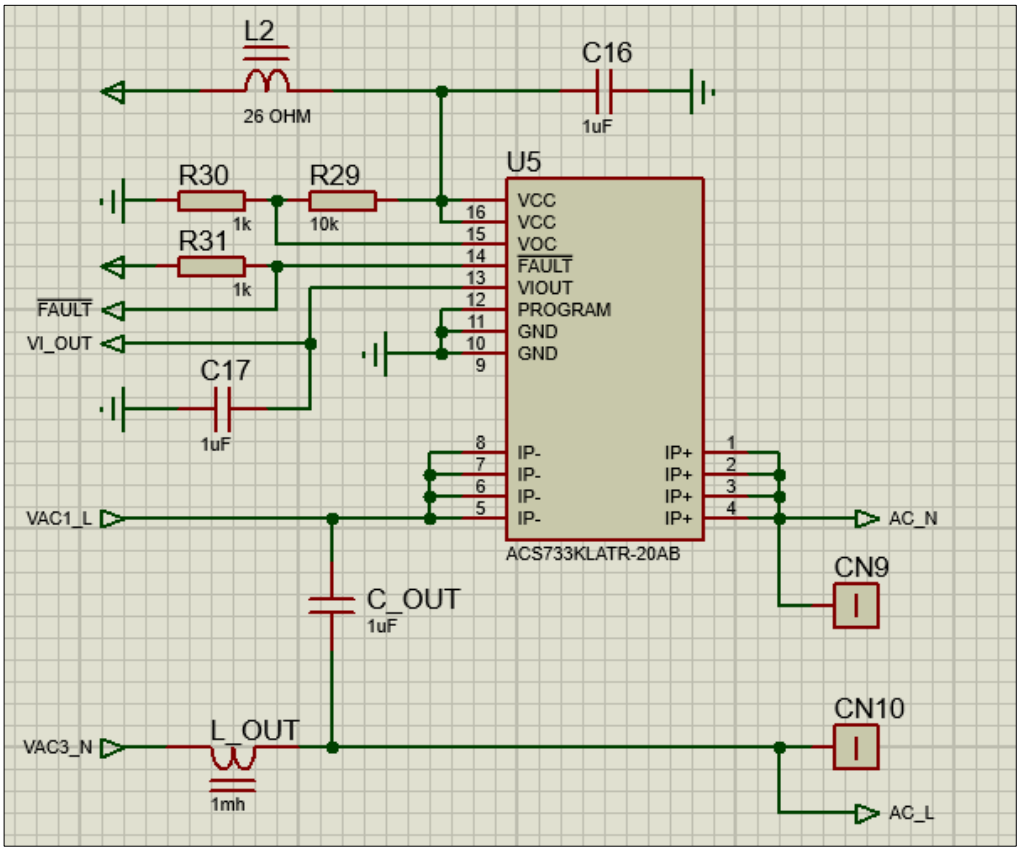

Figure 4.12 Schematic Design of the Current Measurement Circuit

4.6 DC-DC Power Supply Design

Since the chosen inverter topology requires three isolated power supplies of 1VDC, 3VDC, and 9VDC, respectively, for the three cascaded bridges, it is often impractical and difficult to find such a combination of power sources. For instance, to reproduce an AC output voltage of 230VAC, a total DC voltage of 325V is required (neglecting the effect of dead-time insertion between the top and bottom MOSFET for each inverter leg).

This means that three power supplies (25, 75, and 225 VDC) are required for such an inverter. This is a difficult obstacle to make such inverters usable in real applications. As a result, the use of a single power

source is the best solution, but it requires three isolated output stages to convert this source into three isolated sources.

The chosen solution is to design a DC-to-DC full-bridge converter with three isolated outputs, using a full-bridge MOSFET circuit in the secondary, an amorphous high frequency transformer, and three rectifiers for each of the three secondary sides, as shown in Figure (4.13).

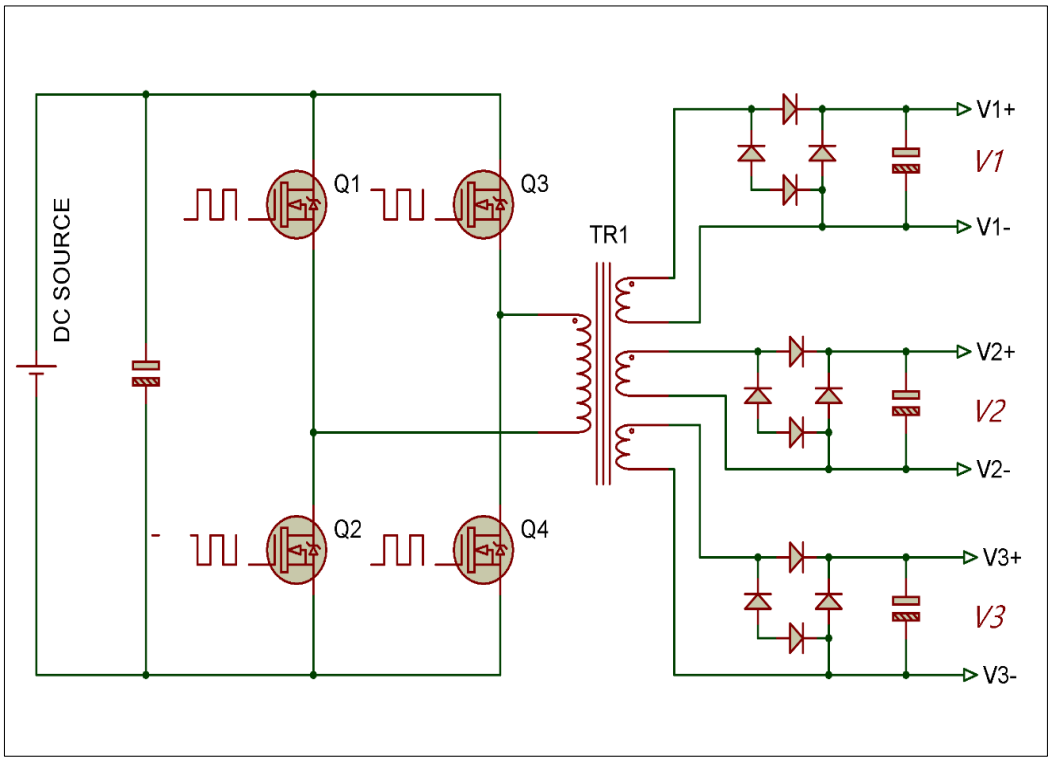

Figure 4.13 Single Source to Three Isolated Sources, 1kW DC-to-DC Converter

A low RDS(ON) MOSFET is selected, which is HY4008W (80V/200A RDS(ON) = 2.9 mΩ), to minimize heat and increase efficiency as much as possible. The high-frequency transformer was selected in toroidal shape to facilitate the winding process. The amorphous nano-crystalline cores are far superior to the conventional ferrite cores in terms of higher saturation flux density, lower magnetic losses and higher permeability and are used in this work.

The CMC040032015H nano-crystalline core was selected by Magnetics, Inc. that is suitable for the current design in terms of power range. The core has a saturation flux density of 1.25T (Tesla) (compared to a maximum of 0.2T for conventional ferrite cores). Calculation of the required number of turns requires the input DC voltage for the converter, which was selected as a $53V_{DC}$/1.5kW power supply readily available in the laboratory.

The number of turns for the primary is given by Equation (4.2) [71]:

$$N_{PRI} = \frac{10^8 V_{IN}}{4 f_{SW} B_{MAX} A_C} \quad (4.2)$$

Where:

- V_{IN}: maximum DC input voltage across the primary, which is 53V
- f_{SW}: switching frequency for the converter, 20 kHz is selected.
- B_{MAX}: maximum flux density of the core (in Gauss), 12500 G from datasheet (1 Tesla = 10,000 Gauss).
- A_C: core effective cross-sectional area, 1.2 cm^2 from datasheet.

Thus, 4.4 turns are required for the primary side of the transformer, or 5 turns after rounding up to the nearest whole number, since the number of turns cannot be a fraction. To obtain 25V at the first secondary output, the following equation is used to calculate the first secondary turn number [71]:

$$\frac{N_{PRI}}{N_{SEC}} = \frac{V_{PRI}}{V_{SEC}} \quad (4.3)$$

As a result, 3 or 4 turns are required, producing an approximate voltage of 31 V. This is quite a high voltage, since the total sum of the three voltages ($1V_1 + 3V_1 + 9V_1 = 13V = 13*31 = 403\ V_{DC}$). A simpler solution is to extend the primary winding by on more turn to 6 turns. This results in a voltage of 344 V_{DC}, which is quite acceptable. Since the primary windings can be easily controlled, the design is more tolerant of different input DC power sources.

For the second secondary coil (V2), three turns multiplied by three (V2 = 3V1) or 9 turns are required. Accordingly, 27 turns are needed for the third secondary winding.

For the gate driver circuit of the converter, the IR2110 half-bridge driver is used to drive the full-bridge MOSFET (two ICs were used). The self-oscillating IR2153S IC is used to provide two complementary PWM outputs for the IR2110 driver ICs. The complete primary side power and driver circuit is shown in Figure (4.14)

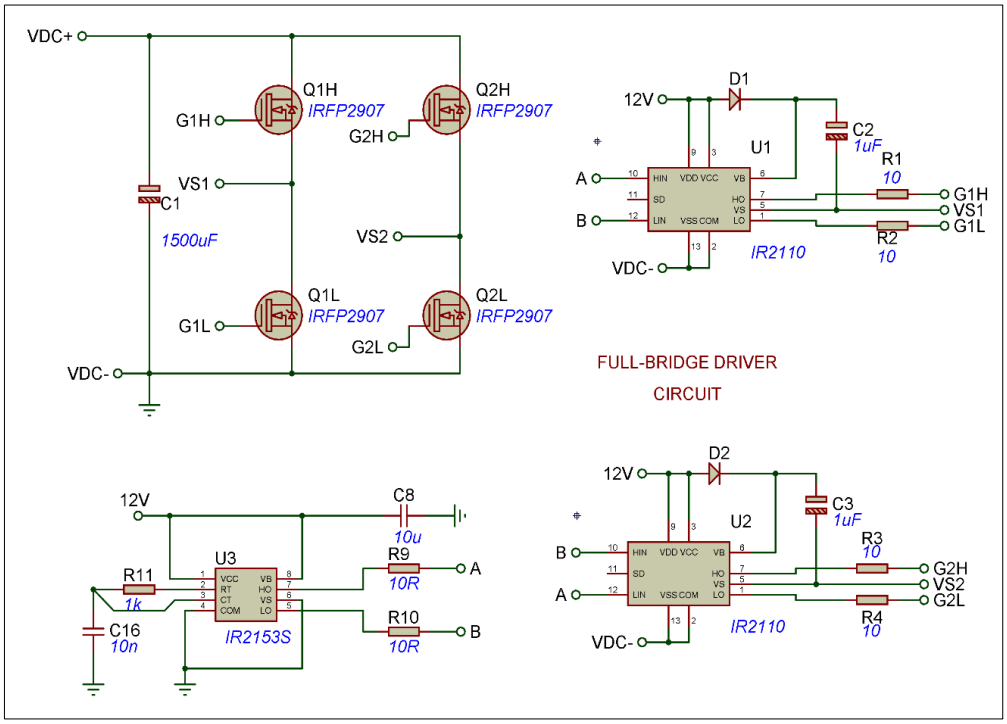

Figure 4.14 Primary Side Circuit of The DC-DC Converter

The secondary side consists of three identical bridge rectifiers that convert the high-frequency AC waveforms into pure DC voltages whose magnitude depends on the number of turns. Figure (4.15) shows the circuit of the secondary side output voltage V1:

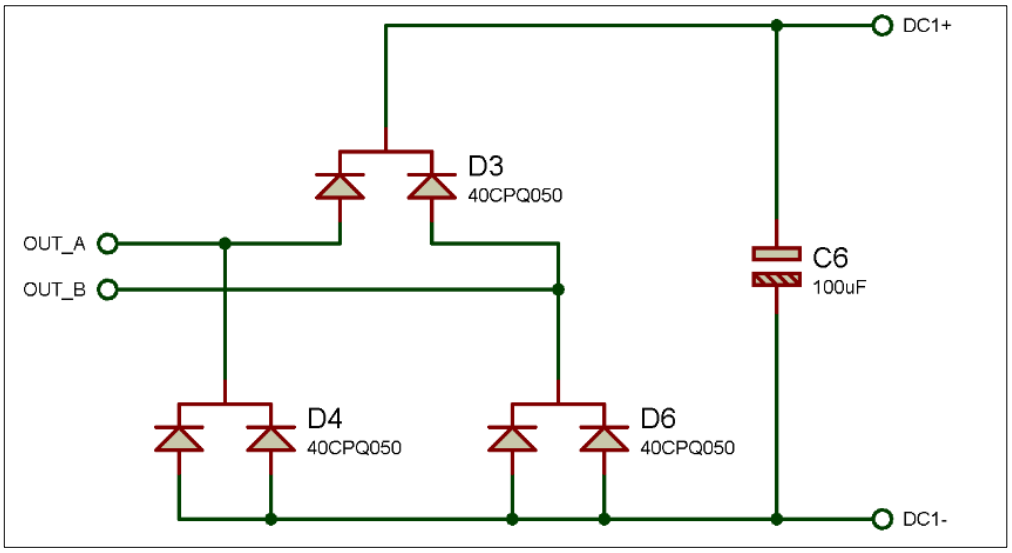

Figure 4.15 Secondary Rectifier Circuit for V1 (25VDC) Output

The PCB is then converted into a true printed circuit board by toner transfer to the copper layer and an etching solution (ferric chloride).The completely constructed DC-to-DC converter circuit is shown in Figure (4.16)

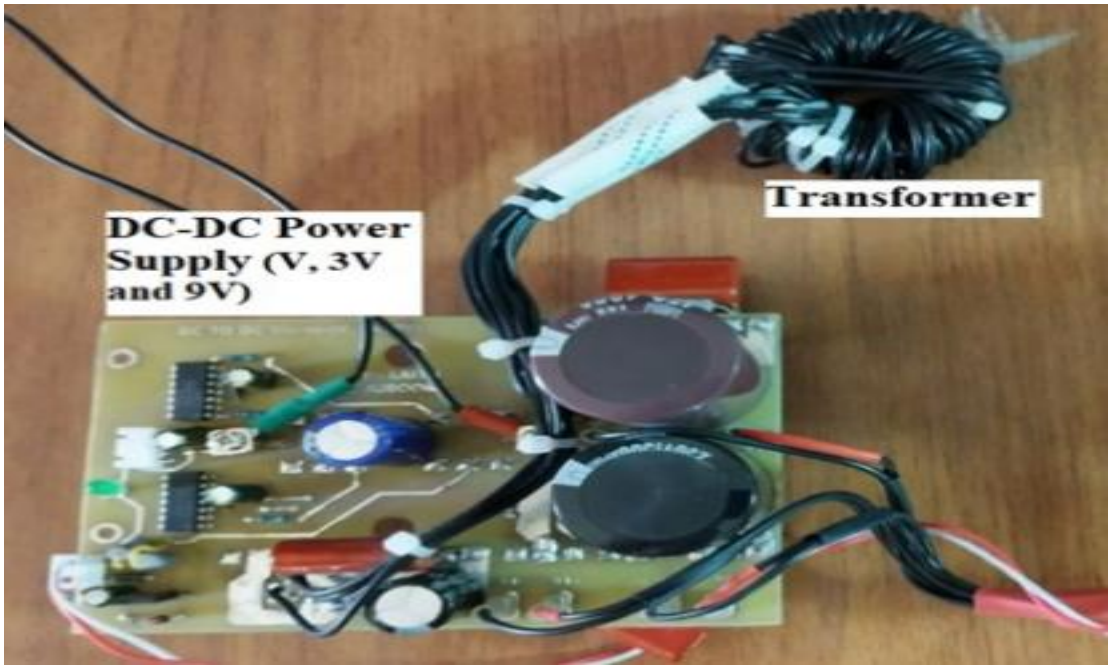

Figure 4.16 Complete DC-DC Converter Circuit

4.7 Experimental Results

Since the simulation demonstrates that two modulation methods (i.e., Nearest Level and SPWM) generate signal with low THD, the board is designed to accommodate these two methods while SHE is excluded. After assembling all the designed boards and parts, including the inverter main power supply board, the two driver daughter boards, and the isolated DC-DC power supply, the board was programmed (MCU and CPLD). The final experimental setup is shown in Figure (4.17):

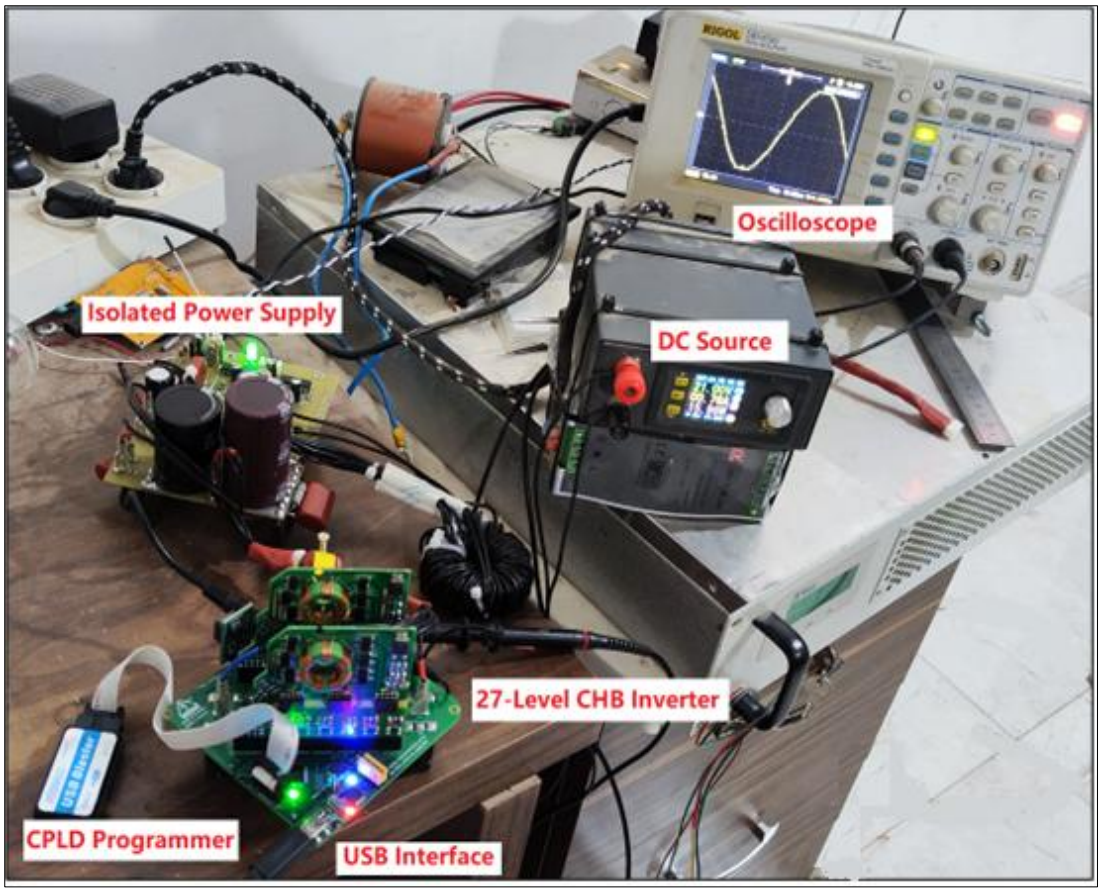

Figure 4.17 Experimental Setup

As shown in Chapter 3, the best harmonic distortion levels were obtained using nearest level modulation in combination with SPWM at each level to add the rest of the level for the reference sine wave as PWM. In this way, more accurate waveform can be obtained if a suitable LC filter is used as in this work. Two experimental tests for THD level were performed using different modulation schemes: SPWM with filter and Nearest Level without filter. In addition to the THD tests, the efficiency is calculated for different loads.

4.7.1 THD Measurement

Since the used oscilloscope does not have a function to measure THD this function is achieved using an Analog to Digital Converter (ADC) that is built into the STM32 microcontroller MCU used. The MCU samples the output voltage of the inverter at 50 KSPS (Kilo Samples Per

Second) and stores the samples in a uint16 array (Since ADC is a 12-bit array). It then sends the array to the host PC via the USB connection. The PC then receives the samples using a serial terminal program such as Tera-Term program. Finally, the ADC samples received in the terminal program are copied and pasted into the MATLAB code to calculate the THD. Figure (4.18) shows a screenshot of the program running under Windows PC, which explains how to query the output voltages of the inverter AC for analysis with MATLAB:

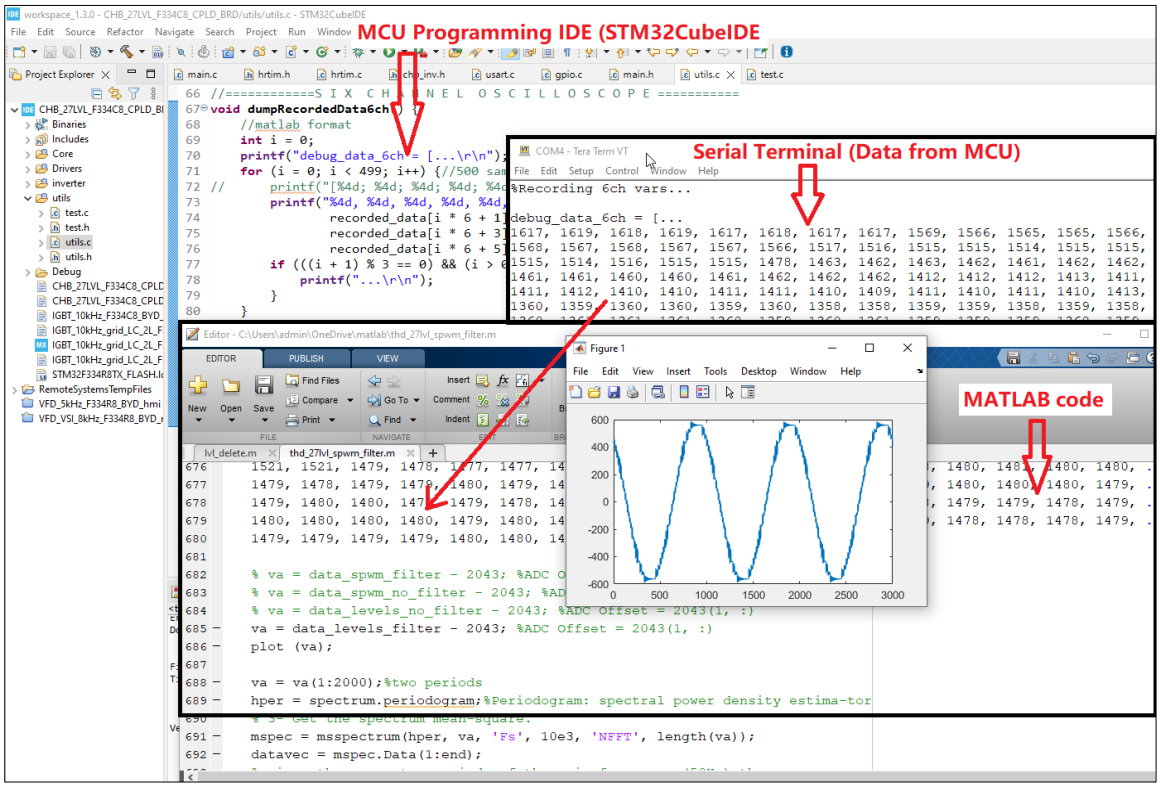

Figure 4.18 A Screenshot from the PC Showing the Process of Collecting Waveform Data Samples from the Inverter

After inserting the ADC data array into the MATLAB code editor, the following code is used to calculate the THD for each waveform:

```
va = va(1:2000);%two periods (50KSPS/ 50Hz = 1000 samples per period)
hper = spectrum.periodogram;%Periodogram: spectral power density estima-tor
% 3- Get the spectrum mean-square.
mspec = msspectrum(hper, va, 'Fs', 50e3, 'NFFT', length(va));
datavec = mspec.Data(1:end);
% since there are two periods of the main frequency (50Hz) the
% Largest spectrum is located after position 2 in the datavec array
% The other spectrum components come after that (from 4 to infinity)
% so THD = sqrt(the other harmonics sum)/sqrt(50-Hz fundamental)*100%
thd_lvls_filter =  sqrt(sum(datavec) - datavec(3))/sqrt(datavec(3))*100
```

A. Nearest Level Modulation

In this type of modulation, two scenarios were studied with respect to the output AC voltage of the inverter: before and after the LC filter. Figure (4.19) shows the scope screenshot of the waveform in this type of modulation without LC filter (before the filter):

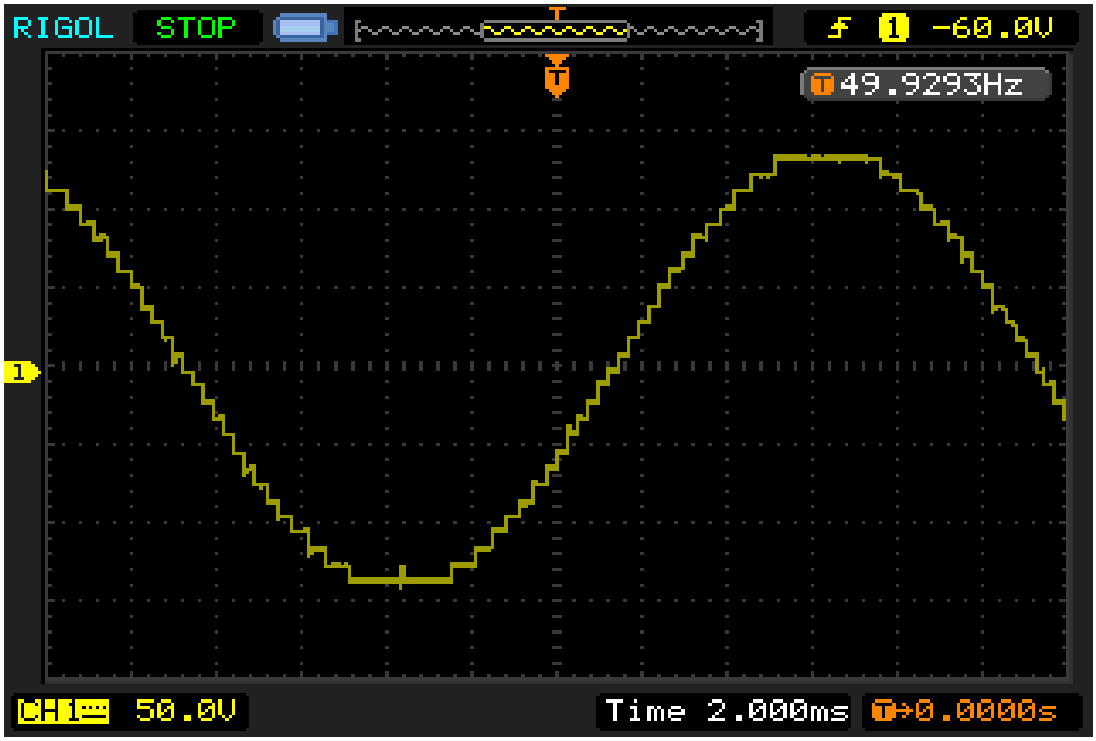

Figure 4.19 Inverter output Waveform using Nearest-level Modulation (w/o filter), Scale: 100:200kΩ Potentiometer (2×50= 100V/div)

Using the above code and technique, the THD is calculated to be 3.1135% which is just above its counterpart in the simulation results in Chapter 3 (i.e., 2.95%).

B. SPWM Modulation

In this type of modulation, the output voltage of the inverter AC is shown with the LC filter in Figure (4.20):

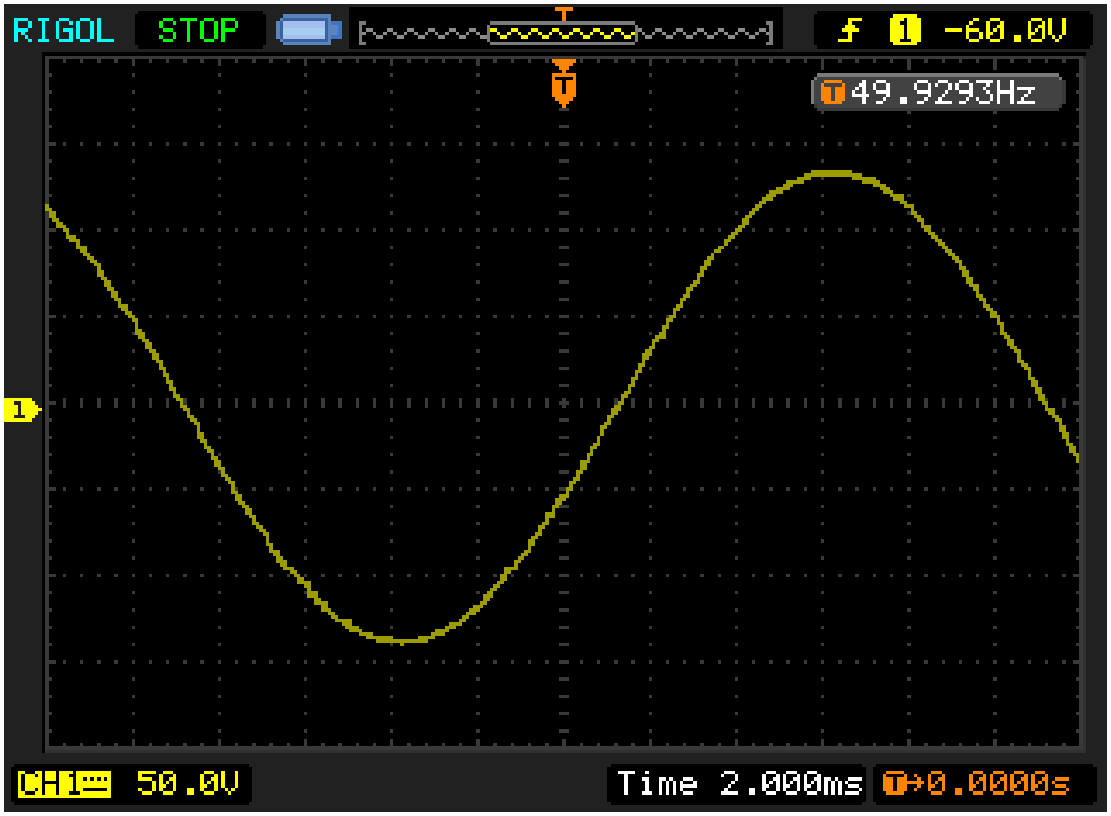

Figure 4.20 Inverter Output Waveform Using Nearest-level Modulation Combined with PWM (with LC Filter), Scale: 100:200kΩ Potentiometer (2×50= 100V/div)

The same technique explained in Figure (4.18) is used to obtain the samples from the MCU, increasing the ADC sampling frequency to handle the many details in the waveform due to the high frequency PWM (10 kHz). The sampling frequency is increased to 1000 KSPS. The THD is 0.8892% compared to 0.56% in the simulation results.

Table (4.2) shows the measured THD compared to the expected THD from the simulation results:

Table 4.2 THD Experimental Results versus Simulation

Modulation Method	Experimental THD	Simulated THD
Nearest-level without LC filter	3.1135%	2.95%
SPWM with LC filter	0.8892%	0.56%

4.7.2 Inverter Efficiency

Inverter efficiency is measured for multiple load levels using both the nearest-level and SPWM modulation methods. The efficiency is calculated by dividing the load power by the input power. The load is a variable resistance heater element whose position is changed with respect to the current carrying terminal (L) of the inverter. On the other hand, the other end is connected to the neutral (N). The maximum tested load is about 1KW. Table (4.3) lists the measurements during the efficiency test for the combined SPWM modulation method.

Table 4.3 Measurements for Different Load Steps for Efficiency Calculations in SPWM Modulation (with LC Filter)

Parameter \ Load	23.5%	48.1%	77.2%	96.5%
Output Voltage ($V_{AC(RMS)}$)	223.6	220.5	219.8	218.6
Output Current ($A_{AC(RMS)}$)	1.05	2.18	3.51	4.41
Output Power (W)	235	481	772	965
Input Voltage (V_{DC})	38.6	38.6	38.6	38.6
Input Current (A_{DC})	6.66	13.33	20.91	26.36

Input Power (W)	257.2	514.8	807.3	1017.7
Efficiency (%)	91.36	93.43	95.62	94.82

Nearest-level modulation uses a similar procedure to calculate efficiencies for the same load steps (same load but not power, as there is a slight difference between the AC output voltage for the two modulation strategies, as the AC voltage tends to have a lower RMS value for nearest-level modulation, as shown in Table (4.3) and Table (4.4). Table (4.4) illustrates these measurements:

Table 4.4 Measurements for Different Load steps for Efficiency Calculations using Nearest-level Modulation (without LC Filter)

Load / Paramet	22.78%	47.40%	75.38%	94.83%
Output Voltage ($V_{AC(RMS)}$)	220.15	218.9	217.2	216.7
Output Current ($A_{AC(RMS)}$)	1.035	2.165	3.471	4.37
Output Power (W)	228	474	754	948
Input Voltage (V_{DC})	38.6	38.6	38.6	38.6
Input Current (A_{DC})	6.45	13.12	20.32	25.75
Input Power (W)	249.2	506.6	784.4	994.3
Efficiency (%)	91.43	93.57	96.11	95.37

As shown in Table (4.3) and (4.4), the efficiency of the nearest-level modulation is slightly better than that of the SPWM modulation method because the latter includes a high frequency PWM in the switching devices (SiC MOSFETs), which increases the switching losses of the transistors and thus reduces the overall efficiency of the system. In contrast, in nearest-level modulation, the transistors switch on or off only in response to the level change, which is 54 times per AC cycle in the worst-case scenario (the lower H-bridge consisting of Q1-Q4 is the fastest bridge) while in the SPWM method each AC cycle contains 200 switching states (10kHz/50Hz), resulting in larger switching losses.

Figure (4.21) shows the efficiency curve for several load levels for the two selected modulation methods.

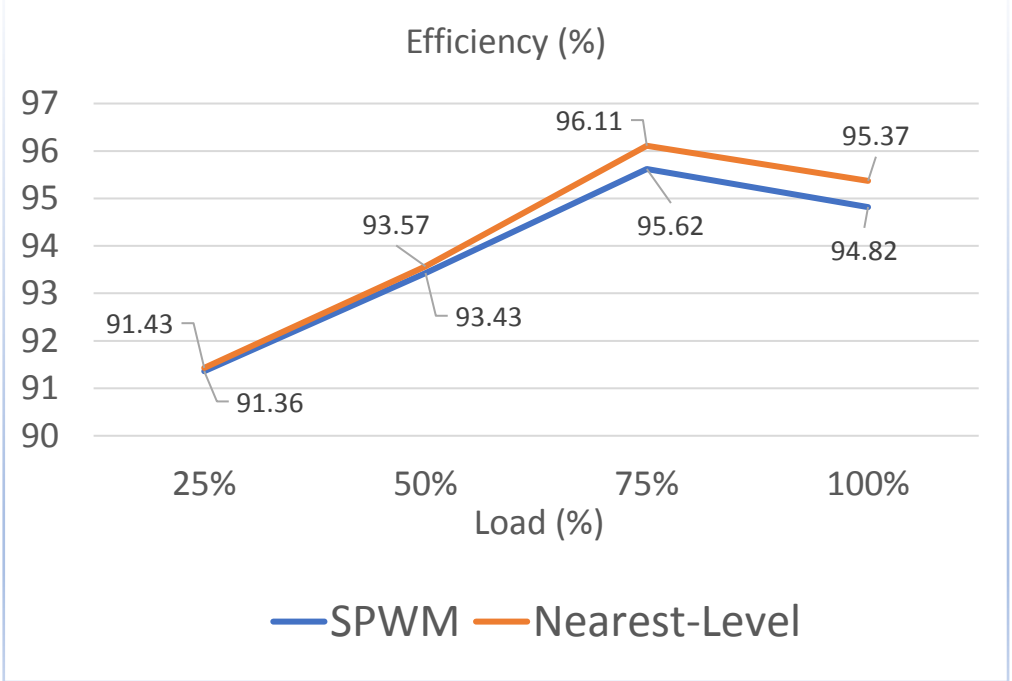

Figure 4.21 Efficiency over Multiple Load Steps for SWPM and Nearest-level Modulation Methods.

CHAPTER FIVE

CONCLUSIONS AND FUTURE WORKS

5.1 Introduction

From the simulation results, it was found that traditional nearest-level modulation in cascaded H-bridge inverters has better THD than SHE in single-phase inverters, despite its relative simplicity in level determination.

This method adds a PWM to each specific level to switch between the current and next level with a duty cycle which depends on the difference between the reference sine wave and the current level.

This AC output waveform from the inverter is then fed to a LC filter to remove the PWM higher frequency components, yielding a near-perfect sinusoidal waveform that is far better than the conventional nearest-level waveform.

From a hardware perspective, the use of the advanced 32-bit STM32 microcontroller greatly improved the overall design of the system by leveraging its high-resolution PWM timers, fast 10-bit ADC, and high-speed CPU to produce error-free PWM signals in addition to accurate voltage and current measurements.

The using of CPLD has significantly reduced the high computational cost of the MCU by multiplexing PWM signals at the level set by the MCU and outputting the correct signals to gate-driver circuits.

Using the CPLD, the MCU was freed from the simultaneous combination of PWM and signal levels, which requires the use of 12

PWM timers (one PWM timer per transistor), by programming the CPLD for this task. This solution allowed simplifying the role of the MCU, which generates a PWM signal whose width is directly proportional to the difference between the reference sinusoidal signal and the amplitude of the current level. The MCU also generates the required level, which is output in binary form through its General-Purpose Input/Output (GPIO) in addition to the measurements of AC voltage and current. Finally, the MCU is responsible for communicating with the host PC to transmit the sampled voltage waveforms.

The use of SiC-MOSFETs has also contributed to the stability, performance, and efficiency of the overall system to their low switching and conduction losses and high-speed switching capability compared to conventional silicon-based IGBTs and MOSFETs.

5.2 Future Works and Recommendations

This design of this inverter has shown a promising result, the generated signal has very low THD. In addition, its efficiency exceeds 95% nearby the full load. Moreover, the output voltage has neglectable voltage drop between the no load and full load.

Therefore, such achievement could be used for future work as below:

1 - This inverter could be integrated with MPPT solar array and used in solar energy harvesting.

2 - Developing the existing board to be connectable with other boards with self-synchronization for load sharing.

3 - Reduce the number switches while maintain the number of levels or increase them.

4 - Design and applying different modulation methods to then achieve better performance.

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الخلاصة

أصبح تحويل التيار المستمر إلى التيار المتناوب موضوعًا مثيرًا للاهتمام نتيجة استخدام موارد الطاقة المتجددة بشكل متزايد واستثمارها كمصدر تنافسي للطاقة مقارنة بالموارد التقليدية. يقدم هذا البحث منهجيات فعالة لتحويل جهد التيار المستمر إلى تيار متناوب حيث إن الهدف الرئيسي هو تصميم عاكس عالي الكفاءة يولد إشارة تيار متردد جيبية نقية قليلة التشوه قدر الإمكان. لذلك، تم تصميم ومحاكاة العاكس المتتالي ذو 27 مستوى بواسطة برنامج محاكاة الماتلاب. يشتمل التصميم العاكس على ثلاثة مراحل من العاكسات على شكل حرف Hمربوطة على التوالي، كل مرحلة من هذه المراحل متصلة بمصدر جهد تيار مستمر منفصل. وبالتالي، هناك حاجة إلى ثلاثة مصادر جهد مستمر مختلفة الجهد قيمتها تحقق النسبة 1: 3: 9 للحصول على 27 مستوى يتراوح من سالب 13 إلى موجب 13.

تم ايضا دراسة العديد من طرق السيطرة على الترانسستورات لإجل توليد الجهد المتناوب والتي يمكن تطبيقها على النوع المذكور أعلاه من المحولات، على سبيل المثال، التوافقيات الانتقائية، والمستوى الأقرب، وتضمين عرض الموجة . تكشف نتائج محاكاة طرق التعديل الثلاثة أن طريقة المستوى الأقرب تحتوي على أقل مستوى تشوه في الموجة عند 2.95 بالمائة عندما لا يتم تطبيق أي فلتر.، بينما حققت طريقة تضمين عرض الموجة أدنى نسبة تشوه كلي بمقدار 0.56 بالمائة عند استخدام الفلتر. نتائج المحاكاة ساهمت في تحديد أفضل التقنيات لتصميم العاكس المناسب لهذه التقنيات.

يتكون تصميم العاكس من عدة مراحل، الأولى وحدة التحكم الصغيرة القابلة للبرمجة MCUحيث يتم استخدام جهاز منطق قابل للبرمجة المعقدة CPLD كجدول بحث لتقليل مهام MCUوبالتالي تقليل الكود البرمجي. المرحلة الثانية دائرة عزل ضوئي لعزل وحدة MCU التي تعمل بجهد منخفض عن العاكس والتي تحتاج إلى جهد عالي. نظرًا لأن دائرة العزل الضوئي تتطلب مصدري جهد منفصلين، تم تصميم مصدر طاقة منفصل لتزويد دائرة العزل. تتضمن مرحلة العاكس من ثلاث عاكسات متصلة لتبديل قطبية مصدر التيار المستمر الخاص بكل وحدة وبالتالي بناء شكل موجة التيار المتناوب. كل وحدة عاكس تتكون من أربعة مفاتيح الكترونية. نظرًا لأن الترانزستورات المصنعة من مادة السيليكون كارباید تتميز بمقاومة عالية للإدخال وتعمل بترددات عالية، فإنه يتم استخدامه كمفتاح. بالإضافة إلى ذلك، يتم استخدام المرشح لتنعيم الإشارة المولدة وبالتالي تقليل التشوه في الإشارة المتولدة. الإشارات الناتجة عن العاكس العملي لها نفس النسبة المئوية للتشوهات مقارنة بنظيراتها التي نتجت بالمحاكاة. تم

اختبار العاكس مع مختلف الأحمال لاختبار الكفاءة. لوحظ تغير بالكفاءة ومع ذلك، فقد حافظت الكفاءة على قيمتها أعلى من 90٪.

جـامعـة نينوى

كلية هندسة الالكترونيات

قسم الإلكترونيك

دراسة مقارنة لطرق السيطرة على عاكس متعدد المستويات باستخدام اقل عدد من المفاتيح

ليث سعدي سلمان احمد الفاضل

رسالة ماجستير في هندسة الإلكترونيك

بإشراف

الدكتور حارث أحمد محمد البدراني

1444 هـ

2022 م

دراسة مقارنة لطرق السيطرة على عاكس متعدد المستويات باستخدام اقل عدد من المفاتيح

رسالة تقدم بها

ليث سعدي سلمان احمد الفاضل

إلى

مجلس كلية هندسة الالكترونيات –جامعة نينوى

وهي جزء من متطلبات نيل شهادة الماجستير

علوم في هندسة الالكترونيك

بإشراف

الدكتور حارث أحمد محمد البدراني

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