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Performance Analysis of Fractional N PLL Frequency Synthesizer Operating at 2.4 GHz

Noor Zaid Naktal Kashmola

M.Sc. Thesis

In

Electronics Engineering

Supervised by

Prof. Dr. Khalid Khaleel Mohammed

Asst. Prof. Dr. Aws Zuheer Yonis Alashqar

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Performance Analysis of Fractional N PLL Frequency Synthesizer Operating at 2.4 GHz

A Thesis Submitted

By

Noor Zaid Naktal Kashmola

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Supervised by

Prof. Dr. Khalid Khaleel Mohammed

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سورة الأنعام

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صَدَقَ اللهُ العَظِيمُ

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We certify that the dissertation entitled (**Performance Analysis of Fractional N PLL Frequency Synthesizer Operating at 2.4 GHz**) was prepared by **Noor Zaid Naktal** under our supervision at the Department of Electronic Engineering, Ninevah University, as a partial requirement for the Master of Science Degree in Electronic Engineering.

Signature:

Name: Prof. Dr. Khalid Khaleel Mohammed

Date: / /2022

Signature:

Name: Asst. Prof. Dr. Aws Zuheer Yonis Alashqar

Date: / /2022

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I certify that the linguistic reviewing of this dissertation was carried out by me and it is accepted linguistically and in expression.

Signature:

Name: Asst. Lecturer Ameen Abdulrhman Dhiaa

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I certify that this dissertation was carried out in the Department of Electronic Engineering. I nominate it to be forwarded to discussion.

Signature:

Name: Assist. Prof. Dr. Ahmad T. Younis

Date: / /2022

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According to the recommendations presented by the supervisors of this dissertation and the linguistic reviewer, I nominate this dissertation to be forwarded to discussion.

Signature:

Name: Assist. Prof. Dr. Ahmad T. Younis

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We the examining committee, certify that we have read this dissertation entitled (**Performance Analysis of Fractional N PLL Frequency Synthesizer Operating at 2.4 GHz**) and have examined the postgraduate student (**Noor Zaid Naktal**) in its contents and that in our opinion; it meets the standards of a dissertation for the degree of Master of Science in Electronic Engineering.

Signature:

Name: Assist. Prof. Dr. Mujahid Fahmy Ibrahim
Head of committee
Date: / /2022

Signature:

Name: Assist. Prof. Dr. Mohamed Tariq Yassin
Member
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Name: Lecturer. Dr. Ahmed Mohamed Salama
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Signature:

Name: Prof. Dr. Khalid Khaleel Mohammed
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Date: / /2022

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Name: Asst. Prof. Dr. Aws Zuheer Yonis Alashqar
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Date: / /2022

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Dean of the College

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Council registrar

Date: / /2022

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Researcher

Noor Zaid Naktal kashmola

ABSTRACT

Fractional-N PLL frequency synthesizers are widely used in the field of communications such as mobile phones, satellites, and radio devices because it generates a large Bandwidth with fine frequency resolution at very high reference frequency, fast switching between channels, minimum of phase noise and spurs noise for various electronic applications.

So, the work was done in this thesis on designing a Fractional-N PLL circuit with specifications, which makes it able to be used in the field of Bluetooth application according to the specific parameters of the Bluetooth system. MATLAB program and ADS program were used to design and simulate a low pass filter and a Σ-Δ modulator due to the importance of these two parameters in improving the noise performance of the frequency synthesizer circuits. Passive loop filter was designed due to its easer of construction and making the frequency synthesizer circuit more stable, where the filter is designed with 2^{nd} ,3^{rd} and 4^{th} order. Also the single loop sigma-delta modulation is designed with 1^{st} ,2^{nd}, and 3^{rd} order. Thus, there are three circuits design for the frequency synthesizers circuit (Fractional N-PLL with a 2^{nd} order loop filter and 1st order Σ-Δ modulator, Fractional N-PLL with a 3^{rd} order loop filter and 2^{nd} order Σ-Δ modulator, and Fractional N-PLL with a 4^{th} order loop filter and 3^{rd} order Σ-Δ modulator), at frequency bandwidth of 75, 125,250-kHz and for each value of the phase margin (47 ,57) degree.

The results indicate that the second proposed frequency synthesizer give better performance of producing high output signal and pure from any spurs noise, with acceptable value of phase noise that equal to -156.061 dBc/Hz at 2 MHz frequency offset and -163.555 dBc /Hz at 3 MHz frequency offset, with better settling time 7.719 μsec.

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TABLE OF SYMBOLS

Symbol	Name
Ai	loop filter coefficient ith:0,1,2,3
G(S)	Close loop transfer function
I_1	Charge current of charge pump
I_2	Discharge current of charge pump
I_{net}	Charge pump total current
K_{VCO}	VCO gain
$K_{ø}$	Charge pump gain
N	Division ratio
O(s)	Open loop transfer function
T1,T2,T4	Loop filter pole
T2	The loop filter zero
T31	Ratio of pole T3 to pole T1
T43	Ratio of pole T4 to pole T3
T(s)	The loop filter Transfer function

Tol	Tolerance
$T.f$	Transfer Function
V_{tune}	VCO input voltage
V_{out}	Loop filter output voltage
ω_c	Carrier frequency
ω_S	Spurs noise frequency
ω_{int}	Interference frequency
ω_{IF}	Information signal frequency
$\emptyset$	Phase margin
$\emptyset_{vco}$	VCO output Phase
$\Delta\emptyset$	Phase detector output signal
θ_e	Phase error
θ_i	Input phase
$\propto$	Fractional part for the division ratio
β	Delta sigma modulator input signal
ζ	Damping factor

γ	Gamma Optimization Parameter

TABLE OF ABBREVIATIONS

Abbreviation	Name
ADC	Analogue To Digital Converter
ADS	Advanced Design System
BW	Bandwidth
CMOS	Complementary Metal Oxide Semiconductor
CP	Charge Pump
DDS	Direct Digital Synthesis
DFF	D-Flip Flop
DDFS	Direct Digital Frequency Synthesizer
DAC	Digital To Analog Converter
F_{ref}	Input reference frequency
F_{FR}	Free running frequency

F_{out}	Output frequency
F_{vco}	VCO output frequency
FIR	Finite Impulse Response
Δ f	Frequency offset
FPGA	Field Programmable Gate Array
GSM	Global System For Mobile
IIR	infinite impulse response
LPF	Low Pass Filter
LFSR	Linear Feedback Shift register
LNA	Low Noise Amplifier
MASH	Multi Stage noise Shaping
NTF	Noise Transfer Function
OSR	Over Sampling Ratio
PM	Phase Margin
PN	Phase Noise
PA	Power Amplifier

PSD	Power Spectral Density
PFD	Phase Frequency Detector
RBW	Resolution Bandwidth
SNR	Signal To Noise Ratio
SSPLL	sub-sampling PLL
VCO	Voltage Control Oscillator
WIMAX	Worldwide Interoperability for Microwave Access
Σ-Δ	Sigma-Delta

CHAPTER ONE

Introduction and Previous Researches

1.1 Introduction

Wireless communications have become an essential and important part of the modern era where several innovations in telecommunications have emerged rapidly during the last half of the twentieth century [1].

For example, social communication between countries and continents around the world has become easily available at low cost and with high accuracy. Wireless communication is not limited to communication between people only but the possibility of sending large-sized information over vast distances through the use of satellites and the transmission of voice video, and other types of data [2]. Despite the existence of a large number of wireless communication technologies but the Wi-Fi network remains the most important and most common in use where this network operates on globally defined and internationally agreed frequencies which are (2.4,3.6,5-GHz) [3]. The main device in any wireless communication system is Transceiver (transmitter and receiver fusion). One of the most important components in the transceiver are their local oscillator [4], in general local oscillators with a single reference frequency are called frequency tuning devices figure (1-1) [5].

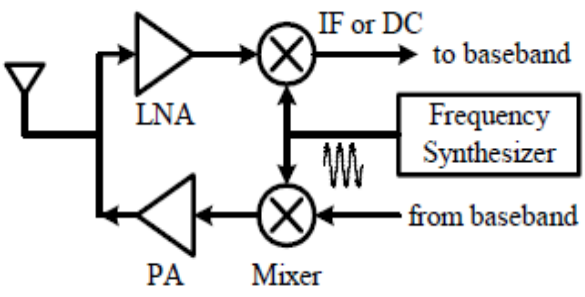


Figure 1-1: Frequency synthesizer in transceiver circuit [5].

There are several frequency tuning techniques, the most important of which is a phase-locked loop (PLL) which is a frequency synthesis device based on a single reference frequency used to generate multiple output frequencies covering several channels in multiple bands. Figure (1-2) [6] show the basic phase-locked loop circuit.

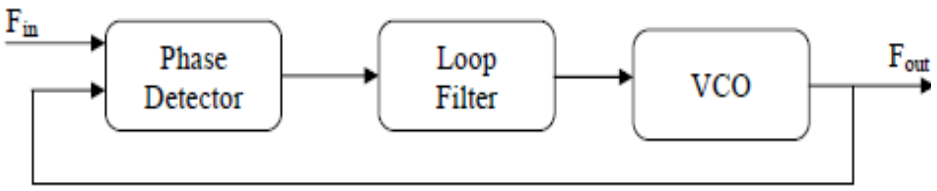


Figure 1-2: Block diagram of PLL [6]

PLL based frequency synthesizers are capable of providing high-frequency outputs with stability the same as a low reference frequency. For example, when the reference frequency of the frequency synthesizer based on PLL is equal to 40 MHz, the output frequencies band that this frequency will generate with range between 2.3 to 2.95 GHz and 4.77 to 5.9 GHz. This wide range of frequencies covers all channel devices within two bands 2.4 GHz and 5.9 GHz [3], as in the Bluetooth system based on the frequency 2.4 GHz, this system can provide a short rang remote connection between communication devises system. It consists of 79 frequency channels separated by a frequency distance of 1 MHz and a frequency range between 2402 to 2480 MHz .Figure (1-3) shows the distribution of the frequency bands in Bluetooth systems [7].

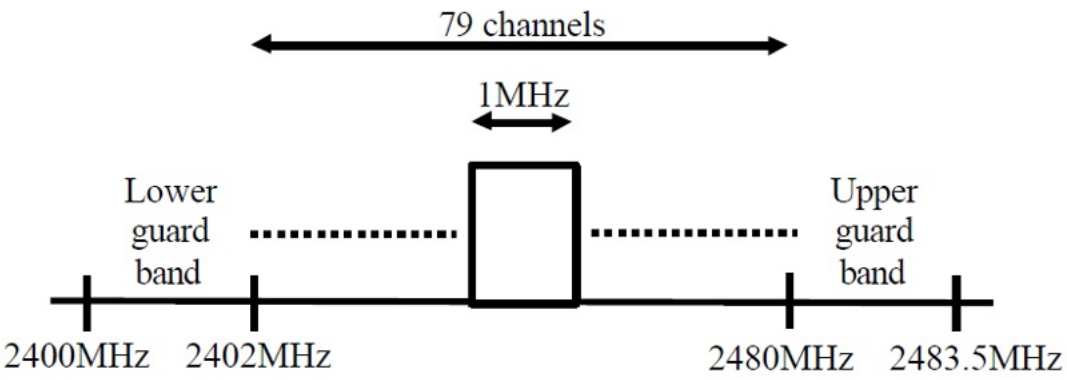


Figure 1-3: The frequency bands in Bluetooth systems [7].

Equation (1-1) calculate the central frequency of the frequency channels [7]:

$$f_{\text{channel}} = 2402 + (A - 1) \quad \text{MHz} \tag{1-1}$$

where:

A= the number of channel which is selected.

1.2 Aims of Thesis

1- Recognizing the importance of utilizing a PLL circuit as a frequency synthesizer circuit, the types of the PLL circuits that used in the field of telecommunications, and the problems of the PLL circuit.

2- Achieving the best design of the Fractional-N PLL circuit that gives the best performance for the Bluetooth system of providing a high-frequency signal with low phase noise, few spurs noise, high accuracy in the received signals, and speed of switching between frequency channeling.

1.3 Literature Review

1-In 2011, Chan-Pang et al., create a phase locked loop frequency synthesizer with a 3.9 GHz output frequency and a 300 kHz loop bandwidth, and simulate it using a novel approach to decrease fractional Spurs and quantization noise. To acquire several phases of the input signal, they utilize numerous stages of delay units between the reference input signal and the

phase detector. To obtain the appropriate phase signal, the compensating control unit was employed. They employ a sigma-delta modulator in the second and third stages. They use CMOS technology to accomplish this design. Theoretical findings suggest that the quantization process and fractional spurs noise levels increase by 13dB [8].

2- In 2016, presented study and design of a Fractional frequency synthesizer using MATLAB and ADS programs. A single loop Sigma Delta modulator and a passive loop filter were designed in three orders to achieve the best design of the fractional -N PLL that gives a good noise performance that was acceptable in Bluetooth specifications. the study referred to the proposed design of a Fractional N-PLL frequency synthesizer with a 3^{rd} order loop filter and a 2^{nd} order sigma-delta modulator was the best-proposed design that generates a high output frequency signal that is free from any spurious noise, acceptable phase noise, and fast switching time [9].

3- In 2017, Kong et al. proposed a new way for eliminated the Σ-Δ modulator noise while maintaining a moderate loop bandwidth, by using a cascaded synthesizer architecture for 2.4-GHz RF standards that doesn't require LC oscillators or charge pumps, but is mainly used a digital delay-line-based filter and an analog noise trap to decrease the quantization noise of the Σ-Δ modulator. the reference frequency of the frequency synthesizer circuit is 22.6 MHz, the synthesizer achieves a bandwidth of 10 MHz in the first loop and 12 MHz in the second, heavily suppressing the phase noise of its constituent ring oscillators. Realized in 45-nm digital CMOS technology, the synthesizer exhibits an in-band phase noise of -109 dBc/Hz at 1MHz offset frequency, with reference spurs noise about -70 dBc [10].

4- In 2018, Gowthami has implemented two architectures for the Fractional-N PLL frequency synthesizer, where the first architecture was using MASH

1-1-1-1 Σ-Δ modulator, and the second was using MASH 1-2 Σ-Δ modulator. The macro model was validated using MATLAB and ADS programs, a comparison was made between the results of both architectures for the purpose of choosing the best model that gives the best performance in terms of reducing the amount of phase noise and spurs noise. 20 MHz was chosen as a reference frequency in order to obtain a frequency output ranging between 200-220 MHz. It concluded from the results that increasing the order of the Σ-Δ modulator will increase the levels of phase noise, spurs noise, and the best design of Fractional-N synthesizer with MASH 1-2 third-order delta-sigma modulator which is least complexity, and it gives better noise shaping and suppresses reference and fractional spurs, with -44dBc/Hz phase noise at 210MHz offset frequency. The transfer function proves that the system is stable because the phase margin is greater than 45° and less than 90° [11].

5- In 2018 Kong et al., proposed A Fractional-N synthesizer architecture that depending on the digital CMOS technology. Were the circuit consist of simple FIR filter that produce a 35-tap finite impulse response that suppresses the Σ-Δ modulator noise, but does not affect the loop Bandwidth, with a three-stage ring oscillator, and avoids analog circuits such as charge pumps and forward cancellation DAC .The circuit is operating at 22.6 MHz as a reference frequency with a loop Bandwidth equal to (F_{REF} / 4) which is around 5.6 MHz to produce 2.31-3.05 GHz in the output frequency signal of the synthesizer circuit. this technique provides heavily suppression of the Σ-Δ modulator noise and the significant attenuation of the VCO phase noise [12].

6- In 2018, Liao et al., published a concept of A Fractional-N sub-sampling PLL(SSPLL) with fast robust locking employing a dual-loop structure with

automatic soft loop switching. This technique was applied in 2.4 GHz applications. A quadrature voltage-control oscillator (VCO) is employed, with 16 output phases interpolated. Automatic soft switching between the sub-sampling phase control loop and the frequency control loop is presented to improve loop robustness against disturbances and interferences, resulting in more stable loop dynamics for a wider range of phase errors. For 16-phase clock production from quadrature phases, a capacitive phase interpolation network is used. With a subsampling phase detector, the 16 phases are also used to accomplish Fractional-N operation. For Fractional-N mode, this passive phase interpolation at the VCO frequency adds no extra noise or power and prevents in-band phase noise degradation. The SSPLL chip achieves a measured in-band phase noise of −120 dBc/Hz with 16 output phases. The measured reference spur and fractional spur levels are −72 and −52 dBc, respectively [13].

7- in 2019, Heng et al., have used the hybrid infinite impulse response (IIR) phase noise filtering technique for Σ-Δ Fractional-N PLL at 2.4 GHz. Where the IIR phase noise filtering technique can suppress 5 dB more phase noise than the same or fewer filter order of the hybrid finite impulse response (FIR) filtering technique, with a small area, and lower or comparable power performance. The In-band phase noise and Fractional spur level were reduced to -102 dBc/Hz at 100 kHz offset and -54.7 dBc respectively. [14].

1.4 Thesis Organization.

This thesis consists of five chapters distributed as follows:

Chapter one includes an introduction to wireless communications and the most important frequency synthesis circuit the phase-locked loop circuit (PLL), and its use in the field of Bluetooth application, in addition to the motivation of this study, and a review of previous research.

Chapter two includes an introduction to the PLL circuit and the practical applications of this circuit in addition to the types of PLL circuits where PLL is based on the basic components of this circuit whether these components are digital or analog, the architectures used in PLL circuit, the main problems in the operation of the frequency synthesizer, and the techniques used to solve them.

Chapter three discusses the designing of the loop filter at 2^{nd} ,3^{rd} ,4^{th} order. In addition, the designing of the Σ-Δ modulator also at 1^{st} ,2^{nd} ,3^{rd} order to get the best performance for the Fractional-N PLL circuit design making it suitable for Bluetooth applications.

Chapter four illustrates the results of simulations and discussed the different circuit design of the fractional-NPLL frequency synthesizer by Σ-Δ modulator technique and make comparisons between these results.

Chapter five includes conclusions that have been reached through this study with suggesting some of the future works in this field.

CHAPTER TWO

Theoretical Background

2.1 Introduction

The phase-locked loop circuit was first dealt with in 1932 by the scientist Bellescize and it was defined as the simultaneous reception of radio signals [15], in addition to the widespread use of this theory in television receivers. The phase-locked loop circuit is defined as the contribution of a group of analog and digital devices that work together sequentially to obtain one goal, which is to extract a group of high frequencies from a single reference frequency source of low frequency that makes this circuit necessary and plays a basic goal in the up/down conversion that occurs in the transceivers of radiofrequency generating stations that generates frequencies reach to a few GHz or more .The principle working of PLL circuit is based on the comparison between the reference frequency that may be sourced from a crystal oscillator with the resonant frequency generated by the voltage-controlled oscillator circuit VCO after being divided by the Divider-N. The advantage of the PLL circuit is that it uses two types of oscillators to improve the properties of one oscillator by the other. The crystal oscillator is characterized by providing a signal of high purity, where the frequency signal coming out from the crystal oscillator has a low noise value, the reason that makes the crystal oscillator undesirable in RF radio frequency devices is that the crystal oscillator is capable of generating a single frequency signal with a value less than the required frequencies in RF circuits that reach to a few GHz. Solving this problem of the crystal oscillator by providing high output frequencies by the voltage controlled oscillator VCO where the output frequencies were adjusted by controlling the input voltage of the oscillator and thus the possibility of switching between different channels of

frequencies, but one of the disadvantages of the voltage-controlled oscillator VCO is that the output frequency signal of the oscillator contains noise resulting from two sources, the first resulting from internal noise of the oscillator which it adds random noise to the output signal as in equation (2-1) [16].

$$X(t) = A\cos[\omega_c t + \emptyset_n(t)] \qquad (2\text{-}1)$$

Where $\emptyset_n(t)$ is random phase noise, that changes the zero-crossing points of the signal generated by the VCO, as indicated. in figure (2-1) [16].

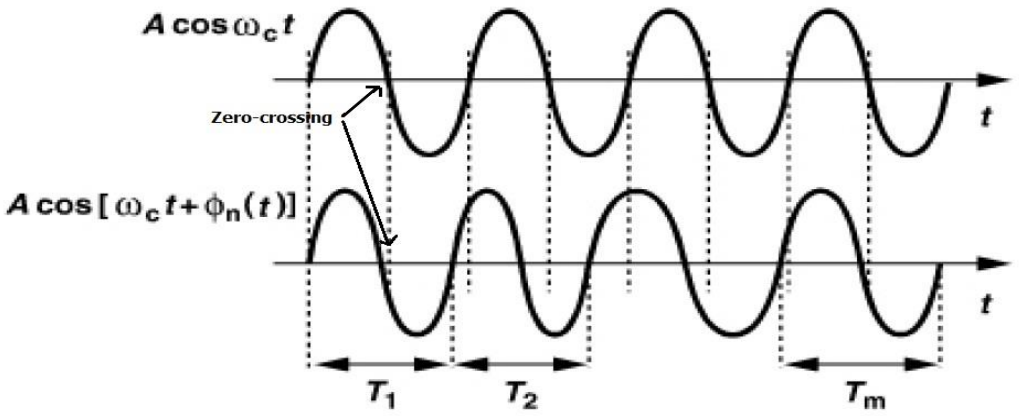


Figure 2-1: Influence of phase noise in the output VCO signal [16].

Where T_1, T_2 , T_M are the time of one period cycle of the output VCO signal .The second source of noise comes from the noise signal in the control voltage of the VCO, which is caused by the phase detector having non-ideal components that leads to the introduction of high-frequency noise in the error signal and thus this noise will reach the control voltage of the VCO, causing inaccuracy in selecting the desired channel frequency, as a frequency shift occurs after a period of time of frequency adjustment. This type of noise can be reduced by using loop filter components before the voltage control

oscillator to remove the noise entering the voltage control oscillator. These types of noise will be discussed in section 2.5.
A good performing PLL circuit is distinguished if the voltage input to the VCO is constant, and this happens when the error signal coming out of the phase detector PFD is zero or has a small value. The quality of the PLL circuit is not only the noise level in the output signal, but it depends on some variables such as settling time, lock range and capture range [17].

2.1.1 Settling Time

The settling time is defined as the time it takes for the oscillator output signal to achieve a steady-state during the transition from one channel to the next. The settling time is proportional to the loop filter's bandwidth, which should be ten times less than the reference frequency to keep the loop stable. The faster the settling process, the wider the loop bandwidth [17]. Therefore, to achieve a faster transient settling time, a PLL-based frequency synthesizer needs a high reference frequency.

2.1.2 PLL Lock Range

PLL Lock range refers to the frequency range across which PLL will monitor the input frequency signal and remain locked. As shown in figure (2-2) [18], the lock range is generally a band of frequencies above and below the PLL free-running frequency.

The PLL circuit will not be able to lock if the frequency of the input signal is outside the PLL lock range. The VCO frequency jumps to its basic free-running frequency in this situation.

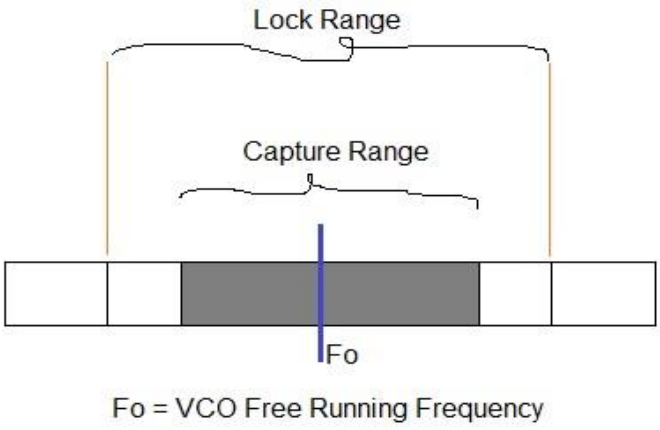


Figure 2-2: PLL Lock Range [18].

2.1.3 PLL Capture Range

When a frequency is within the range of PLL lock, the circuit will be modified and will remain in a locked state. Any future change will then be corrected with the functions of a jumper phase detector, a low-pass filter, and the functions of a voltage control oscillator. Once the input signal is captured, the PLL will remain locked and track fluctuations in the input signal until it falls within the lock range. PLL pickup range refers to the range of input frequencies over which the PLL will pick up the input signal, and it is much narrower than the PLL lock range as show in figure (2-2). The free operating frequency VCO is in the middle of both the PLL lock and pickup ranges. PLL acts as a band pass filter which is successful in removing noise and interference from the input signal if it exists.

The PLL circuit is usually called a frequency and phase multiplier circuit due to the phenomenon of accumulation of the phase error signal coming out of the phase detector due to the presence of a phase difference between the two input signals of the detector where this difference continues to accumulate but with the presence of the feedback line of the PLL circuit the

output signal will be redirected to reduce the phase difference with input signal.

2.2 Application of PLL Circuit as a Frequency Synthesizer

PLL circuits have wide applications due to their low cost and high performance. The following are some of the most important applications of PLL circuits [19]:

1- A detector of weak signals that may carry information in its phase and frequency.

2- They are used as frequency multipliers, demodulators, tracking circuits, or clock recovery circuits.

3- They were used after being developed with very complex architectures in measuring and tracking devices in space that require signals that are characterized by high characteristics in terms of narrow bandwidth and high purity.

4- It has a great use in the field of radio frequencies, complex phase switches, signal splitters, modulation, and demodulation such as dual-phase and quadruple phase.

5- It is used in the field of telecommunications in the transmitter and receiver devices of analog modulation AM and FM frequency modulation circuits.

2.3 PLL Types

There are many types of PLL circuits [20] according to the type of elements that make up the circuit, whether digital or analog elements. Which are Linear PLL (also known as an Analog PLL), All-digital PLL (ADPLL), Digital PLL. In addition, these three types there are the fourth type that is popular to use in frequency synthesizers applications namely Charge pump

PLL, it is similar to digital PLL components except that it has a charge pump device in the loop to improve the power supply noise

2.3.1 Charge Pump PLL

The basic PLL circuit consists of three main components. The phase frequency detector (PFD), the voltage-control oscillator (VCO), and the low pass filter (LPF), but by adding the charge pump (CP) then the circuit is called a (Charge Pump PLL) and by adding a frequency divider (Divider- N) to this circuit is called (PLL Frequency Synthesizer), and the following is an explanation of the components of the PLL circuit and their effect on the circuit:

2.3.1.1 Reference Signal

A crystal oscillator is mainly used to generate a reference signal with a small amount of noise. This noise is extremely low compared with noise that comes from the other components in the PLL circuit hence, reference noise contribution can be neglected. However, not all the required reference frequencies are available from crystal oscillators therefore, many PLLs employ a crystal clock conjunction with a frequency divider to obtain the accurate reference frequency**.**

2.3.1.2 Phase Frequency Detector

It is the first block used in the PLL circuit. It is a form of comparison whose output is a series of differential square waveforms whose width is proportional to the amount of phase difference between the two detector input signals, as the phase detector has a phase difference accuracy range of $\pm 2\pi$. Figure (2-3) [20] shows the characteristics of the input and output signal of the phase-frequency detector.

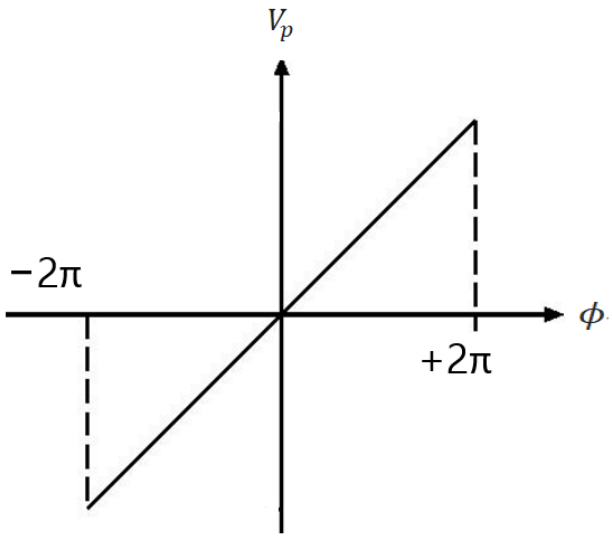


Figure2-3: Characteristic of phase input and voltage output of PFD [20].

The phase detector output can be represented in Equation (2-2) [21]:

$$V_p = K_p * (\phi_1 - \phi_2) \quad (2\text{-}2)$$

Where:

V_p is the phase detector output voltage.

K_p is the Phase detector gain in volt/radian.

ϕ_1, ϕ_2 are the phase of the reference input signal and the phase of the outgoing signal from the divider, respectively.

There are two main types of the PFD: multiplier phase detector, and the sequential phase detector. The sequential phase detector is of great use in the Integer-N PLL components and the Fractional-NPLL components and It has been called sequential because the output state of the circuit depends on the logical state of its previous inputs. Figure (2-4) [21] shows the sequential

PFD that consist of storage memory type edge-triggered D flip-flops with logical gate type AND gate.

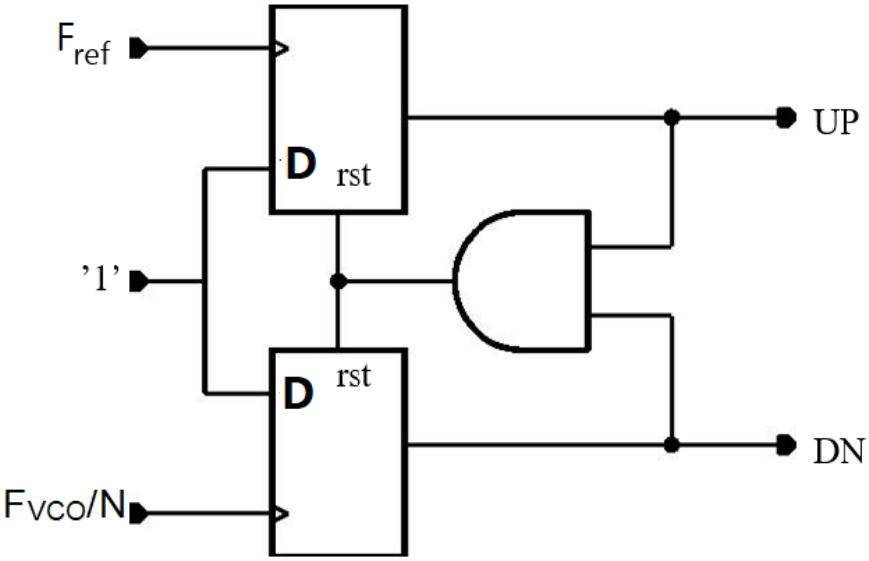


Figure 2-4: Phase/Frequency detector block diagram [21].

In the case of operating the upper flip flop circuit (when the reference frequency signal(Fref) is leading the signal leaving the divider ($F_{VCO/N}$) then the up line to logic (1) will be activated while the output of the lower flip flop will be equal to zero on the down terminal. This condition continues until the $F_{VCO/N}$ is leading the Fref signal, and in this case, the lower flip flop will be turned on so that the output on the terminal down is at logic (1) and the output on the terminal Up at logic zero .When both PFD outputs are at logic 1, the AND gate activates the reset of both flip-flops thus, the UP and DN signals remain HIGH simultaneously for a duration given by total delay through the AND gate and reset path of the flip-flop

. Figure (2-5) [22] shows the timing diagram of operating the PFD and the criteria that cause the "Up" and "Down" signals to appear. In terms of synthesizer functioning, it implies that when “Up” is set to high, the VCO is

told to oscillate quicker. When “Down” is high, the VCO is turned up to cover the phase difference to calm down the oscillations.

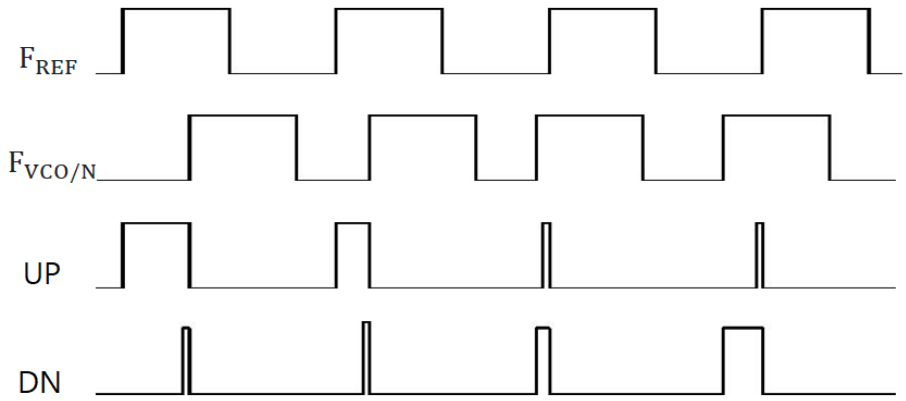


Figure 2-5: Timing diagram PFD [22]

The operation that occur inside the PFD can be divided into three operating modes depending on the difference between the two detector input signals [23]. They are the frequency detection stage, when the phase difference between the two input signals is greater than 2π, so the charge pump output current will remain constant, while the input voltage of the VCO will change continuously due to the integration procedure performed by the filter. The second operational mode is the phase detection mode which occurs when the phase difference between the two input signals is less than 2π in this case the charge pump will operate only in the period when there is a phase difference between the two signals and the third operational mode is the phase lock mode in which the phase difference between the two signals are equal to zero and the control voltage of the input signal is in the form of a continuous signal.

2.3.1.3 Charge Pump

This component must be contained in a phase-locked loop circuit to be immune to source noise, analog signal circuits, analog-digital signal circuits,

and radiofrequency circuits use this component. The charge pump has two current sources. The first one is a VCCS (Voltage Control Current Source) type that links to a switch that is controlled by the error voltage signal of the PFD on the UP end, and the other current source is a Current Sink type that connects to the error voltage signal of the PFD on the DN end. Figure (2-6) illustrates the charge pump circuit component's [24]. The current that comes out of the charge pump ($I_{CP)}$, passes through the filter to purify the signal of the noise generated by the PFD before it passes through the VCO.

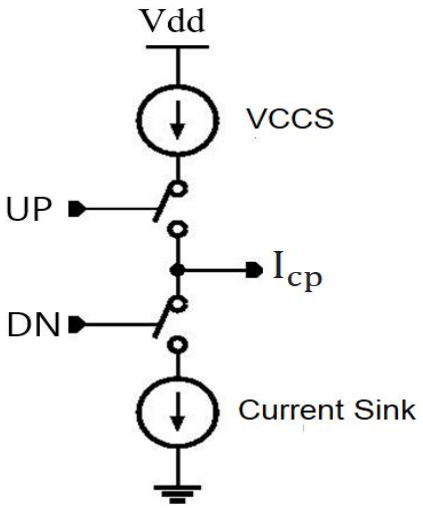


Figure 2-6: Charge pump circuit [24]

If the error voltage signal is present on the UP end of the PFD, the upper switch is closed and the VCCS source current (Voltage Control Current Source) charge the filter capacitor thus increasing the control voltage VCO. In another case if the error voltage signal is present on the DN end then the filter capacitor is discharged at the lower current source (Current Sink), caused decreasing the control voltage VCO. If the PLL circuit is locked, both switches of the charging pump are in a closed condition, and the control voltage VCO will be constant [4,22,25]. A well-built charge pump should

have numerous characteristics, including equal charge and discharge currents, correction of "Up" and "Down" pulse skews, mismatches, charge injection, clock feed-through reduction, and so on [4,26,27]. The charge pump has three topologies: source switch charge pump, drain switch charge pump, and gate switch charge pump [19]. Because of the low power consumption and equivalent switching time the source switch charge pump technology is the most popular in the frequency synthesizer circuits based on PLL. There are several technologies used in the design of the charge pump, including current steering, differential charge pump, and Charge pump with an active amplifier, as well as all three structures.

2.3.1.4 Loop Filter

The basic part of the phase-locked loop circuit based in the mixed-signal system is the low pass filter. The main purpose of using this component is to passing low frequencies that contain the desired signal and remove unwanted high frequencies that represent as ac voltage coming from quantization of the divider and non-linear properties of the elements in the circuit which reduces the stability [28,29]. Where the loop filter's coefficients determine the performance of the entire synthesizer, including open and closed-loop gains, phase margin, and the most significant factor

is the stability (because the loop filter determines the bandwidth of the PLL frequency synthesizer and hence the circuit's stability time). Additional poles are supplied to the filter transfer function when the order of the filter is increased, and this new pole provides the noise improvement in the output signal of the circuit. There are two types of filters used in PLL circuits as shown in figure (2-7), which are passive and active loop filters, and each type has its advantages and disadvantage of use. The filter type is determined according to the type of the phase/frequency detector that used in the PLL

circuit. Table (2-1) shows the comparison between the passive and active loop filters [20,30,31].

Table 2-1: Comparison between the passive and active loop filters [20,30,31].

Active loop filter	Passive loop filter
It implemented by an active element like (op-amp) along with passive elements like resistors and capacitors. As shown in Figure (2-8-a)	It implemented by passive elements like resistors, capacitors. As shown in Figure (2-8-b)
The active filter does not require a charge pump because it is directly connected to the PFD portion to make the output voltage pulses of the PFD much smoother and turned it to a relatively stable modulation signal for the VCO control	The charge pump is generally connected to the passive loop filter, the passive loop filter(or current-driven loop filter) transforms the input current pulses from the CP to steady state voltage and eliminates the harmonics contained in these pulses.
complex construction, large size occupation, and high power consumption	simple construction, small size occupation, and low power consumption.
Make the PLL circuit does not stabile because the active components in the active loop filters may have non-linear performance or parasitic durations, such as track lengths, therefor cause undesired phase shifts throughout the loop, causing instability thus, the use of this type of filter is reduced in some real synthesizer designs.	Make the PLL circuit stabile the voltage range is limited and the current source must be kept in the saturation area while the PLL is locked

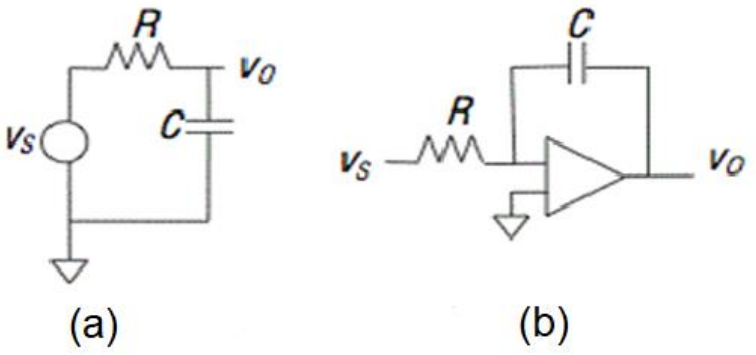


Figure 2-7: Types of loop filters: (a) passive (b) active [28].

2.3.1.5 Voltage Control Oscillator

A voltage controlled oscillator (VCO) converts voltage to frequency and is an analog element of a phase locked loop (PLL). In other words, it is a negative feedback system that generates and amplifies its own noise before returning to itself and growing to the point where it creates a periodic output signal in accordance with the closed loop. The noise amplitude will only grow to a certain point; thus it will climb. To produce a steady vibration, increase the loop gain. The VCO principal goal is to use a control element to change the output frequency. The most significant characteristic of the quality of VCO is their ability to adjust the output frequencies and thus high accuracy in choosing the desired channel. A simple representation of the control voltage versus oscillation frequency is shown in Figure (2-8) [32], and can be represented by the following equation (2-3) [33].

$$F_{out} = F_{FR} + dF = F_{FR} + K_{VCO}.V_{tune} \qquad (2\text{-}3)$$

Where K_{VCO} refer to the VCO gain , and it can be expressed as the following equation(2-4) [33]:

$$K_{VCO} = 2\pi \frac{F_{max} - F_{min}}{V_{max} - V_{min}} \qquad (2\text{-}4)$$

Where V_{tune}: input voltage signal , F_{FR} : free Running Frequency

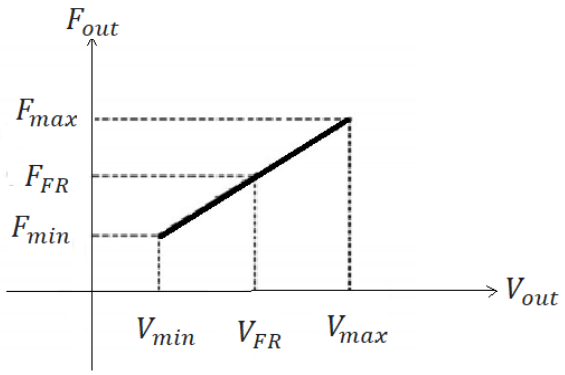


Figure 2-8: I/O Relationship for the VCO [29].

In many situations, the VCO frequency rises quickly at first then gradually rises with a flatter slope as the tuning voltage rises. As a result, VCO gain drops with increasing operating frequency, which distinguishes performance of VCO oscillators from each other that phase and temperature stability (spectral purity), linearity of frequency vs. control voltage, gain factor, bandwidth, and cost. Ring oscillator and LC tank oscillator are the two most common forms of the VCO [34,35] each type is utilized in accordance to requirements of application space, power constraint, and phase noise are all factors to consider. Ring oscillator is shown in figure (2-9) [36], were it has a larger tuning ranges and a simpler structure than LC tank oscillators, but they have the disadvantage of containing active devices that consume a lot of power and produce a lot of noise.

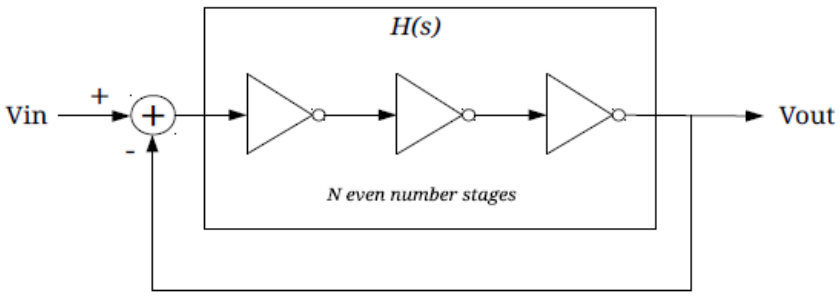


Figure 2-9: Ring oscillator block diagram [40].

Whereas LC tank oscillators have better noise performance making it more popular in radio frequency synthesizers. The LC tank oscillator drawback is that it takes up a lot of space and has a complicated design. The LC tank oscillator circuits is implemented by inductors (L) and capacitors (C) they were positioned in parallel with the current source. Figure (2-10) [34] depicts a basic LC-tank circuit, commonly known as an LC resonator if it is constructed properly.

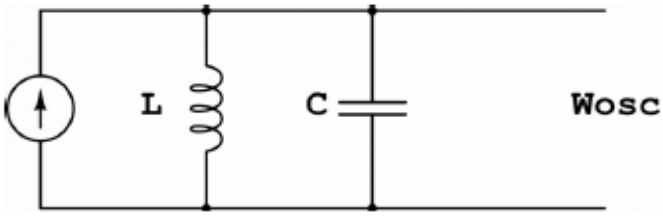


Figure 2-10: LC tank oscillator block diagram [40].

The tank can generate enough output oscillation to satisfy the required restrictions. The output oscillation can be described as follows equation (2-5) [34].

$$w_{osc} = \frac{1}{\sqrt{L*C}} \qquad (2\text{-}5)$$

2.3.1.6 Frequency Divider

The important and only part in frequency synthesizer circuits that operates at high frequency. It function is to divide the output high frequency from VCO for compare it with the reference frequency by the PFD as in equation (2-6) [34].

$$F_{div} = \frac{F_{out}}{N} \qquad (2\text{-}6)$$

In some cases, it requires to use a series of divider blocks (pre-scaler) to reduce the high output frequency of the VCO. The division ratio in the

frequency divider may be a fixed value, as in Integer –N PLL frequency synthesizers where in this category of the frequency synthesizers the division ratio is adjusted to a fixed channel frequency, then the programmable multi-bit control signal is used as a counter to switch between frequency channels to select the desired channel, or the division ratio is a variable value and if this variable value is a fractional number then the frequency synthesizer is named (Fractional-N PLL frequency synthesizer). There are two types of fractional frequency dividers, multi-modulus frequency dividers and dual-modulus frequency dividers [34-39], in a dual-modulus divider the division ratio is a single fractional value ranging between two consecutive integers values .For example figure(2-11) [39] shows a dual modulus divider with divided ratio equal to (2/3) the output of this divider regulated by (asynchronous stage's outputs (÷2),(÷3) frequency dividers), and the control input signal of a dual-modulus divider that provided by an accumulator through the input signal MOD, when the value of the mod signal is zero, the division ratio is equal to 3, and when the value of the mod signal is equal to 1, the division ratio is equal to 2. The advantage of this type of the divider is that only the first stage of divider operated at high frequencies of the input, then the frequency decreases gradually in the following stages.

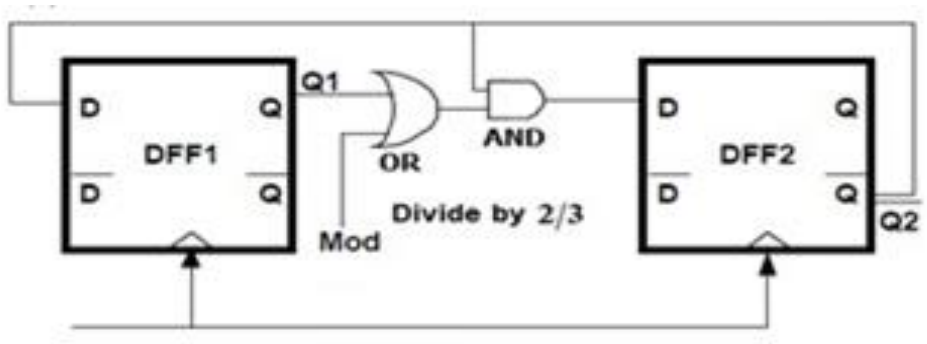


Figure 2-11: Dual modulus divider block diagram [39].

In multi-modulus frequency dividers, the division ratio is ranging between more than one fractional value to obtain the required division ratio. Σ-Δ modulators are used to control this divider to allow for smaller output frequency step sizes relative to the reference frequency, enhancing settling time, and phase noise. Figure (2-12) [36] shows the structure of the multi-modulus frequency dividers that consist of multi-stages of dual frequency dividers and it is controlled by the control signal c_0 , c_1,c_{n-1}. More details about Fractional-N frequency synthesizers and Integer–N frequency synthesizers are in the next section (2.4).

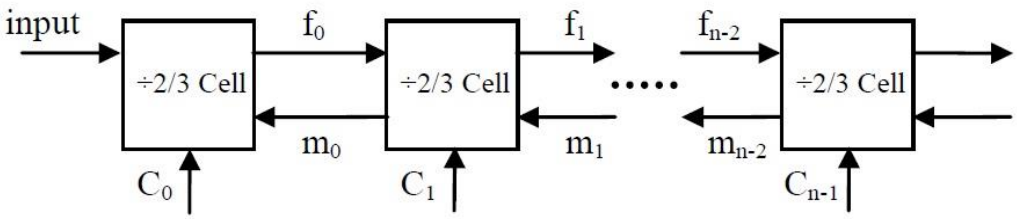


Figure 2-12: Structure of the multi-modulus frequency divider [36].

2.4 Frequency Synthesizer Categories

There are several frequency synthesis structures, each of which is appropriate for a particular purpose. These structures are classified into two categories based on the method of generation of the frequency signal [40].

2.4.1 Direct Frequency Synthesizers

They are either composed of digital or analog devices, where the digital frequency synthesizers consist of digital memory, a digital-to-analog converter (DAC), sampler, filter, and divider. The digital memory generates a signal with the same frequency as a reference clock. DAC is used to convert the digital signal into an analog signal. The outgoing signal Is cleaned by a

low pass filter to remove harmonics caused by the digital-to-analog conversion and then sampled after being divided allowing the synthesizer to be programmable. The disadvantage of this type of frequency synthesizer is the difficulty of creating a signal with great spectral purity without using a high-order analog filter, as well as the high power consumption. As a result of the limited operating frequency it can't be used in wireless applications that require high output frequency with low phase noise [41]. The other type of direct frequency synthesizer is the direct analog synthesizer, which has only analog circuit components, such as an analog reference oscillator LC tank, cascade mixers, and frequency dividers components that are used to convert the frequency to various values. This form of synthesizer has the advantage of being able to create signals with better spectral purity than the previous one, but it consumes high power, and takes up a lot of space owing to a large number of dividers and mixers. Mixers create a signal with a greater harmonic amplitude than the fundamental signal since they are nonlinear component [40], as a result, high-order filters must also be designed [42].

2.4.2 Indirect Frequency Synthesizers

They use a PLL arrangement to create the signal. This type of frequency synthesizer uses both analog and digital blocks and is the most common method for generating signals, with advantages that make it suitable for use in radio frequency applications where the signal generated by this technology reaches a few Gigahertz with high accuracy, fast settling time, and phase noise less than the previous two structures, in addition to low cost and low energy consumption in high-frequency applications .One of the most significant indirect frequency synthesizers based on PLL technology is

Fractional-N PLL Frequency Synthesizers and Integer-N PLL Frequency Synthesizers.

2.4.2.1 Integer-N Phase Locked Loop Frequency Synthesizer

An indirect frequency synthesizer technology that are mixes between an analog, and digital component that are consists of VCO, PFD, LPF, reference source, and digital divider with integer division ratio (N) [43-48], as shown in figure (2-13) [47].

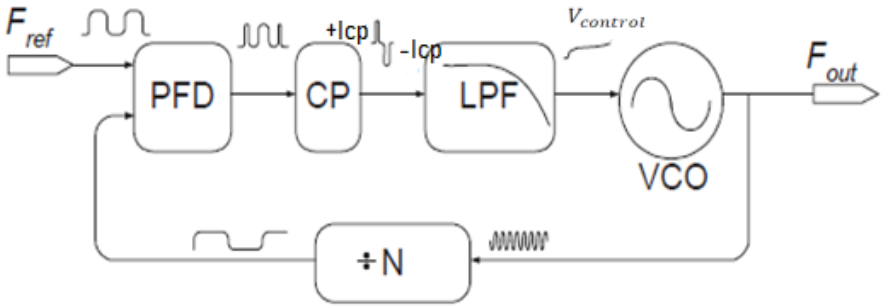


Figure 2-13: Integer-N PLL frequency synthesizer circuit [47].

One of the most important equations of the Integer-N PLL [44].

$$F_{out} = N * F_{ref} \quad (2\text{-}7)$$

$$Channel\ Spacing = F_{ref} \quad (2\text{-}8)$$

Equation (2-7) depicts the relation between the voltage-controlled oscillator output frequency and the frequency of the input signal, where N is an integer number indicating the division ratio. The output frequency is equal to or doubles the input frequency according to the division ratio.

Equation (2-8) illustrates that the distance between the frequency channels is equal to the reference frequency, which is one of the reasons why

the Integer-N PLL circuit is less commonly used in radio frequency synthesizers that require a small frequency distance between the channels to provide a fast locking time and thus increase the circuit's efficiency by increasing the speed of switching time between one channel and another, is reduced the distance will reduce the reference frequency. Several factors depend on the reference frequency, including [36,44,49-53]:

1- The bandwidth of the filter depends on the reference frequency, therefore reducing the reference frequency will reduce the bandwidth and thus increase the time required for the oscillation signal, coming from the VCO, to become stable.

2- According to the equation (2-7), to keep the output frequency constant when decreasing the reference frequency, an increase in the division ratio N is required, so the phase noise will increase by $20\log(N_{new} - N_{old})$ dB.

3-The synthesizer frequency channel resolution is limited by the value of the reference frequency; hence great resolution necessitates a low reference frequency. The low reference frequency can be proportional with a small PLL Bandwidth, to avoid significant spurs noise levels because the loop filter suppresses reference spurs at lower frequency offsets.

Another drawback that makes the Integer N-PLL frequency synthesizer unsuitable for radio frequency applications (such as the Bluetooth system, which requires the generation of multiple frequencies from a single reference frequency) is that the division ratio is fixed on the frequency of one channel, therefore necessitating the use of a counter to allow switching between frequency channels. So to overcome these problems, Fractional-N PLL usually used and dismiss the disadvantages found in the Integer-N PLL.

2.4.2.2 Fractional-N PLL Frequency Synthesizer

The Fractional -N frequency synthesizers are similar to the Integer -N frequency synthesizers in terms of circuit component construction and circuit working principle, but it used fractional division ratio instead Integer value [60]. Figure (2-14) [47] illustrates the Fractional –N PLL frequency synthesizers with accumulator as a controller circuit.

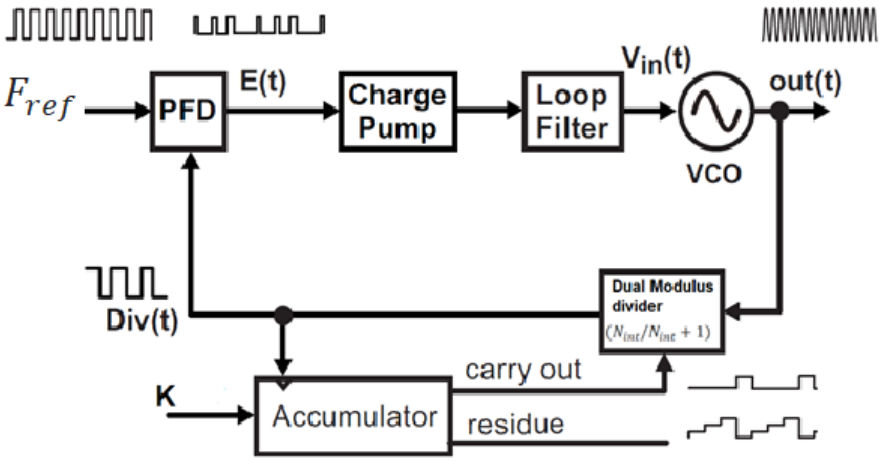


Figure 2-14: Basic component of the Fractional-N PLL circuit [47].

The fractional synthesizers based the PLL architecture is realized by changing unpredictably the division modulus factor at each reference frequency cycle ,where the digital input (K) is applied to the accumulator ,Then the accumulator combines (K) value at each reference frequency F_{ref} period until the Overflow occurs then the carry-out changed from zero to one, and that will changed the division ratio from N_{int} to $N_{int}+1$ [4,55]. This irregular switching between division modulus factors is to get an average divided ratio value (N_{frac}), as well as the fractional value as in the following equation (2-9) [56].

$$N_{frac} = \frac{(F-k)* N_{int}+K*(N_{int}+1)}{F} = N_{int} + \frac{K}{F} == N_{int}+\propto \quad (2\text{-}9)$$

Where $N_{int} + 1$, N_{int} the division ratio, K is the digital input signal and it calculated by equation (2-10) [57].

$$K = \propto * F \quad (2\text{-}10)$$

Where F is equal to 2^m, and it represent the total number of samples coming out of the accumulator for m-bits , $\propto$ the residue of a division's fractional value.

During the accumulator adding process the phase error signal gradually grows, and when there is an overflow (the moment of changing the carryout state from zero to one or vice versa), the phase error signal disappears, as shown in the diagram (2-15) [58].

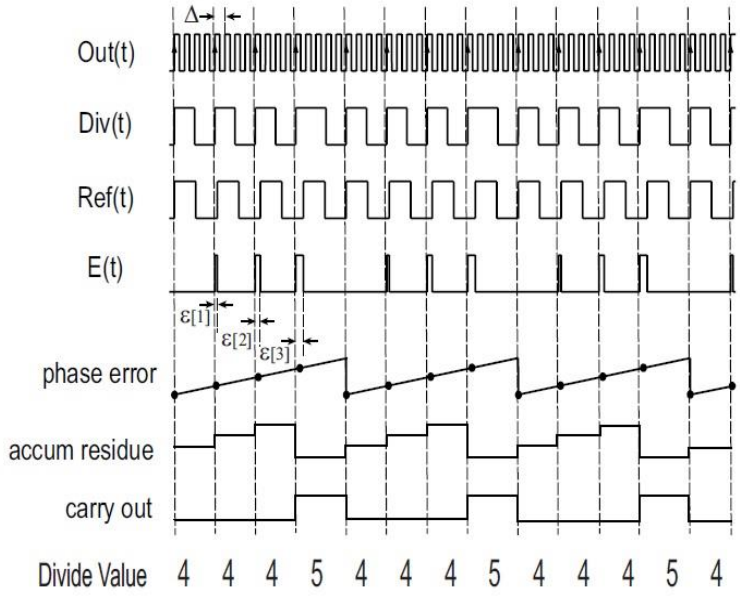


Figure 2-15: Schematic diagram for Fractional-N PLL Frequency Synthesizer function [58].

The phase error signal oscillatory variable by frequency $(\propto F_{ref})$ produces spurs noise in the output spectrum of the frequency synthesizer called Fractional Spurs Noise , as a consequence of a continuous variation

in the division ratio from N_{int} to Nint+1. To solve this problem several techniques were used to reduce this type of spurs noise, which will be clarified in the next section (2.5.3). The output frequency of the VCO as the following equation (2-11) [26,53-60].

$$F_{vco} = F_{ref} * \left(N + \frac{K}{F}\right) \quad (2\text{-}11)$$

Where F_{ref} is the input reference frequency, F_{vco} the output VCO frequency .If it is taken as example to compare the properties of the Integer-N with Fractional-N frequency synthesizers , for 500 kHz as a reference frequency with the division ratio N_{int} of 1000, the channel spacing equal to 50 kHz, and K = 1, it can determine the following parameters .By applying equation (2-12) [61].

$$Channel\ Spacing = \frac{F_{ref}}{F} \quad (2\text{-}12)$$

Then $F = \frac{F_{ref}}{channel\ Spacing} = \frac{500}{50} = 10$

So it needed to change N_{int} from (1000) to $N_{int} + 1$ (1001) one out of every 10 reference cycles. Then by applying equation (2-11) to get the output frequency of the frequency synthesizer:

$F_{vco} = F_{ref} * \left(N + \frac{K}{F}\right)$ = 500 x(1000 +$\frac{1}{10}$)= 500.05MHz.

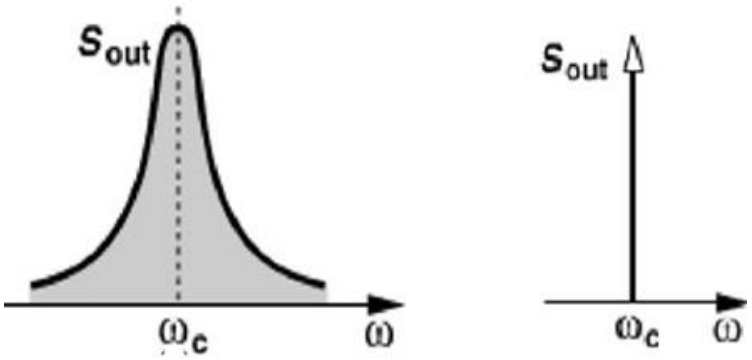
The next step is to maintain the same value of the output frequency of the Fractional-N frequency synthesizer that equal to 500.05 MHz. It is necessary to reduce the reference frequency to 50 kHz instead of 500 kHz with increasing the division ratio by ten times larger than in Fractional-N synthesizer to be *N=10001*, then the output frequency of the Integer -N synthesizer will be:

$F_{out} = F_{IN} * N$ = 50 x 10001=500.05 MHz

This example shows the significance of a divider with fractional division ratio in the Fractional -N frequency synthesizer circuits in terms of obtaining a high reference frequency and thus reducing the problems that occurred in Integer -N frequency synthesizers in terms of providing a large bandwidth, i.e. low stability time and high switching speed between frequency channels [8,62,63], in addition to the small division ratio of the frequency divider means low phase noise[4,55,60].Thus this properties make the Fractional-NPLL mixes high accuracy , quickness and majority of use in the various electronic applications.

2.5 Non -ideal Fractional - N PLL Performance.

In principle, the signal generated by Fractional - N PLL circuits should be of great spectral purity and noise-free but in fact there are many forms of noise in the signal spectrum that appear as random changes surrounding the generated signal at frequency (w_C) ,as shown in figure (2-16) [24].



(a) : Non ideal spectrum (b) : Ideal spectrum

Figure 2-16: Ideal and the non-ideal frequency synthesizer output spectrum [24].

The following is a presentation of the most common forms of noise, as well as their causes and the techniques for reducing them. Where two main forms of noise appear in output frequency of the Fractional –N PLL circuit, random and periodic noise. Thermal noise, shot noise and flicker noise are all inevitable forms of random noise in electronic components. These types of noise are called a "Timing Jitter" in the time domain, and it can be represented as an error time function (j(t)) as shown figure (2-17) [64]. The timing jitter makes the location of the transition time t_0 to randomly change and is not possible to predict it exactly.

$$V_{Jitt}(t) = v\,(t + j(t))$$

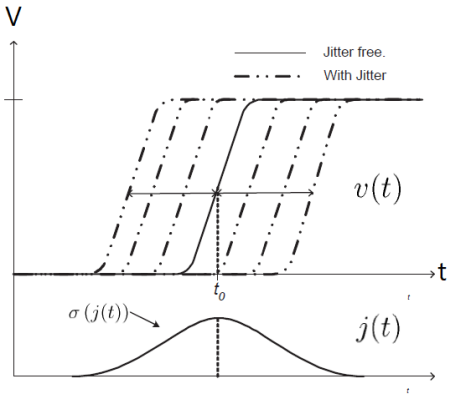


Figure 2-17: Jitter distribution effecting in the time domain [64].

And the second name of the noise is a "Phase Noise" in the frequency domain as shown in figure (2-18) [36].

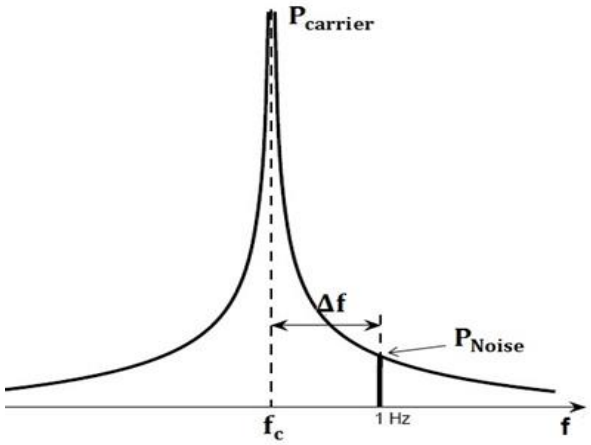


Figure 2-18: Phase noise effecting in the frequency domain [36].

The phase noise can also be expressed by the following equation (2-13) [24,36].

$$Phase\ Noise = 10\ log \frac{P_{Noise}(at\ f_c + \Delta f\ in\ 1\ Hz\ bandwidth)}{P_{carrier}(at\ f_c)}\ dBc/Hz \quad (2\text{-}13)$$

Where P_{Noise}: The power of the noise signal with (1Hz) bandwidth at frequency offset equal (Δf) from the carrier frequency.

$P_{carrier}(at\ f_c)$: The power of the signal at carrier frequency.

The phrase "periodic noise" is used to characterize the noise that occurs as a result of digital switching events in the PFD and charge pump. Non ideal characteristic in the PFD and charge pump element's cause a periodic signal fluctuation in the voltage control VCO called Reference Spurs Noise, either form of spurs noise appears in a fractional phase locked loop that uses a fractional divider with a fractional value which it causes tones in the spectrum of the output signal called Fractional Spurs Noise, as mentioned earlier." The spurs" noise can be defined as undesirable and non-harmonically based signal that appears at the voltage control oscillator's output spectrum. It is expressed by the following equation (2-14) [25,39,65]:

$$Spurs\ Noise = 10\ log\frac{P_{spurs}}{P_{carrier}} \quad \text{dBc} \qquad (2\text{-}14)$$

Where P_{spurs} : represents the noise power at offset frequency equal (Δf) from the frequency of the oscillator ,and it inversely related to the reference frequency [66].

$P_{carrier}$: represents the power at frequency equal to the carrier frequency.

This equation can be clarified by the following figure (2-19) [45] that shows the shape of the spurs noise in the spectrum of the frequency synthesizers output signal.

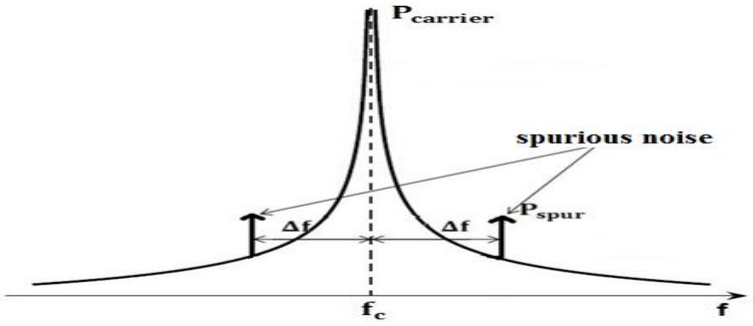


Figure 2-19: Spurs noise effecting in the frequency domain [39].

2.5.1 Reference Spurs Source

There are many reasons of generation the reference spurs that occur at a frequency offset equal to the reference frequency and its integer multiples [67], and it includes (68,69).

- PFD delay.
- Charge pump switching delay.
- Charge pump current leakage.
- Charge pump current mismatch.
- Charge injection and charge sharing.
- Charge pump current rise and fall time.

2.5.1.1 PFD Delay

The main working of the PFD is to produce the error signal resulting from comparing frequencies and phases between the reference input signal and the divider signal [70], when a phase difference between PFD input signals is too small to be sensitive from the PFD. Therefore, the status(ON/OFF) of the switches that connected with the charge pump's input does not change so the phase output signal will be fluctuated randomly. This problem is named the dead zone and it can be solved by linking the reset output of the PFD with delay stages as in the figure (2-20) [70], that working to generate a sufficient period of time to change the keys cases.

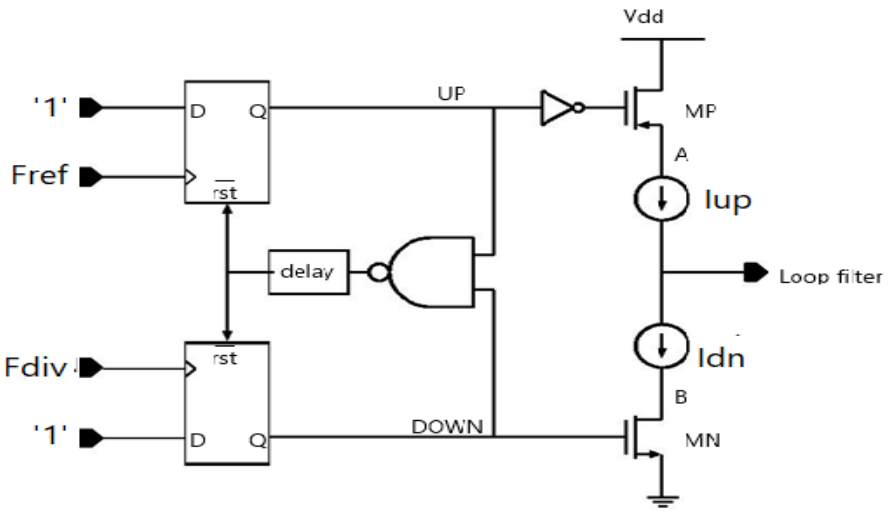


Figure 2-20: Phase frequency detector, charge pump and delay stage logic diagram [70].

2.5.1.2 Charge Pump Current Mismatch

It is one of the contributory factors to the PFD delay [71]. Ideally, the amount of the charge pump output current should be constant, but the difference in the types of the switch "up" that represents by PMOS transistor, and the switch "DOWN" that represented by NMOS transistor, will lead to

differences in the channel length modulation and locking time of the two keys, these differences contribute to the current mismatch. To eliminate this problem, the operating time of the switches must be adjusted in terms of lengthening the operating duration of the less charge current source, and thus the comparative equality between the charge pump current sources.

2.5.1.3 Charge Pump Switching Delay

The mismatch between the UP and DOWN switches come from using the PMOS transistor for UP switch that requiring uses an inverter to invert signals from the PFD, this inverter leads a delay to the UP signal as shown in figure (2-21) [68], affecting to the VCO tuning voltage this type of noise can be reduced by using a transmission gate to equality between the UP and DOWN signals or by using a complementary differential cascade inverter to reduce this delay unfortunately. Neither of these methods fully remove the delay, resulting reference spur noise at the output signal.

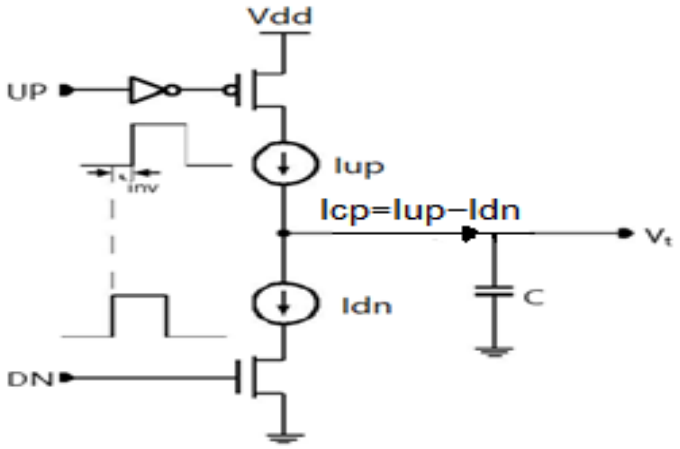


Figure 2-21: Charge pump with Switching delay logic diagram [68].

2.5.1.4 Charge Pump Current Leakage

When the PLL circuit is locked, both UP and DN switches are in OFF state therefore there is no current flows to the filter. However due to a sub-

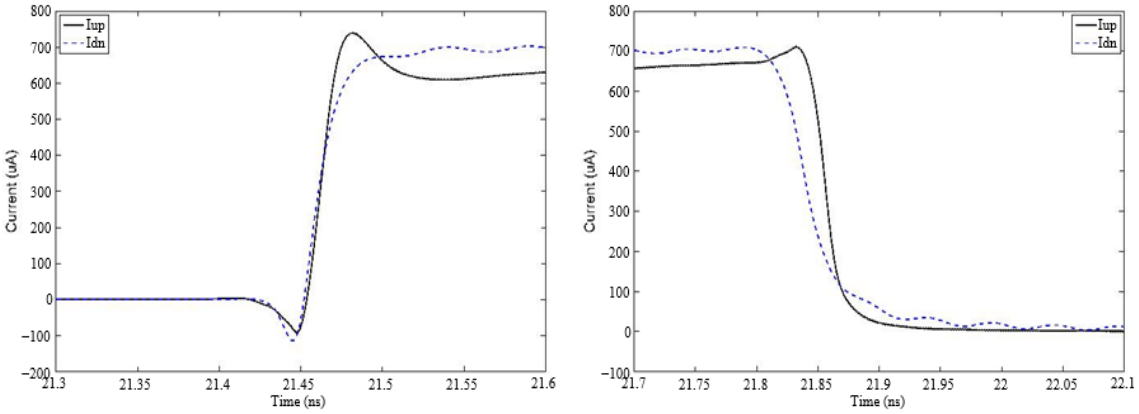
threshold leakage there is still a little current passes through the UP and DN switches, causing the capacitor in the loop filter to charge and discharge, resulting in variations in the VCO tuning voltage, the amount of leakage current is also affected by the VCO tuning port leakage so it should be making the input impedance of VCO very large [72-74].

2.5.1.5 Charge Pump Current Rise and Fall Time Characteristics

The rise and fall times of the charge pump current sources are changed with respect to:

1-The difference in the size and type of the transistors that uses as a control switch for the input of charge pump current sources, where the upper switch is a PMOS type transistor while the lower switch is NMOS type transistor.

2-use the different types of the loop filter also gives a different load to the charge pump, therefor affected to the rise time and fall time characteristics. Figure(2-22) [74] illustrate the simulation results of rise time response and fall time response ,for the charge pump current sources.



a-Rise time characteristic. b- Fall time characteristic.

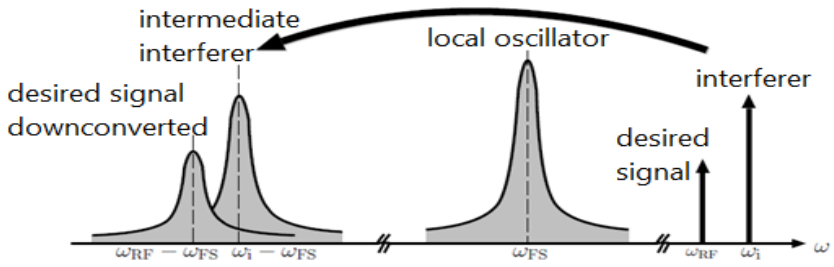
Figure 2-22: Charge pump current sources response [80].

2.5.1.6 Charge Injection and Charge Sharing

Charge injection is a term that is given to the charges that remain in the transistor channel switch in the on-off state of the switches [75,76]. A small size of transistor switch gives a small injection charging. The charge sharing is a term of sharing the charges from node A and B as shown in figure (2-20) in the charge pump as a result of mismatches turn on times of the transistors switch [77]. There are several techniques to reduce the sharing charges phenomenon, one of this ways are by using two charge pump in type source switched charge pump connected together, this technique is called a" current steering".

2.5.2 Effect of Frequency Synthesizer Noise on the RF Communication Systems

The importance of the purity of the signal coming out of the frequency synthesizers comes from the fact of this circuit is an essential part in the radio frequency receiving circuits as previously explained in figure (1-1). As a result the inclusion of the frequency synthesizers on the non-ideal components adds phase noise and spurs noise to the received signal and thus distort the basic information of the received signal. Figure (2-23), and figure (2-24) [78] show this noise effecting.



(c):Final received signal after the downconverter process.

(b):Frequency synthesize Output signal.

(a):The received signal.

Figure 2-23: Phase noise problem in the received signal [78].

Where:

Interfere: It is a strong interference signal that exists within the received signal resulting from the noise that the signal is exposed to during the transition from the transmitter to the receiving side at interferer frequency (w_i).

Desired signal: It indicates the transmitted information received signal at frequency (w_{Rf}), this signal is called the intermediate signal at frequency (w_{iF}) after it received by the frequency synthesizer and the down-conversion process is performed.

Local oscillator: frequency synthesizer output signal that contain the phase noise at frequency (w_{Fs}).

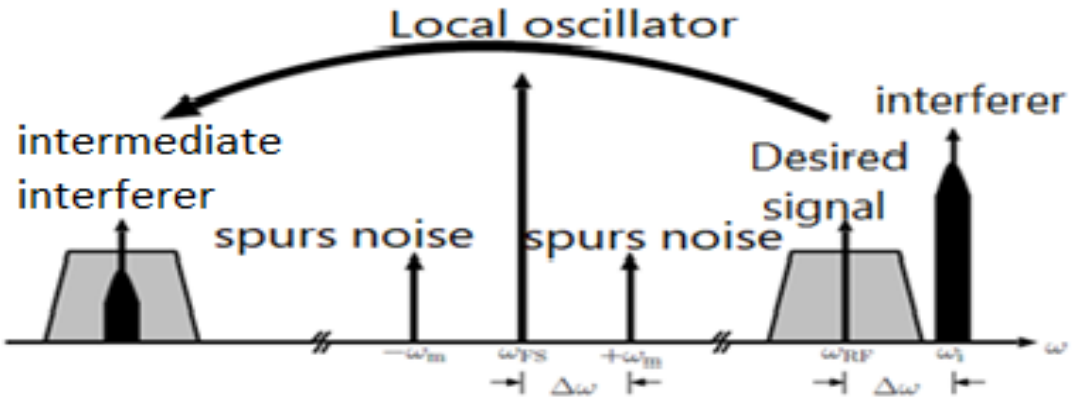


Figure 2-24: Spurs noise problem in the received signal [78].

Where

spurs noise is undesirable signal that appears in the sideband of the frequency synthesizer output at frequency (w_m). And if

$$w_{Rf} - w_{Fs} = w_i - w_m = w_{if}$$

This mean the interference signal will be translated into the desired information signal band and as a result that distort the intermediate signal [78].

2.5.3 Techniques of the Fractional-N PLL Circuit

There are many methods that have been used to reduce some of the problems that appears in the Fractional-N PLL circuit, including noise problems. Some of these techniques are [79-84] (Phase Interpolation, Pulse Swallowing, and Wheatley Random Jittering. These three techniques have proven insufficient in improving the noise levels compared to the fourth most common technique in frequency synthesizer circuit, which is the Sigma-Delta Modulator technique).

2.5.3.1 Sigma- Delta Modulator Technique

Sigma-Delta Modulator (Σ-Δ) technology or Delta-Sigma Modulator (DSM) was used as a digital frequency divider control in a fractional -N PLL frequency synthesizer circuits for the first time by Miller and Riley .Then the Σ-Δ modulator has become an essential part in the data converters circuit [85 ,86],due to it feature characteristics that of producing a high spectral purity that is free from spurs noise that distort the important information in the signal, by eliminates the iterative process of division between two integer values and instead it creates an average value equal to the desired fractional value [87,88] as shown in figure (2-25) [89].

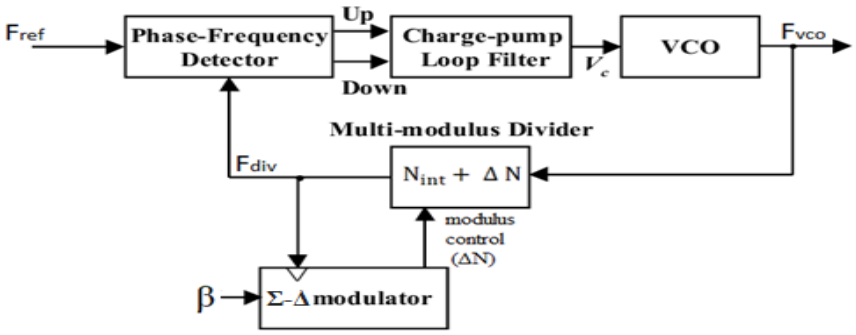


Figure 2-25: Fractional –N PLL circuit diagram with Σ-Δ modulator [89].

Where the VCO output frequency can be represented by the following equation (2-15) [90].

$$F_{vco} = (N_{int} + \Delta N).F_{ref} \quad (2\text{-}15)$$

Where:

N_{int} : the integer division ratio part.

ΔN: the fractional division ratio part depends on the number (bits/word) DC input (β), where the fractional resolution will be smaller and more precise when (β)is larger. The fractional part can be more expressed as

$$F_{vco} = (N_{int} + \frac{K}{F}).F_{ref} \quad (2\text{-}16)$$

Where:

K: the decimal representation of the DC input number.

F: the decimal representation of the resolution of the DC input number.

Also, Σ-Δ modulator provides accuracy to the information signal as a multi-quantum Nyquist-rate device [91]. The principle working of the Σ-Δ modulator depending on the over sampling rate and noise shaping properties [92], where the spectrum of the quantization noise is shaped. Therefore, a

small magnitude of the noise power will be transmitted with the useful signal band, and the remain part of the quantization noise "phase noise" is pushed by the modulator to higher frequencies to removed it by using a loop filter with order that larger or equal to the Σ-Δ modulator order, in order to protect the VCO's output frequency from this type of noise [93-96], which the quantization noise should less than PFD and VCO noise [97] to give acceptable noise performance for frequency synthesizer circuit.

2.5.3.1.1 First Order Σ-Δ Modulator

In a feedback loop technique, the main components of the first order Σ-Δ modulator is as shown in figure (2-26) [98]. The principle working of this circuit as the following steps, first the analog comparator compares between the input signal and the quantized output value (i.e. the quantization error between the current input and the previous sampled output. The second step is to integrated the output signal of the comparator by an Integrator then is to quantized the final signal to 1-bit as a pulse-density modulated signal by the quantizer, and it represented the average magnitude of the signal over a specific period [99]. Then the final signal is fed back to re-compared it with the DC current input signal to generate the desired output signal, during the subsequent sampling periods. the disadvantage of the first order Σ-Δ modulator that it added a high quantization error to the produced signal due to the two-level quantized.

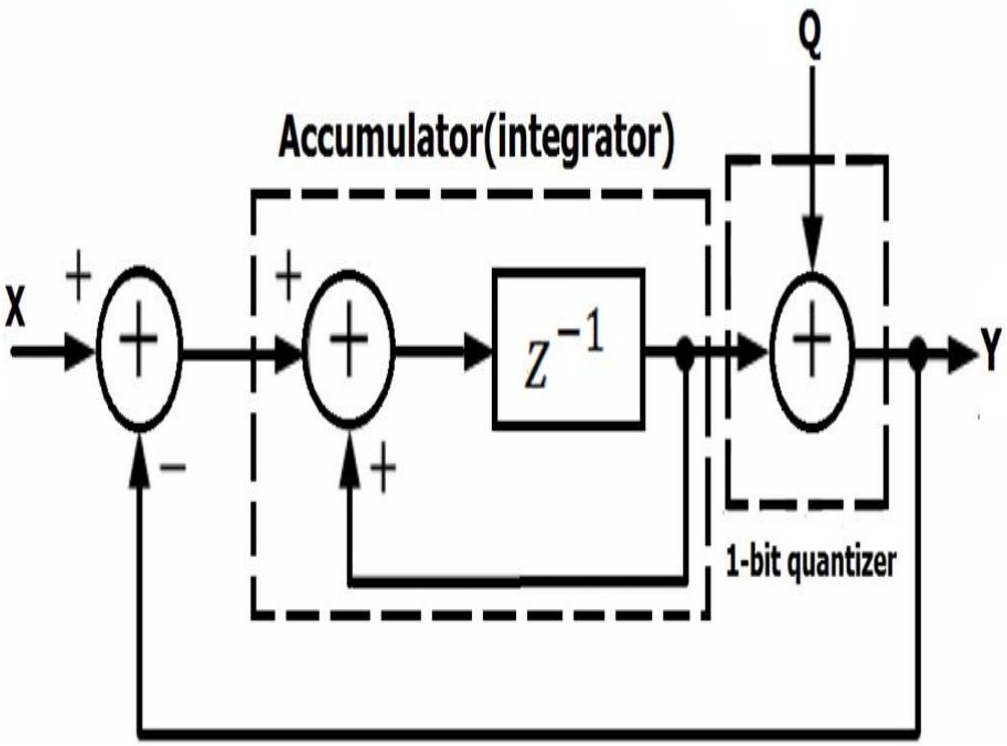


Figure 2-26: First order Σ-Δ modulator circuit [98]

Also, the repeated action of the feedback loop will produce a string of 1 or 0 output which can be averaged over many sampling periods to give a very precise result [100]. Thus, the action of the first order Σ-Δ modulator is similar to the action of the accumulator in adding a series of spurs with higher amplitude to the output signal spectrum [101]. Therefore, a high order of the sigma delta modulation with high quantization levels will be used, which in turn adds another type of noise that in less effecting on the output spectrum than the spurs noise named a "white noise", and it appears more clearly at a high values of the bandwidth. Table (2-3) [102-108] shows some of the important circuits of high order Σ-Δ modulator.

Table 2-2: Techniques of the high order Σ-Δ modulator [102-108]

Σ-Δ	Σ-Δ Order	Synt. Order and (Fc/F_{ref})	Dither	Spurs
Single-Loop	3	4 (0.005)	2^{24} LFSR	-80dB@200kHz
Multi-Loop	4	5 (0.023)	No dither	-70dB@300kHz
Error-Feedback	3	4 (0.0153)	2^{10} off-chip LFSR	No
Hybrid	≥ 4	5 (0.02)	No dither	-70dB@10MHz
Hybrid	≥ 6	3 (0.0031)	No dither	No
Chebyshev	3	5 (0.0106)	No dither	No
MASH	3	4 (0.00135)	off-chip dither	No

Where:

Fc/F_{ref} : is the loop filter cut off.

Dither characteristic: It is generation of randomness at the output to avoid the appearance of tones, which requires a multi-phase frequency divider and an inline high order multi bit output to ensure achieved delay between stages.

It was noted from the table (2-3) that Hybrid [102,103], Chebyshev[104] and Multi-Loop [105,106] architectures have a large (Fc/F_{ref}) values, with free spur tones in the output signal so it doesn't needed to dither signal ,but they required a high cost according to use a large number of modulator devises . On the other hand a multi-stage noise shaping (MASH) [107]

distinguished by its easer of construction from some adders and registers ,so less cost with lack of (Fc/F_{ref}) consumption , but it required a high performance of a low pass filter to eliminates the spur tones . In a Single-loop technique [108], although it uses a dither sign (as a Least Significant Bit (LSB), from a Linear Feedback Shift Register (LFSR) with more than 24-bit) that added to disable the tones that appears at high frequency, but it increased the complexity to realize the forward loops and the increased in-band noise (that can be easily filtered by designing a high-quality low pass filter). For further comparison, figure (2-27) [109] presents the noise modulation figures for the architectures discussed where PSD is the Power Spectral Density .Chebyshev has the best noise modulation because it reduces noise at higher frequencies .Single-Loop architectures was improved the noise formation and MASH architecture has the same noise modulation function for Multi-Loop architecture.

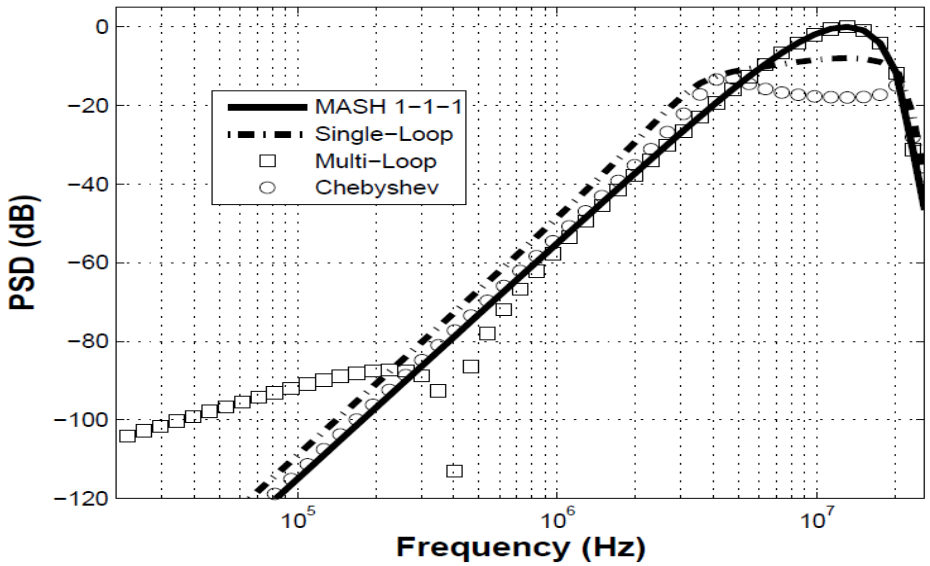


Figure2-27 : Comparition between Σ-Δ modulator techniques in noise shaping [109].

CHAPTER THREE

Design and Simulation of the Fractional N-PLL Circuit Using Σ-Δ Modulator Technique

3.1 Introduction

According the reviews in the previous chapters about the importance of the Fractional –N PLL circuit in high frequency applications, in addition to discussing the main parts of the circuit's and their effect's on the performance of the circuit, the work was done in this thesis on designing a Fractional -NPLL circuit with specifications that make it able to be used in the field of Bluetooth application according to the specific parameters of the Bluetooth system shown in the table (3-1) [110-115].

Table 3-1: Basic Specification of Bluetooth application

Specification	Bluetooth
F_{ref} (MHz)	13,19.2,20,26,39.2,40
Frequency Range (MHz)	2402 to 2480
Channel Spacing (MHz)	1
Accuracy (kHz)	± 75
Phase Noise (dBc/Hz)	-110 @ 2MHz, -119 @3MHz
Settling Time (μsec)	≤ 220
Reference Spurs (dBc)	≤ -49
Fractional Spurs (dBc)	Free

In this thesis, MATLAB and ADS programs are used where a MATLAB2020b program [is a programming design program that is used to analyse and design systems and circuits, the language of the program is a matrix-based language allowing the most natural expression of computational mathematics]. And Advance Design System ADS2017 program [is the best program for creating and simulating high-frequency circuits where it is nearly unique in this regard, like radio and microwave frequencies that reach to Gigahertz frequency or more, the program is produced by key sight formerly known as Agilent]. This software offers professional and comprehensive capabilities for all stages of planning, design, simulation, and analysis. A low pass filter and a Σ-Δ modulator are designed, because the importance of these two elements in improving the performance against noise of the frequency synthesizer circuits, the passive loop filter was designed because its easer of construction and making the phase-lock loop circuit more stable, where the loop filter parameters (phase margin, filter order, bandwidth) determine the performance of the entire synthesizer circuit. Because the loop filter determines the bandwidth of the PLL frequency synthesizer and therefore, the circuit settling time. Also, the order of the filter plays a major role in improving the noise performance of The filter where the order of the filter is increased when additional poles are provided to the filter transfer function. And the phase margin determines how far the system is from instability. The filter is designed with 2nd,3rd, and 4th order. Also, the single loop Σ-Δ modulator type with 1^{st} ,2^{nd}, and 3^{rd} order is designed, because it has an acceptable noise modulation compared with the other Σ-Δ modulator techniques mentioned in chapter two which it reduces the high noises at higher frequencies. Thus, there are three circuits design for the frequency synthesizers circuit (Fractional N-PLL with a 2^{nd} order loop filter and 1^{st} order Σ-Δ modulator, Fractional N-PLL with a 3^{rd}

order loop filter and 2nd order Σ-Δ modulator, and Fractional N-PLL with a 4th order loop filter and 3rd order Σ-Δ modulator), under the influence of different values of bandwidth and phase margin. Figure (3-1) shows the structure of a fractional frequency synthesizer circuit designed using ADS program.

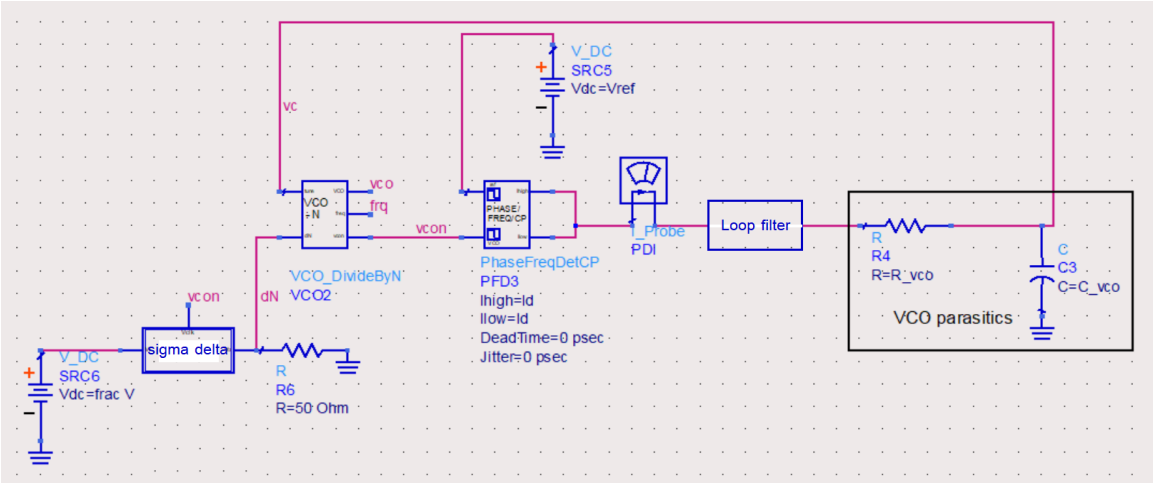


Figure 3-1: **Structure of the Fractional frequency synthesizer circuit.**

3.2 Second-Order Loop Filter Design

The second-order loop filter is the simplest filter type which consists of two capacitors and one resistor. Therefore, it added one pole to the filter transfer function. Figure (3-2) illustrates the basic design of the second-order loop filter that used in this thesis using the ADS program.

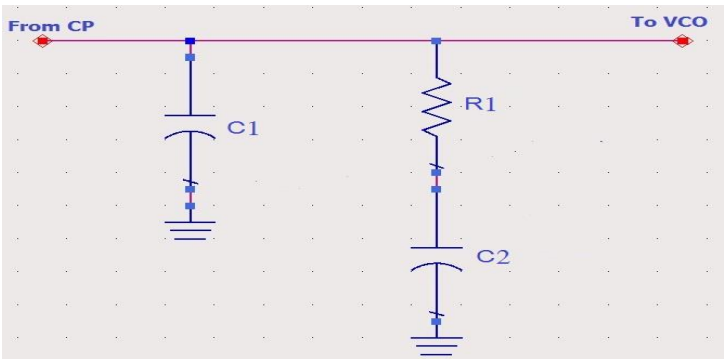


Figure 3-2: Second order loop filter design in ADS.

The second order filter design was based on the equations in the table (3-2) [116].

Table 3-2: Second order loop filter design equations [116]

Abbreviations	Definition	Equation of 2nd order loop filter
T(s)	the loop filter's transfer function	$\frac{1 + S\,T2}{S\,A0(1 + S\,T1)}$
N	Division ratio	F_{out}/F_{ref}
T1	The first pole in the loop filter transfer function	$\frac{\sqrt{(1+\gamma)^2 \tan^2\emptyset + 4\gamma} - (1+\gamma)\tan\emptyset}{2\,fc}$
T2	The zero in the loop filter transfer function	$\frac{\gamma}{T1\,fc^2}$
A0	The loop filter coefficient	$\frac{K_\emptyset\,K_{vco}}{N\,wc^2} * \sqrt{\frac{(1+T2^2 fc^2)}{(1+T1^2\,fc^2)}}$
C1	The first capacitor in the loop filter	$A0\,\frac{T1}{T2}$
C2	The second capacitor in the loop filter	A0-C1
R1	The first resistor in the loop filter	$\frac{T2}{C2}$
O(s)	The open loop gain of the loop filter	$\frac{T(s)K_\emptyset\,K_{vco}}{S\,N}$
G(s)	The close loop gain of the loop filter	$\frac{O(s)}{1 + O(s)}$

3.3 Third-Order loop filter design

Third-order loop filters are widely used in frequency synthesizer because they have good stability which it added two poles to the filter transfer function and for their simple architecture. Also, it provided an efficient filtering operation for the spurs noise that occurs at frequency distance equal to ten times of the loop Bandwidth [117]. Figure (3-3) illustrates the basic design of the third-order loop filter that is used in this thesis using the ADS program.

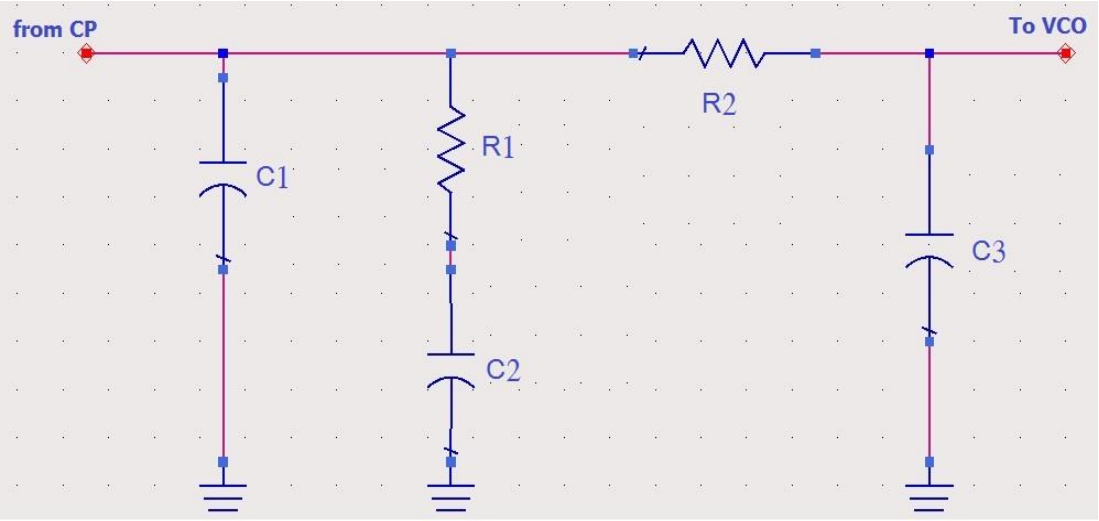


Figure 3-3: Third order loop filter design in ADS

Third order filter design was based on the equations in the table (3-3) [117].

Table 3-3: Third order loop filter design equations [117]

Abbreviations	Definition	Equation of 3rd order loop filter
T(s)	the loop filter's transfer function	$\frac{1 + S\,T2}{S(S^2A2 + S\,A1 + A0)}$
N	Division ratio	F_{out}/F_{ref}
T1	The first pole in the loop filter transfer function	$\frac{\sec(\emptyset) - \tan(\emptyset)}{fc(1 + T31)}$
T2	The zero in the loop filter transfer function	$\frac{\gamma}{fc^2(T1 + T3)}$
A0	The loop filter coefficient	$\frac{K_\emptyset\,K_{vco}}{N\,wc^2} * \sqrt{\frac{(1 + T2^2\,fc^2)}{(1 + T1^2\,fc^2)\,(1 + T3^2 fc^2)}}$
C1	The first capacitor in the loop filter	$\frac{A2}{T2^2}(1+\sqrt{1 + (T2\,A0 - A1)\frac{T2}{A2}})$
C2	The second capacitor in the loop filter	A0-C1-C3
R1	The first resistor in the loop filter	$\frac{T2}{C2}$
O(s)	The open loop gain of the loop filter	$\frac{T(s)K_\emptyset\,K_{vco}}{S\,N}$
G(s)	The close loop gain of the loop filter	$\frac{O(s)}{1 + O(s)}$
R2	Resistor 2 of the 3rd order loop filter	$\frac{A2}{T2C1C3}$
C3	Capacitor 3 of the 3rd order loop filter	$\frac{-T2^2\,C1^2 + T2\,A1\,C1 - A2\,A0}{T2^2C1 - A2}$
T3	The second pole in the 3rd order loop filter transfer function	T1 T31
A1	The loop filter coefficient	A0(T1+T3)
A2	The loop filter coefficient	A0 T1T3

3.4 Forth- Order Loop Filter Design

Forth order loop filters have a more complex design and it provided more circuit stability which it added three poles to the filter transfer function. Also, it provided an efficient filtering operation for the spurs noise that occurs at a frequency distance equal to twenty times of the loop bandwidth [118]. Figure (3-4) illustrate the basic design of the fourth-order loop filter that is used in this thesis using the ADS program.

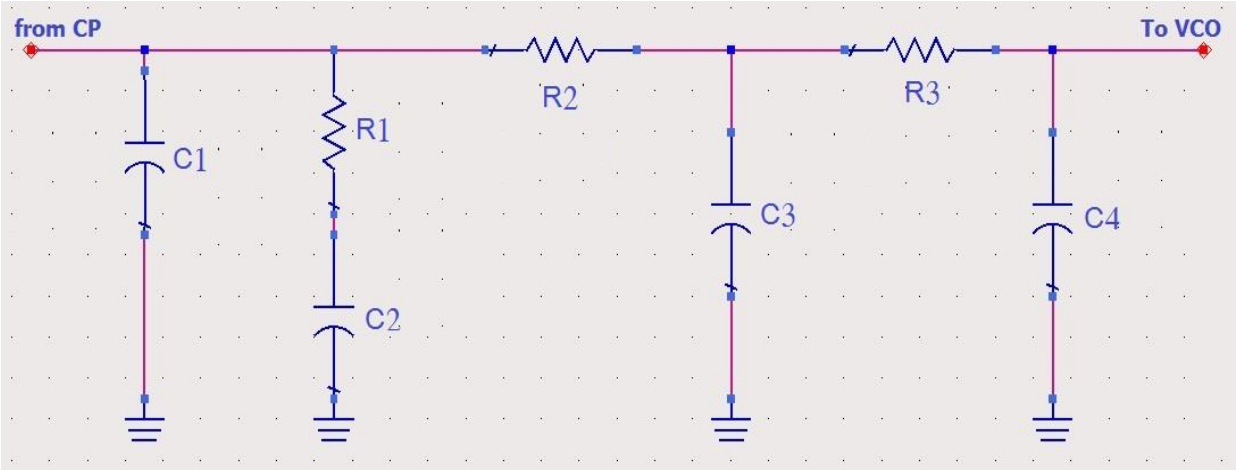


Figure 3-4: Forth Order Loop Filter Design in ADS

Fourth order filter design was based on the following equations:

T1: It found by numerical solution in MATLAB after that can easily find the zero (T2), pole(*T3*), and pole (*T4*)

$$T3 = T1.T31 \quad (3\text{-}1)$$

$$T4 = T1.T31.T43 \quad (3\text{-}2)$$

After finding the values of zero and poles, the loop filter coefficients A0, A2 and A3, in addition to the values of the resistors and capacitors of the fourth order loop filter R2, R3, R4, C1, C2, C3, and C4 can be found by applying the series of equations in appendix A [118].

3.5 First Order Single Loop Σ-Δ Modulator Design

This modulator is implemented by one accumulator and a single-bit quantizer that produces either zero or one. This type of modulator is similar in working the accumulator illustrated in chapter two.

Therefore, sometimes the accumulator block is called a first-order Sigma-Delta modulator. Figure (3-5) illustrate the basic design of the first-order single loop Σ-Δ modulator that is used in this thesis using the ADS program. The relationship between the modulator input and output can be represented in the following equation [16]:

$$Vo = Vi.z^{-1} + Q(z)\,(1-z^{-1}) \qquad (3\text{-}3)$$

$$NTF = (1-z^{-1}) \qquad (3\text{-}4)$$

Where *Vi* is the input voltage, *Vo* is the output voltage of the modulator, *Q(z)* is the noise produced by the accumulation process, and NTF is noise transfer function.

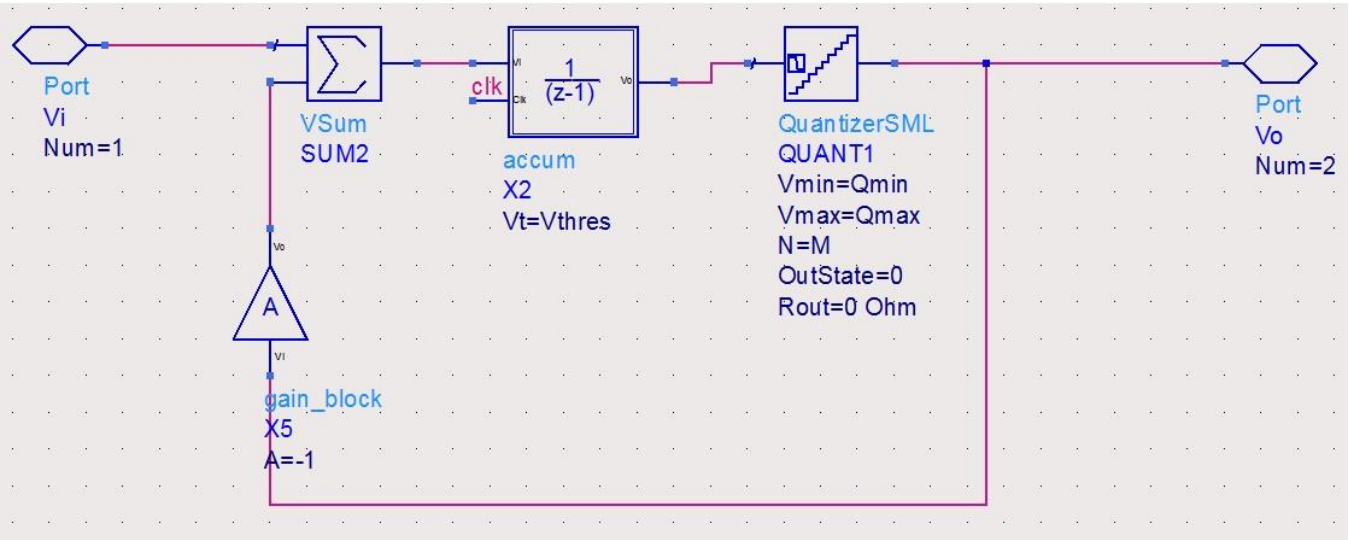


Figure 3-5: First order single loop Σ-Δ modulator design.

3.6 Second-Order Single Loop Σ-Δ Modulator Design.

The order of the modulator is according to the number of the accumulator blocks that will be used in the circuit. So the second- order single loop sigma-delta modulator is consisting of two accumulators, two-loop gains, and a multi-bit quantizer that produces the output signal ranging between two values (-1 and 2) due to the two accumulator blocks. Figure (3-6) illustrates the basic design of the second-order single loop Σ-Δ modulator that is used in this thesis using the ADS program. The following equations are representing the relationship between the modulator input, output and the noise transfer function NTF [119]:

$$[(((Vi - Vo)\frac{1}{z-1}) - 2\,Vo).\frac{1}{z-1}] + Q(z) = Vo \qquad (3\text{-}5)$$

$$Vi.\frac{z^{-2}}{(1-z^{-1})^2} - V0.\frac{z^{-2}}{(1-z^{-1})^2} - 2\,Vo.\frac{z^{-1}}{1-z^{-1}} + Q(z) = Vo \qquad (3\text{-}6)$$

$$Vo.[1+\frac{2.z^{-1}}{1-z^{-1}} + \frac{z^{-2}}{(1-z^{-1})^2}] = Vi\,\frac{z^{-2}}{(1-z^{-1})^2} + Q(z) \qquad (3\text{-}7)$$

$$Vo = Vi.z^{-2} + Q(z).(1 - z^{-1})^2 \qquad (3\text{-}8)$$

$$NTF = (1 - z^{-1})^2 \qquad (3\text{-}9)$$

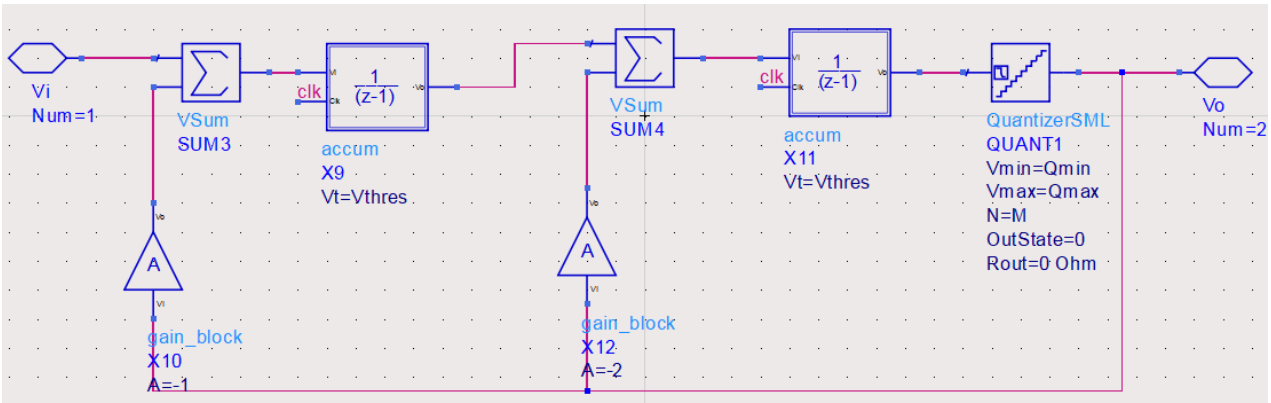


Figure 3-6: Second order single loop Σ-Δ modulator design

3.7 Third-Order single loop Σ-Δ modulator design

In this type of modulator, there are three accumulators (three integrated circuits), three-loop gains with a single multi-bit quantizer. The importance of using the modulators is to decrease the phase noise at low frequencies. Figure (3-7) illustrates the basic design of the third-order single loop Sigma-Delta Modulator that is used in this thesis using the ADS program. The relationship between the modulator input, output, and NTF for the third – order Σ-Δ modulator are representing in the following [96]:

$$[((Vi - Vo)\frac{1}{z-1} - 3.125\ Vo).\frac{1}{z-1} - 3\ Vo]\frac{1}{z-1} + Q(z) = Vo \qquad (3\text{-}10)$$

$$[((Vi - Vo)\frac{z^{-1}}{1-z^{-1}} - 3.125Vo)\frac{z^{-1}}{1-z^{-1}} - 3\ Vo]\ \frac{z^{-1}}{1-z^{-1}} + Q(z) = Vo \qquad (3\text{-}11)$$

$$Vi\frac{z^{-3}}{(1-z^{-1})^{-3}} - Vo\frac{z^{-3}}{(1-z^{-1})^{-3}} - 3.125Vo\frac{z^{-2}}{(1-z^{-1})^{-2}} - 3Vo\frac{z^{-1}}{1-z^{-1}} + Q(z) = Vo \qquad (3\text{-}12)$$

$$Vo[1+\frac{z^{-3}}{(1-z^{-1})^{-3}} + 3.125\frac{z^{-2}}{(1-z^{-1})^{-2}} + 3\frac{z^{-1}}{1-z^{-1}}] = Q(z) + Vi\frac{z^{-3}}{(1-z^{-1})^{-3}} \qquad (3\text{-}13)$$

$$NTF = \frac{(1-z^{-1})^3}{1+0.125\ z^{-2} - 0.125\ z^{-3}} \qquad (3\text{-}14)$$

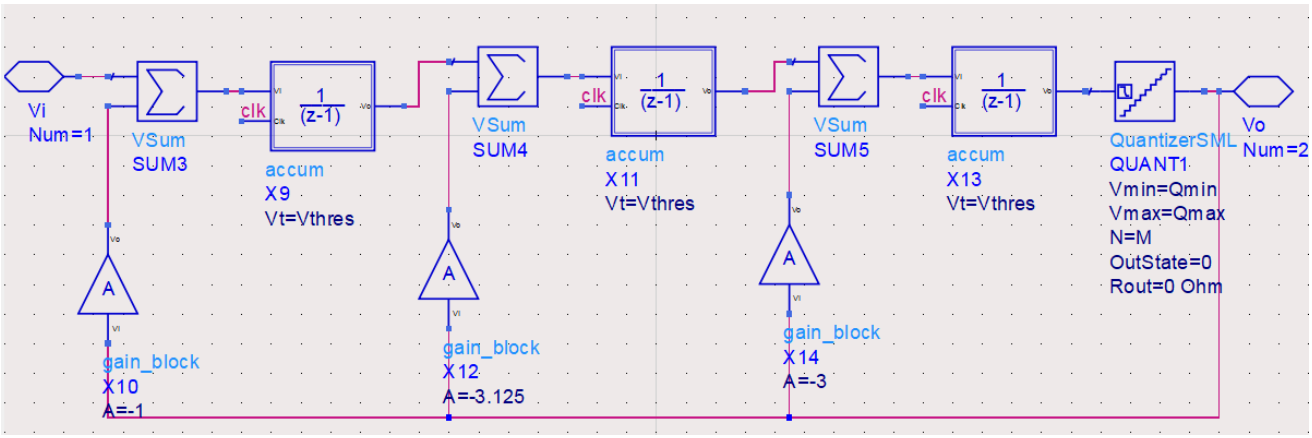


Figure 3-7: Third order single loop Σ-Δ modulator design

In the next chapter, the simulation result and discussion of the three designed Fractional-NPLL circuits [Fractional N-PLL circuit with a second-order loop filter and a first-order sigma-delta modulation, Fractional N-PLL circuit with a third-order loop filter and second-order sigma-delta modulation, and Fractional N-PLL circuit with a fourth-order loop filter and third-order sigma-delta modulation] will be presented.

CHAPTER FOUR

Simulation Results and Discussion

4.1 Introduction

Based on what was discussed in chapter three, that there are three structures designed for the frequency synthesizer circuit (Fractional N-PLL circuit with a 2^{nd} order loop filter and a 1^{st} order Σ-Δ modulator, Fractional N-PLL circuit with a 3^{rd} order loop filter and a 2^{nd} order Σ-Δ modulator, and a Fractional N-PLL circuit with a 4^{th} order loop filter and a 3^{rd} order Σ-Δ modulator) for the purpose of choosing the optimal design that suits the requirements of the Bluetooth application. In this chapter, the simulation results of the frequency response for the Fractional-NPLL circuits will show the results of the circuit designed using (MATLAB2020b, ADS2017) programs, where the MATLAB program was used to (find the component values of the filters of the frequency synthesizer circuits which are the capacitors and resistors at each values of the frequency bandwidth and for each phase margin, also the filter impedance, open loop and closed loop gain). Where the filter was designed with three orders second, third and fourth, in addition to displaying and comparing the simulation results of the amplitude and phase of the frequency response for each filter. Then the designed filters were connected to the Fractional N-PLL circuits by ADS design program. In additional, the results were presented and comparisons were made to simulate the frequency response of the frequency synthesizer circuits and the results of simulating the noise response (spurs noise, phase noise, settling time, output spectrum). Furthermore, simulation results of designing the sigma-delta modulator for each designed circuit.

4.2 Simulation Results of the 1st Proposed Frequency Synthesizer Circuit.

This section will show and discuss the simulation results of the first design of a Fractional N-PLL circuit with a 2nd order loop filter and a 1st order Σ-Δ modulator ,where a MATLAB program was used to design a frequency synthesizer circuit second order loop filter based on the equations in table(3-2) ,and by applying the design factors [118] K_{vco}=210 MHz/V, K_{ϕ}=50 mA, F_{ref}=19.2MHz (table 3-1) , the selection of the bandwidth was based on the relationship BW≤ $0.25F_{ref}$ [12], and therefore more than one value of the bandwidth were chosen (50,75,125,250, and 500) kHz, in order to select the appropriate bandwidth that gives the best results .The design are chosen for each value of the phase margin (30°,35°,40°,47°,57°,65°,70°), where the values of the second order filter component are shown in the table (4-1).

Table 4-1: 2nd order loop filter component values

PM (degree)	Filter component values R (KΩ), C (PF)														
	BW=50KHz			BW=75KHz			BW=125KHz			BW=250KHz			BW=500kHz		
	R1	**C1**	**C2**	**R1**	**C1**	**C2**	**R1**	**C1**	**C2**	**R1**	**C1**	**C2**	**R1**	**C1**	**C2**
30	5.61	491	982	8.4	218	436	14	78.6	157	28	20	39	56	4.9	9.8
35	5	443	1191	8	197	529	12.8	71	191	26	17.7	48	51	4.4	11.9
40	4.77	396	1428	7	176	634	11.9	63.5	228	24	16	57	48	4	14
47	4.42	335	1825	6.6	149	811	11	53.6	292	22	13.4	73	44	3.3	18
57	4	252	2621	6	112	1165	10	40	419	20.5	10.1	104	41	2.5	26
65	3.9	188	3650	6	84	1622	9.8	30	584	20	7.5	146	39	1.9	36.5
70	3.86	150	4676	6	67	2078	9.6	24	748	19.3	6	187	38.6	1.5	47

The value of the phase margin ranges between 30°and 70°, the value of the PM is usually chosen between 45° and 55°[118], to make the system more stable .The magnitude and phase frequency response of the second order loop filter was found by finding the value of the filter transfer function T(s) , and then applying the rule of the open loop circuit gain function O(s) to find the phase response of the filter, and the rule of the close loop circuit gain function G(s) to find the magnitude frequency response of the filter.

4.2.1 Simulation Results of the 1st Proposed Frequency Synthesizer Circuit at PM=47°

This section includes the simulation of the Fractional N-PLL circuit with a 2nd order loop filter and a 1st order Σ-Δ modulator under varying three values of the bandwidth 250 KHz, 125 KHz and 75 KHz. At the same value of phase margin that is equal to 47°, the design process included three stages, the first stage was in the section (4-2-1-1) that included the simulation results of design a second-order loop filter for the first proposed Frequency Synthesizer circuit at 75,125,250 -KHz using MATLAB, while the second stage was in the section (4-2-1-2) that included the simulation of the first-order sigma-delta modulator using ADS .The third stage was in the section (4-2-1-3) that include the simulation result(output spectrum and the settling time) of the Fractional N-PLL circuit using ADS at (250,125,75-KHz).

4.2.1.1 Simulation Results of The 1st Proposed Frequency Synthesizer at PM=47° Using MATLAB

A second-order loop filter for the first proposed frequency synthesizer circuit is designed at three values of the bandwidth 75,125 and 250 –KHz at 47° phase margin. Then the frequency response of the first proposed

frequency synthesizer circuit using MATLAB program was shown in figure (4-1) and figure (4-2).

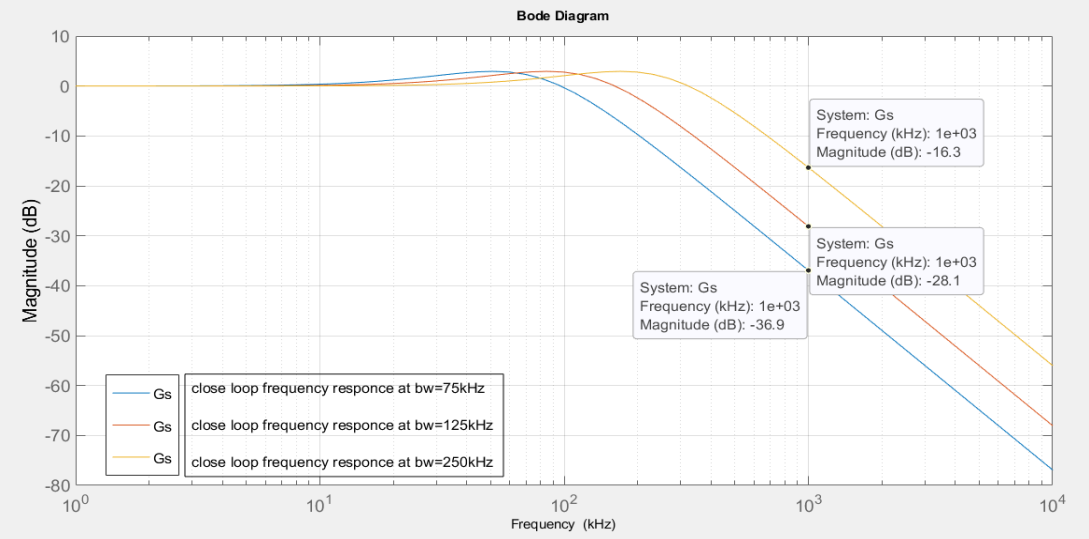


Figure 4-1: Frequency response magnitude for the 1st proposed frequency synthesizer at PM=47°

It is noted from the figure (4-1) that increasing the bandwidth doesn't improve the amplitude-frequency response gain. Also, it is noted that the values of the response gain will become unwanted values at high frequencies ≥ 1MHz, and it's one of the characteristics of low-pass filter. Furthermore, when the slope gain is in the stopband region the frequency response is faster to go down. Therefore, it should choose a low value of bandwidth to give the best frequency response as shown in the table (4-2).

Table 4-2: Magnitude frequency response comparison for the 1st proposed frequency synthesizer at PM=47°

Frequency (MHz)	Close loop Transfer function magnitude (dB)		
	BW=75KHz	BW=125KHz	BW=250KHz
1	-36.9	-28.1	-16.3
10	-76.9	-68	-56
100	-117	-108	-96

Table 4-2 shows a close-loop comparison between the magnitude frequency response for the first proposed frequency synthesizer at 75,125,250- kHz bandwidth. Where the magnitude frequency response for proposed frequency synthesizer at 75 kHz bandwidth is equal to -117 dB at 100 MHz offset frequency and it is better than the frequency response for proposed frequency synthesizer at 125 kHz and 250 kHz which are equal to -108 dB and -96 dB respectively.

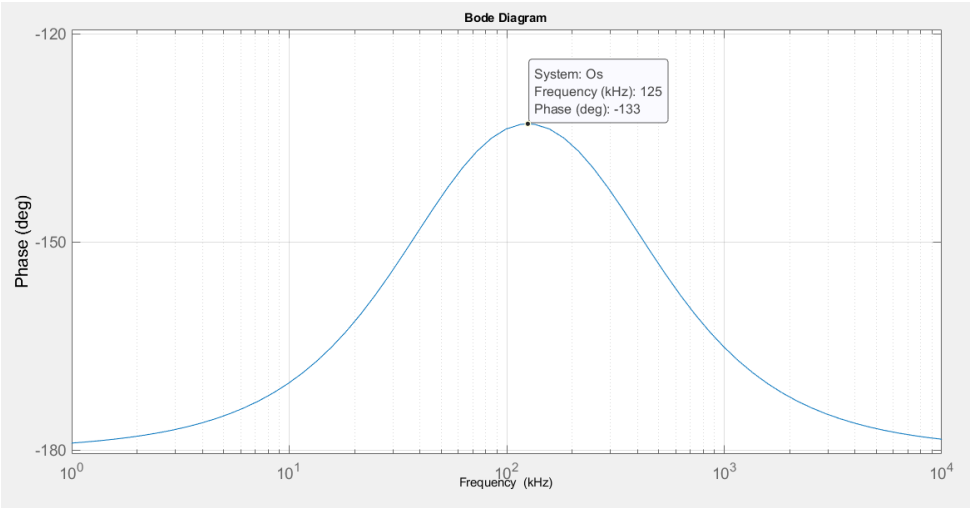


Figure 4-2: Frequency response phase for the 1st proposed frequency synthesizer at PM=47°

It can be noted from the figure (4-2) that the phase of the open-loop transfer function is equal to -133˚, then the change in open-loop phase needed to make a closed-loop system stable is the phase margin it can be easily calculated by the following equation [118]:

$$Phase\ Margin = 180^{\circ} - |phase\ of\ open\ Loop\ T.f\ (in\ deg)| \quad (4\text{-}1)$$

Where the phase margin is equal to 47˚at 125 kHz and it is the same value that was selected in the design process.

4.2.1.2 Simulation Result of the 1st order Σ-Δ Modulator

The sigma-delta modulator is considered one of the necessary parts of the Fractional- NPLL circuit. The order of the Σ-Δ Modulator was chosen to be less than the order of the loop filter. By applying the equation (2-15) and with depending on the values chosen for the design, the input value of the modulator will be:

$$F_{vco} = (N_{int} + \Delta N).F_{ref} \quad (2\text{-}15)$$

$$\frac{F_{vco}}{F_{ref}} = N_{int} + \Delta N = \frac{2420}{19.2} = 125.1041667$$

Where $N_{int} = 125$ represent the integer part of the division product ,and $\Delta N = 0.1041667$ represent the fractional part of the division product and it is the input value of the modulator. The product of dividing the frequency synthesizer's output frequency (F_{vco}) by its input frequency (F_{ref}) can be depicted in the figure (4-3) using ADS program.

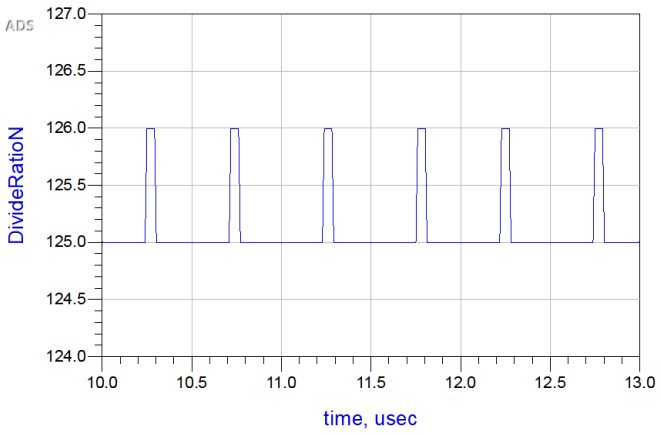


Figure 4-3: Total division ratio of the 1st proposed frequency synthesizer.

It can be noted from figure (4-3) that the division ratio ranges between two consecutive integers values (125) and (126) to produce the required total division ratio (125.1041667) ,where the output of the modulator can be represented in figure (4-4)[9].

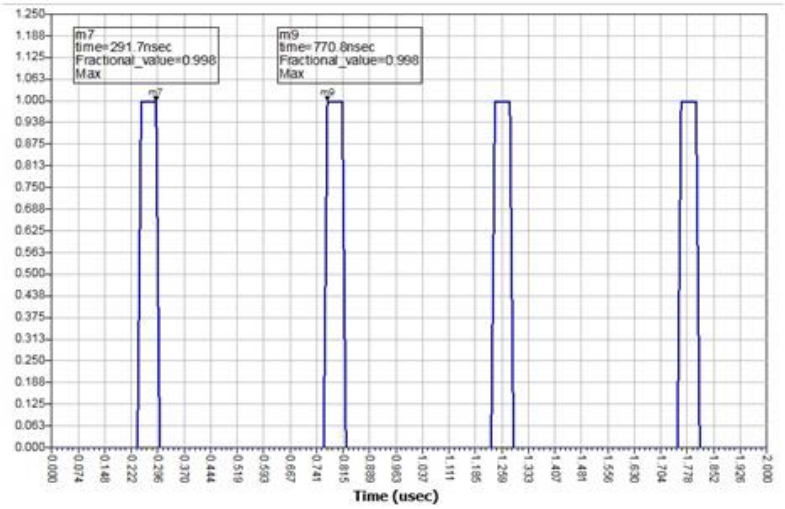


Figure 4-4: Output of the 1st order Σ-Δ modulator [9].

It is noted from figure (4-4) there will be only two levels of the modulator output signal (zero and one) with an interval of 479.1 nsec between the output samples. Where the repeated change of the fractional deviation ratio between the values zero and one will lead generation to the fractional spurs

noise in the output spectrum of the modulator as shown in the figure (4-5), which affects the frequency synthesizer output signal quality.

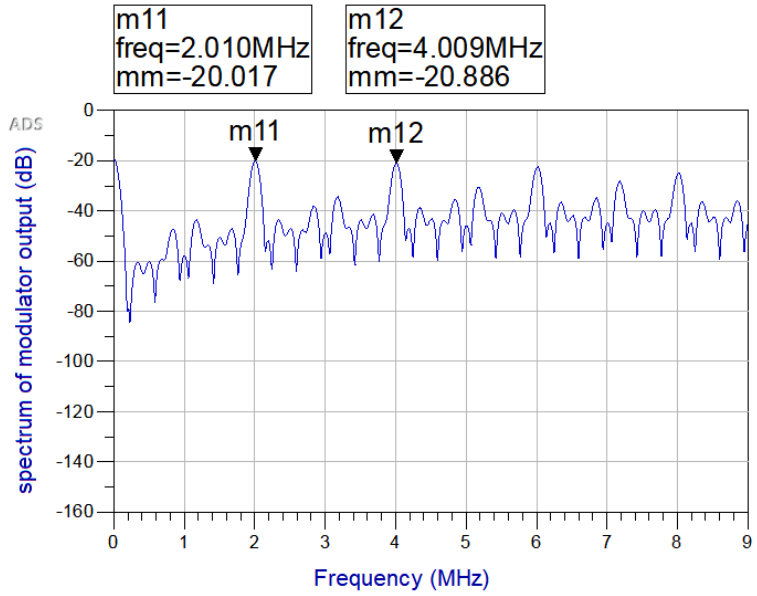


Figure 4-5: Output spectrum the1st order Σ-Δ modulator

It is noted from figure (4-5) that the fractional spurs noise will appear every 2MHz of the spectrum signal output which meaning at2MHZ,4MHZ ,6MHZ etc. Due to the offset time will equal to 497.1 nsec then the offset frequency will be equal to 1/497.1 nsec and that equals to approximately 2MHz.

4.2.1.3 Simulation Results of the 1st Proposed Frequency Synthesizer at PM=47° Using ADS Program

In this section the simulation results of the designed circuit at 250,125 and75-KHz bandwidth with 47° phase margin will be shown, which are output spectrum and the settling time. They are measured for each filter designed.

4.2.1.3.1 Output Spectrum and The Settling Time of The 1st Proposed Frequency Synthesizer at BW=250KHz

The output spectrum of the first proposed frequency synthesizer circuit at 47° phase margin and 250KHz bandwidth is show in figure 4-6

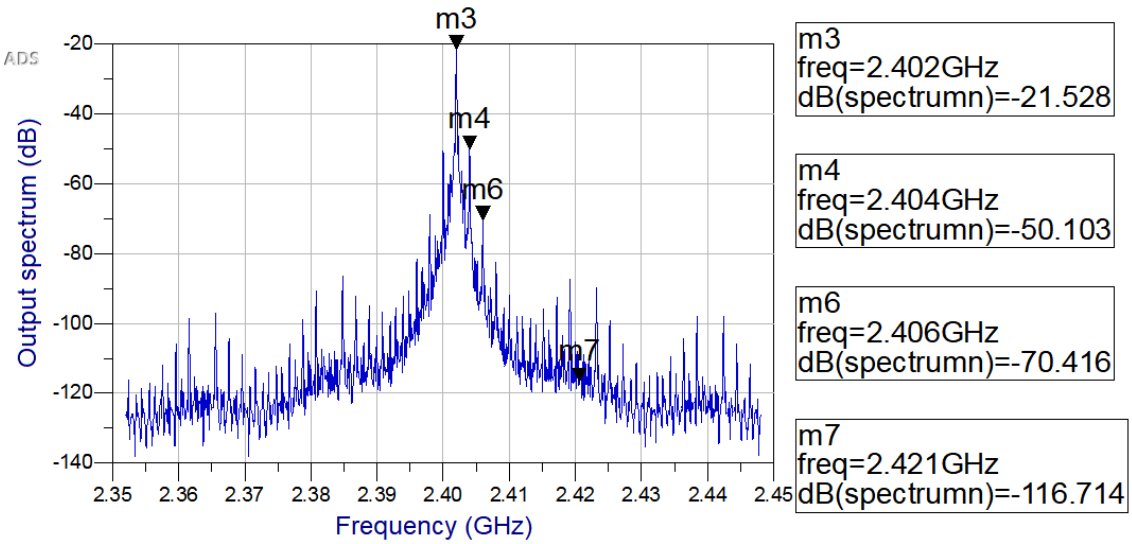


Figure 4-6: Output spectrum of the 1st proposed frequency synthesizer

It is noted from figure (4-6) that the designed circuit has a not good behavior for the output spectrum due to the containing of large values of the noises (fractional spurs noise, reference spurs noise, and the phase noise). The spurs noise levels can be measured by the following equation (4-2) [118].

$$Spurs\ Level = P\_Noise_{(at\ offset\ freq)} - P\_Carrier \qquad (4\text{-}2)$$

Where $P\_Noise_{(at\ offset\ freq)}$ is the power of the noise signal at a particular frequency offsets, $P\_Carrier$ is the power of the carrier signal.

Then the first level of fractional spur noise will appears in figure (4-6) at 2 MHz frequency offsets and it is equal to -28.575 dBc, while the first level of reference spur noise will appear at 19.2 MHz frequency offsets and it is

equal to -95.186 dBc .The phase noise will also measure depending on the equation (4-2) [118].

$$Phase\ Noise\ (PN) = (P\_Noise_{(at\ offset\ freq)} - P\_Carrier\ - 10\ log\ (1.2\ *RBW)\ +\ 1.05\ dB + 1.45\ dB) \qquad (4\text{-}3)$$

Where RBW is the bandwidth resolution of the spectrum analyzer, the number 1.05 is the detector response value for the spectrum analyzer, and 1,45 represent the Logarithmic pressure of the noise signal of the Gaussian-type spectrum analyzer.

Then the phase noise will equal -81.924 dBc/Hz at 2 MHz frequency offsets. While it equal to -116.818 dBc/Hz at 3 MHz frequency offsets. Within the Bluetooth system's requirements, these values are considered undesirable, as the phase noise value must be equal -110 dBc at 2 MHz frequency offsets and -119 dBc at 3 MHz frequency offset. Also, it is necessary to calculate the time it takes for the oscillator output signal to reach a steady state during the transition from one channel to another and thus, the speed of the performance of the frequency synthesizer circuit. Figure (4-7) shows the values of the settling time response for the first proposed frequency synthesizer at 250 KHz bandwidth and 47° phase margin.

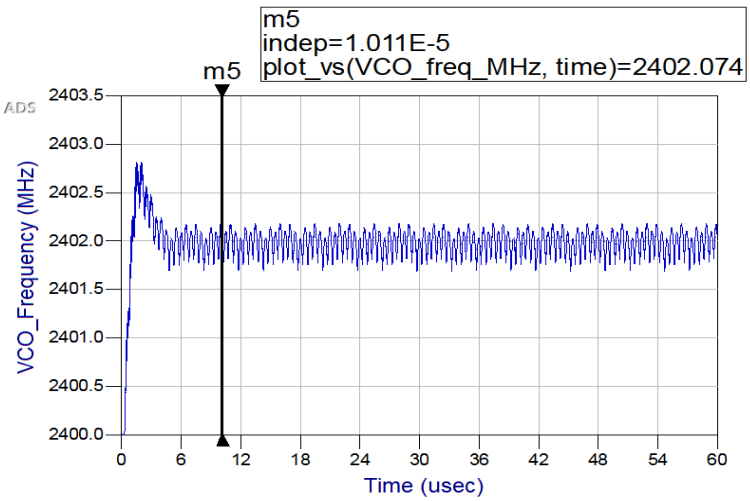


Figure 4-7: Output frequency of the 1st proposed frequency synthesizer

It is noted from figure (4-7) that the designed circuit has a good stability time value and is acceptable in the Bluetooth system which is approximately 10.11 ≤220 μsec, but this designed circuit is still inefficient because it contains a high level of spurs noise and phase noise, in addition to the fact that the error rate of the output frequency signal of the designed circuit was within 74 kHz which is (2402.074-2402) MHz .

Therefore, the bandwidth of the designed circuit was decreased to 125kHz and then to 75kHz, in order to observe the effect of bandwidth on the level of the spurs noise and phase noise in the output spectrum of the frequency synthesizer designed circuit, in addition to the response of the settling time.

4.2.1.3.2 Output Spectrum and The Settling Time of The 1st Proposed Frequency Synthesizer at BW= 125KHz

The output spectrum of the first proposed frequency synthesizer circuit at 47° phase margin and 125KHz bandwidth is show in figure (4-8).

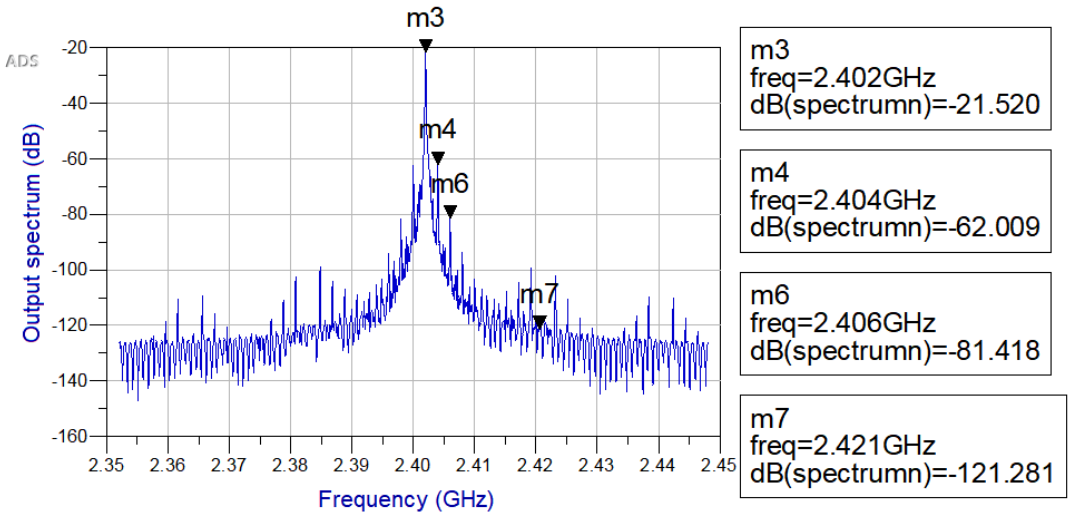


Figure 4-8: Output spectrum of the 1st proposed frequency synthesizer.

It can be observed that reducing the bandwidth improves the frequency response of the filter, and hence the level of spurs noise, and phase noises, where the value of the reference spurs noise will become -99.761 dBc, the fractional spurs noise will become -40.489 dBc and the phase noise will become -93.838 dBc at 2MHz offset frequency and -125.787 dBc at 3MHz offset frequency. Despite the improvement in the noise power values of the synthesizer designed circuit, these values are still unacceptable within the Bluetooth system's limits. The value of the settling time of the first proposed frequency synthesizer circuit at 125 KHz bandwidth and 47° phase margin was found in the figure (4-9).

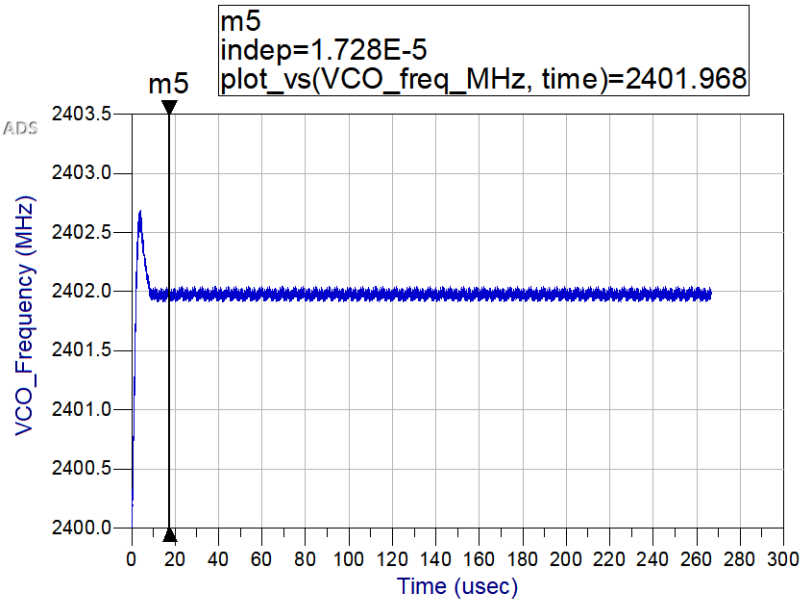


Figure 4-9: Output frequency of the 1st proposed frequency synthesizer.

The value of the settling time has been taken form the curve directly by observation at the point of reaching the steady state performance. This procedure has been applied to the settling time values throughout the rest of this thesis. It can be seen from figure (4-9) that the output frequency signal of the designed circuit will reach a steady-state at the value of time

approximately equal to 17.28 µsec with 32 KHz error rate of the output signal frequency, where the output signal frequency is equal to 2401.968 MHz, this value of error is better than the error signal of the output frequency for the previous design. The value of the settling time for this design is still accepted in the Bluetooth system limited , but the value of the settling time was increased when the bandwidth is decreased to 125 kHz where the value of the settling time was 10.11 µsec at 250 kHz bandwidth.

4.2.1.3.3 Output Spectrum and the Settling Time of The 1st Proposed Frequency Synthesizer at BW= 75KHz

The output spectrum of the first proposed frequency synthesizer circuit at 47° phase margin and 75KHz bandwidth is show in figure (4-10)

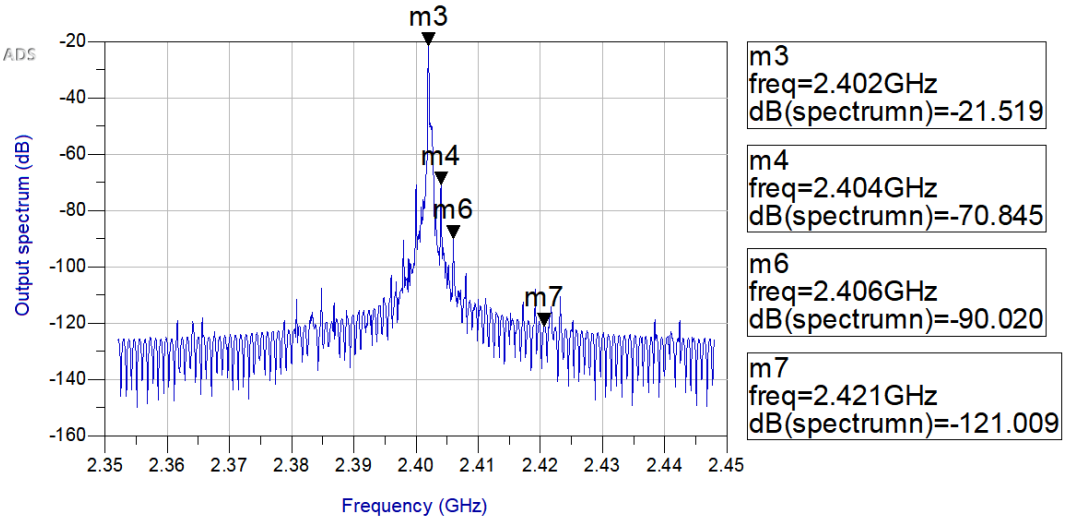


Figure 4-10: **Output spectrum of the 1st proposed frequency synthesizer**

It can be observed from figure (4-10) that reducing the bandwidth to 75 kHz give output frequency signal with improved noise level than the previous two design of the frequency synthesizer at 250 kHz and 125 kHz. The following table (4-3) is a presentation of the noise power comparison

(phase noise, fractional noise, reference noise) for the Fractional N-PLL circuit with a second-order loop filter and a first-order sigma-delta modulator at (250,125 and75- kHz) bandwidth and 47° phase margin.

Table 4-3: Noise power comparison for the 1st proposed frequency synthesizer at PM= 47°

Bandwidth KHz	Noise Power				
	Phase Noise dBc/Hz		Reference Spurs Noise dBc	Fractional Spurs Noise dBc	
	Offset frequency= 2MHz	Offset frequency= 3MHz	Offset frequency= 19.2MHz	Offset frequency= 2MHz	Offset frequency 4MHz
75	-102.765	-127.221	-99.481	-49.323	-68.496
125	-93.843	-125.787	-99.77	-40.494	-59.904
250	-81.924	-116.819	-95.186	-28.575	-48.894

It is noted from table (4-3) that the Fractional N-PLL circuit with a second-order loop filter and a first-order sigma-delta modulator (1st proposed frequency synthesizer) have better noise performance (low values of Phase Noise, Reference Spurs Noise, Fractional Spurs Noise) at 75 KHz bandwidth because the magnitude frequency response of the frequency synthesizer circuit is improved at low values of bandwidth

Also, the time steady state of the 1st proposed frequency synthesizer is measured in the following figure (4-11).

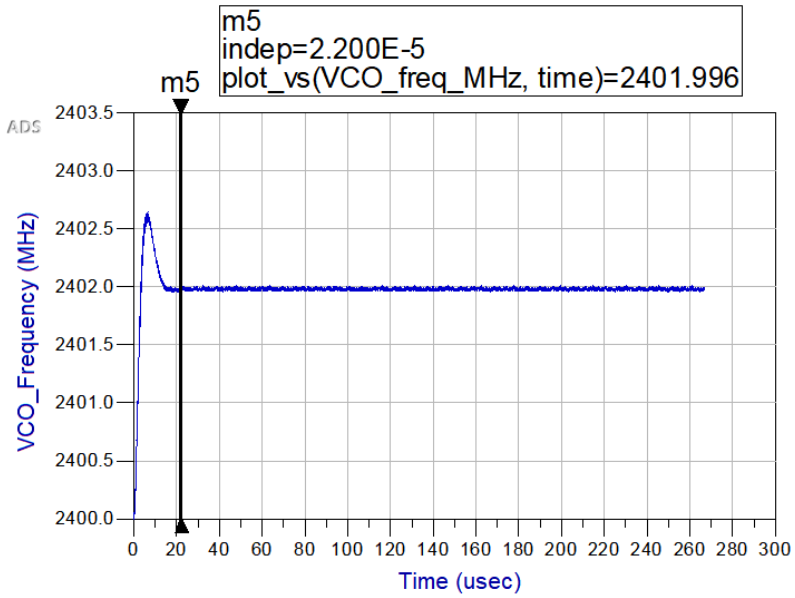


Figure 4-11: Output frequency of the 1st proposed frequency synthesizer

It can be seen from figure (4-11) that the output frequency signal of the designed circuit at 75 kHz Bandwidth will reach a steady-state at the value of the time equal to 22 µsec with 4 KHz error ratio in the output signal frequency, where the output signal frequency is equal to 2401.996 MHz . It is possible to compare the value of the settling time and the frequency accuracy of the frequency synthesizer output signal for the three designed circuits of the Fractional N-PLL at (250,125 and75- kHz) bandwidth and 47° phase margin in the flowing table (4-4).

Table 4-4: Settling time and the accuracy comparison for the 1st proposed frequency synthesizer at PM= 47°

Bandwidth (KHz)	Settling Time (µsec)	Output frequency accurate(KHz)
250	10.11	74
125	17.28	32
75	22	4

It is noted from the table (4-4) that the Fractional N-PLL circuit with a second-order loop filter and a first-order sigma-delta modulator has the best value of the settling time at 250 KHz bandwidth where the settling time decreases with increasing the bandwidth, but the accuracy of the output frequency of the circuit was not good for this design. So the work was done to increase the value of the phase margin to 57°, to improve the accuracy of the output frequency signal and to get the best value of the settling time.

4.2.2 Simulation Results of The 1st Proposed Frequency Synthesizer Circuit at PM=57°.

This section includes the simulation results of the Fractional N-PLL circuit with a 2nd order loop filter and a 1st sigma-delta modulator under effecting three values of the bandwidth 75,125 and 250-kHz. At the same value of phase margin that is equal to 57°. There are two parts in this section, where in (4-2-2-1) will show the simulation results of the second-order loop filter at 75,125,250 -kHz using the MATLAB program, while in (4-2-2-2) will show the simulation result (output spectrum and the settling time) of the Fractional N-PLL circuit using ADS program at (75,125,250-kHz) and 57° phase margin.

4.2.2.1 Simulation Results of The 1st Proposed Frequency Synthesizer at PM=57° Using MATLAB

A second-order loop filter for the first proposed frequency synthesizer circuit is designed at three values of the bandwidth 75,125 and 250 –kHz at 57° phase margin. Then the frequency response of the first proposed frequency synthesizer circuit using the MATLAB program is shown in figure (4-12) and figure (4-13).

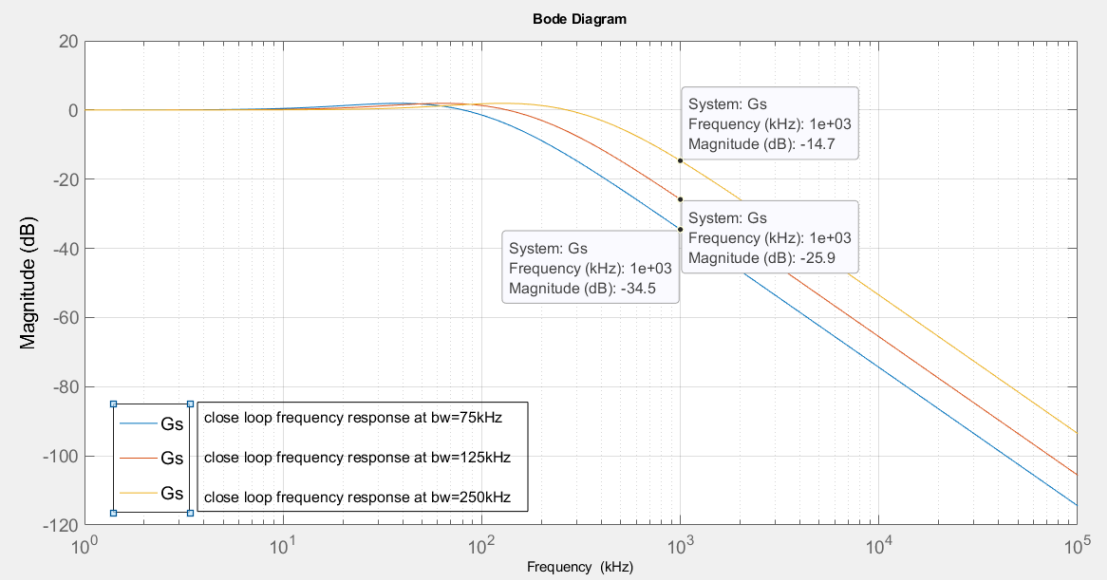


Figure 4-12: Frequency response magnitude for the 1st proposed frequency synthesizer at PM=57°

It is noted from the figure (4-12) that at small values of the bandwidth the spurs noise is eliminated more effectively because the slope gain is faster to go down and the frequency response is quickly reduced due to the second-order filter. Furthermore, raising the phase margin values will not improve the frequency response gain at high frequencies as seen in the Table (4-5).

Table 4-5: Magnitude frequency response comparison for the 1st proposed frequency synthesizer at PM=57°

Frequency (MHz)	Close loop Transfer function magnitude (dB)		
	BW=75KHz	BW=125KHz	BW=250KHz
1	-34.5	-25.9	-14.7
10	-74.4	-65.6	-53.5
100	-114	-106	-93.5

Table 4-5 shows a close-loop comparison between the magnitude frequency response for the first proposed frequency synthesizer at 75,125,250- kHz bandwidth and 57° phase margin. Where the magnitude frequency response for proposed frequency synthesizer at 75 kHz bandwidth is equal to -114 dB at 100 MHz offset frequency and it is better than the frequency response for proposed frequency synthesizer at 125KHz and 250 kHz which are equal to -106 dB and -93.5 dB respectively.

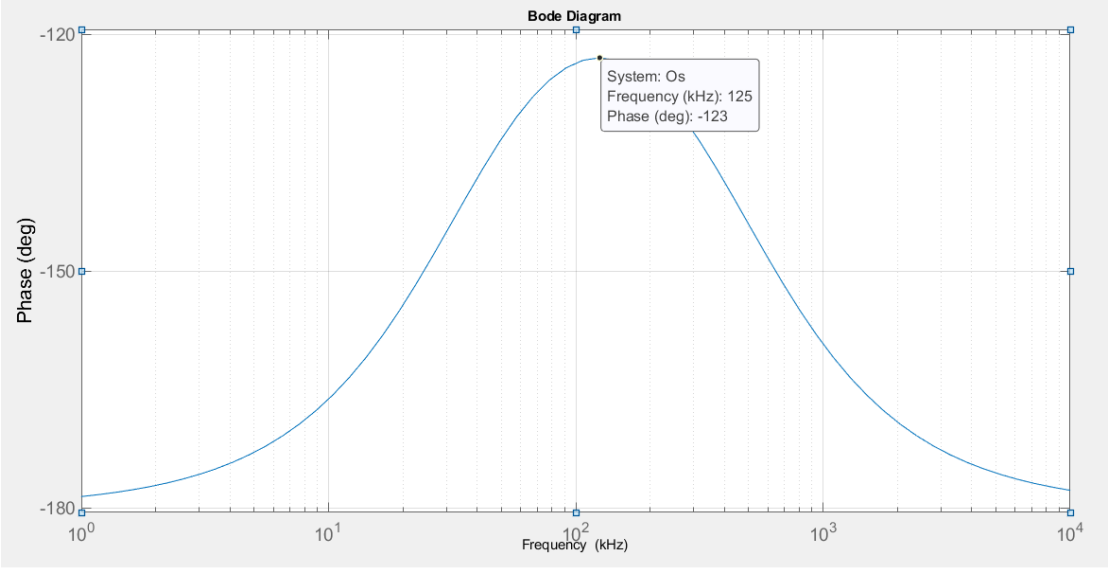


Figure 4-13: **Frequency response phase for the 1st proposed frequency synthesizer at PM=57°**

It can be noted from figure (4-13) that the phase of open loop transfer function equal -123˚ at a bandwidth of 125 kHz. Then the phase margin of the 1st proposed frequency synthesizer circuit is equal to 57˚ and it is the same value that was selected in the design process.

4.2.2.2 Simulation Results of The 1st Proposed Frequency Synthesizer at PM=57° Using ADS.

In this section, the simulation results (output spectrum and the settling time) of the first proposed circuit at 250,125 and75 -kHz bandwidth with 57° phase margin will be shown using ADS program.

4.2.2.2.1 Output Spectrum of The 1st Proposed Frequency Synthesizer at BW=75KHz

The output spectrum of the designed circuit at 75KHz bandwidth and 57° phase margin is show in figure 4-14.

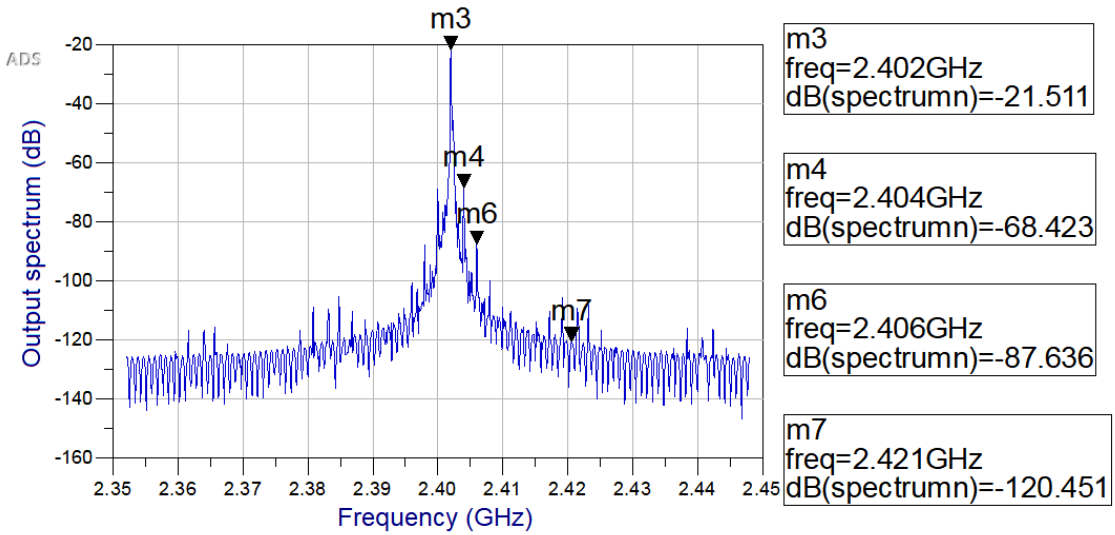


Figure 4-14: Output spectrum of the 1st proposed frequency synthesizer.

It can be seen from figure (4-14) that increase the phase margin led to an increase in the phase noise level, due to an increase in the magnitude frequency response at the high frequencies of the filter as explained in table (4-5) The noise power comparison (phase noise, fractional noise, reference noise) for the designed circuit at 47° phase margin with the noise power for the designed circuit at 57°phase margin are explained in table (4-6).

Table 4-6: Noise power comparison for the 1st proposed frequency synthesizer at PM= 47°and PM= 57°

	1st proposed frequency synthesizer at PM= 47°					**1st proposed frequency synthesizer at PM= 57°**				
	Phase Noise (dBc/Hz)		Reference Spurs Noise (dBc)	Fractional Spurs Noise (dBc)		Phase Noise (dBc/Hz)		Reference Spurs Noise (dBc)	Fractional Spurs Noise (dBc)	
BW (KHz)	**@ 2MHz**	**@ 3MHz**	**@ 19.2MHz**	**@ 2MHz**	**@ 4MHz**	**@ 2MHz**	**@ 3MHz**	**@ 19.2MHz**	**@ 2MHz**	**@ 4MHz**
75	-102.76	-127.22	-99.48	-49.32	-68.49	-100	-127	-98.98	-46.89	-66.18
125	-93.84	-125.78	-99.77	-40.49	-59.90	-91.4	-125.3	-99.98	-38	-57.6
250	-81.92	-116.81	-95.18	-28.57	-48.89	-79.7	-112.6	-94.05	-26.4	-46.77

It is noted from the table (4-6) that the Fractional N-PLL circuit with a 2nd order loop filter and a 1st order Σ-Δ modulator design was not efficient in terms of the value of the phase noise and the fractional spurs noise, where it

was give the lowest value of the phase noise and the fractional spurs noise at a bandwidth of 75 kHz and a phase margin of 47°, and this values was still unacceptable in the Bluetooth system.

4.2.2.2.2 Settling Time Response of The 1st Proposed Frequency Synthesizer at BW= 250 KHz

The effect of increasing a phase margin on the stability time of the designed circuit is chosen at the highest bandwidth of 250 KHz due to the inverse relationship between the bandwidth and the stability time, as the circuit becomes more stable at higher values of bandwidth. Figure (4-15) illustrates the magnitude of the settling time response for the Fractional N-PLL circuit with a second-order loop filter and a first-order sigma-delta modulator at 250 KHz bandwidth and 57° phase margin.

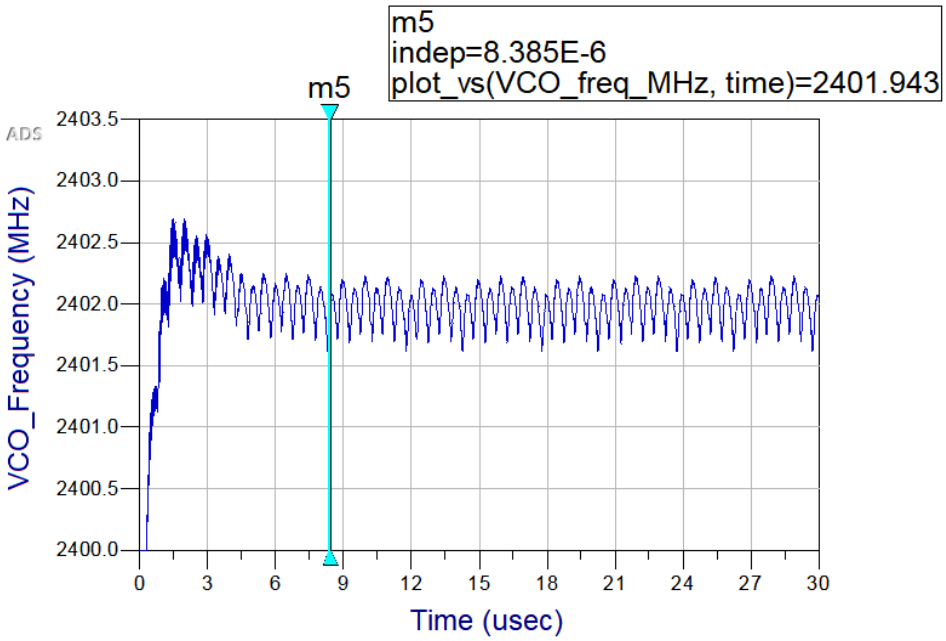


Figure 4-15: Output frequency of the 1st proposed frequency synthesizer

It can be seen from the figure (4-15) that the settling time is equal to 8.38 µsec by the amount of error 47 kHz, where the frequency of the outgoing

signal of the composite is equal to 2401.943 MHz, which is much better than the settling time of the circuit designed at 47° phase margin and 250 kHz bandwidth, which is approximately equal to 10.11 μsec by the accuracy of 74 kHz.

4.3 Simulation Results of The 2nd Proposed Frequency Synthesizer Circuit

Due to what was presented in the previous design of the frequency synthesizer circuit, it was noted that the design did not achieve acceptable and good results for the values of phase noise, fractional spurs noise and the reference spurs noise values. So, the order of the filter increased to reduce the phase noise values, as well as the increase in the order of the sigma-delta modulator to reduce the value of the fractional spurs noise to design a frequency synthesizer circuit called " Fractional N-PLL circuit with third-order loop filter and a second order sigma-delta modulator ", or "the 2nd proposed frequency synthesizer circuit". A MATLAB program was used to design a frequency synthesizer circuit 3rd order loop filter based on the equations in table (3-3) ,and by applying the values of the constants K_{vco}=210MHz/V, K_{ϕ}=50mA, F_{ref}=19.2MHz at different values of the bandwidth (75,125,250) kHz and for each value of the phase margin 47° and 57°,where the values of the capacitors and resistors of the third order loop filter are presented in the table (4-7).

Table 4-7: 3rd order loop filter component values

PM	Filter component values R(KΩ),C(PF)														
	BW=75 kHz					BW=125 kHz					BW=250 kHz				
	R1	**R2**	**C1**	**C2**	**C3**	**R1**	**R2**	**C1**	**C2**	**C3**	**R1**	**R2**	**C1**	**C2**	**C3**
47°	5.9	42	72	908	9.47	10	70	26	327	3.4	19.7	139	6.48	81.7	0.85
57°	5.77	43.6	53.6	1240	6.8	9.6	72	19	446	2.5	19.2	145	4.8	111.6	0.61

4.3.1 Simulation Results of The 2nd Proposed Frequency Synthesizer Circuit at PM=47°

This section includes the simulation results of the Fractional N-PLL circuit under effecting three values of the bandwidth 75,125 and 250-KHz at the same value of phase margin that is equal to 47°. The design process included three stages, the first stage was discussed in the section (4-3-1-1) which included the simulation results of the third-order loop filter at 75,125 and 250 -kHz using the MATLAB, while the second stage was in section (4-3-1-2) and it included the simulation results of the second-order Sigma-Delta Modulator using ADS, and the third stage was presented in the section (4-3-1-3) and it included the simulation result(output spectrum and the settling time) of the Fractional N-PLL circuit using ADS at 250 and 75-kHz.

4.3.1.1 Simulation Results of The 2nd Proposed Frequency Synthesizer at PM=47° Using MATLAB

A third-order loop filter for the second proposed frequency synthesizer circuit is designed at three values of the bandwidth 75,125 and 250 –kHz at 47° phase margin. The frequency response of the 2nd proposed frequency synthesizer circuit using MATLAB was shown in figure (4-16) and figure (4-17).

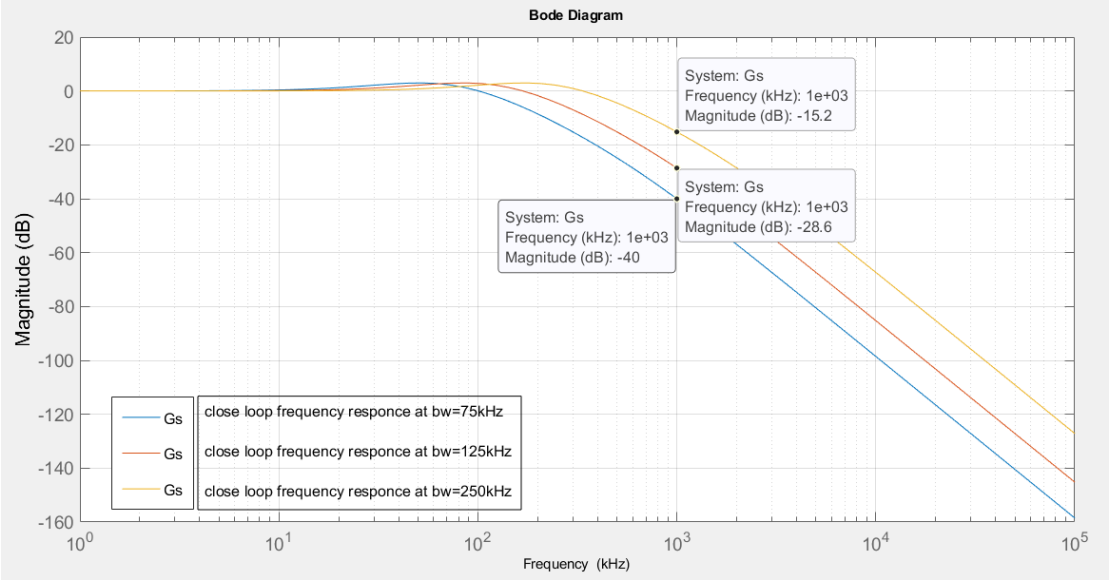


Figure 4-16: Frequency response magnitude for the 2nd proposed frequency synthesizer at PM=47°

It can be observed from figure (4-16) that when the order of the filter increased, the response gain will be increased due to the location of the extra pole of the third- order loop filter T3. Then the slope of the gain frequency response in the third-order loop filter is faster to go down than in the second-order loop filter at high frequency. So the amplitude of the frequency response is better, which lead better removal for noises at high frequency as will be illustrated in table (4-8).

Table 4-8: Magnitude frequency response comparison for the 2nd proposed frequency synthesizer at PM=47°

Frequency (MHz)	Close loop Transfer function magnitude (dB)		
	BW=75KHz	BW=125KHz	BW=250KHz
1	-40	-28.6	-15.2
10	-98.5	-85.2	-67.3
100	-159	-145	-127

Table (4-8) shows a close-loop comparison between the magnitude frequency response for the second proposed frequency synthesizer at 75,125 and 250- kHz Bandwidth. Where the magnitude frequency response for the 2nd proposed frequency synthesizer at 75 kHz bandwidth is equal to -159 dB at 100 MHz offset frequency, it is better than the frequency response for 1st proposed frequency synthesizer that equal to -117 dB at the same bandwidth and offset frequency.

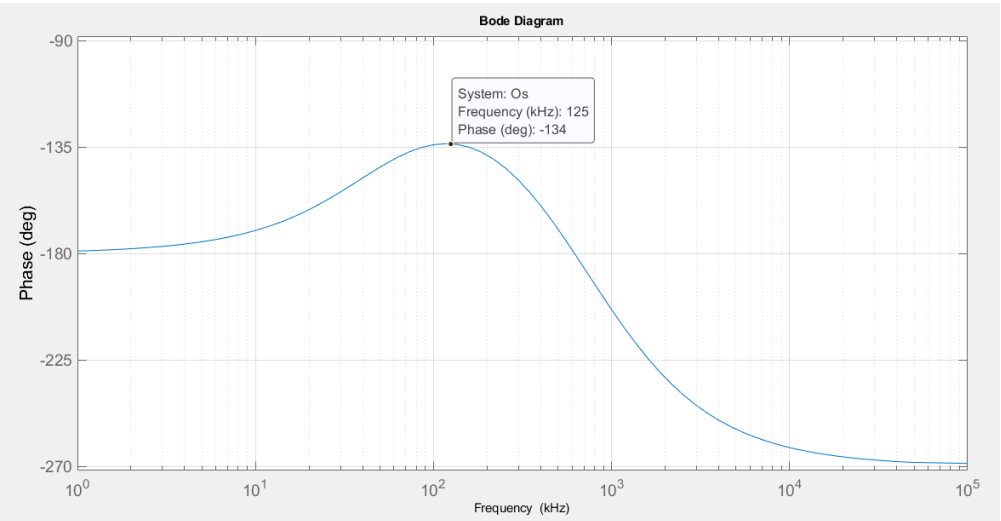


Figure 4-17: Frequency response phase for the 2nd proposed frequency synthesizer at PM=47°.

It can be noted from figure (4-17) that the phase of open loop transfer function is equal to -134˚. Then the phase margin magnitude of the frequency synthesizer design circuit is equal to 46˚ and it is approach to the value that was selected in the design process which is 47˚.

4.3.1.2 Simulation Result of The 2nd Order Σ-Δ Modulator

It can be seen from the previous design that the work of the first-order sigma-delta was not sufficient to improve the quality of the frequency synthesizer output spectrum in removing the fractional spurs noise. Therefore, the number of levels for the modulator output increased to four levels by designing a 2nd order single-loop Σ-Δ modulator, the division ratio will change between four values 124,125,126 and 127 in order to generate the required division ratio 125.1041667, as shown in figure (4-18).

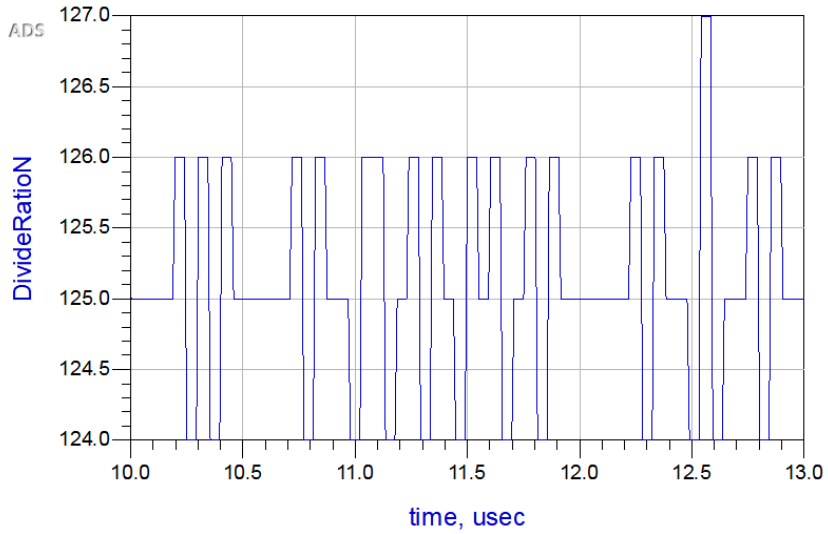


Figure 4-18: Total division ratio of the 2nd proposed frequency synthesizer.

Where the output signal of 2nd order single-loop Σ-Δ modulator as in figure (4-19)

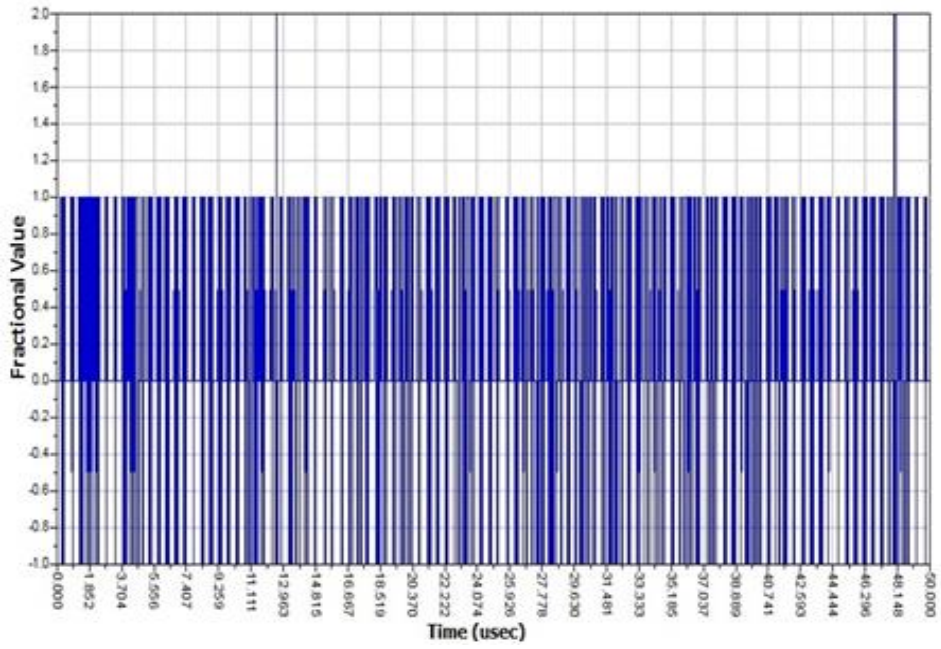


Figure 4-19: Output of the 2nd order Σ-Δ modulator

It can be noted from figure (4-19) that the output signal of the second-order sigma-delta modulator are changes between four levels (-1,0,1,2) due to the presence of a two-bit quantizer. So the number of levels (L) will become (L=$2^n = 2^2 = 4$) where(n) is the number of bits. In additional to the presence of two accumulator circuits whose work is to push the fractional spurs noise to high frequencies to be removed it by the filter and reduce phase noise at low frequencies. The output spectrum of the modulator was illustrated in the figure (4-20).

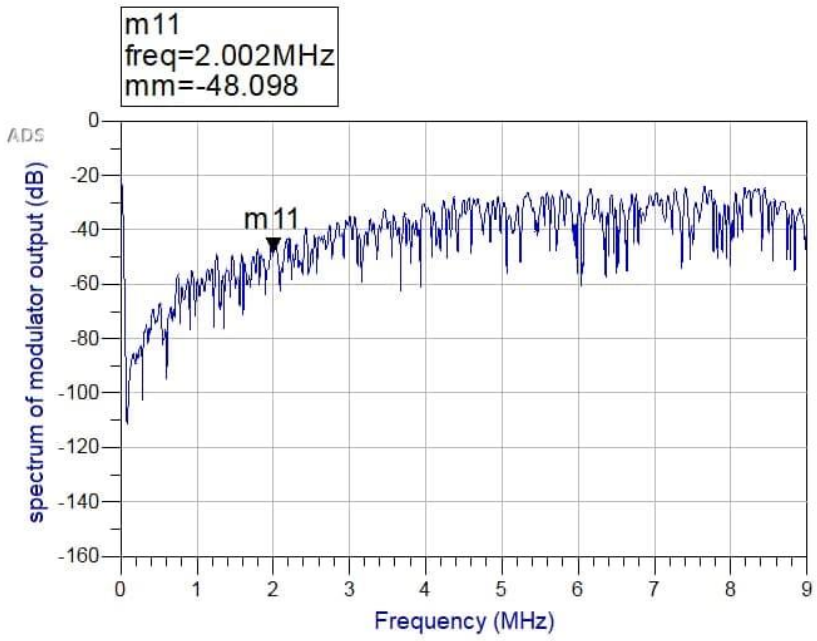


Figure 4-20: **Output spectrum the 2nd order Σ-Δ modulator.**

It can be seen from figure (4-20) that the output spectrum of the second-order sigma-delta modulator gives better performance than the first-order sigma-delta modulator, which is free from fractional spurs noise with small values of the noise power comparing with the first-order sigma-delta modulator which the value of the power noise at 2 MHz offset frequency for the second-order sigma-delta modulator is equal to -48.098 dBc and at 4 MHz offset frequency is equal to -32.787 dBc .While the power noise of the first-order sigma-delta modulator at 2MHz offset frequency was equal to -20.017 dBc and at 4 MHz offset frequency is equal to -20.886 dBc .

4.3.1.3 Simulation Results of The 2nd Proposed Frequency Synthesizer at PM=47° Using ADS

In this section the simulation results of the designed circuit at 250 and75-KHz bandwidth with 47° phase margin will be shown, which are output spectrum and the settling time, they are measured for each filter designed.

4.3.1.3.1 Output spectrum and the settling time of the 2nd proposed frequency synthesizer at BW= 75KHz

The output spectrum of the designed circuit at 47° phase margin and 75KHz bandwidth is shown in figure (4-21)

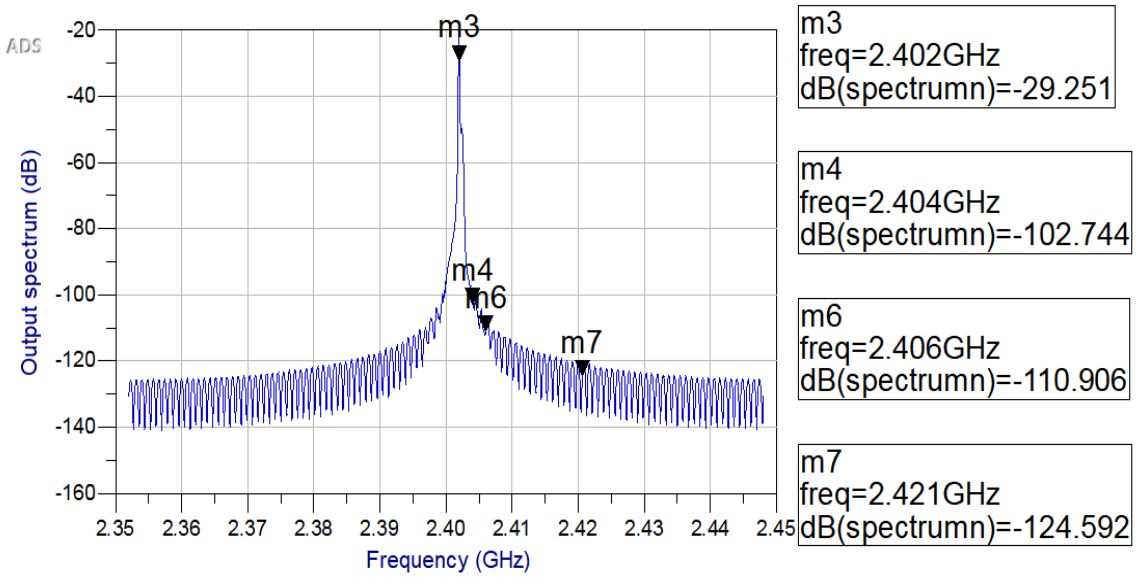


Figure 4-21: Output spectrum of the 2nd proposed frequency synthesizer

It can be seen from figure (4-21) that the output spectrum of the frequency synthesizer designed circuit does not contain any spurs noise (fractional and reference) due to the property of reshaping the noise generated by the quantizer of the sigma-delta modulator. This is in addition to improving the value of the phase noise to a good and acceptable value in Bluetooth system limitation ,due to the additional pole of the third-order filter T3 which is improves the phase noise at higher frequencies , where the value of the phase noise for the designed circuit was -156.061dBc/Hz at a frequency offset 2MHz ,and -134.304 dBc/Hz at a frequency offset equal to 3MHz ,while the value of the phase noise of the previous design

(Fractional N-PLL circuit with second-order loop filter and a first order sigma-delta modulator) at the same value of the bandwidth and the phase margin of this design was -102.765 dBc/Hz at a frequency offset 2MHz ,and -127.221 dBc/Hz at a frequency offset equal to 3MHz . The settling time was computed for this design and it will be as in figure (4-22)

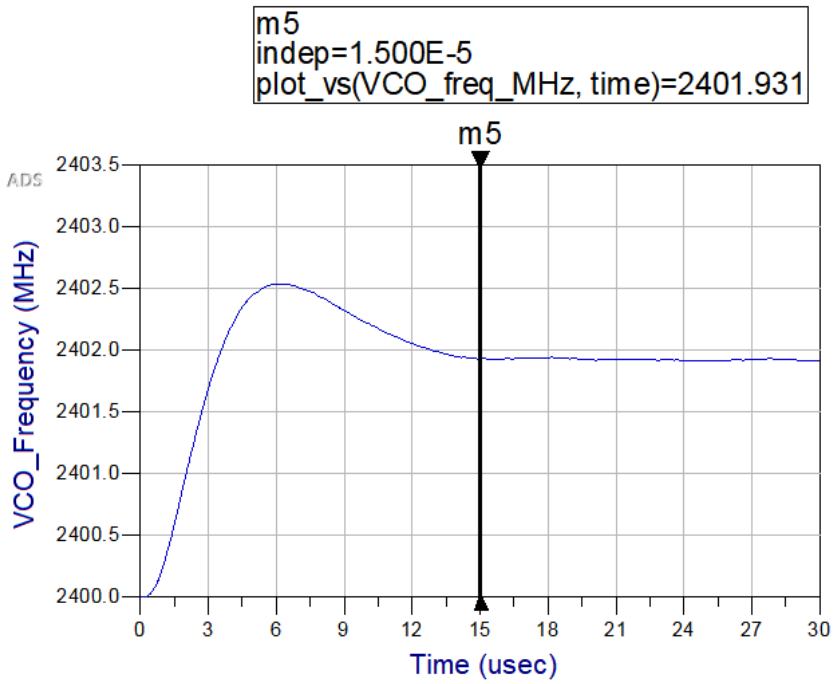


Figure 4-22: Output frequency of the 2nd proposed frequency synthesizer

It is noted from figure (4-22) that the value of the settling time of the circuit designed at 47° phase margin and 75KHz bandwidth was about 15µsec with error accuracy equal to 69 KHz, which is less than the error accuracy of the previous design at the same value of the phase noise and bandwidth. This is due to the increase in the number of division levels of the second-order sigma-delta modulator, and therefore greater fluctuation in the output signal of the modulator. From the results obtained, it can be said that

the 2nd proposed frequency synthesizer circuit give better noise performance and setting time than the 1st proposed frequency synthesizer circuit at BW=75kHz, PM=47°, as shown in the table (4-9).

Table 4-9: Comparison of the results between the 1st and 2nd proposed frequency synthesizer

Variables	1st proposed frequency synthesizer	2nd proposed frequency synthesizer
Phase noise @2MHz (dBc/Hz)	-102.765	-156.061
Reference spurs noise (dBc)	-99.49	n/a
Fractional spurs noise (dBc)	- 49.326	n/a
Settling time (µsec)	22	15
Accuracy of the o/p frequency signal (KHz)	4	69

Although improvement the settling time for the 2nd proposed frequency synthesizer circuit, the accuracy of the output frequency signal is still not acceptable. Therefore, two methods were used for the purpose of improving the accuracy of the output signal frequency and reducing the settling time:

-The first method is to increase the bandwidth of the designed circuit.

-The second method is to increase the value of the phase margin.

4.3.1.3.2 Settling Time Response of The 2nd Proposed Frequency Synthesizer at BW=250KHz

The settling time response of the 2nd proposed frequency synthesizer at 47° phase margin and 250 kHz Bandwidth was shown in the following (4-23) using ADS program.

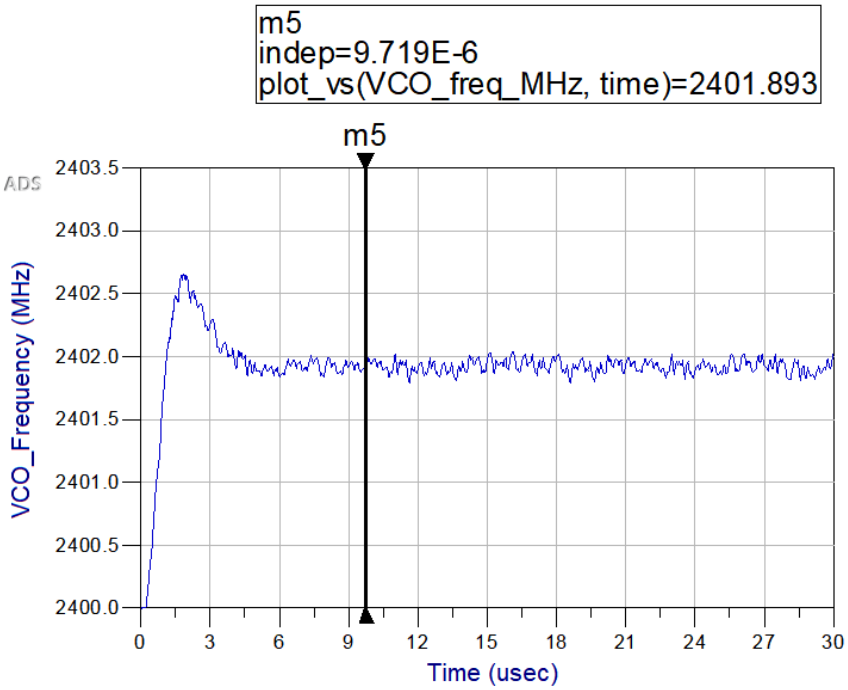


Figure 4-23: Output frequency of the 2nd proposed frequency synthesizer

It can be noted from figure (4-23) that increasing the bandwidth from 75 kHz to 250 kHz will improve the settling time of the output frequency signal about 5,281 µsec. But this also increases the output frequency accuracy to 107 KHz, therefore the second method was used, which increases the value of phase margin as explained in the next section.

4.3.1.3.3 Settling Time Response of The 2nd Proposed Frequency Synthesizer at PM=57°

A second-order sigma-delta modulator was designed using the ADS program , then a third-order filter was designed using the MATLAB program at PM= 57°, BW=250KHz K_{vco}=210MHz/V, K_{ϕ}=50mA and F_{ref}=19.2MHz. The values of the filter component were found R1=20.5KΩ, C1=10.1pf, C2=104pf. After that the fractional frequency synthesizer circuit was implemented using ADS. Then settling time response of the fractional frequency synthesizer designed circuit was found as shown in figure (4-24).

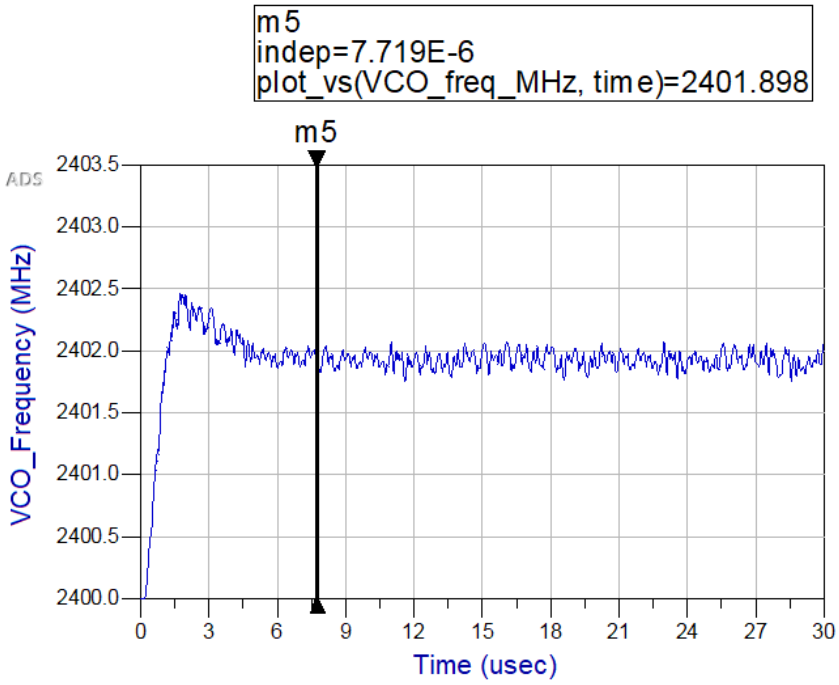


Figure 4-24: Output frequency of the 2nd proposed frequency synthesizer

Figure (4-24) shows an improvement in the value of the settling time and the output frequency accuracy of the 2nd proposed frequency synthesizer circuit at phase margin 57°and 250 KHz bandwidth, compared to the 2nd proposed frequency synthesizer circuit at the same bandwidth and phase

margin 47°, where the value of the settling time at PM=57° was equal to 7.719 μsec, which is the best value obtained. On the other hand, The error ratio of the frequency output signal was increased to 102KHz with an inverse relationship with the improvement of the settling time.

4.4 Simulation Results of The 3rd Proposed Frequency Synthesizer Circuit

This section presents the simulation results and discussions of the third design of a frequency synthesizer circuit "Fractional N-PLL circuit with a 4nd order loop filter and a 3st order Σ-Δ modulator". Where the MATLAB program was used to design the 4th order loop filter of the frequency synthesizer circuit based on the equations ((3-1)-(3-28)) ,and by applying the values of the constants K_{vco}=210MHz, K_{ϕ}=50A, F_{ref}=19.2MHz at different values of the bandwidth 75,125and 250 KHz and for each value of the phase margin 47° and 57° where the values of the capacitors and resistors of the 4th order loop filter were as in the table (4-10).

Table 4-10: 4th order loop filter component values

PM	Filter component values R (KΩ), C (PF)																			
	BW=75kHz							BW=125kHz							BW=250kHz						
	R1	R2	R3	C1	C2	C3	C4	R1	R2	R3	C1	C2	C3	C4	R1	R2	R3	C1	C2	C3	C4
47°	5.9	9	17.6	48.7	889	16.7	11.17	9.8	15	29	17.5	320	6	4	19.6	30	58.6	4.3	80	1.5	1
57°	5.7	9.3	18.3	36.7	1200	12.2	8.1	9.6	15.6	30.5	13.2	432	4.4	2.9	19.2	31.2	61	3.3	108	1.1	0.73

4.4.1 Simulation Results of The 3rd Proposed Frequency Synthesizer at PM=47°

This section includes the simulation of the Fractional N-PLL circuit under effecting the values of the bandwidth 250,125 and 75-KHz at the same value of phase margin that is equal to 47°. The design process included three stages, the first stage was in the section (4-4-1-1) and it included the simulation of the fourth -order loop filter at 75,125 and 250 -kHz using the MATLAB, while the second stage was in the section (4-4-1-2) and it included the simulation of the 3rd order Σ-Δ modulator using ADS , and the third stage was in the section (4-4-1-3) and it included the simulation result(output spectrum and the settling time) of the 3rd proposed frequency synthesizer circuit using ADS.

4.4.1.1 Simulation Results of The 3rd Proposed Frequency Synthesizer at PM=47° Using MATLAB

The designing of the fourth order loop filter is chosen at bandwidth equal to 75,125 and 250-kHz with phase margin=47°.

The frequency response of the third proposed frequency synthesizer circuit using MATLAB program was shown in the figure (4-25) and figure (4-26):

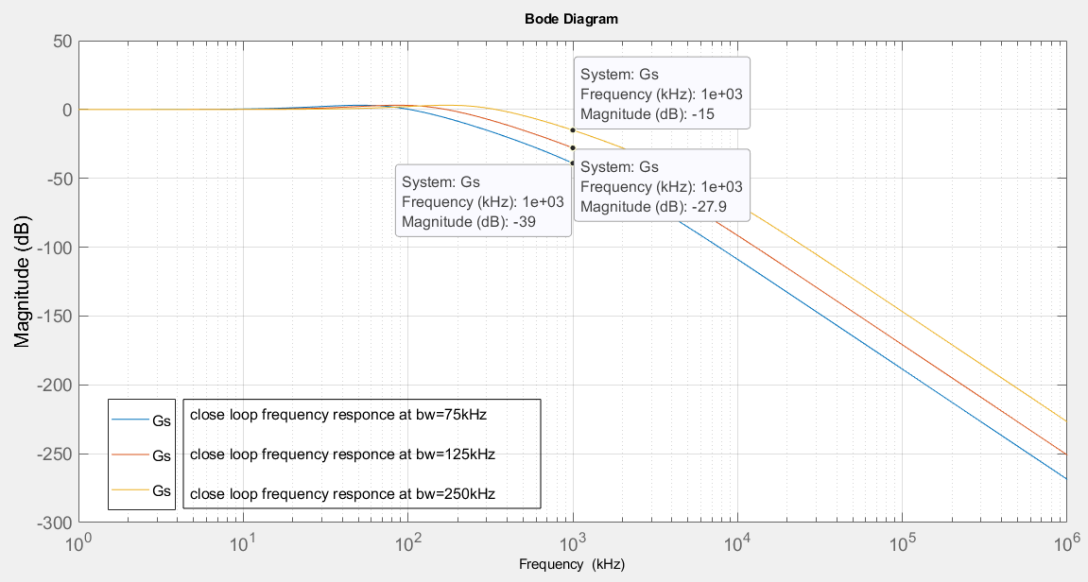


Figure 4-25: **Frequency response magnitude for the 3rd proposed frequency synthesizer at PM=47°**

It can be noted from figure (4-25) that when the order of the filter increased, the response gain will be increased due to the location the extra pole of the fourth- order filter T4. It can be observed that the slope of the gain frequency response in the fourth-order loop filter is faster to go down than in the third-order loop filter at higher frequencies so the amplitude of the frequency response is better, which lead better removal for noises at high frequency as will be illustrated in the table (4-11).

Table 4-11: Magnitude frequency response comparison for the 3rd proposed frequency synthesizer at PM=47°

Frequency (MHz)	Close loop transfer function magnitude (dB)		
	BW=75KHz	BW=125KHz	BW=250KHz
1	-39	-27.9	-15
10	-109	-91.5	-69.1
100	-189	-171	-147

Table 4-11 shows a close-loop comparison between the magnitude frequency response for the third proposed frequency synthesizer at 75,125 and 250- kHz bandwidth. Where the magnitude frequency response for the 3rd proposed frequency synthesizer at 75 kHz bandwidth is equal to -189 dB at 100 MHz offset frequency and it is better than the frequency response for 1st and 2nd proposed frequency synthesizer that equal to -117 dB and -159 dB respectively at the same bandwidth and offset frequency.

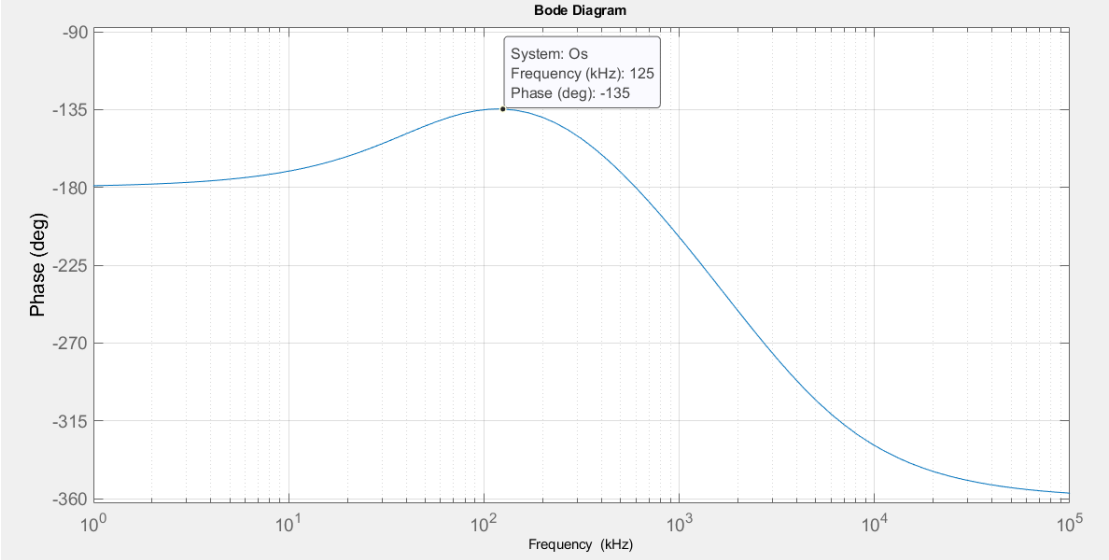


Figure 4-26: Frequency response phase for the 3rd proposed frequency synthesizer at PM=47°

It can be noted from figure (4-26) that the phase of open loop is equal to -135° at a bandwidth of 125 KHz. Then the phase margin of the 3rd proposed frequency synthesizer circuit is equal to 45˚ and it is approach to value that was selected in the design process which is 47˚.

4.4.1.2 Simulation Result of The 3rd Order Σ-Δ Modulator

In the third-order single-loop Σ-Δ modulator, the number of levels of the modulator output increased to seven levels. Therefore, the division ratio will

change between seven values from 122 to128 in order to generate the required division ratio (125.1041667) as shown in figure (4-27).

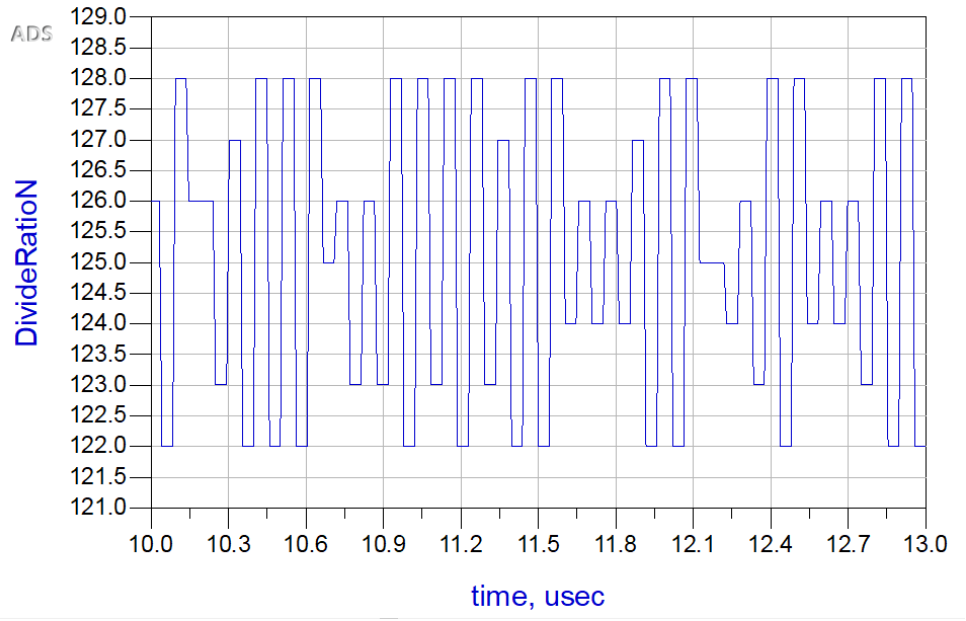


Figure 4-27: Total division ratio of the 3rd proposed frequency synthesizer

Where The output signal of the 3rd order Σ-Δ modulator will be as in figure (4-28).

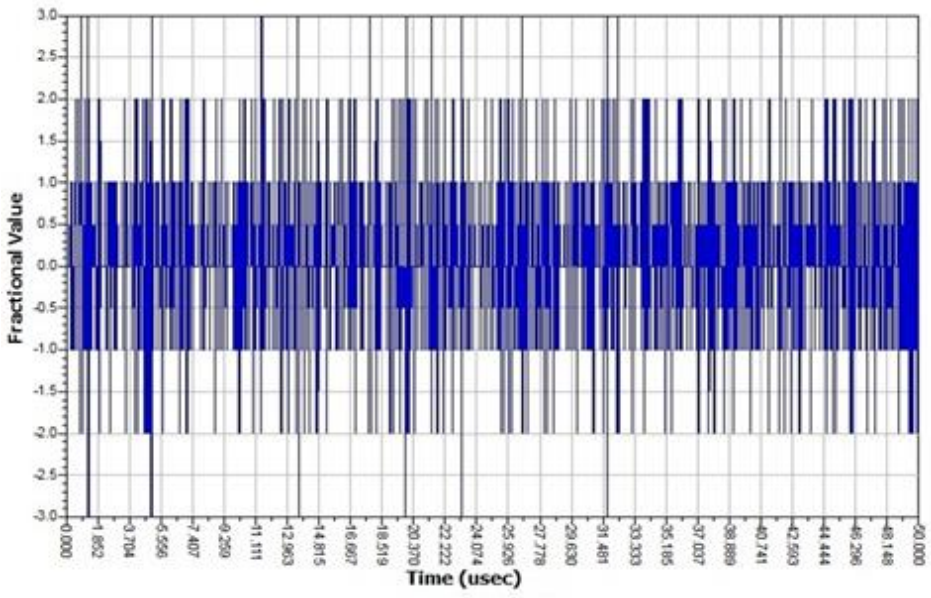


Figure 4-28: Output of the 3rd order Σ-Δ modulator

It is noted from figure (4-28) that the output signal of the third order sigma delta was fluctuates very quickly and randomly in order to generate the required partition ratio due to the presence of a multi-bit quantizer. This is in addition to the presence of three accumulator circuits whose work is to push the fractional spurs noise to high frequencies to be removed by the filter and reduce phase noise at low frequencies. The output spectrum of the modulator was illustrated in the figure (4-29).

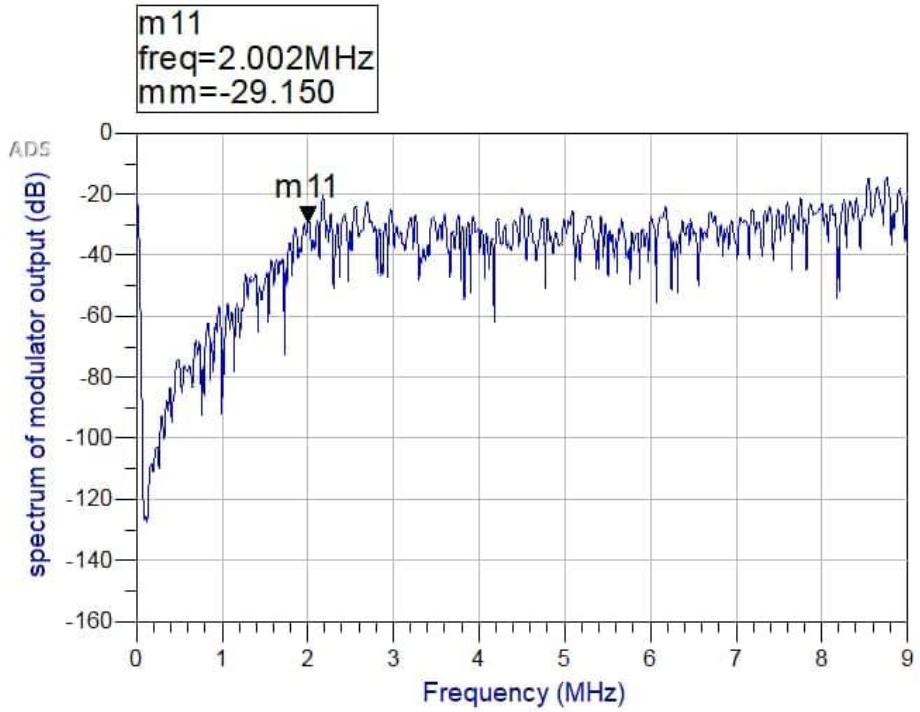


Figure 4-29: Output spectrum the 3rd order Σ-Δ modulator

It can be seen from figure (4-29) that the output spectrum of the 3rd order sigma-delta modulator is free from any fractional spurs noise, but the values of the power noise at high frequencies are higher than the power noise of the 2nd order sigma- delta. The value of the power noise at 2 MHz offset frequency for the 2nd order sigma-delta modulator is equal to -48.098 dBc .While the power noise of the 3rd order sigma-delta modulator at 2 MHz offset frequency was equal to -29.15 dBc .

4.4.1.3 Simulation Results of The 3rd Proposed Frequency Synthesizer at PM=47° Using ADS

This section will present the simulation results of the output spectrum and the settling time for the 3rd proposed circuit at 250 and 75-kHz Bandwidth.

4.4.1.3.1 Output Spectrum and The Settling Time of The 3rd Proposed Frequency Synthesizer at BW=75 KHz

The output spectrum of the third proposed frequency synthesizer circuit at 47° phase margin and 75 kHz bandwidth is show in figure (4-30).

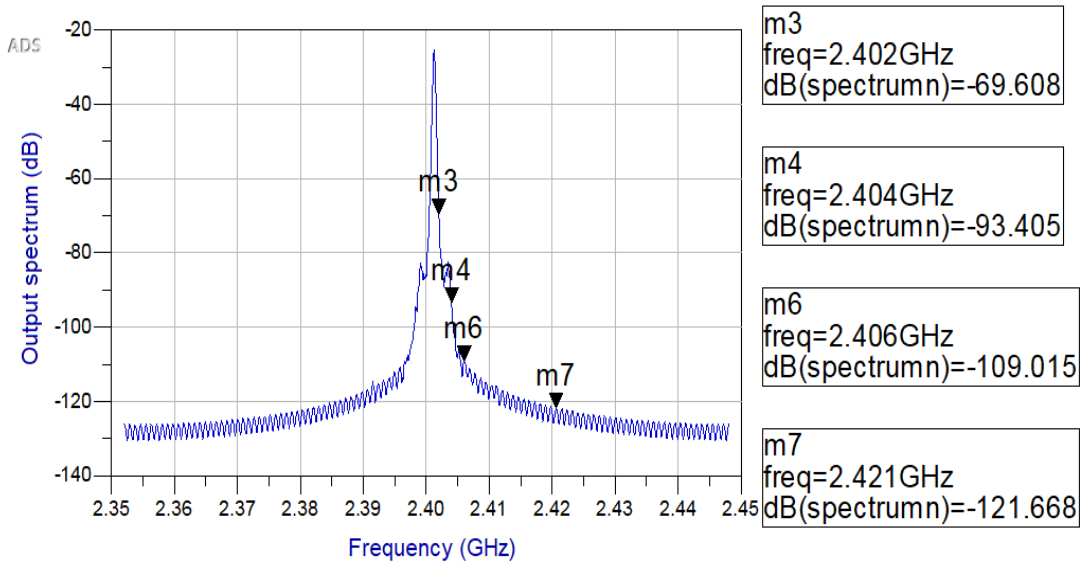


Figure 4-30: Output spectrum of the 3rd proposed frequency synthesizer

It can be seen from figure (4-30) that the output spectrum of the third proposed frequency synthesizer circuit does not contain any spurs noise (fractional and reference) due to the property of reshaping the noise generated by the quantizer of the sigma delta modulator. But the values of the phase noise at high frequencies are higher than the phase noise values in the previous designs. Table (4-12) below represents a comparison of the

value of phase noise (PN) at low and high frequencies between the two designs (Fractional N-PLL circuit with a third-order loop filter and a second-order sigma-delta modulator and Fractional N-PLL circuit with a fourth-order loop filter and a third-order sigma-delta modulator) at 75KHz bandwidth and 47° phase margin.

Table 4-12: Phase Noise comparison between the 2nd and 3rd proposed frequency synthesizer

Offset Frequency	Phase Noise (dBc/Hz)	
	2nd proposed frequency synthesizer	3rd proposed frequency synthesizer
100KHz	-100.63	-128.492
200KHz	-102.416	-133.106
250KHz	-104.471	-133.77
450KHz	-105.482	-140.406
550KHz	-111.859	-139.189
750KHz	-131.173	-142.609
850KHz	-138.897	-131.426
1MHz	-143.728	-139.349
2MHz	-156.061	-146.775
3MHz	-163.555	-160.844

It can noted from table (4-12) that the 3rd proposed frequency synthesizer circuit gives better performance in terms of improving the values of phase noise at low frequencies (less or equal to 750) KHz. The reason for this is due to the increase in the order of the sigma- delta modulator which works as a high pass filter. Thus, when the order of the modulator is increased, the phase noise will be decreased in the low frequencies and increased in the high frequencies. For this reason, the 2nd proposed frequency synthesizer circuit gives better values for phase noise at frequencies (greater or equal to 850) KHz. The settling time was computed for the 3rd proposed frequency synthesizer circuit at 75 KHz bandwidth and 47° phase margin as shown in figure (4-31).

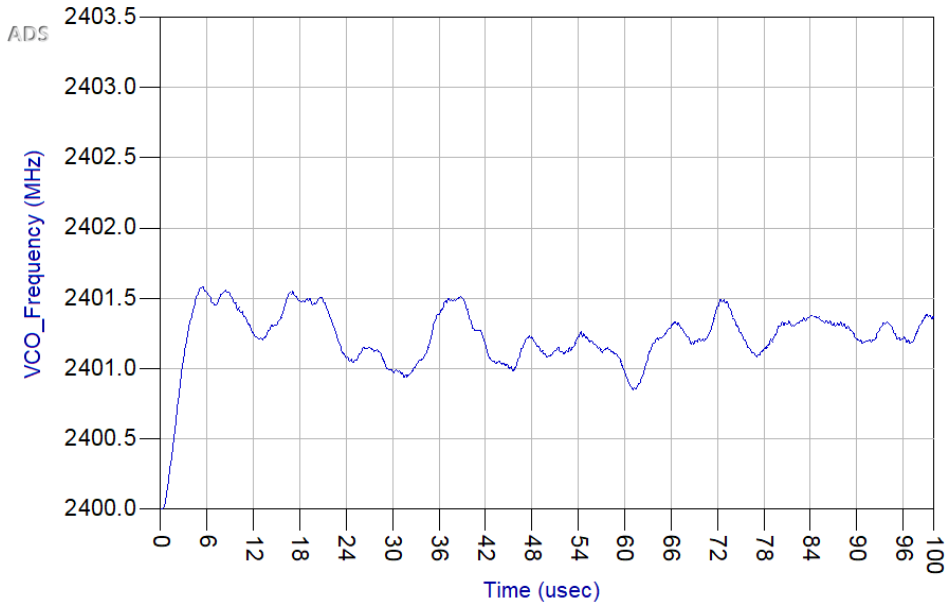


Figure 4-31: Output frequency of the 3rd proposed frequency synthesizer.

It can be noted from figure (4-31) that the output signal of the frequency synthesizer designed circuit is oscillating and unstable, and the reason is due to the wide change in the output of the 3rd order Σ-Δ modulator as a result of

the increase in the number of division levels, which negatively affected the generation of an accurate fractional division ratio that led to the disturbance of the output frequency of the designed circuit.

Therefore, the phase margin increased to 57° and the bandwidth of the frequency synthesizer circuit increased to 250 KHz in order to improve the settling time and frequency accuracy of the output signal. The output frequency signal is illustrated in figure (4-32).

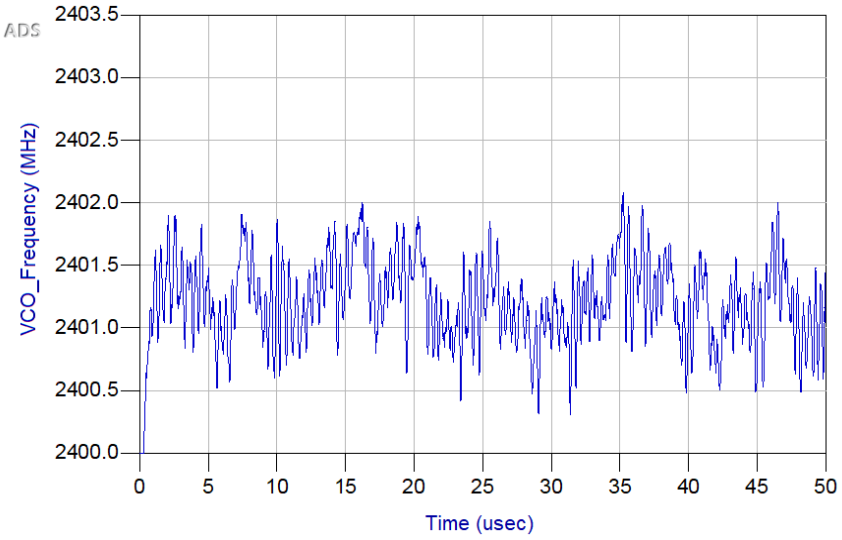


Figure 4-32: Output frequency of the 3rd proposed frequency synthesizer.

It can be noted from figure (4-32) that the output signal of the 3rd proposed frequency synthesizer circuit is unstable and fluctuates greatly despite increasing the phase margin factor and the bandwidth. And thus, this design is not ready for use in the Bluetooth application system because the condition of obtaining a stable speed for the frequency of the phase-locked loop circuit output signal has been lost, resulting in a delay in the transition between frequency channels. On the other hand, this design was good in terms of obtaining a pure signal free of spurs noise with small ratio of the phase noise

values at low frequencies. Table (4-13) illustrates the advantages and disadvantages between the circuits that have been designed.

Table 4-13: Comparison between the 1st, 2nd and 3rd proposed frequency synthesizer

Circuit Designed Name	Advantage	Disadvantage
1st proposed frequency synthesizer	Obtaining good and acceptable values in the Bluetooth system for the settling time and the accuracy of the output signal, where the values at 47° PM are (22μsec with 4KHz error rate @ 75 KHz BW,17.28μsec with 32KHz error rate @ 125 KHz BW, 10.11μsec with 74KHz error rate @ 250 KHz BW). and at 57° PM the values are (19.2μsec with 3KHz error rate.@ 75 KHz BW, 15.16μsec with 17KHz error rate@ 125 KHz BW, 8.38μsec with 47KHz error rate@ 250 KHz BW).	The appearance of not good and not acceptable values of a spurs noise and phase noise in the output spectrum signal, and the reason is the continuous change in the division ratio of the 1st order Σ-Δ modulator , that is similar to the work of the accumulator.
2nd proposed frequency synthesizer	Removing the fractional spurs noise and the reference spurs noise, improving the values of phase noise to acceptable values in the Bluetooth system, where the value of phase noise was equal to -156.061dBc/Hz at frequency offset 2MHz, and -163.555 dBc/Hz at frequency offset 3 MHz, improving the settling time to 7.719 μsec , which is the best value obtained.	The accuracy of the output signal is not acceptable in the Bluetooth system, where the error rate of the output signal was 102 KHz at 75 KHz bandwidth and 57° phase margin.
3rd proposed frequency synthesizer	Removing the fractional spurs noise and the reference spurs noise, improvement of phase noise values at low frequencies (less and equal to 750 kHz).	Not obtaining a stable output signal due to the fluctuation in the third-order sigma-delta modulation as a result of the increase in the number of the quantization levels.

Table (4-14) illustrates a comparison between the results that are obtained in this thesis and the results of previous researches in the field of the Bluetooth system. Where the obtained values are better than the results of other researches in terms of obtaining an output spectrum free of spurs noise, with lower values of phase noise in addition to obtaining the best value for the stability time.

Table 4-14: Comparison the results of the proposed research with the results of previous research

Parameter/ References	Bluetooth requirements	[120] 2004	[121] 2007	[122] 2008	[123] 2010	[9] 2016	2nd proposed frequency synthesizer
Output frequency	2.402 to 2.480 GHz	2.4 GHz	2.4 GHz	2.4 GHz	900 MHz	2.402 GHz	2.402 GHz
Input frequency (MHz)	13,19.2,20,26, 39.2,40	48	12	12	8	19.2	19.2
Bandwidth (KHz)	N/A	100	730	975	40	100	75-250
Phase noise (dBc/Hz)	-110 dBc/Hz @ 2 MHz, -119 dBc/Hz @ 3 MHz	-96 @ 460 KHz	-101	-121 @ 3 MHz	-135 @ 3 MHz	-101.5@ 600 KHz, -125.5 dBc/Hz @ 2 MHz, -131.5 @ 3 MHz	-163 dBc/Hz @ 3 MHz, -156 dBc/Hz @ 2 MHz, -111 dBc/Hz @ 550 KHz
Spurs noise (dBc)	≤ -49	-66	N/A	-70	-96	Free	Free
Switching time (µsec)	≤ 220	N/A	35	N/A	N/A	13.69	7.7

CHAPTER FIVE

Conclusions and Suggestions for Future Work

5.1 Conclusions

The purpose of this thesis was to propose a Fractional N-PLL design circuit for improving the Bluetooth system's performance based on 2.4 GHz, in order to obtain a pure high-frequency signal with acceptable accuracy and high speed of transmission between frequencies channels. Three designs for the Fractional-N PLL frequency synthesizer circuit were proposed to choose the most appropriate design that gives the best results within the parameters of the Bluetooth system. Accordingly, the following conclusions have been drawn:

1- There was an effect of the Σ-Δ modulator on the performance of the Fractional-NPLL circuit.

It noted from the results that the effect of increasing the order of the Σ-Δ modulator works on:

a- Disappearance the fractional and reference spurs noise, from the output frequency signal of the frequency synthesizer circuit.

b- Reducing the value of the phase noise at a lower frequency of the output signal of the frequency synthesizer circuit, and increasing it in higher frequencies due to the principle work of the modulator, which acts as a high pass filter, therefore increasing the order of the modulator will improve the value of the phase noise in the lower frequencies.

c- Reducing the accuracy of the output signal of the frequency synthesizer circuit, due to the increase in the number of quantization

levels of the modulator, and thus the disturbance and instability of the output signal of the frequency synthesizer circuit.

2- There was an effect of the filter (bandwidth, phase margin, filter order's) on the performance of frequency synthesizer circuit:

a- Increasing the order of the filter will improve the value of the phase noise at high frequencies of the output signal of the frequency synthesizer circuit. This is due to the location of the additional pole of the filter, which makes the frequency response of the filter closer to the ideal state in removing the noise at high frequencies (in stopband region).

b- Increasing the phase margin leads to an improvement in the accuracy of the output signal of the frequency synthesizer circuit also an improvement in the stability time.

c- Increasing the bandwidth leads to a decrease in the settling time due to the inverse relationship between increasing the bandwidth and improving the settling time, but decreasing the bandwidth will improve the value of the reference and fractional spurs noise at the output frequency signal of the frequency synthesizer circuit.

5.2 Suggestions for Future Works

1- Reaching to a method that improves the accuracy of the output frequency signal of the frequency synthesizer circuit.

2- The Fractional-N frequency synthesizer may have the capability to be used across all bands in the 802.11 standards. Additionally, if a frequency multiplier is added at the output stages of the synthesizer, the synthesizer may be able to span a considerably broader bandwidth, allowing it to be utilized in a much wider range of wireless applications.

3- Making the Fractional-N frequency synthesizer circuits more energy efficient by reducing the noise from circuit elements to a low level as possible.

Appendix A

Fourth order loop filter design equations:

$$A0=\frac{K_{\emptyset}*K_{vco}}{N*\omega c^2}*\sqrt{\frac{(1+\omega c^2*T2^2)}{(1+wc^2*T1^2).(1+\omega c^2*T3^2).(1+\omega c^2*T4^2)}} \quad \text{(A-1)}$$

$$a1T3 = A0.(T1+T3) \quad \text{(A-2)}$$

$$a2T3 = A0.T1.T3 \quad \text{(A-3)}$$

$$c1T3 = \frac{a2T3}{T2^2}(1+\sqrt{\left(1+\frac{T2}{a2T3}\right)*(T2*A0-a1T3)} \quad \text{(A-4)}$$

$$c3T3 = \frac{(-T2^2*c1T3^2)+(T2*a1T3*c1T3)-(a2T3*A0)}{(T2^2*c1T3)-(a2T3)} \quad \text{(A-5)}$$

$$r3T3 = \frac{a2T3}{c1T3*c3T3*T2} \quad \text{(A-6)}$$

$$a1T4 = A0(T1+T4) \quad \text{(A-7)}$$

$$a2T4 = A0*T1*T4 \quad \text{(A-8)}$$

$$c1T4 = \frac{a2T4}{T2^2}(1+\sqrt{\left(1+\frac{T2}{a2T4}\right)*(T2.A0-a1T4)} \quad \text{(A-9)}$$

$$c3T4 = \frac{(-T2^2*c1T4^2)+(T2*a1T4*c1T4)-(a2T4*A0)}{(T2^2*c1T4)-(a2T4)} \quad \text{(A-10)}$$

$$r3T4 = \frac{a2T4}{c1T4*c3T4*T2} \quad \text{(A-11)}$$

$$C1 = \frac{c1T3+c1T4}{2} \quad \text{(A-12)}$$

Where c1T3, c1T4: Intermediate calculation for finding C1

$$R3 = \frac{r3T3+r3T4}{2} \quad \text{(A-13)}$$

Where r3T3, r3T4: Intermediate calculation for finding R3

$$A1 = A0(T1 + T3 + T4) \quad \text{(A-14)}$$

$$A2 = A0((T1 * T3) + (T1 * T4) + (T3 * T4)) \quad \text{(A-15)}$$

$$A3 = A0 * T1 * T3 * T4 \quad \text{(A-16)}$$

$$k0 = \left(\frac{A2}{A3}\right) - \left(\frac{1}{T2}\right) - \left(\frac{1}{C1*R3}\right) - \left(\frac{(A0-C1)*T2*R3*C1}{A3}\right) \quad \text{(A-17)}$$

$$k1 = A1 - (T2 * A0) - \frac{A3}{T2*R3*C1} - (A0 - C1) * R3 * C1 \quad \text{(A-18)}$$

$$a = \frac{A3}{(T2*C1)^2} \quad \text{(A-19)}$$

$$b = (T2 + (R3\ (C1-A0)) + \left(\left(\frac{A3}{T2.C1}\right).\left(\frac{1}{T2} - k0\right)\right)) \quad \text{(A-20)}$$

$$c = k1 - \frac{ko*A3}{T2} \quad \text{(A-21)}$$

$$C2 = \frac{-b+\sqrt{b^2-4*a*c}}{2*a} \quad \text{(A-22)}$$

Where k0,k1a,b,c: Intermediate calculation for finding C2

$$R2 = \frac{T2}{C2} \quad \text{(A-23)}$$

$$C3 = \frac{T2*A3*C1}{R3\{(k0*T2*A3*C1) - (C2(A3 - (R3*(T2*C1)^2)))\}} \quad \text{(A-24)}$$

$$C4 = A0\text{-}C1\text{-}C2\text{-}C3 \quad \text{(A-25)}$$

$$R4 = \frac{A3}{T2*R3*C1*C3*C4} \quad \text{(A-26)}$$

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إقرار المشرف

نشهد بأن هذه الرسالة الموسومة **(تحليل أداء مُركب التردد Fractional N PLL بتردد2.4 جيجا هرتز)** تم اعدادها من قبل الطالبة **(نور زيد نكتل)** تحت اشرافنا في قسم هندسة الالكترونيك / كلية هندسة الالكترونيات / جامعة نينوى، وهي جزء من متطلبات نيل شهادة الماجستير/علوم في اختصاص هندسة الالكترونيك.

التوقيع:
الاسم: أ.د. خالد خليل محمد
التاريخ: / /2022

التوقيع:
الاسم: أ.م.د. اوس زهير يونس
التاريخ: / /2022

إقرار المقوم اللغوي

اشهد بأنه قد تمت مراجعة هذه الرسالة من الناحية اللغوية وتصحيح ما ورد فيها من أخطاء لغوية وتعبيرية وبذلك أصبحت الرسالة مؤهلة للمناقشة بقدر تعلق الأمر بسلامة الأسلوب أو صحة التعبير.

التوقيع:
الاسم: م.م. امين عبدالرحمن ضياء
التاريخ: / /2022

إقرار رئيس لجنة الدراسات العليا

بناءً على التوصيات المقدمة من قبل المشرف والمقوم اللغوي أرشح هذه الرسالة للمناقشة.

التوقيع:
الاسم: أ.م.د احمد ذنون يونس
التاريخ: / /2022

إقرار رئيس القسم

بناءً على التوصيات المقدمة من قبل المشرف والمقوم اللغوي ورئيس لجنة الدراسات العليا أرشح هذه الرسالة للمناقشة.

التوقيع:
الاسم: أ.م.د أحمد ذنون يونس
التاريخ: / /2022

إقرار لجنة المناقشة

نشهد بأننا أعضاء لجنة التقويم والمناقشة قد اطلعنا على هذه الرسالة الموسومة (**تحليل أداء مُركب التردد Fractional N PLL بتردد2.4 جيجا هرتز**) وناقشنا الطالبة (**نور زيد نكتل**) في محتوياتها وفيما له علاقة بها بتاريخ 12 / 12 /2021 وقد وجدناها جديرة بنيل شهادة الماجستير/علوم في اختصاص هندسة الالكترونيك.

التوقيع:

رئيس اللجنة: أ.م.د. مجاهد فهمي ابراهيم

التاريخ: / /2022

التوقيع:

عضو اللجنة: أ.م.د. محمد طارق ياسين

التاريخ: / /2022

التوقيع:

عضو اللجنة: م.د. احمد محمد سلامة

التاريخ: / /2022

التوقيع:

عضو اللجنة (المشرف): أ.د. خالد خليل محمد

التاريخ: / /2022

التوقيع:

عضو اللجنة (المشرف): أ.م.د. اوس زهير يونس

التاريخ: / /2022

قرار مجلس الكلية

اجتمع مجلس كلية هندسة الالكترونيات بجلسته المنعقدة بتاريخ: / /2022

وقرر المجلس منح الطالبة شهادة الماجستير علوم في اختصاص هندسة الالكترونيك

مقرر المجلس: أ.م.د. صدقي بكر ذنون

التاريخ: / /2022

رئيس مجلس الكلية: أ.د. خالد خليل محمد

التاريخ: / /2022

الخلاصة

تُستخدم أجهزة توليف التردد القائمة على دائرة قفل الطور والتردد الكسرية على نطاق واسع في مجال الاتصالات مثل الهواتف المحمولة والأقمار الصناعية وأجهزة الراديو لأنها تولد نطاقًا ترديدًا كبيرًا مع دقة تردد عالية بتردد مرجعي عالي جدًا ، وتبديل سريع بين القنوات الترددية ، والحد الأدنى من ضوضاء الطور والنتوءات الضوضائية المرجعية والكسرية لمختلف التطبيقات الإلكترونية. لذلك تم العمل في هذه الرسالة على تصميم دائرة مركب تردد كسري , بمواصفات تجعلها قابلة للاستخدام في مجال تطبيق نظام البلوتوث وفقًا للمعايير المحددة لنظام البلوتوث. تم الاعتماد على برنامج MATLAB وبرنامج ADS لتصميم ومحاكاة مرشح امرار الترددات الواطئة ومضمن سيكما دلتا ,نظرًا للتاثير الكبير لهذين العنصرين في تحسين الاداء لاجهزة توليف التردد . حيث تم تصميم مرشح امرار الترددات الواطئة نوع passive loop filter وتم تصميم المرشح بثلاث رتب وهي الرتبة الثانية والثالثة والرابعة . كما تم تصميم المضمن سيكما دلتا نوع الدائرة المفردة بثلاث رتب ايضا وهي الرتبة الاولى والثانية والثالثة ,بالتالي تم الوصول الى ثلاث تصاميم لدائرة مركب التردد وهي (دائرة مركب تردد كسري مكون من مرشح حلقة من الدرجة الثانية ومضمن سيكما دلتا من الدرجة الأولى ، دائرة مركب تردد كسري مكون من مرشح حلقة من الدرجة الثالثة ومضمن سيكما دلتا من الدرجة الثانية ، دائرة مركب تردد كسري مكون من مرشح حلقة من الدرجة الرابعة ومضمن سيكما دلتا من الدرجة الثالثة) ، عند عرض حزمة (250,125,75) كيلوهيرتز ولكل قيمة من هامش الطور(47 ، 57) درجة.

تم الاستنتاج ان دائرة المركب الكسري المكونة من مرشح الحلقة من الدرجة الثالثة ومضمن سيكما دلتا من الدرجة الثانية تعطي أفضل اداء حيث تم الحصول على إشارة اخرج عالية بتردد 2401.898 ميكاهيرتز مع قيمة مقبولة لضوضاء الطور تساوي 156.061- ديسيبل /هيرتز عند ازاحة ترددية 2 ميكاهرتز و 163.555- ديسيبل /هيرتز عند ازاحة ترددية 3 ميكاهيرتز، وأفضل زمن استقرار 7.719 مايكروثانية اضافة الى نقاء الاشارة من اي نتوءات ضوضائية كسرية ومرجعية .

تحليل أداء مُركب التردد Fractional N PLL بتردد 2.4 جيجا هرتز

رسالة تقدمت بها

نور زيد نكتل

إلى
مجلس كلية هندسة الالكترونيات
جامعة نينوى
كجزء من متطلبات نيل شهادة الماجستير
في
هندسة الالكترونيك

بإشراف

ا.د. خالد خليل محمد

ا.م.د. أوس زهير يونس

1443 هـ **2022 م**

وزارة التعليم العالي والبحث العلمي

جامعة نينوى

كلية هندسة الالكترونيات

قسم هندسة الالكترونيك

تحليل أداء مُركب التردد Fractional N PLL بتردد 2.4 جيجا هرتز

نور زيد نكتل

رسالة ماجستير علوم في هندسة الالكترونيك

بإشراف

ا.د. خالد خليل محمد

ا.م.د. أوس زهير يونس

1443 هـ 2022 م