Ninevah University

College of Electronics

Electronic Department

Three-phase Five-level Inverter Topology for Grid-Connected PV Systems

Hadeel Saad Taher Maaroof

A Thesis in

Electronic Engineering

Supervised by

Dr. Ahmad T. Younis

Dr. Harith Al-Badrani

1443 A.H. **2021 A.D.**

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To

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In

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بِسْمِ اللَّهِ الرَّحْمَنِ الرَّحِيمِ

﴿يَرْفَعِ اللَّهُ الَّذِينَ آمَنُوا مِنْكُمْ وَالَّذِينَ أُوتُوا الْعِلْمَ دَرَجَاتٍ وَاللَّهُ بِمَا تَعْمَلُونَ خَبِيرٌ﴾

صَدَقَ اللهُ العَظِيم

المجادلة: 11

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Researcher

ABSTRACT

This work presents a new approach for connecting solar energy to the grid, the proposed system uses a three-phase Five-Level Cascaded H-bridge (5L-CHB) for this objective, which provides benefits at an improve the quality of output voltage waveform, and, most importantly, energy production availability under different operation conditions. The system's versatility allows for varied cases of operation based on the available photovoltaic PV condition, which is taken into account in all of the work's specifics. It can be shown that to be a good solution in the developing countries for integrating small generation systems into the grid. Each phase of (5L-CHB) inverter consists of two H-bridge connected in series fed by separated DC sources, which is a PV array in this work. The interaction between the CHB and the grid was regulated using a voltage oriented control (VOC) approach with two feedforward methods added for modulation index correction. Which are described in this work each aimed at a specific target. The first method, which is dependent on the zero-sequence signal injected into the reference signal, results in a balanced power that will inject into the grid even when asymmetrical energy output occurs between the three phases due to model mismatch, partial shade on the PV array, fault degradation. And the second is for tracking for the maximum power point for each PV array connected to the inverter without needing extra dc-dc converters which are required in traditional methods. In the modulation stage, the phase shift pulse width modulation (PS-PWM) is used to control the output voltage of the inverter.

MATLAB simulation is performed to verify the results which show the system reliability and operational flexibility due mainly to separate Maximum Power Point Tracking (MPPT) function at each HB unit and the balanced

power that injected into the grid even when the PV generates asymmetrical power in different conditions.

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LIST OF ABBREVIATIONS

ABBREVIATIONS	DESCRIPTION
3L-NPC	Three-Level Neutral Point Clamped.
5L-CHB	Five-Level Cascaded H-Bridge.
AC	Alternating Current.
AGC	Automatic Gain Controller.
APODPWM	Alternative Phase Opposition Disposition Pulse Width Modulation.
CF-DAB	Current Fed Dual Active Bridge.
CHB	Cascaded H-Bridge.
CHBMLI	Cascaded H-bridge Multilevel Inverter.
DC	Direct Current.
DCC	Diode-Clamped Converter.
DMPP	Distributed Maximum Power Point Tracking.
FC	Flying Capacitor.
FF	Fill Factor.
FFT	Fast Fourier Transform.
HB	H-Bridge.
IGBT	Insulated Gate Bipolar Transistor.
LF	Low Pass Filter.
LS-PWM	Level Shift-Pulse Width Modulation.
MCPWM	Multi-Carrier Pulse Width Modulation.
MDCI	Multilevel Diode Clamped Inverter.
MFCI	Multilevel Flying Capacitor Inverter.

MLI	Multilevel Inverter.
MPP	Maximum Power Point.
MPPT	Maximum Power Point Tracking.
NPC	Neutral Point Clamped.
PD	Phase Detector.
PDPWM	Phase Disposition-Pulse Width Modulation.
PI	Proportional Integral.
PLL	Phase Lock Loop.
PODPWM	Phase Opposition Disposition Pulse Width Modulation.
PR	Proportional Resonant.
PS-PWM	Phase Shift Pulse Width Modulation.
PV	Photovoltaic.
PWM	Pulse Width Modulation.
P&O	Perturb and Observation.
RMS	Root Mean Square.
SCC	Series Capacitor Commutated Inverter.
SHE	Selective Harmonic Elimination.
SVM	Space Vector Modulation.
SVPWM	Space Vector Pulse Width Modulation.
THD	Total Harmonic Distortion.
VCO	Voltage Controlled Oscillator.
VOC	Voltage Oriented Control.
VSI	Voltage Source Inverter.

LIST OF SYMBOLS

SYMBOL	DESCRIPTION
A_c	Amplitude of triangle carrier signal.
A_m	Peak to peak amplitude of the sinusoidal reference signal.
C_{DC}	DC-link capacitors.
C_P	Number of required capacitors in flying capacitor topology.
D	Number of diodes.
e_t	Error signal for voltage loop.
f_s	Switching frequency.
HB-a1	Upper HB unit in CHB inverter phase *a*.
HB-a2	Lower HB unit in CHB inverter phase *a*.
h	Number of cells in CHB topologies.
I	RMS line current.
I_0	Reverse diode current.
I_c	Solar cell output current.
I_{d}	Diode current.
I_{mpp}	Maximum current obtained from the solar cell.
I_{out}	Output current obtained from the solar cell.
I_{SC}	Short circuit current for the solar cell.
I_{ph}	Photo current for solar cell.
$i_{DC\text{-}HB\ ij}$	Instantaneous DC current obtained from the PV array connected to H-bridge in phase ($i=a, b, c$) cell ($j=1,2$).
i_α and i_β	Currents in the stationary α-β frame.

$i_{a,}$ i_b, and i_c	Instantaneous line current for phase *a*, *b*, and *c* respectively.
i_d and i_q	Currents in the rotating d-q frame.
i^*_d and i^*_q	d- and q- component of the reference current in the rotating d-q frame.
K	Boltzmann constant.
k	Number of cells in flying capacitor.
L	Level of the output voltage.
L_f	Filter inductance.
m_a	Amplitude modulation index.
N	Grid neutral point.
n	Neutral point for the inverter.
P	Active power.
P_{av}	Average power obtained from PV arrays.
$P_{DC\text{-}HB\ ij}$	Instantaneous power produced from the PV array connected to H-bridge in phase (i=*a, b, c*) cell (j=*1, 2*).
P_{mpp}	Maximum power obtained from the solar cell.
P_{out}	Output power obtained from the solar cell.
P_t	Theoretical power.
Q	Reactive power.
q	Electron charge.
R_f	Resistance of the filter.
$S_{1\text{-}8}$	Switches states combination for CHB.
$S_{HB\ i}$	Instantaneous produced power in inverter phase (i= *a, b, c*).

$S_{HB\,ij}$	Instantaneous produced power of the H-bridge unit (i= a, b, c), (j=1,2).
S_{IR}	Sun irradiation.
S_a, S_b, S_c	Instantaneous apparent power produced in phase a, b and c respectively.
$S_x(t)$	Switching pulse during the modulation period.
$Sin\ (\omega t)$	Modulating signal.
s	Number of semiconductor switches.
T	Operating temperature for solar cell.
$Tri\ (t)$	Carrier signal.
V_c	Terminal voltage of the solar cell.
$V_{DC\text{-}HB\,i}$	Instantaneous DC-link voltage of inverter phase (i= a, b, c).
$V_{DC\text{-}HB\,ij}$	$V_{DC-HB\,ij}$ instantaneous DC-link voltage of the H-bridge unit (i= a, b, c), (j=1,2).
V_{L1L2}, V_{L2L3},V_{L3L1}	Grid line to line voltages.
V_{L1N}, $V_{L2N,}$ V_{L3N}	Grid phase voltage in phase $L1$, $L2$ and $L3$ respectively in relation to the neutral point (N) of the grid.
$V_{MPPT\text{-}HB\ ij}$	Reference voltages obtained from MPPT algorithm unit for a certain DC-link connected to H-bridge in phase (i=a, b, c) cell (j=1, 2).
V_{OC}	Open circuit voltage for solar cell.
V_a, $V_{b,}$ V_c	RMS voltage of the inverter in phase a, b and c respectively.
V_{ab}, $V_{bc\ ,}$ V_{ca}	Line to line voltages of the inverter.

V_{an} , V_{bn} , V_{cn}	CHB Output phase voltage in phase *a*, *b* and *c* respectively in relation to the neutral point (n) of the inverter.
$V_{error\text{-}HB\ ij}$	DC-link error for H-bridge unit in phase (*i=a, b, c*) cell (*j=1, 2*).
V_g	RMS voltage of the grid.
V_{mpp}	Maximum voltage obtained from the solar cell.
V_{nN}	Common mode voltage between the inverter (n) and the grid (N) neutral points.
V_{out}	Output voltage obtained from the solar cell.
$V_o(t)$	Output voltage of the inverter.
$V_{o.1}(t)$	Output voltage in the upper HB uint inverter.
$V_{o.2}(t)$	Output voltage in the lower cell of the inverter.
$V_{ref\,\alpha,}$ $V_{ref\,\beta}$	α- and β-component of the reference voltages in the stationary α-β frame.
$V_{ref\,d,}$ $V_{ref\,q}$	d- and q-component of the reference voltages in the rotating d-q frame.
$V_{ref\,a}$, $V_{ref\,b}$, $V_{ref\,c}$	Reference voltages for phase *a*, *b*, and *c* respectively.
$V'_{ref\,a}$, $V'_{ref\,b}$, V'_{refc}	Reference voltages after compensation process in per-phase for phase *a*, *b*, and *c* respectively.
$V''_{ref\,a}$, $V''_{ref\,b}$,V''_{refc}	Reference voltages after compensation process in per-cell for phase *a*, *b*, and *c* respectively.
V^*_{DC}	Reference voltages.
$\overline{V_{DC}}$	Maximum allowable voltage ripple.
$v_{\alpha,}$ v_β	Voltages in the stationary *α-β* frame.
v_d , v_q	Voltages in the rotating d-q frame.

ΔV_{MPPT}	Perturbation step size.
x_α and x_β	α- and β- component for the grid (x can be current or voltage) in α-β coordinate.
x_d and x_q	d- and q- component for the grid (x can be current or voltage) in d-q coordinate.
Zero-vector	Zero-sequence voltage.
θ	Displacement angle between the α-axis and d-axis.
ω	Frequency of grid voltage in radian.

CHAPTER ONE

INTRODUCTION AND LITERATURE REVIEW

1. 1 Introduction

In recent years, the generation of electricity using different renewable sources such as photovoltaic and wind energy has become an important and unlimited issue. As well as it is clean, widely available, and renewable. Therefore, to connect these sources to the grid, power electronic converters are required to use. These parts are known as inverters that convert a DC power to an AC power [1]. The conventional inverter usually provides an output voltage with two levels ($\pm V_{DC}$), hence it is called a two-level inverter [2], [3]. The two-level inverter has been utilized in grid connection since the mid-1970s [4], [5]. In high voltage and power field applications, this inverter operates at a high switching frequency suffering high switching losses, high *dv/dt* stress, and a high level of total harmonic distortion, making it unsuitable for medium to high voltage grid connection [6].

Multilevel inverters (MLIs) have existed in industrial applications since 1975, especially those that require high power AC drive systems such as electric trains, power stations, and renewable sources applications [6]. Multilevel inverters can provide several features summarized that include higher output voltage levels, low switching losses, higher power quality, reduced output harmonic distortion, staircase waveform quality, and small common-mode voltage [1], [6], [7]. Multilevel inverters may be realized in three main topologies, Cascaded H-Bridge inverter (CHB) [8], Diode Clamped/Natural Point Clamped inverter (NPC) [9], [10], and Flying

Capacitor (FC) topology [11]. Although there is much research to improve the performance of these topologies, some of these topologies are hybrid or modifies the existing configurations [12].

The topology of cascaded H-bridge multilevel inverter (CHBMLI) has been commonly utilized in photovoltaic (PV) applications [13]–[22], wind application and hybrid systems [23]–[26]. It offers a large number of output voltage levels by connecting a large number of separated DC sources. This topology also improves the efficiency of the system by allowing separated maximum power point tracking (MPPT) for each H-bridge. Therefore, this topology is a more suitable method for grid connection photovoltaic systems [16], [27].

The main challenge in a three-phase cascaded H-bridge inverter is the power balancing between the three phases resulting from the partial shadow and inconsistent temperature on the PV array which is connected to the inverter as a DC source. That means the total injected current should be balanced hence the grid voltage is already balance. This project presents a three-phase five-level inverter in grid connection PV application.

A control system is designed and simulated to overcome the problem of unbalanced operation condition PV system. In addition to the unbalanced problem, the maximum power point tracking unit is designed to satisfy maximum power injection to the grid.

1. 2 Literature reviews

In the following some important works that related to the present work are reviewed and discussed:

Alvarado and Eltimsahy had introduced the first grid connected PV inverter system. Where in the middle of the 1970s, a study was made about the solar cell arrays performance when it is directly coupled to the three-phase electric power networks [4].

Potter has presented an analysis study in 1981 about the power switching for a series of capacitors commutated inverter (SCC) to effectively interface the photovoltaic system to the power electric grid improvement, so that power quality is improved [2].

At the end of the 1980s, Jewell et al. have introduced the centralized photovoltaic inverter topology in some projects in the USA to interface the photovoltaic to the grid [5].

The multi-central inverter was proposed by Bae and Kim [3] which is a high-capacity three-phase full-bridge inverter system that was achieved by connecting many PV power plants.

There are various modified and enhanced variants of the three-level neutral point clamped NPC inverter (3L-NPC) that were designed and studied by Saridakis et al. for grid connection PV string inverters [10].

A control scheme for single-phase seven-level cascaded H-bridge (CHB) inverter for PV grid connection system discussed by Kouro et al. [13]. The control method is based on the traditional voltage oriented control (VOC) with a cascaded voltage loop and current loop in both loops, a proportional integral (PI) controller has been used with two additional stages. The first one is to control the DC-link voltage drift by adding a feedforward scheme in the modulation stage while the other tracks the maximum power point for individual PV strings.

The characteristic of eleven-level CHB inverter for grid connection of PV system discussed in [14] by Huang et al. who is used a double loop control method similar to [13] except that the controller used in the current loop is proportional resonant (PR) which is an improved PI controller and can track AC signal with zero steady-state error. In addition, the characteristics of CHB which use The phase shift pulse width modulation (PS-PWM) were described. The basic principle of this technique is that each unit combination has been used the conventional sinusoidal PWM but it needs five triangular carrier signals. These signals are shifted from each other by $\pi/5$, and the modulation waves for the right arm and left arm in each H-bridge are ahead for 180°.

A control method for a three-phase five-level inverter is presented by Agoro et al. [15]. In this paper, the number of the semiconductor switches is reduced to eighteen switches compared to the conventional multilevel inverter to reduce the switching losses and the system cost. A modulation method is used to regenerate the control signal into two main signals: one for the upper leg and the other for the lower leg to handle the unbalanced power between PV each phase.

Comparison and analysis between two zero-sequence injection methods and a novel method proposed by Wang et al. [16]. Analysis and simulation of a three-phase 5-level inverter was applied to obtain the phase angle and amplitude of zero-sequence component via the power errors calculation in order to solve the power unbalance issue.

Two feedforward compensation circuits are proposed by Rivera et al. [17], for seven-levels cascaded H-bridge PV system to deal with unbalanced power that occurs not among the cell in each phase only, but also among the three phases.

Ajith and Fernandes used a method to eliminate the phase unbalance power [19] which has employed a topology driven from traditional CHB and needed an isolated dc-dc converter to eliminate the leakage current and to extract the maximum power point for each PV independently. This topology redistributes the power equally between the phases but required a multi-winding transformer which increases the complexity of the design.

A single-phase multi-string PV configuration for a large scale PV system with a single DC bus bar is experimentally confirmed by Fuentes et al. [20]. The system has several conversions stages where the PV string with their dc-dc converter are connected to a common bus which is connected to the H-bridge (HB) units through isolated fly-back dc-dc converters. Because of the increased number of conversion stages, the system achieves galvanic isolation and independent MPPT at a lower system efficiency and cost. Furthermore, while fly back converters are known for their low cost and simple design, they suffer from discontinuous output currents that increase the generated harmonics and impair efficiency compared to other isolated topologies.

A three-phase 7-level cascaded H-bridge converter has been presented by Rivera et al. [21]. It is used for grid connection of large scale PV system with multiple string dc-dc converter to obtain the maximum power point for each string. The proposed configuration used in this paper allows to increase the total capacity of the PV and improve the power quality and efficiency and handle power balancing between phases from one side and another side, power balancing between cells in each phase.

A three-phase cascaded H-bridge multilevel inverter for PV grid connection application was studied by Noman et al. [22] with two other cascaded voltage source inverter (VSI). One of them used inductors and the

other used coupled transformers. In all topologies, the perturb and observation (P&O) algorithm was used, and an isolated Cuk dc-dc converter was used with each PV module for best maximum power point tracking, but in CHB, the total cost for the system and switching losses are increased. The three configurations are functional as the simulation and experimental results shows.

Li et al. have presented a large-scale grid connected PV system with cascaded H-bridge cells coupled to PV modules via an isolated current fed dual active bridge (CF-DAB) dc-dc converters which enabled by using a small film capacitor to prevent the large frequency DC voltage ripple produced by the PV array. In addition, the variable step size maximum power point tracking algorithm is proposed [28], [29].

Boonmee and Kumsuwan have presented a control scheme for a single-phase five-level cascaded H-bridge based on modified ripple correlation control maximum power point tracking (MRCCMPPT). The mean function concept was used to design this algorithm which continuously corrects the maximum power point of power transferring from each PV string and quickly reaches the MPP in rapidly shading irradiance [30].

An enhanced distributed maximum power point tracking (DMPPT) algorithm is proposed by Coppola et al. [31], The suggested control technique overcomes the working limits of the CHB inverter by integrating a limitation of the individual cell modulation index into the MPPT algorithm.

The space vector modulation (SVM) proposed by Matsa et al. [32], [33] is one of the modulation techniques. These papers resolved the space vector diagram for five-level CHB into two level inner and outer space vector

hexagons. The proposed method reduces the time of calculation and effort without affecting the inverter's output voltage.

The same system configuration used in [21] was employed by Morya and Shukla in [34], except that each HB unit of a five-level inverter was linked to a dc-dc converter so that MPPT can perform separately. A space vector modulation approach (SVM) is also employed instead of phase shift PWM.

Ranjan et al. has presented the Level shift PWM (LS-PWM) [35], in this paper, analysis of the performance for 5, 7, 9, 11, 13, and 21-level CHB with level shift PWM method phase disposition (PDPWM), phase opposition disposition (PODPWM), and alternative phase opposition disposition (APODPWM) and a comparison study for total harmonic distortion (THD) at two different switching frequency was produced. And found that CHB with lower THB is widely used in practical applications such as solar cells.

Mishra and Singh have presented a PV system connected to the grid through a single stage single-phase five-level cascaded H-bridge inverter. Decoupled control has been added to ensure good power flow for the system with sinusoidal PWM switching which helps to correct reactive power and gives good harmonics mitigation [36].

1. 3 Aims of work

The aim of this project can be summarized as follows:

1. The photovoltaic grid connection system is designed and simulated using MAT LAB/Simulink environment under different operation conditions, in which the resulted unbalanced power is addressed.
2. A three-phase cascaded H-bridge multilevel inverter is employed to integrate the PV arrays into the grid. In addition to modularity, the proposed configuration intends to address the unbalanced power that arises not only between the multi cells in one phase but even within the three phases. The modules mismatches, partial shading, and dust are affecting the PV arrays productivity and generate unbalanced power leading to unbalanced injected current to the grid which is effectively most be compensated.
3. Traditional voltage oriented control (VOC) with two extra stages is used and realized for the compensation technique without using dc-dc converter units. The PV arrays have been directly connected to the inverter and the output of MPPT algorithm has been carried to be used in feedforward compensation in the modulation stage.
4. The phase shift pulse width modulation (PS-PWM) has been used to generate the pulse train to control the ON/OFF time for the semiconductor switch of the CHB inverter.

1. 4 Thesis organization

This thesis is structured into five chapters. The chapters' outline is summarized as following:

Chapter Two involves the theoretical background for Cascaded H-Bridge multilevel inverter grid connection PV system.

Chapter Three describes the proposed system topology in details with its characteristics and features.

Chapter Four presents and discusses the simulation results for the system performance.

Chapter Five discusses the conclusions and suggestions for future studies.

Part of this work has been published in the 1st International Ninevah Conference on Engineering and Technology (INCET 2021)/ IOP Conf. Series: Materials Science and Engineering [37].

CHAPTER TWO

THEORETICAL BACKGROUND

2. 1 Introduction

This chapter presents the multilevel inverter fundamentals and the modulation techniques that can be used. In addition, the basic model for the photovoltaic panels is presented as it is required to illustrate the idea proposed in this study are also presented.

2. 2 Multilevel inverter and its topologies

The voltage source inverter (VSI) that generates an output voltage with (0 or ± V_{DC}) is called a two-level inverter. To obtain an output with good quality waveform and with minimum harmonics, a high switching frequency is required. However, this inverter has some limitations at high frequency when it operates at high power and high voltage due to the device rating constraints and switching losses. Furthermore, semiconductor switching devices should be employed in such a way to avoid difficulties with their series–parallel combinations, which are required to achieve high voltage and current [38].

In the late 1960s, multilevel inverter technology began with the invention of the multilevel stepped waveform concept with connected several H-bridge (HB) in series which is called a cascaded H-Bridge inverter. In the same year, the low-power development of a flying capacitor (FC) topology was closely developed. The diode-clamped converter (DCC) was initially founded in the late 1970s, and developed into the three-level NPC (3L-NPC) converter we know today, which is the first real multilevel converter for medium voltage

applications. After that, the CHB inverter was introduced again in the late 1980s, though it would reach greater industrial relevance in the mid-1990s. Similarly, in the early 1990s, the FC circuit, which was first proposed in the 1960s for low power, evolved into the medium-voltage multilevel converter topology as it is known today [39].

Multilevel inverter presents a good solution due to its features that focused to improve the quality of output voltage waveform closer to sinusoidal by increasing the levels of its output which means a reduction in total harmonic distortion (THD) [40] as shown in figure (2-1). In addition, it has high power handling capability and it reduces the switching losses and operates with lower (*dv/dt*) , as well as its ability to draw the current with low distortion [41]. These features make the multilevel inverter very attractive in a large range of industrial applications as shown in figure (2-2) [12].

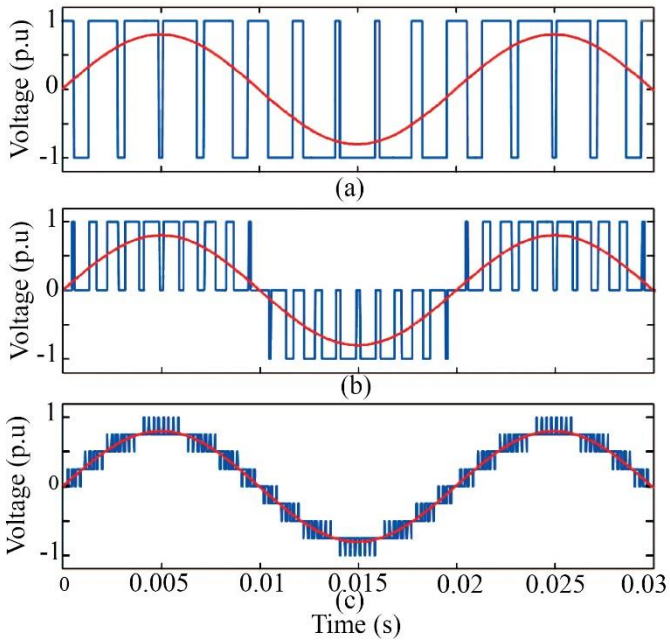


Figure (2-1): The output phase voltage for (a): two-level inverter, (b): three-level inverter, (c) nine-level inverter.

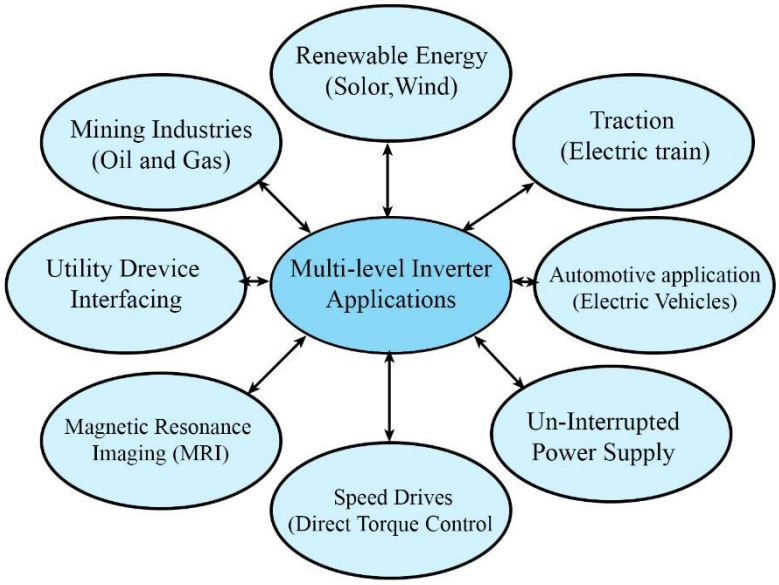


Figure (2-2): Multilevel inverter applications.

2.2.1 Neutral point clamped (NPC) multilevel topology

The three-level output voltage stepped waveform is produced using both diodes clamped to the middle of both DC-link capacitors. The middle point between the DC-link capacitor is considered as the natural point as well as the reference point for the phase voltage. Because the output voltage waveform is generated from the DC-link capacitor voltage, the number of diode elements required to clamp increases as the number of output voltage levels increases. Therefore, this (3L-NPC) topology evolves to a multilevel diode clamped inverter (MDCI). As the number of output voltage levels increases, the number of capacitors needed in the DC-link increases [42]. The number of semiconductor switches (s) and the diodes (D) for (L) output phase voltage level may be given as [43]:

$$s = 2[L - 1] \tag{2-1}$$

$$D = 2[L - 2] \tag{2-2}$$

The number of DC-link capacitors (C_{DC}) may be determined as:

$$C_{DC} = L - 1 \tag{2-3}$$

The DC voltage theoretically should equally have distributed between the DC-links, but practically, the mismatch between the active and passive elements will cause unbalance condition. Furthermore, due to the switching method adopted, the amount of charging and discharging current flowing through the diodes clamped between each pair of DC-link capacitors is unequal. As a result of the imbalanced DC-link capacitor voltages, the MDCI topology becomes ineffective and difficult to obtain a higher number of output phase voltage levels. The three-phase multilevel diode clamped inverter is shown in figure (2-3) [43].

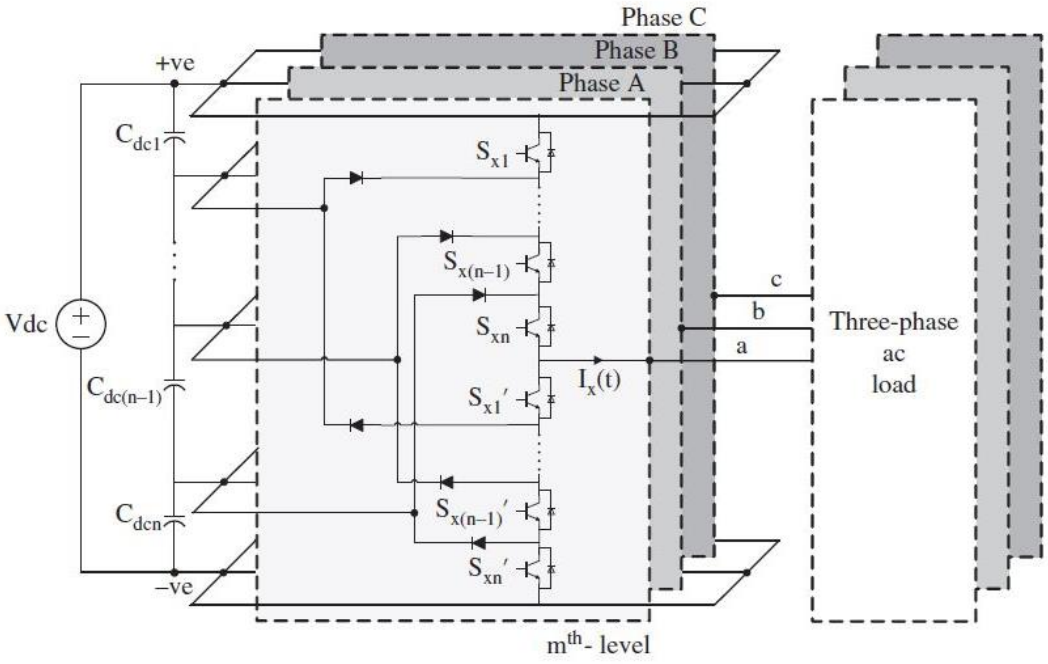


Figure (2-3): Three-phase multilevel diode clamped inverter [43].

2.2.2 Multilevel Flying Capacitor Inverter (MFCI) topology

The MFCI inverter topology does not need to use any clamped diode, instead of that it uses capacitors without connecting directly to the negative or positive rails of the DC source, hence the name " flying" or "floating" capacitor topology [44]. The three-phase flying capacitor multilevel inverter is shown in figure (2-4). This topology builds in cell concept whereas each cell consists of two semiconductor switches with its clamped capacitor. As the number of cells increases, the number of the output phase voltage level increase. The number of semiconductor switches (s) and capacitor (C_P) that are required for ($L= k+1$) output voltage level can be found by equations (2-4) and (2-5) respectively depending on the number of cells (k).

$$s = k * 2 \tag{2-4}$$

$$C_P = k - 1 \tag{2-5}$$

As the number of capacitor elements increased for high-level MFCI, a large inrush current was produced at the startup period is caused by damage in semiconductor power rating. Because the capacitor is a passive element that stores energy, this stored energy affects the voltage quality across it and affects switching and conducting losses.

As a result, these factors are considered as a disadvantage in the design of MFCI for high output level, and make the MFCI is utilized for high speed drives and for applications that require low current ripples [43].

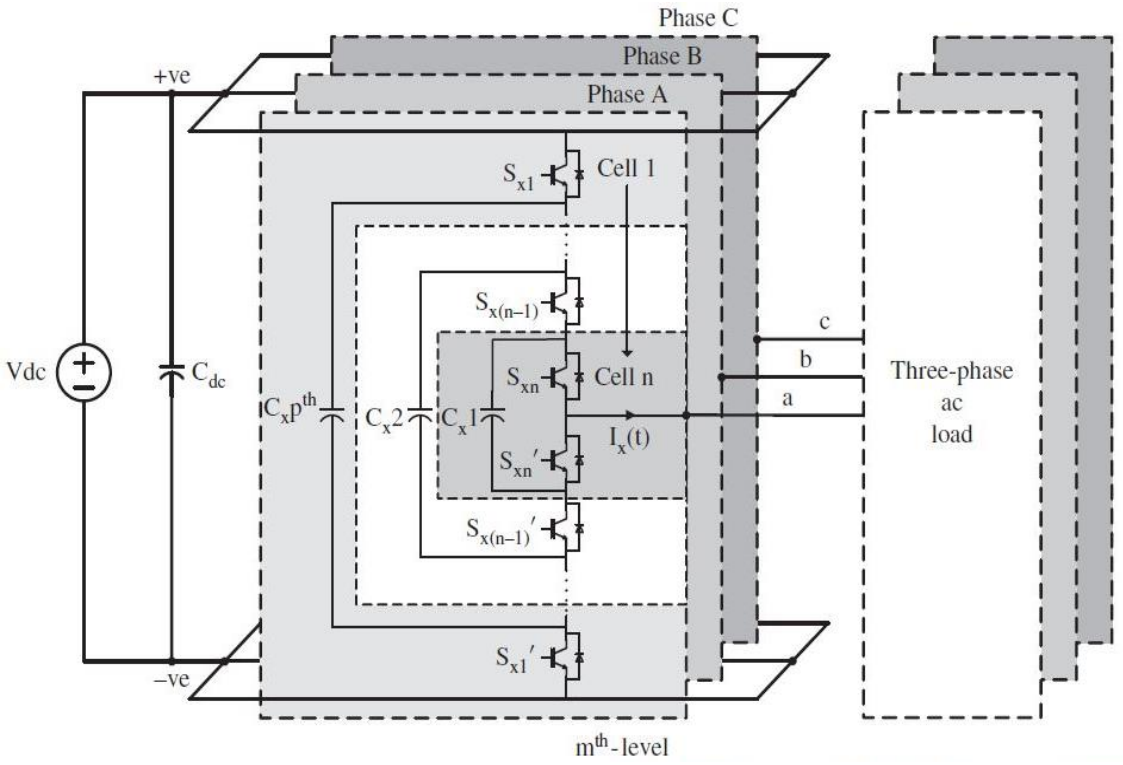


Figure (2-4): Three-phase n-cell multilevel flying capacitor inverter [43].

2.2.3 Cascaded H-Bridge multilevel inverter (CHBMLI) topology

The three-phase cascaded H-bridge multilevel inverter (CHBMLI) is shown in figure (2-5). Three-phase CHBMLI means three single CHB are connected in (Y) form. Each phase consists of several full-bridges each has a separate DC source called a cell. In contrast, the bridge consists of four IGBTs switches with an anti-parallel diode. The number of cells (h) that are used in a single-phase determines the specified output voltage level (L) as in equation (2-6) [45].

$$L = 2h + 1 \qquad (2\text{-}6)$$

The total output voltage level of each phase is the sum of the voltages that are generated by the cells, where each cell is capable of producing an output voltage level of $-1V_{DC}$, 0, $+1V_{DC}$. The output voltage for a 5-level inverter is $-2V_{DC}$, $-1V_{DC}$, 0, $+1V_{DC}$, $+2V_{DC}$ voltages [35].

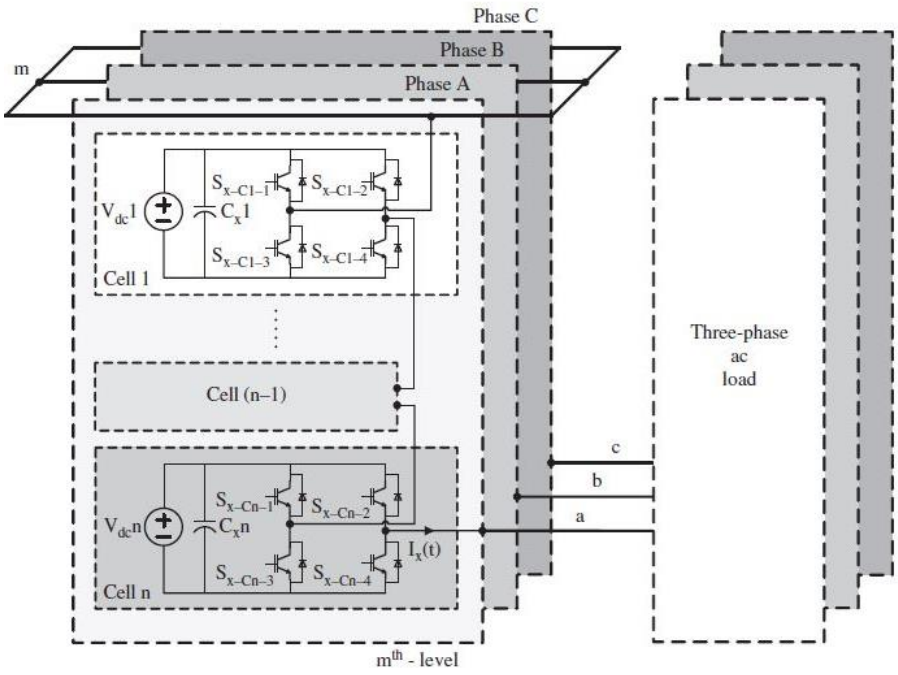


Figure (2-5): Three-phase cascaded H-bridge [43].

The CHBMLI has become preferred at high output voltage levels (more than 11-level). The voltage looks as close as the pure sinusoidal which means it can obtain both lower total harmonic distortion and reduces the filter's size. But the disadvantage of this topology is that it needs a separated DC source for each HB which increases the system size and cost. In situations where several distinct DC sources currently existing, such as PV arrays or hybrid systems with many discrete sources, the architecture CHB becomes particularly interesting. [12], [43].

The number of switches (s) and the DC-link capacitor (C_{DC}) can be calculated through equations (2-7) and (2-8) respectively depending on the number of the cell (h) [43].

$$S = h * 4 \tag{2-7}$$

$$C_{DC} = h \tag{2-8}$$

2. 3 Modulation methods for multilevel inverter

To obtain an output voltage with low distortion as smooth as sinusoidal waveform, it is important to design a modulation circuit to generate pulses (gating signals) that control the ON/OFF time for the semiconductor switches [46], The modulation techniques used in the multilevel inverter are [47]:

- Space Vector Pulse Width Modulation (SVPWM).
- Multi-Carrier Pulse Width Modulation (MCPWM).
- Selective Harmonic Elimination (SHE) [47].

The most used technique is Multi-Carrier Pulse Width Modulation (MCPWM), where the gating pulsating signals are typically generated by comparing the reference sinusoidal signal to the triangular carriers. The switching pulses will be in the "ON" condition when the reference signal is greater than the triangular carrier, and vice versa it will be in the "OFF" condition when the reference signal is smaller than the carrier as shown in figure (2-6).

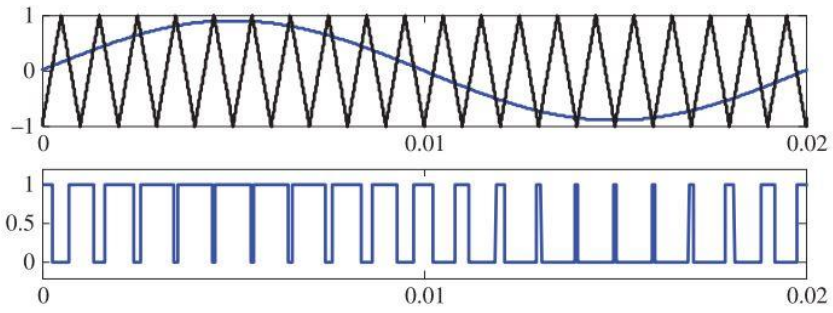


Figure (2-6): Principles of MCPWM [43].

The condition of the switching pulse during the modulation period is expressed as follows in equation (2-9) [43]:

$$s_x(t) = \begin{cases} 1 & \text{if } \sin(\omega t) > \text{tri}(t) \\ 0 & \text{if } \sin(\omega t) < \text{tri}(t) \end{cases} \quad (2\text{-}9)$$

MCPWM comprises two common methods, Level Shift PWM and Phase Shift PWM:

2.3.1 Level Shift Pulse Width Modulation (LS-PWM)

In the level Shift Pulse Width Modulation (LS-PWM), all carrier signals are equal in amplitude, frequency, and phase but dispositioned vertically relative to the zero reference line. For a 5-level CHB inverter, it needs (L-1) carrier signals for (L) output voltage levels resulting in four carrier signals, two of them are above the zero reference line, and the other two signals are below the zero reference line. The amplitude modulation index is defined as in equation (2-10) [7], [48]:

$$m_a = \frac{A_m}{(L-1)A_C} \quad (2\text{-}10)$$

Where: A_m is the peak to peak amplitude of the sinusoidal reference signal.

and A_c is the amplitude of the triangle carrier signal.

Level shift pulse width modulation (LS-PWM) can be classified into three main techniques:

- Phase Disposition (PD): in this category of (LS-PWM), all carrier signals are in phase with each other, as shown in figure (2-7) (a).
- Phase Opposition Disposition (POD): in this technique, the carrier signals above the zero reference line are shifted by 180° out of phase with those signals under zero line. Figure (2-7) (b) shows the carrier signals positioning to the zero line and the sinusoidal reference signal.
- Alternative Phase Opposition Disposition (APOD): in this technique, each carrier signal is dispositioned 180° out of phase with its neighbor carrier, as shown in figure (2-7) (c) [35].

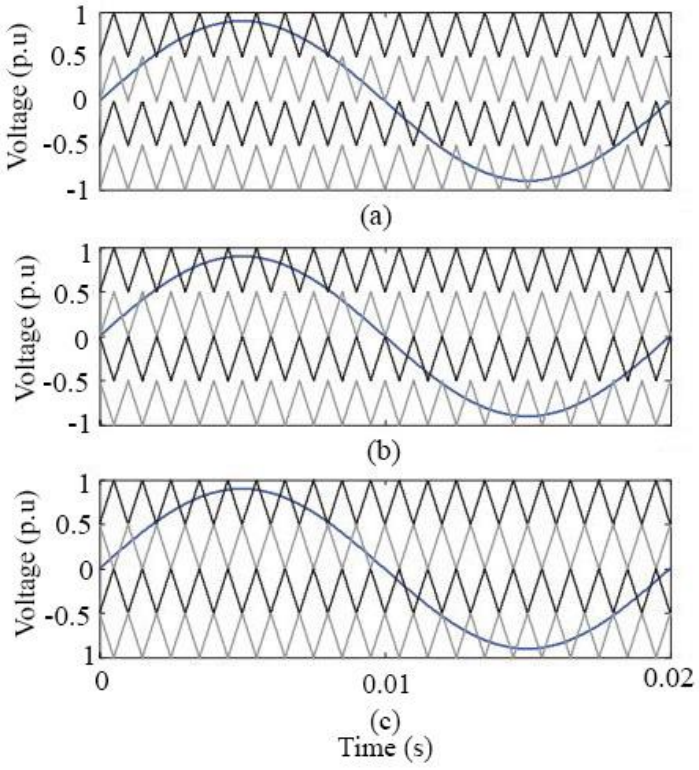


Figure (2-7): LS-PWM technique: (a) PD, (b) POD, (c) APOD [43].

2.3.2 Phase Shift Pulse Width Modulation (PS-PWM)

Phase Shift Carrier Modulation (PS-PWM) is the most common method used in multilevel inverter due to its simple implementation and it has some advantages such as even power distribution and the output current has high quality waveform [49]. The amplitude modulation index can be defined as [50]:

$$m_a = \frac{A_m}{A_C} \tag{2-11}$$

For cascaded H-bridge multilevel inverter shown in figure (2-8) with two HB units "two cells", two carrier signals were needed (which are equal in amplitude and frequency), one for each cell, the two signals are phase shifted by 90^o according to $\frac{180^\circ}{h}$, where *h* is the number of cells in each phase [44], [51]. The block diagram for the modulation circuit and the waveforms are shown in figure (2-9).

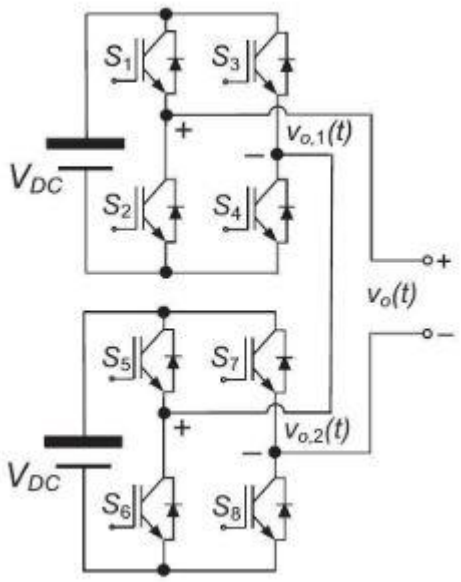


Figure (2-8): Five-level CHB inverter [44].

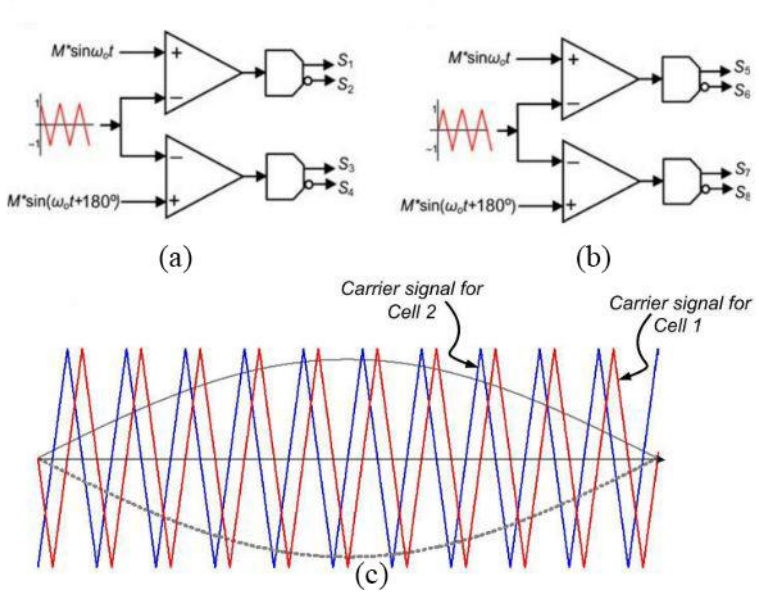


Figure (2-9): PS-PWM circuit block diagram for (a): cell 1, (b): cell 2, (c): PS-PWM waveforms [44].

Where each cell produces a three-level output voltage and by cascading is produces a five-level pulsating output waveform as shown in figure (2-10).

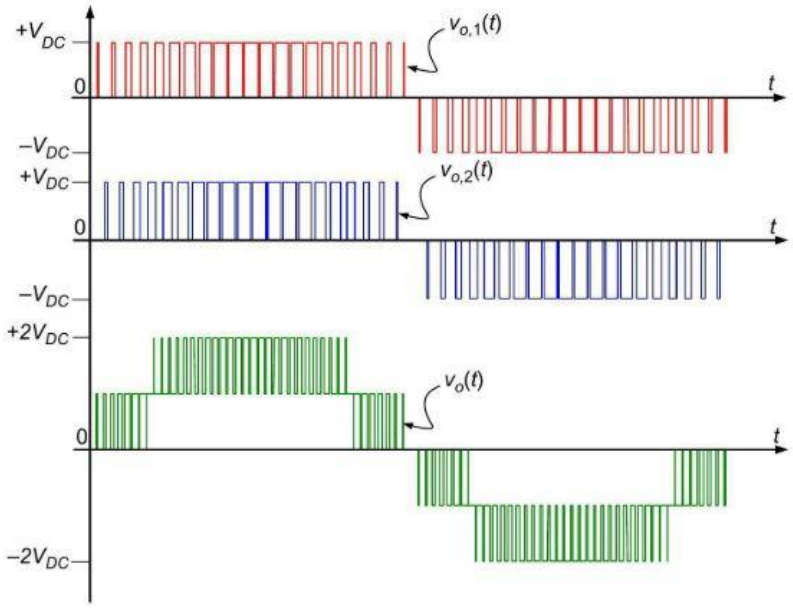


Figure (2-10): Output voltages waveforms for 5-level CHB inverter [44].

2.3.3 Phase Shift PWM with zero-sequence injection

In traditional sinusoidal PWM, the modulation index range is ($0 \leq m_a \leq 1$). However, when ($m_a > 1$), the inverter operates in the over modulation area, resulting in increased harmonics at the output voltage. Therefore, by adding a zero-sequence signal to the reference signal, the utilization of DC-link improved [52]. By using this method, the linear region in phase voltage would have expanded as the modulation index increased to (15%) before getting into over modulation area and the double step in line to line voltage will be reduced as it will be illustrated in chapter 4. Figure (2-11) shows the zero-sequence block diagram. This technique determined the average of instantaneous minimum and maximum of the three-phase reference voltages ($V_{ref\ a}$, $V_{ref\ b}$, and $V_{ref\ c}$) to obtain the *zero_vector* which will be subtracted from each reference voltage individually to get the modified reference signals $V'_{ref\ a}$, $V'_{ref\ b}$, and $V'_{ref\ c}$ as in the following [53]:

$$zero\_vector = \frac{\max(V_{ref\ a}, V_{ref\ b}, V_{ref\ c}) + \min(V_{ref\ a}, V_{ref\ b}, V_{ref\ c})}{2} \quad (2\text{-}12)$$

$$V'_{ref\ a} = V_{ref\ a} - zero\_vector \quad (2\text{-}13)$$

$$V'_{ref\ b} = V_{ref\ b} - zero\_vector \quad (2\text{-}14)$$

$$V'_{ref\ c} = V_{ref\ c} - zero\_vector \quad (2\text{-}15)$$

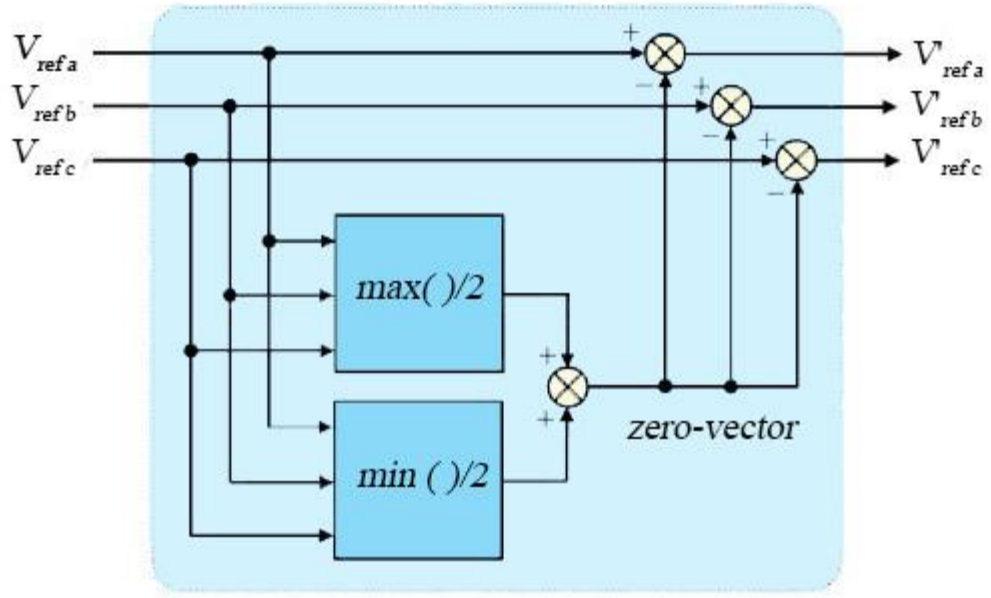


Figure (2-11): The block diagram of zero-sequence injection.

Figure (2-12) shows the three-phase ideal reference voltages $V_{ref\,a}$, $V_{ref\,b}$, and $V_{ref\,c}$ before adding zero-sequence in (a), its maximum and minimum signals with *zero_vector* in (b). And in (c) the reference voltages $V'_{ref\,a}$, $V'_{ref\,b}$, and V'_{refc} after adding *zero-vector*.

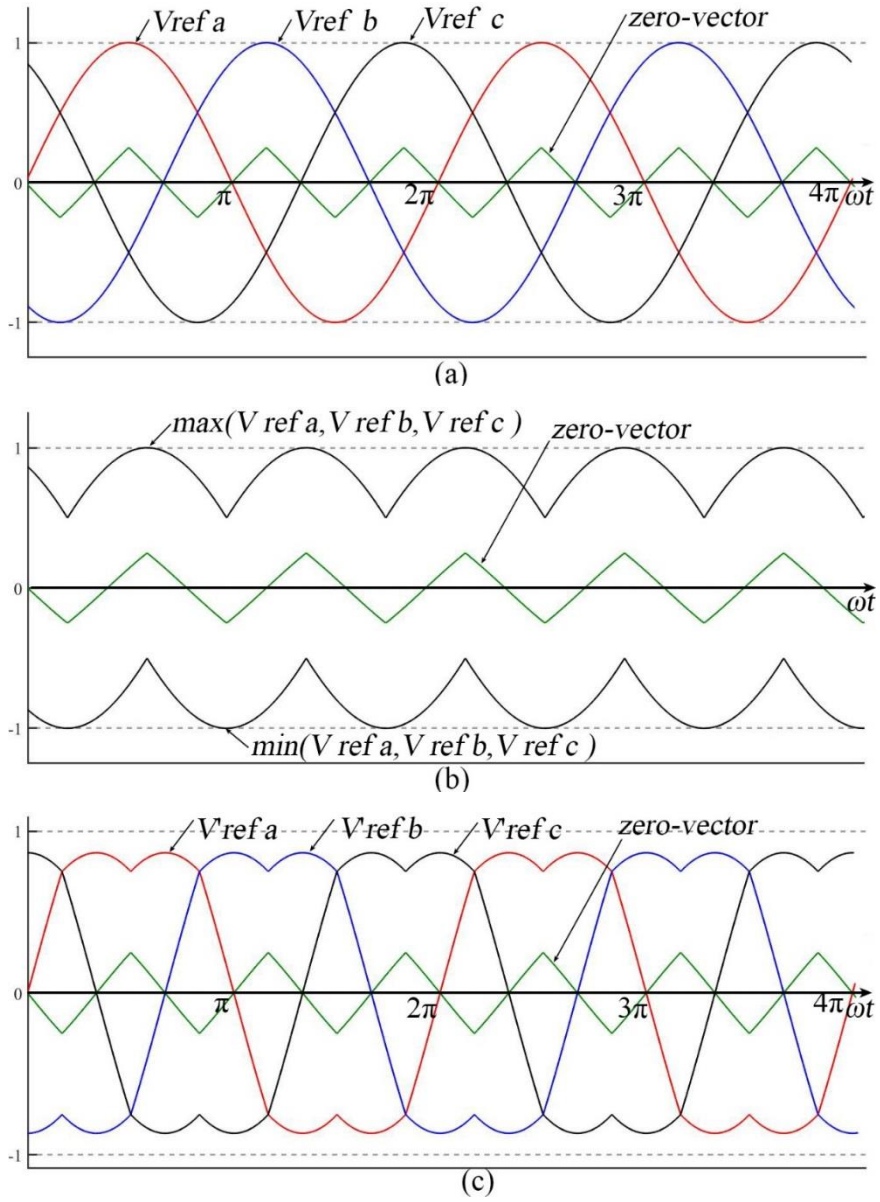


Figure (2-12): PS-PWM with *zero_vector* (zero-sequence signal) (a): ideal reference voltages, (b): the maximum and the minimum signals with *zero_vector*, (c) modified reference voltages.

2. 4 Solar energy

The energy that exists in sunlight is called solar energy. In the outer atmosphere, the density of power radiated from the sun is 1.373 kW/m^2 [53]. The earth's atmosphere absorbs and scatters a portion of this energy.

Therefore, the final incident sunlight on the earth's surface reaches a peak density of 1 kW/m^2 at noon. This energy can be converted to electricity by two methods bases on electrodynamic and thermodynamic concepts. If the energy is directly converted by using semiconductor devices, the resulted is a system known as photovoltaic which can consider the basic concept of the solar cell. On the other hand, if the solar energy is converted to heat, then the system is called thermal energy which is thermodynamic laws dependent and differs from solar energy which is electrodynamic dependent and utilizes the solid state to generate electricity [53], [54].

The electricity generated by the solar cell system is capable of being used in home appliances such as televisions, lamps, and refrigerators. It is intriguing particularly in distant areas where there is poor access to the traditional electrical grid, these types of systems are defined as stand-alone PV systems. In such circumstances, some additional storage units, such as a battery bank, are necessary.

Another method to use the PV source is to link the PV panels with the grid without using a battery bank through power electronic converters. In this configuration different amounts of power can be injected in to the grid from a few kW as it used in home roofs to several megawatts used in large scale PV plants [53].

2.4.1 Solar cell structure

Solar cell is considered as the basic and smallest element in a PV system that converts solar energy to an electrical one. The solar cell structure is nearly to that of the diode. Where, it is composed of two layers of P-type and N-type semiconductor material (often silicon Si) which have different electrical

characteristics due to different doping. In order to obtain the P-type semiconductor some accepter atoms as boron are added to excess the positive charge carrier known as holes, and by adding donor atoms as phosphor to obtain the negative charge carrier in N-type known as electron. According to the doping difference in the layers and at the junction between them an internal electric field will appear.

When sunlight enters the solar cell, the stored energy in the photons of the light forms free charge carriers, and the electrical field at the junction between the two layers separates these carriers which will produce in the internal terminal an electrical voltage while a current will flow if a load connected to it as shown in figure (2-13) [53].

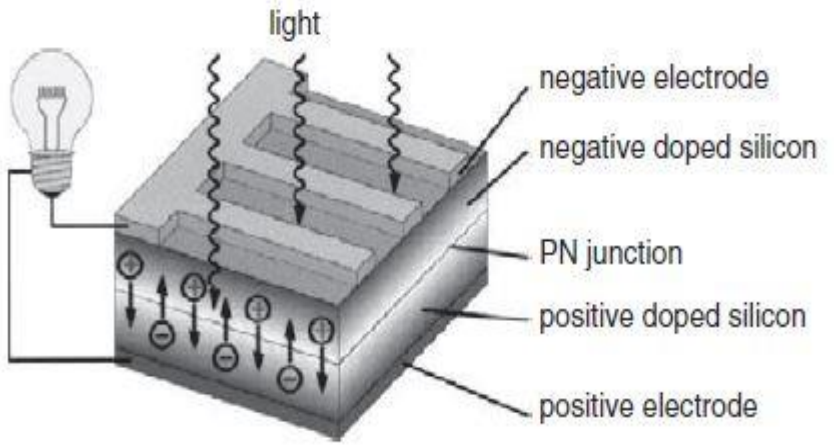


Figure (2-13): The principle of solar cell operating [53].

2.4.2 Ideal solar cell

The ideal solar cell can be modelled as shown in figure (2-14). It is represented as a current source with rectifier diode connected in parallel if a variable resistor load connected to the solar cell, and when the resister value reduced to (zero) which means a short circuit applied to the solar cell terminals

and the voltage across the diode will become almost (zero), at that moment the photo current which is produced by the cell will flow through the load and it will be the maximum current for the cell and is called short circuit current I_{SC}. If the load resister value increased, the photo current divided between the diode and the load as a result a voltage will appear across the two terminals of the solar cell. If the value of the resistor keeps rising to infinity, an open circuit appears and the photocurrent flows through the diode. Also, a voltage will generate between the solar cell terminals. This voltage will be the maximum voltage across the terminals and called the open circuit voltage V_{OC} [53], [55].

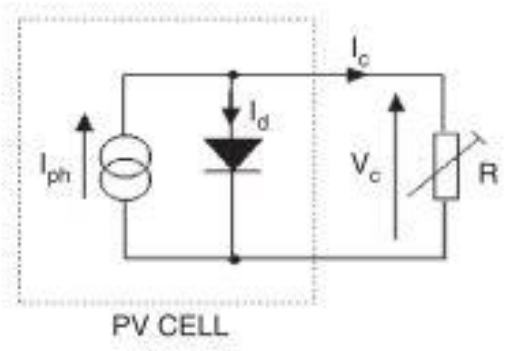


Figure (2-14): Simplified solar cell with variable resister [53].

The respective I-V characteristics can be found by the Shockley solar cell equation (2-16):

$$I_c = I_{ph} - I_0 \left(\exp\left(\frac{qV_c}{KT}\right) - 1 \right) \qquad (2\text{-}16)$$

Where I_{ph} is the photo current, I_0 is the reverse diode current, q is the electron charge, V_C is the terminal voltage of the cell, K is the Boltzmann constant, and T is the operating temperature of the solar cell (°K) [55].

Figure (2-15) illustrates the typical I-V characteristic of the solar cell, where the solar cell can operate at any point on it.

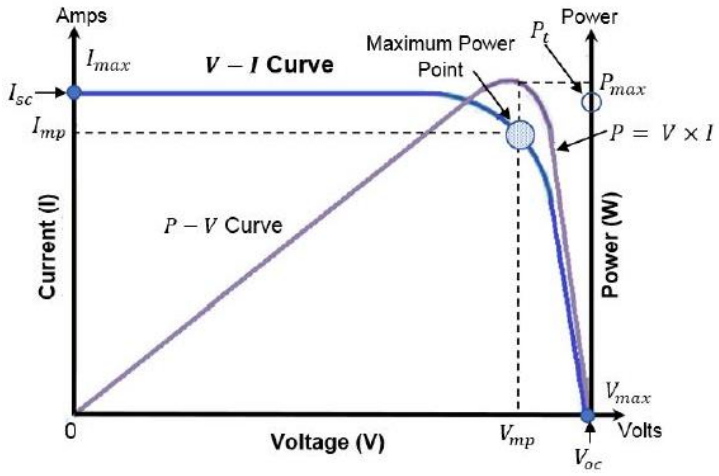


Figure (2-15): I-V and P-V curves for ideal solar cell [56].

2.4.3 Fill factor and maximum power

The fill factor (FF) can be defined as the measurement of the solar cell quality, which is the ratio of the maximum power (P_{mpp}) obtained from the solar cell to the theoretical power (P_t). Graphically fill factor is the ratio between the rectangular, where less rounded I-V curve mains a higher fill factor would provide and a high-quality solar cell [56].

$$FF = \frac{P_{mpp}}{P_t} = \frac{I_{mpp}V_{mpp}}{I_{SC}V_{OC}} \tag{2-17}$$

The output power obtained from the solar cell is determined from the output and the current produced as:

$$P_{out} = v_{out} * I_{out} \tag{2-18}$$

There is no power would generate, under short and open circuit condition, the output power will be (zero) if any of the voltage or current is (zero).

The maximum output power can be obtained from the maximum values of the voltage and current. There is only one point in the curve presents the P_{mpp} and defined in equation (2-19) [56].

$$P_{mpp} = v_{mpp} * I_{mpp} \quad (2\text{-}19)$$

2.4.4 Influence of sun irradiation and ambient temperature on solar cell

The performance and the I-V characteristics of the solar cell effected by two main parameters: the sun irradiation and the operation temperature. Figure (2-16) shows the influences of these two parameters on the solar cell performance, wherein figure (2-16) (a) the short circuit current increase linearity as the sun irradiation increases, therefore, the MPP increases, while the open circuit voltage increases logarithmically with the irradiation increment. In figure (2-16) (b) the effect of the ambient temperature appears on the cell characteristics. The open circuit voltage decreases linearity as the temperature increase, while the short circuit current slightly increased with the temperature increment [57].

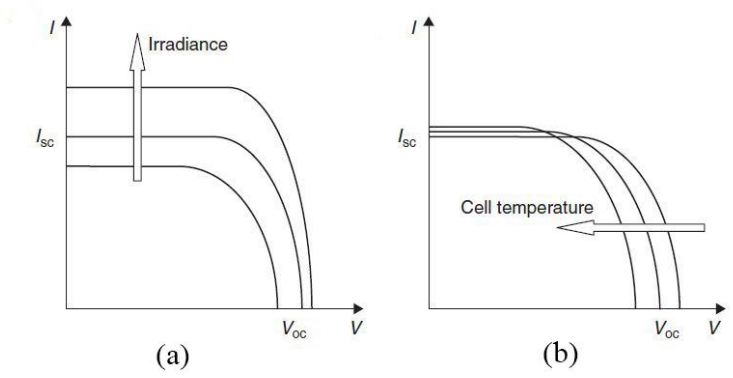


Figure (2-16): I-V characteristics under: (a) irradiation influence, (b): temperature influence [57].

2.4.5 Solar cell configurations

Solar cells can be connected in series or parallel in practice. Figure (2-17) illustrates how the I–V curve changes when two identical cells are connected in (a) in parallel and (b) in series. If two identical cells are connected in parallel, the voltage remains constant while the current duplicated. As the cells are connected in series, the current remains constant while the voltage duplicated [57].

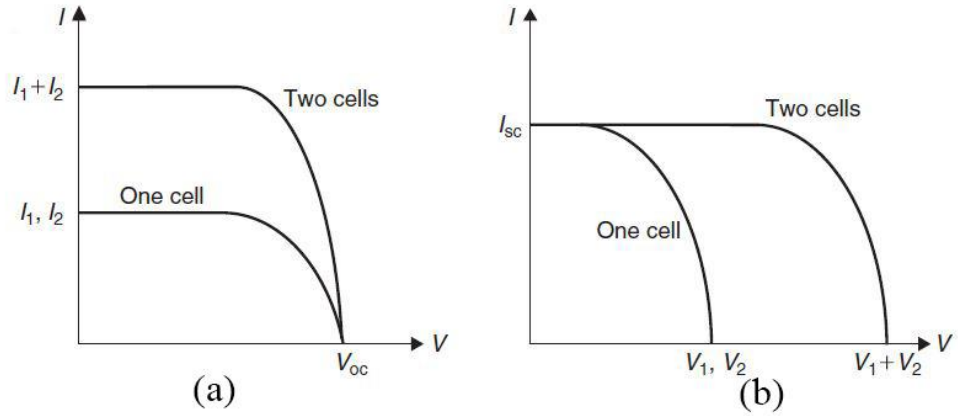


Figure (2-17): Two solar cells connection (a): in parallel, (b): in series [57].

Therefore, a higher voltage produced if several cells are connected in series, that configuration will define as *PV module*, and a higher current produced if connected a number of *PV modules* in parallel, the configuration is called *PV panel*. Additionally, to extract the *PV array* arrangement, more than one *PV panel* connected in series and parallel [53], as shown in figure (2-18).

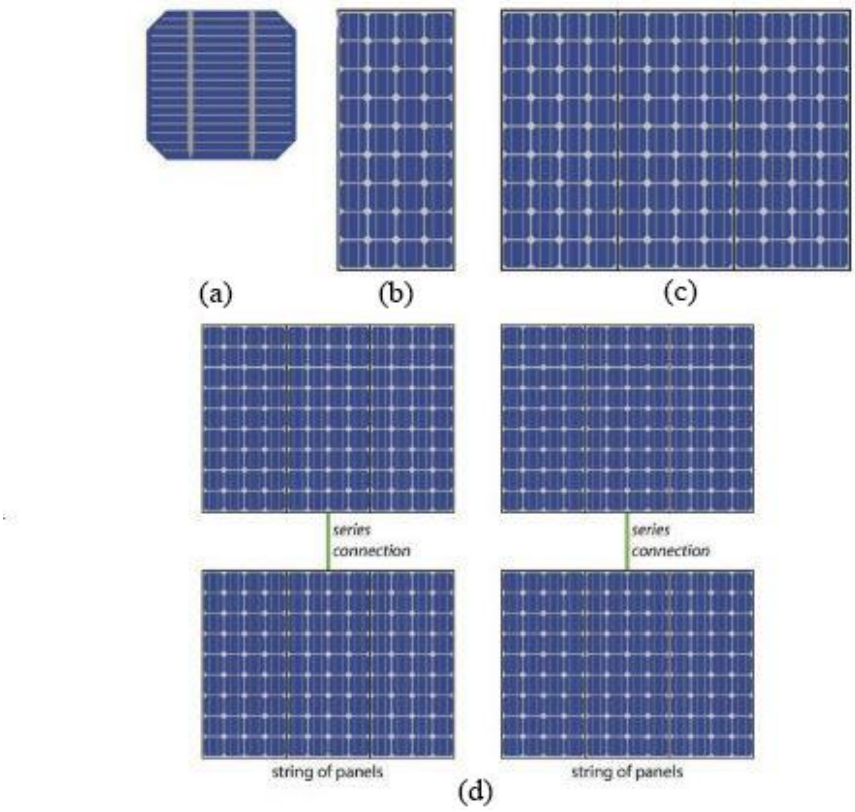


Figure (2-18): PV configurations (a): a cell, (b): a module, (c): panel, and (d): array [54].

CHAPTER THREE

DESIGN OF PV SYSTEM FOR GRID CONNECTION

3.1 Introduction

In this chapter, the complete system for connecting the PV arrays to the grid through cascaded H-bridge inverter is described and investigated with its characteristics and features. The proposed system configuration will be described and the voltage oriented control (VOC) with phase lock loop (PLL) and maximum power tracking (MPPT) and finally the feedforward compensation will be presented.

3.2 Proposed system configuration

The proposed three-phase grid connection system is shown in figure (3-1). In this configuration, six PV arrays are connected to the grid via CHB inverter, where each PV array is connected to individual DC-link for the inverter's cells as proposed in [21] except that the PV arrays are directly connected to the inverter without using dc-dc converter to get more system reliability and to decrease system complexity as the number of components decreased. Furthermore, the use of a CHB allows utilizing an individual MPPT algorithm for each of the converter's power cells.

As shown in figure (3-1) the power system consists of four main parts: cascaded H-bridge multilevel inverter with their independent DC-link, PV arrays that feed to the inverter's DC-link, RL filter, and the grid.

In general, the CHB inverter is composed of H-bridge cells that are all connected in series where each cell produces three different voltage values as an output. The total output voltage is generated by the summation of the

outputs of these series cells. In the used configuration the two series cell will produce a five-level output phase voltage.

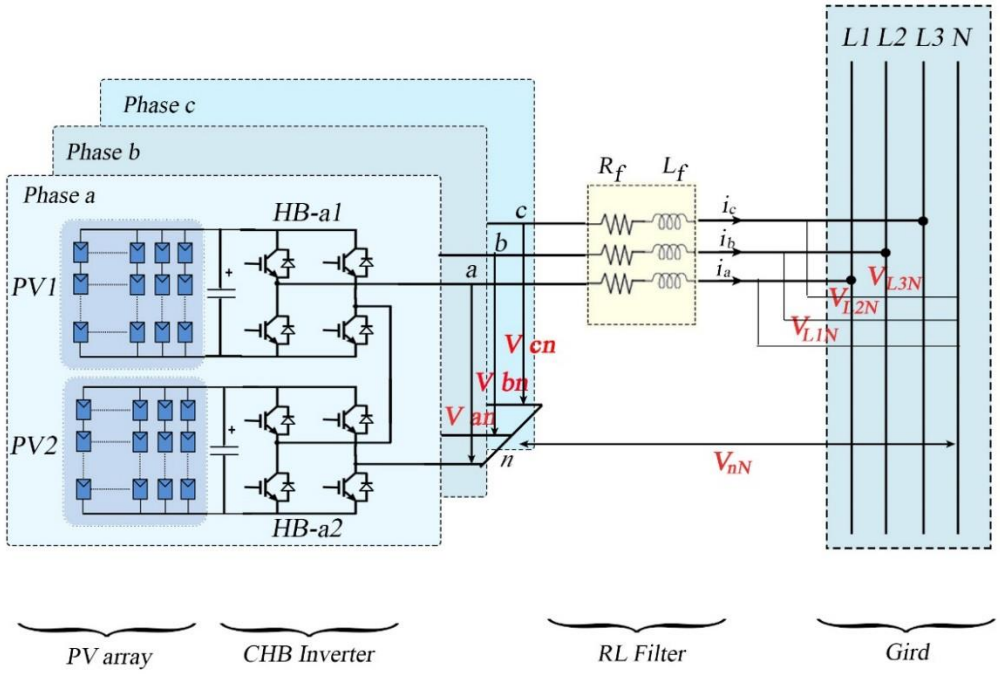


Figure (3-1): Three-phase grid connection PV system.

For three-phase system the output phase voltages for CHB in phase *a*, phase *b*, and phase *c* are given as equations (3-1), (3-2), (3-3) respectively [22].

$$V_{an} = hm_a V_{DC-HB\ ij} \sin(\omega t) \tag{3-1}$$

$$V_{bn} = hm_a V_{DC-HB\ ij} \sin(\omega t - 120°) \tag{3-2}$$

$$V_{cn} = hm_a V_{DC-HB\ ij} \sin(\omega t + 120°) \tag{3-3}$$

Where h is the number of HB units connected in a single-phase, m_a modulation index, and $V_{DC-HB\ ij}$ is the DC-link voltage for the inverter in

phase (i= *a*, *b*, *c*) and (j= *1* for upper cell and j=*2* for lower cell). So, by applying Kirchhoff's voltage law, the line to line voltages are given by equations (3-4), (3-5), (3-6) respectively [22]. The voltage value across the R_f is small and neglected

$$V_{ab} = (j\omega L_f)i_a + V_{L_1L_2} + (j\omega L_f)i_b \quad (3\text{-}4)$$

$$V_{bc} = (j\omega L_f)i_b + V_{L_2L_3} + (j\omega L_f)i_c \quad (3\text{-}5)$$

$$V_{ca} = (j\omega L_f)i_c + V_{L_3L_1} + (j\omega L_f)i_a \quad (3\text{-}6)$$

Where:

$$V_{L_1L_2} = V_{L_1N} - V_{L_2N} \quad (3\text{-}7)$$

$$V_{L_2L_3} = V_{L_2N} - V_{L_3N} \quad (3\text{-}8)$$

$$V_{L_3L_1} = V_{L_3N} - V_{L_1N} \quad (3\text{-}9)$$

And:

$$V_{L_1N} = \sqrt{2}V_g \sin(\omega t) \quad (3\text{-}10)$$

$$V_{L_2N} = \sqrt{2}V_g \sin(\omega t - 120°) \quad (3\text{-}11)$$

$$V_{L_3N} = \sqrt{2}V_g \sin(\omega t + 120°) \quad (3\text{-}12)$$

Whereas V_g is the RMS voltage of the grid, and ω is the grid frequency in radians, $i_a, i_b,$ and i_c are the injected currents to the grid and expressed by equation (3-13), (3-14), (3-15) [22].

$$i_a = \sqrt{2}I \sin(\omega t) \quad (3\text{-}13)$$

$$i_b = \sqrt{2}I \sin(\omega t - 120°) \quad (3\text{-}14)$$

$$i_c = \sqrt{2} I \sin(\omega t + 120°) \tag{3-15}$$

where I is the RMS line current.

The apparent power produced in each phase can be calculated by equations (3-16), (3-17), (3-18) [22].

$$S_a = V_a I_{a,RMS} = \left(\frac{hm_a}{\sqrt{2}} V_{DC-HB\ ij}\right) I_{a,RMS} \tag{3-16}$$

$$S_b = V_b I_{b,RMS} = \left(\frac{hm_a}{\sqrt{2}} V_{DC-HB\ ij}\right) I_{b,RMS} \tag{3-17}$$

$$S_c = V_c I_{c,RMS} = \left(\frac{hm_a}{\sqrt{2}} V_{DC-HB\ ij}\right) I_{c,RMS} \tag{3-18}$$

The power produced by each HB unit in single-phase determined as:

$$S_{HB-ij} = V_{ij} I_{i,RMS} = \left(\frac{m_a}{\sqrt{2}} V_{DC-HB\ ij}\right) I_{i,RMS} \tag{3-19}$$

Whereas i is the phase *a*, *b*, or *c*, and j is the HB unit number.

In order to transfer power from the PV generating part to the grid, the inverter input voltage for each phase must be more than the grid voltage [58].

$$V_{DC-HB\ i} \geq \sqrt{2} V_g \tag{3-20}$$

$$V_{DC-HB\ i} = V_{DC-HB\ i1} + V_{DC-HB\ i2} \tag{3-21}$$

$$S_{HB\ i} = S_{HB\ i1} + S_{HB\ i2} \tag{3-22}$$

For example, by considering a two-cell inverter, if a grid voltage of 220 V RMS and PV module can deliver 29 V at the maximum point, a string of at least eight modules connected in series to each cell is needed to meet this requirement.

3.3 Operation cases for photovoltaic grid connection system

The purpose of using a CHB inverter for a photovoltaic system is to allow the generating PV system to operate and inject the produced power into the grid daytime by operating with independent MPPT for each H-bridge. So, only a single voltage source inverter is used for this purpose with no extra power electronic components connected to it. Furthermore, a control strategy is developed to manage the various cases of operation without requiring any changes in system installation.

If the effects of temperature are ignored and a wide range of sun irradiance is taken into account, the output voltage of the PV will slightly vary. Where, the sun irradiation has low effects on the output voltages as shown in figure (3-2), the PV generated power will vary between minimum and rated output voltage and this varying depends on sun irradiation (S_{IR}).

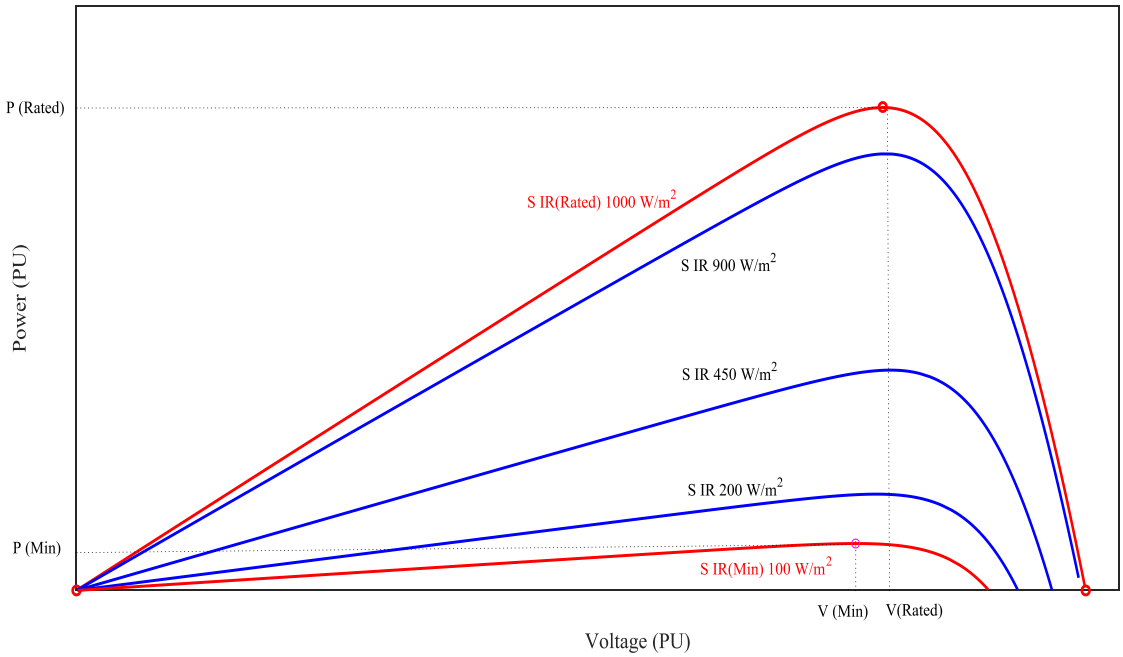


Figure (3-2): P-V characteristics for different sun irradiance.

According to that and as explained in equations (3-21), (3-22), the system has six operating cases depending on the power generated by the PV during the whole day.

- Zero operation case:

There is no power will inject into the grid in this case of operation, because the sun irradiance is (zero) or, in specifically, lower than the sun irradiance range which is able to generate and transfer power.

- Active operation cases:

There are eight operation cases listed in table (3-1), the PV arrays that connected to the inverter as DC source are operating either at their limits or in the region between the minimum and the rated generated power depending on the effects of sun irradiance on it.

Table (3-1): Different operating cases of PV system.

Operating Cases	Upper PV Arrays			Lower PV Array		
	HB-a1	HB-b1	HB-c1	HB-a2	HB-b2	HB-c2
Case 1	Rated power	Rated power	Rated power	Rated power	Rated power	Rated power
Case 2	Minimum power	Rated power	Rated power	Rated power	Rated power	Rated power
Case 3	Minimum power	Minimum power	Rated power	Rated power	Rated power	Rated power
Case 4	70% rated power	Rated power	Rated power	Minimum power	Rated power	Rated power
Case 5	Minimum power	Minimum power	Minimum power	Rated power	Rated power	Rated power

Case 6	Minimum power	Minimum power	Minimum power	Minimum power	Minimum power	Minimum power
Case 7	0	Rated power	Rated power	Rated power	Rated power	Rated power
Case 8	0	Minimum power	Minimum power	Minimum power	Minimum power	Minimum power
Case 9	0	0	0	0	0	0

3.4 DC-link capacitor calculation

The capacity of the DC capacitor depends on the input DC voltage source and the maximum allowable voltage ripple as given in equation (3-23) [59]:

$$C_{DC} = \frac{S}{2\omega V_{DC}\overline{V_{DC}}} \tag{3-23}$$

Where C_{DC} is the DC-link capacitor value in Farad, S is the rated power of the inverter, ω is the grid frequency in radian, V_{DC} is the input DC voltage, and $\overline{V_{DC}}$ is the maximum allowable voltage ripple typically it should be below 8.5% to obtain maximum power from the PV array [59].

3.5 Control strategy of grid connection PV system

The major duty of the inverter in the field of grid integration of renewable power sources is to control the amount of active and reactive power that is delivered to the grid. The Voltage Oriented Control (VOC) approach is used in this study because it has a modulator stage in the control loop, whereas the modulator stage is having a great deal in this work because it generates a simple maximum power point tracking algorithm (MPPT) that is applied to each H-bridge unit separately. Furthermore, as will be explained in the

feedforward modulation index compensation stage, it is suitable to deal with power unbalance problems.

3.5.1 Proposed voltage oriented control (VOC)

Voltage oriented control is the most common control scheme in the grid connection application that consists of the modular stage that regulates the interaction between the CHB and the utility grid [17].

In VOC, the quantities of the three-phase system are converted to the stationary *alpha-beta* reference frame which is similar to field oriented control for an electrical machine [60].

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{3-24}$$

These new quantities will be converted to DC components in the rotating *d-q* frame because it is easier to deal with DC component as follows:

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{3-25}$$

Where *x* can be current or voltage.

In stationary *α, β* frame, the active power *P* and the reactive power *Q* can be calculated according to the following equations [61]:

$$P = \frac{3}{2}\left(v_\alpha i_\alpha + v_\beta i_\beta\right) \tag{3-26}$$

$$Q = \frac{3}{2}\left(v_\alpha i_\beta - v_\beta i_\alpha\right) \tag{3-27}$$

Where v_α and v_β are voltages in the stationary *α-β* frame.

i_α and i_β are currents in the stationary *α-β* frame.

Using space phasor $\omega t = d\theta/dt$, whereas ωt is the angular frequency of the grid voltage, and the active power P is directly related to the i_d. In contrast, the reactive power Q is related to the i_q according to equations (3-28) and (3-29), respectively [62].

$$P = \frac{3}{2}\left(v_d i_d + v_q i_q\right) = \frac{3 v_d i_d}{2} \tag{3-28}$$

$$Q = \frac{3}{2}\left(v_d i_q - v_q i_d\right) = \frac{3 v_d i_q}{2} \tag{3-29}$$

Where v_d and v_q are voltages in the rotating d-q frame.

i_d and i_q are currents in the rotating d-q frame.

However, it is noticed that when the rotating reference frame is synchronized with the grid voltage, v_q becomes (zero) to inject the current with the unity power factor [62], figure (3-3) shows the stationary and the rotating frames of VOC.

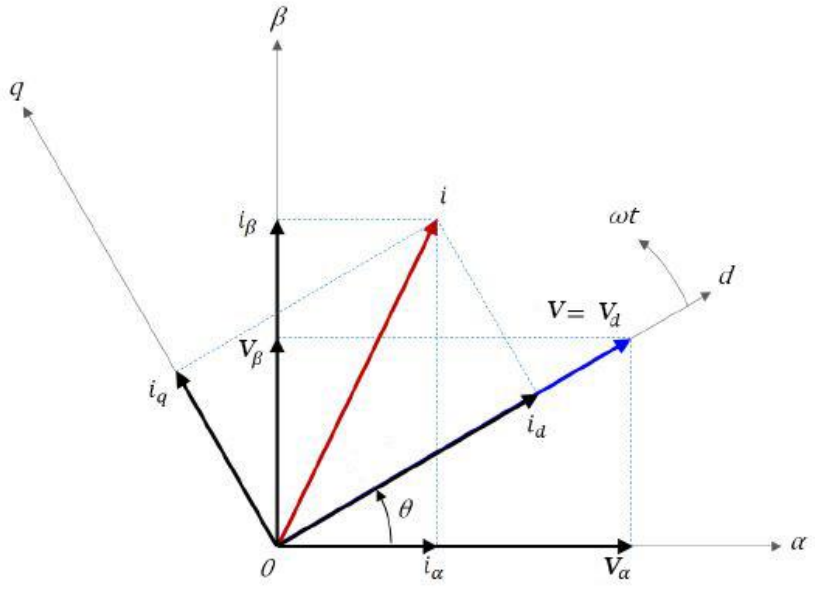


Figure (3-3): Space phasor diagram of VOC.

There are two control loops which identified from the traditional VOC, which is commonly used in conventional inverters with a single DC-Link: the current control loop and the voltage control loop. The current control loop is the inner loop which regulate the injected power between the inverter and the grid, whereas the voltage control loop which is the outer loop used to regulate the inverter's DC-link voltage.

The DC-link voltage V_{DC} in the voltage loop is measured and compared with the reference voltages V^*_{DC} to get an error signal e_t which will set to (zero) by using a proportional integral (PI) controller to produce the reference current value i^*_d.

The current loop started with grid current measurement and transferred from *abc* form to *α-β* to get (i_α and i_β) and then to *d-q* frame to obtain (i_d and i_q) by equations (3-24), and (3-25) respectively. The value of i_q compared with (zero) to ensure unity power factor in renewable sources system, and i_d compared with the i^*_d that obtained from the voltage loop. The error of these comparators will be sent to the PI controller to obtain reference voltages ($V_{ref\ d}$, $V_{ref\ q}$), which is converted to *α-β* coordinate ($V_{ref\ \alpha}$, $V_{ref\ \beta}$) by using equation (3-30) and then to *abc* system ($V_{ref\ a}$, $V_{ref\ b}$, $V_{ref\ c}$) using equation (3-31). The resulting voltages will be used as reference signals for the modulation stage to get the gating signals for the IGBT switches [60].

$$\begin{bmatrix} V_{ref\ \alpha} \\ V_{ref\ \beta} \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_{ref\ d} \\ V_{ref\ q} \end{bmatrix} \tag{3-30}$$

$$\begin{bmatrix} V_{ref\ a} \\ V_{ref\ b} \\ V_{ref\ c} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{ref\ \alpha} \\ V_{ref\ \beta} \end{bmatrix} \tag{3-31}$$

In this work, a five-level CHB inverter is used to interface the PV arrays to the grid. Figure (3-4) shows the voltage oriented control (VOC) block diagram with 5L-CHB. Two extra blocks are added to the traditional VOC: the first one is related to dedicate the performance of the MPPT calculation, and the second one is responsible for modulation index compensation. In the proposed strategy the voltage error signal in the voltage loop can be calculated as the difference between both the summation of the DC-link voltages and the summation of their references voltages determined from the MPPT algorithm.

$$e_t = \sum V_{DC-HB_{ij}} - \sum V_{MPPT-HB_{ij}} \quad (3\text{-}32)$$

Where *i* is the phase *a*, *b*, or *c*

And *j* represents the bridge lower=1, or upper=2.

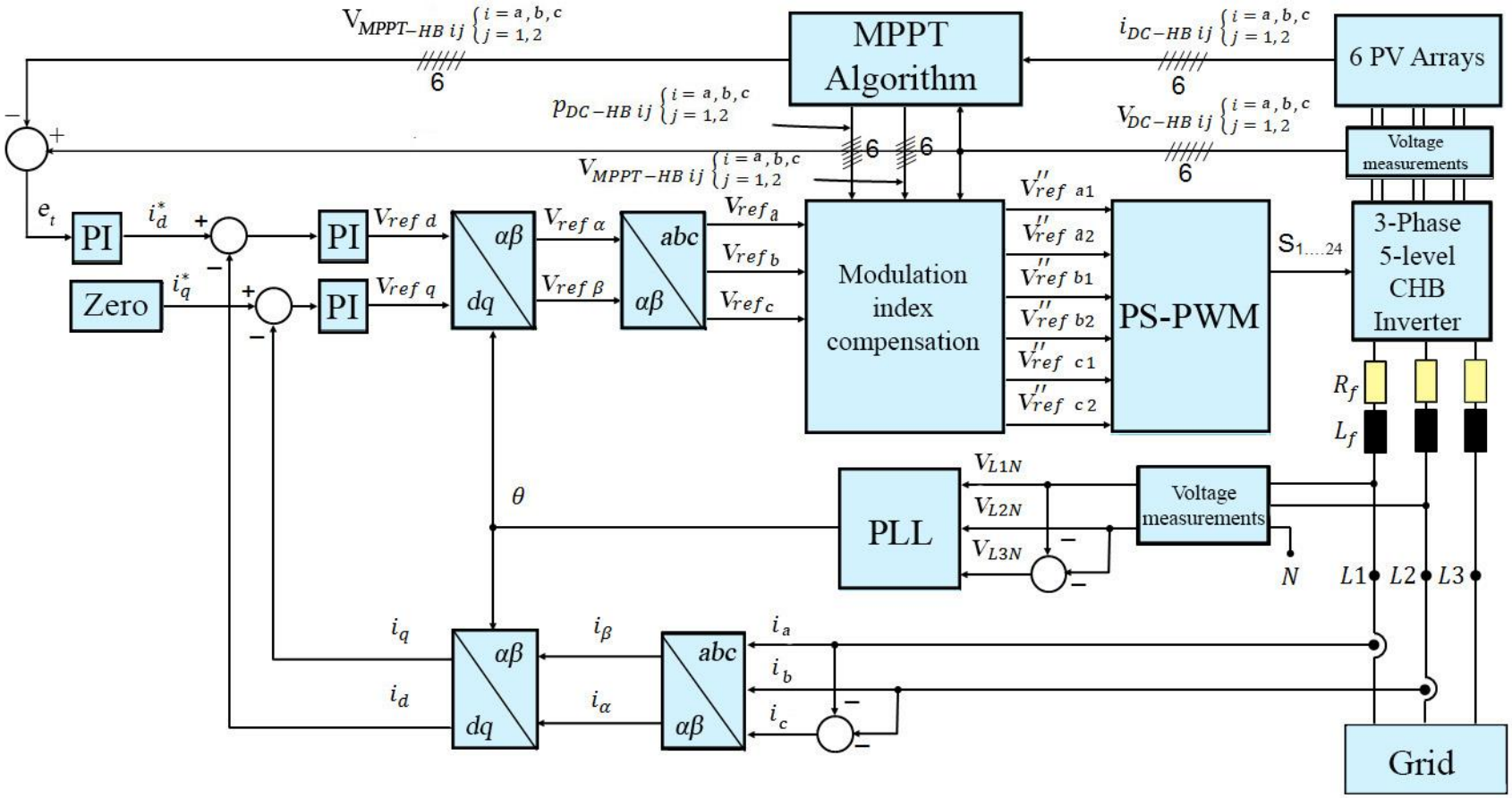


Figure (3-4): Modified VOC with MPPT unit and feedforward compensation.

3.5.2 Three-phase Phase Lock Loop (PLL)

In a grid connection system, the phase angle plays an important role in order to synchronize the inverter with the grid. The phase angle detection for the grid voltage must be fast and accurate to ensure the right alignment of the *d-q* system of coordinates [63]. The Phase Locked Loop (PLL) technique is used for phase angle detection due to its high noise-rejection capacity, so even in the presence of noise, it has a large dynamic range of operation and can identify the phase and frequency of a sinusoidal signal with high resolution [64].

The main function of the PLL is based on the principle of tuning a signal component depending on a reference signal. It consist of three main blocks: one for detecting the phase angle of the input signal by comparing it with the voltage controlled oscillator's (VCO) output signal, low pass filter to reject the noise and unwanted high frequency, and the last one is for generating an output signal using the signal identified in the first block as a parameter, which is utilized to feed the system [65]. Figure (3-5) shows the basic PLL scheme.

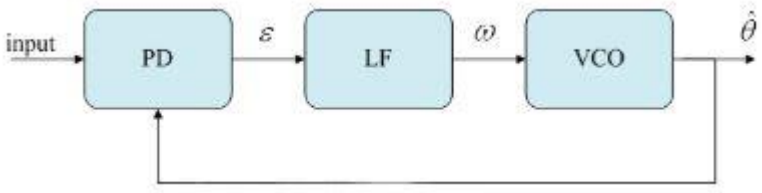


Figure (3-5): Conceptual PLL scheme [66].

The topology of a three-phase PLL is similar to that of a single-phase system. The system remains unchanged in both terms of its constituent parts and the method used to achieve synchronization between inputs and outputs, whereas the unique considerable difference is the *abc/dq* transformation [66].

Figure (3-6) shows the three-phase PLL block diagram. The three-phase voltages (V_{L1N}, V_{L2N} , and V_{L3N}) are converted to a rotating frame (V_d and V_q) using the angular speed of an internal oscillator. The *d* component represents the voltage vector amplitude while the quadrature component which is proportional to the phase difference between the grid voltages and the internal oscillator rotating frame is filtered with a (Mean Variable Frequency) block. The PI with the automatic gain controller (AGC) keep the phase difference equal to (zero) by acting on the controlled oscillator. In addition, the output of the PI controller is sent to filter to obtain the frequency in Hertz which will be used in the Variable Frequency block.

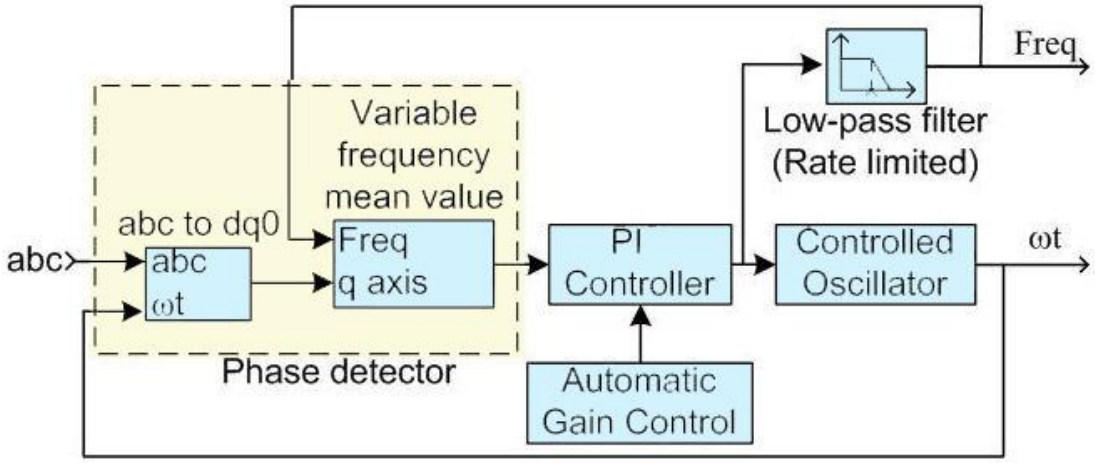


Figure (3-6): Three-phase PLL.

3.5.3 Maximum power point tracking unit

The tracking for the maximum power point algorithm has become an integral part of photovoltaic system operation. The majority of available algorithms provide a balance between simplicity, tracking speed, accuracy, and cost. However, as the generated power by the PV depends on the sun irradiation and the ambient temperature, the MPPT (Maximum Power Point

Tracking) algorithms are being developed to allow PV systems to run at their maximum power under different weather conditions [67]. There are many different algorithms about thirty approaches utilized in a PV system with several variations in implementation and all these methods are presented in [68].

The most common method among these approaches is Perturb and observe (P&O) algorithm. In this method, the controller perturbs the system behavior by changing its operating point slightly, then measures the new power value and compares it to the previous power level to establish the direction of perturbation. For more simplification, if the power increases in the comparison, the P&O algorithm keeps perturbing in the same way, but if the power decreases, it switches the perturbation to proceed in the opposite direction as illustrated in figure (3-7). Where there is only one MPP on the curve and the operation point oscillated between the points (A → MPP→ B→ MPP→ A) and Δ is the perturbation step size [69].

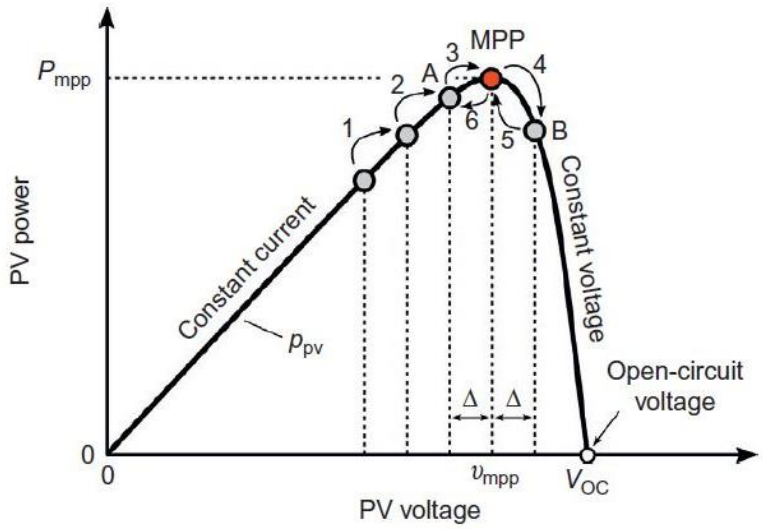


Figure (3-7): Perturb and observe (P&O) MPPT algorithm in P-V characteristics [69].

A dc-dc converter is generally used in the PV generator to interconnect the PV array to the load or the grid connected inverter. This dc-dc converter aligns the load to the PV array, ensuring that the PV operates at maximum efficiency and the maximum power is transmitted from the array to the load, so the duty cycle of the dc-dc converter is modified by the MPPT unit until the optimum power point is reached [70]. One of the modifications of this work is that the PV array is connected directly to the HB unit, eliminating the need for a dc-dc converter. As a result, the adaptation must be done during the modulation stage by adding the compensation as will be shown in the next section.

Generally, the P&O has a simple structure and needs few elements, and can be implemented on a digital controller since the algorithm is simple to code. Figure (3-8) shows the basics of P&O flow chart that run in this study.

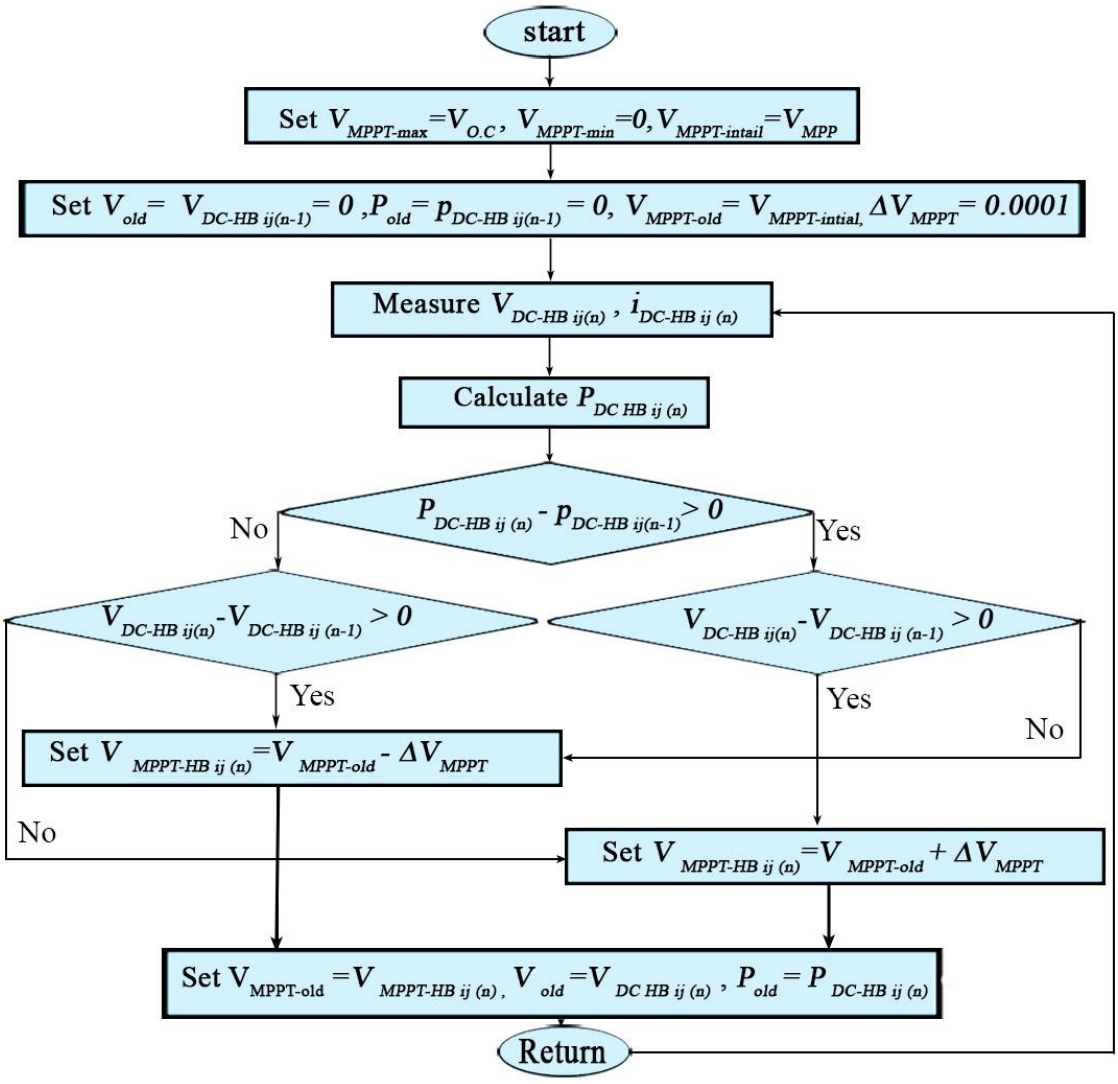


Figure (3-8): Perturb and observe (P&O) MPPT algorithm [67].

According to the principle of operation explained in the flow chart, the perturbation and observation in the grid connection PV system can be explained as follows: For PV1 that connected to the HB1 for phase *a*, the same process is executed for all PV. At every sampling time period, the current and the voltage is measured and the power is calculated too. The calculated power and measured voltages are compared with previously obtained values. Therefore, four operating modes are available, as shown in table (3-1).

Table (3-2): Operating modes of the P&O algorithm.

	$V_{DC\text{-}HB\ a1\ (n)} \uparrow$	$V_{DC\text{-}HB\ a1\ (n)} \downarrow$
$P_{DC\text{-}HB\ a1\ (n)} \uparrow$	Mode 1 $V_{MPPT\text{-}HB\ a1(n)} = V_{MPPT\text{-}old} + \Delta V_{MPPT}$	Mode 2 $V_{MPPT\text{-}HB\ a1(n)} = V_{MPPT\text{-}old} - \Delta V_{MPPT}$
$P_{DC\text{-}HB\ a1\ (n)} \downarrow$	Mode 3 $V_{MPPT\text{-}HB\ a1(n)} = V_{MPPT\text{-}old} - \Delta V_{MPPT}$	Mode 4 $V_{MPPT\text{-}HB\ a1(n)} = V_{MPPT\text{-}old} + \Delta V_{MPPT}$

It can be observed from the above table the following:

1. In modes 1 and 4: The output of the MPPT unit which is considered as a reference voltage ($V_{MPPT\text{-}HB}$) of this cell increased by a small perturbation value (ΔV_{MPPT}) in these modes the power goes to increment.
2. In modes 2 and 3: The reference voltage ($V_{MPPT\text{-}HB}$) is decreased by a small perturbation value (ΔV_{MPPT}) and the power will also increase.

3.5.4 Modulation index Feedforward compensation

As previously stated, the produced power from the PV array governed by two parameters: the sun irradiation and the operation temperature. Even when the same operating temperature affects the PV arrays, each of HB unit in the inverter is fed by several of PV panels in many sectors and as a large array. This will make them to work under different and changing conditions. So, the cloud for example, will make a partial shading on some of this PV array, therefore the maximum power produced by the PV connected to the HB unit in the phase will be different comparing with those operating in fully sun irradiation.

Therefore, two extremely essential considerations must be made in order to conduct grid integration of PV system using a CHB inverter. The first one is the balancing issue, in other words, the injected power should be balanced in order to transfer to the grid, and as the grid provide a voltage which is always balanced the injected current also should be balanced. The second factor to be considered is that it must utilize all of the power obtained from the PV and inject to the grid to get maximum efficiency and good system performance. To achieve that, two feedforward compensation circuits added to the traditional VOC. These circuits are applied on the reference voltages that get it from the current loop in the voltage oriented control VOC before sent it to the modulation stage:

- Per-phase compensation is the first sort of feedforward, and it is achieved by modifying the reference phase voltages.
- Per-cell compensation, on the other hand, is performed by compensating all the reference signal of each separated H-bridge.

1. Per-phase compensation (among the three phases)

The current loop in a VOC scheme is generating the three reference voltages that are delivered to the modulation stage to generate the inverter's output phase voltages waveform. And as all of the DC-link voltages are equal the system operate in balance state. However, even though the system has the same DC-Link voltages, each H-bridge unit of the inverter may send a different amount of power into the grid due to PV mismatching and partial shading, causing in an unbalanced current injected into the grid, and because of the balanced grid voltage, the power becomes imbalanced. To overcome that, an inverse imbalance voltage should be added to the output voltages of

the inverter which must be proportional to the unbalanced power. This achieved by moving the neutral point of the inverter [21]. Where the inverter phase voltages obtained from the power circuit in figure (3-1) can be written as:

$$V_{an} = V_{L1N} + R_f i_a + L_f \frac{di_a}{dt} + V_{n_N} \quad (3\text{-}33)$$

$$V_{bn} = V_{L2N} + R_f i_b + L_f \frac{di_b}{dt} + V_{n_N} \quad (3\text{-}34)$$

$$V_{cn} = V_{L3N} + R_f i_c + L_f \frac{di_c}{dt} + V_{n_N} \quad (3\text{-}35)$$

R_f and L_f is the resistor and the inductor of the filter, V_{n_N} is the common mode voltage which is the difference between the neutral point of the inverter (n) and the grid (N), with an average value equal to (zero) in the balance condition.

The above equations illustrated that the system line current which is also flow in each phase are depending on the output phase voltage of inverter at that phase, as well as depends on the common mode voltage V_{n_N}. Therefore, by shifting the inverter's neutral point, it become feasible to redistribute the power supplied by the three phases of the inverter in order to ensure inject balanced currents into the grid, even when unbalanced power distribution in the H-bridge unit. In this way, the phase of the inverter with the smaller MPP cell will provide a lower output voltage but with the same current as the other phases with normal MPP cells, as a result, the three-phase voltages are unbalanced, while the inverter line voltages, currents, and power become balanced. Figure (3-9) shows the inverter voltages in balance and imbalance conditions on the phasor diagram.

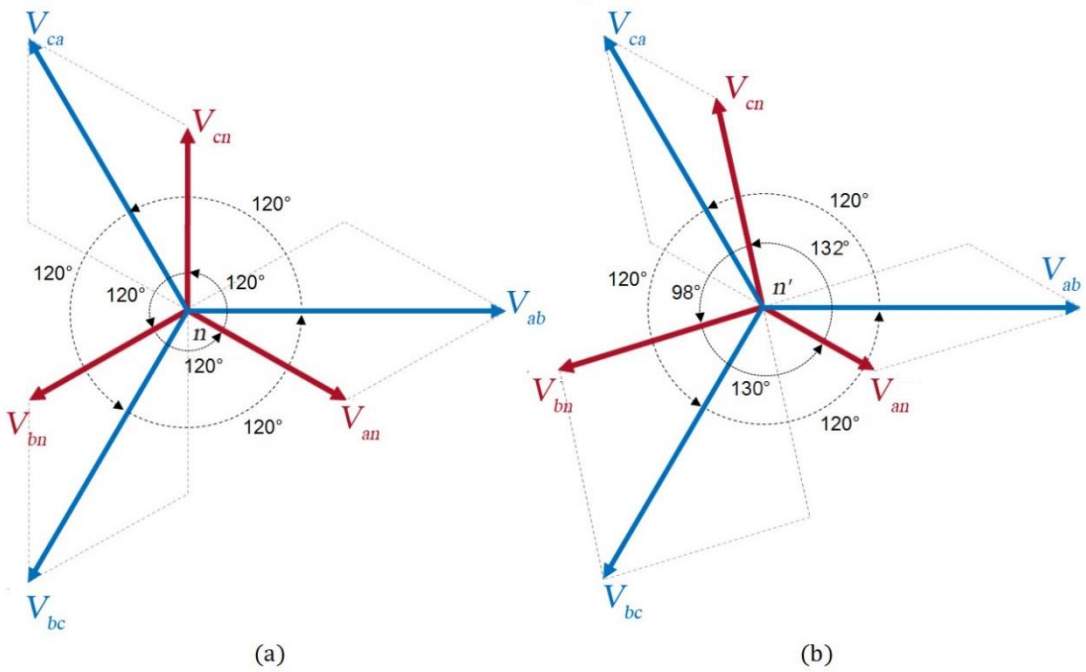


Figure (3-9): Phasor diagram for inverter voltages (a): in balance condition, (b): in unbalance condition.

Several strategies for shifting the neutral point have been presented in the literature. In [71] the rebalance in the output current for the inverter is done by shifting the neutral point through changing the angle of the phase voltages. The injection of zero-sequence into the inverter output voltage has become effective in solving the power imbalance in three-phase systems [21], [72]. The proposed scheme in this work is based on the concept presented in [21] in which the neutral point is moved by injecting a zero reference in the modulation unit. As this method has simple implementation, it has no effect on the inverter's line to line voltage even in unbalance conditions. The circuit block diagram is shown in figure (3-10) (a). while (b), (c), (d) shows the reference voltages which is get from the current loop of VOC before and after per-phase compensation.

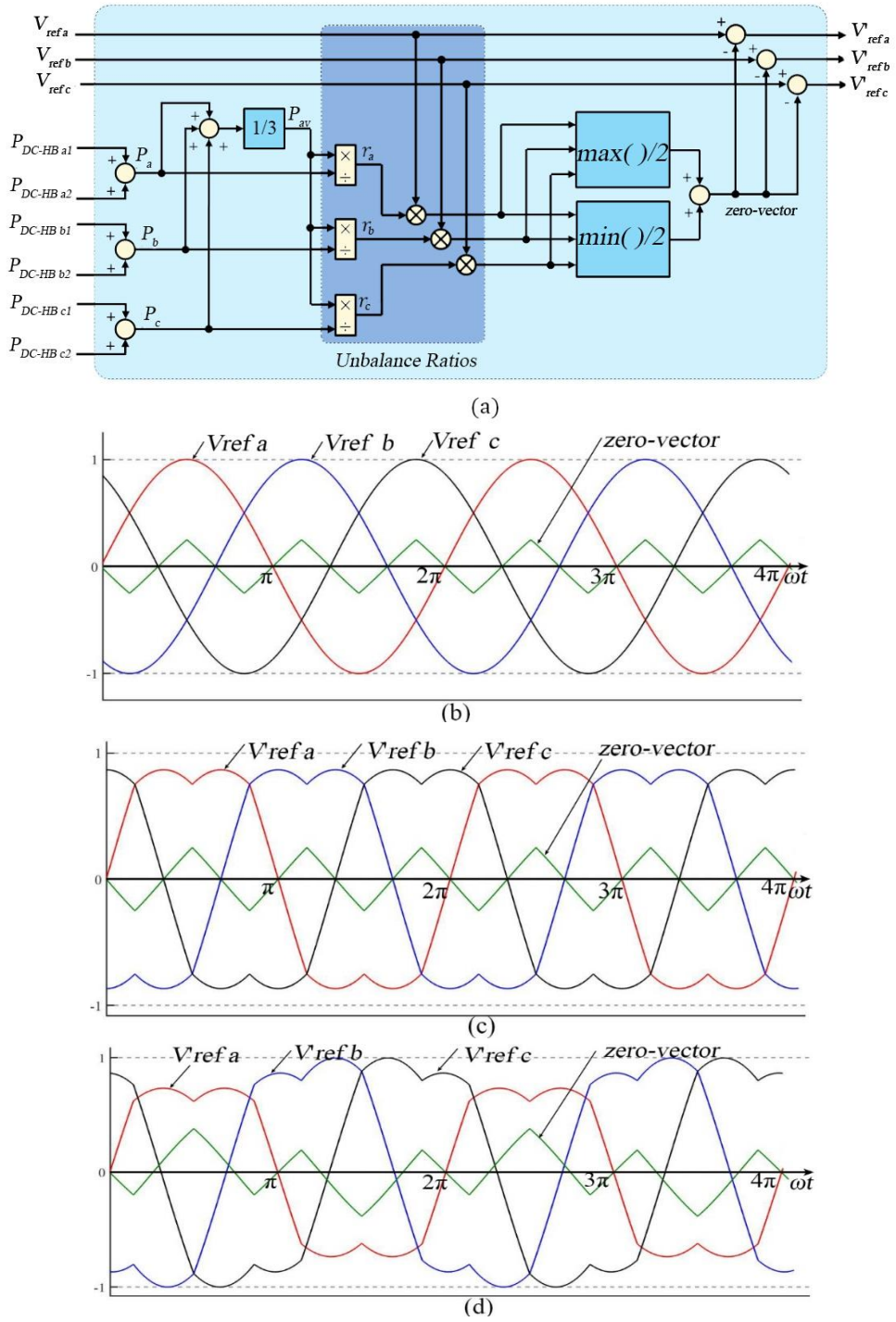


Figure (3-10): Compensation in per-phase (a): circuit layout, (b): the reference voltages before compensation process, (c): the reference voltages after compensation process in balance condition, (d): the reference voltages after compensation process in unbalance condition.

The imbalance ratio in each phase (r_a, r_b, and r_c) is calculated to execute the compensation. as:

$$r_a = \frac{P_{av}}{P_a} \tag{3-36}$$

$$r_b = \frac{P_{av}}{P_b} \tag{3-37}$$

$$r_c = \frac{P_{av}}{P_c} \tag{3-38}$$

Where P_a, P_b, and P_c is the sum of the instantaneous input power for the three phases of the inverter as given:

$$P_a = P_{DC-HB\ a1} + P_{DC-HB\ a2} \tag{3-39}$$

$$P_b = P_{DC-HB\ b1} + P_{DC-HB\ b2} \tag{3-40}$$

$$P_c = P_{DC-HB\ c1} + P_{DC-HB\ c2} \tag{3-41}$$

The average power of the three-phase can be calculated as:

$$P_{av} = \frac{P_a + P_b + P_c}{3} \tag{3-42}$$

After the factor r_a, r_b, and r_c are obtained, the zero-sequence (*zero-vector*) can be calculated from:

$$zero\_vector = \frac{\max(r_a.V_{ref\ a}, r_b.V_{ref\ b}, r_c.V_{ref\ c}) + \min(r_a.V_{ref\ a}, r_b.V_{ref\ b}, r_c.V_{ref\ c})}{2} \tag{3-43}$$

The *max* term refers to the maximum instantons values of these three inputs, and *min* refers to the minimum values of these inputs.

The final step is to obtain the modified reference voltages that given by the equations in chapter two (2-13), (2-14), (2-15).

The compensation approach which described above has the following benefits: no further current measurements or estimators are necessary to compute the received power by each PV connected to the HB unit of the inverter because all of these values have been calculated and are required for the MPPT algorithm. When an imbalance condition occurs in the generated power by the HB units, the compensation works and forces the system to operate in balance again.

2. Per-cell compensation (among individual phase)

After the per-phase compensation approach has modifed the reference signals, the total power in each phase of the inverter must be redistributed between the two HB units. In the modulation stage and when a phase-shifted PWM technique is used, the reference voltage that is received from the VOC compensated by the above stated per-phase approach is utilized by both H-bridge modulation circuits.

The shift in phase angle between the tringle carrier signals provides the multilevel stepped waveform in a CHB inverter. This type of modulation results in the same average cell usage and identical average powers in both HB units.

The per-cell block diagram is shown in figure (3-11) (a). The main concept of this compensation is to redistribute the utilization of HB units in a single-phase in accordance with the unsymmetrical power produced by each HB unit. As a result, the *ON* and *OFF* time of the modulated signal are redistributed as shown in figure (3-11) (b). Any change in the switching time for the switches will affect the received voltage and power as an increment or decrement.

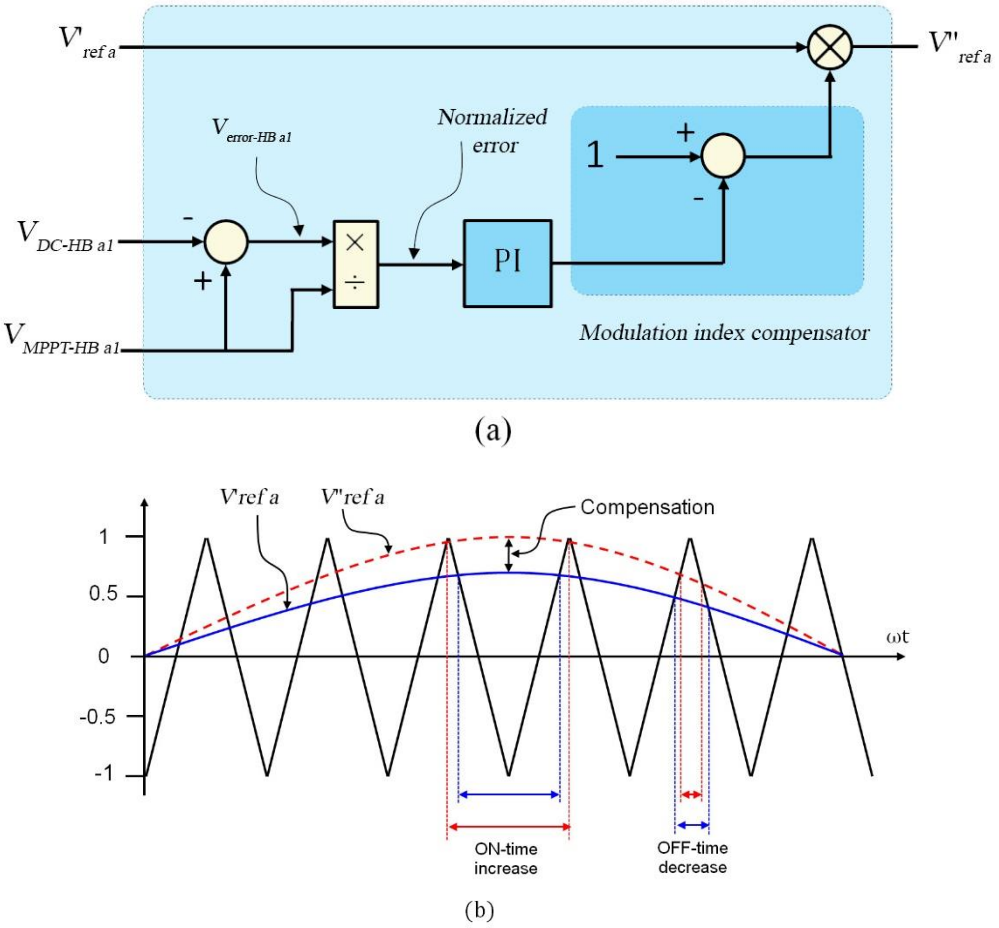


Figure (3-11): Per-cell compensatiom (a): block diagram, (b): ON and OFF effected by the compensation.

The error signal ($V_{error\text{-}HB\ ij}$) for each separated HB in each phase is the difference between the reference voltage obtained from the MPPT unit and the actual voltage measured from the PV.

$$V_{error-HB\ ij} = V_{MPPT-HB_{ij}} - V_{DC-HB_{ij}} \qquad (3\text{-}47)$$

Where *i* is the phase *a*, *b*, or *c*

And *j* represents the bridge lower=1, or upper=2.

This error then normalized and sent to *PI* controller which adjusts the amplitude of the reference signal $V''_{ref\ ij}$ before fed to the modulation stage.

The compensation modifies the amplitude of the references utilized by each HB unit according to the error of their respective DC-link voltages. Where in figure (3-11) (b), the modified signal $V''_{ref\ a1}$ is the reference voltage in HB1 of phase *a* and its effects on ON and OFF time. The ON and OFF time depend on the modulation indexes. As the modulation index increase, the ON time increased and the OFF time decreased, as a result, the desired redistribution of the cells is obtained.

CHAPTER FOUR

SIMULATION RESULTS

4.1 Introduction

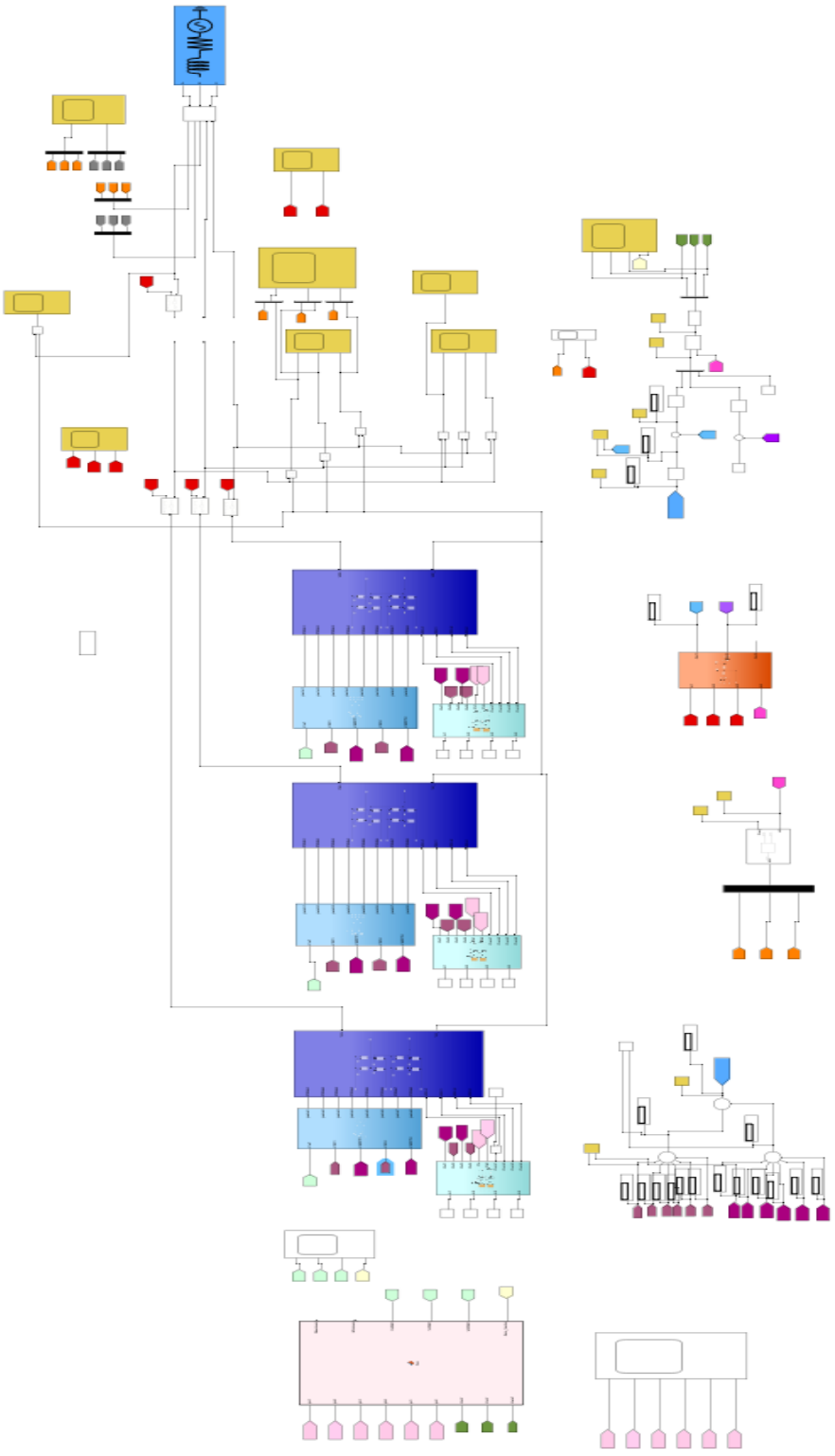
This chapter presents the simulation results to confirm the performance of the control system and feedforwards compensation circuits for the grid connection PV system. It also includes two main sections: the first section is to devote a full description of the system setup in MATLAB, and the second portion is to dedicate the system components performance and system behavior in different operating conditions.

4.2 System setup

The system configuration for grid connection photovoltaic arrays is shown in figure (4-1), the three-phase five-level inverter is implemented by using six units of H-bridge module, each two of them are connected in series to build a phase of the inverter, the H-bridge module consists of four IGBT/Diode switches, their parameters are listed in the table (4-1). A DC-link capacitor of (16 mF) is connected to each HB and all of them are connected to individual PV arrays whose parameters are listed in the table (4-2), the power characteristic curve at a minimum and rated sun irradiance is shown in figure (4-2).

Table (4-1): IGBT parameters.

Parameter	Value
internal resistance R_{on}	1e-3 ohm
Snubber resistance R_s	1e5 ohm
Snubber capacitance C_s	Inf



(a)

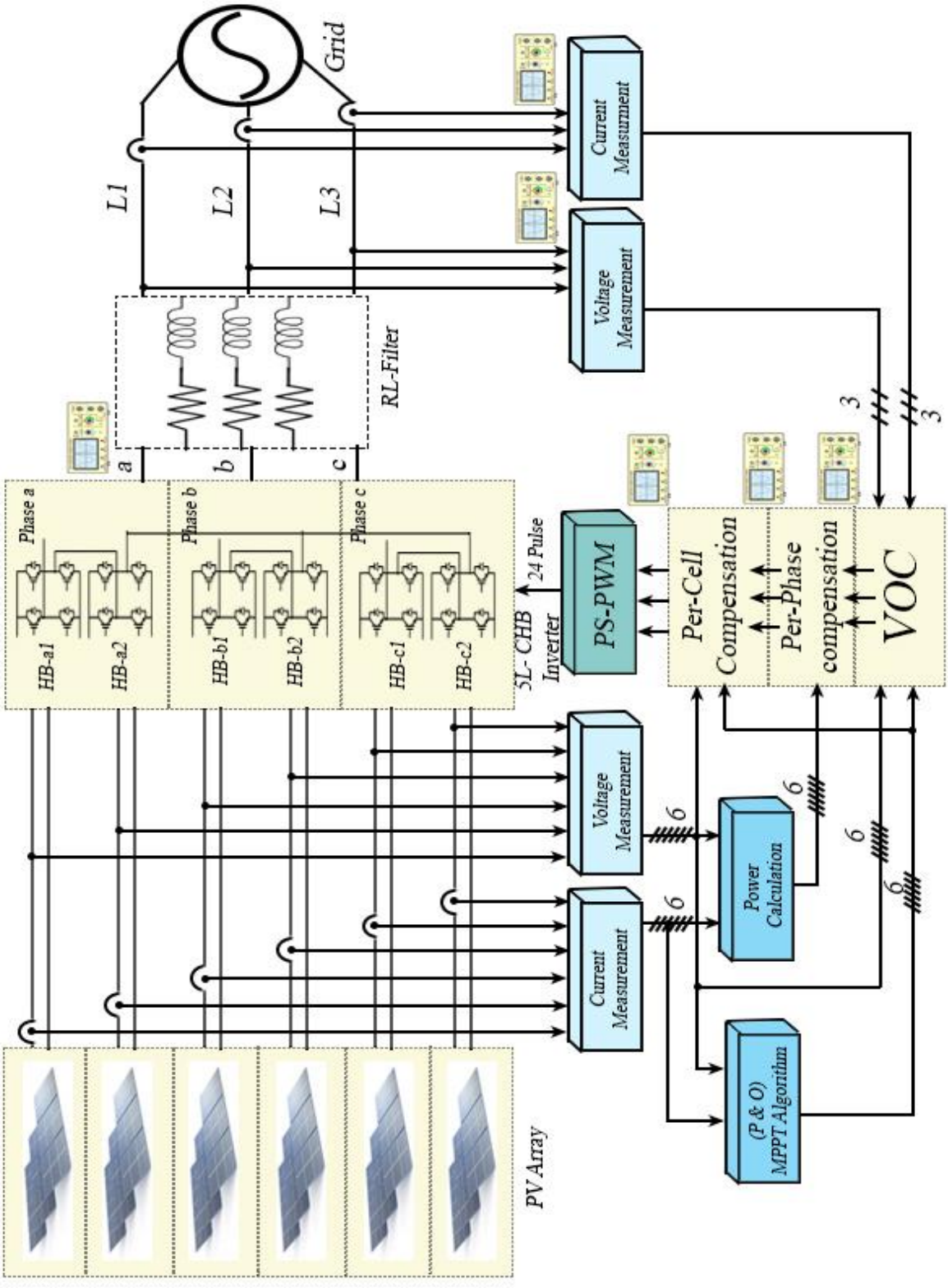


Figure (4-1): Grid connection PV system (a) MATLAB configuration (b) block diagram.

Table (4-2): 1Soltech 1STH-215-P (8 series modules, 16 parallel strings).	
Parameter	Value
$V_{O.C}$	290.4 V
$I_{S.C}$	125.4 A
V_{MPP}	232 V
I_{MPP}	117.6 A
Rated power	27.28 kW

Then the installed CHB inverter is connected to the (380 V RMS, 50 Hz) grid through RL-filter has a resistance (5 mΩ) and inductance (0.3 mH).

The system is controlled by VOC through three-phase PLL, Park and Clark transformers, invers Park and invers Clark transformers, PI controllers, MPPT algorithm, feedforward compensation circuits and finally phase shift pulse width modulation with switching frequency (f_s = 5 kHz).

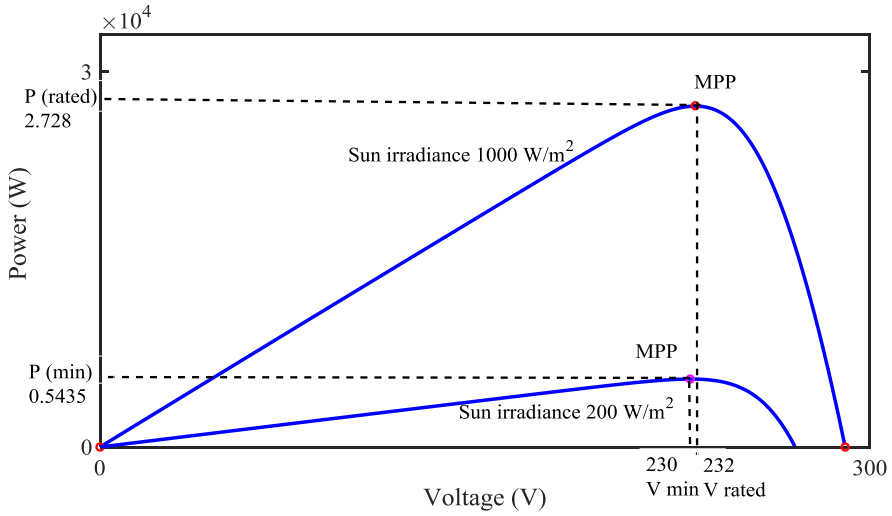
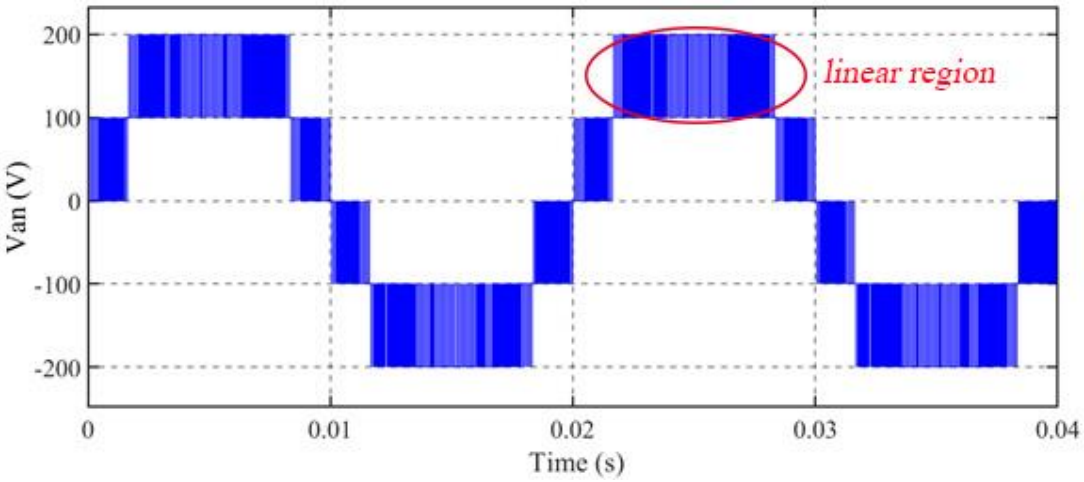


Figure (4-2): PV power vs. its voltage.

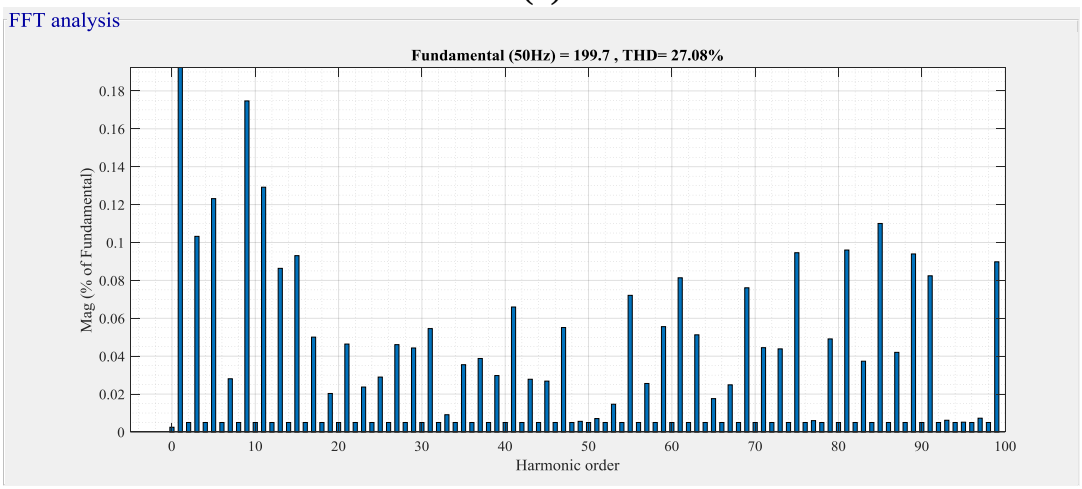
4.3 Simulation results for (PS-PWM)

The PS-PWM technique is validated by simulations in an open loop system with resistive load only. By applying six isolated DC sources (V_{DC}) for each H-bridge unit of the CHB and are set to be (100 V).

The results are obtained at modulation index m_a = 1, and switching frequency *fs* = 5 kHz, figure (4-3) shows the inverter phase *a* voltage before the injection of the zero-sequence signal and its FFT analysis. Figure (4-4) shows the inverter phase *a* voltage after the injection of the zero-sequence signal and its FFT analysis. it is clear from the both figures that each level of the 5L-CHB has a value of (V_{DC} = 100 V). And the linear region of the signal increased as in figure (4-4) part (a) and the fundamental component also increased as shown in part (b) of the figure (4-4) by adding the zero-sequence signal.

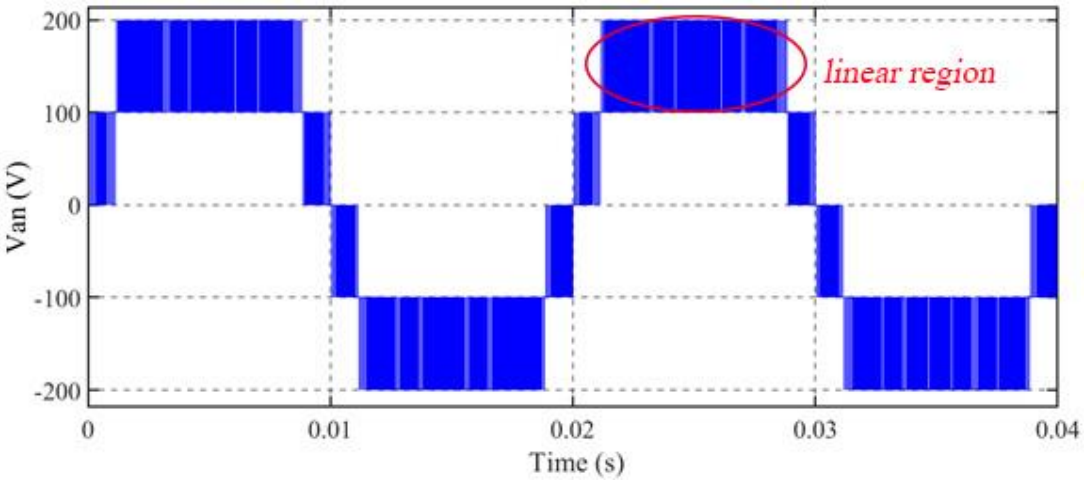


(a)

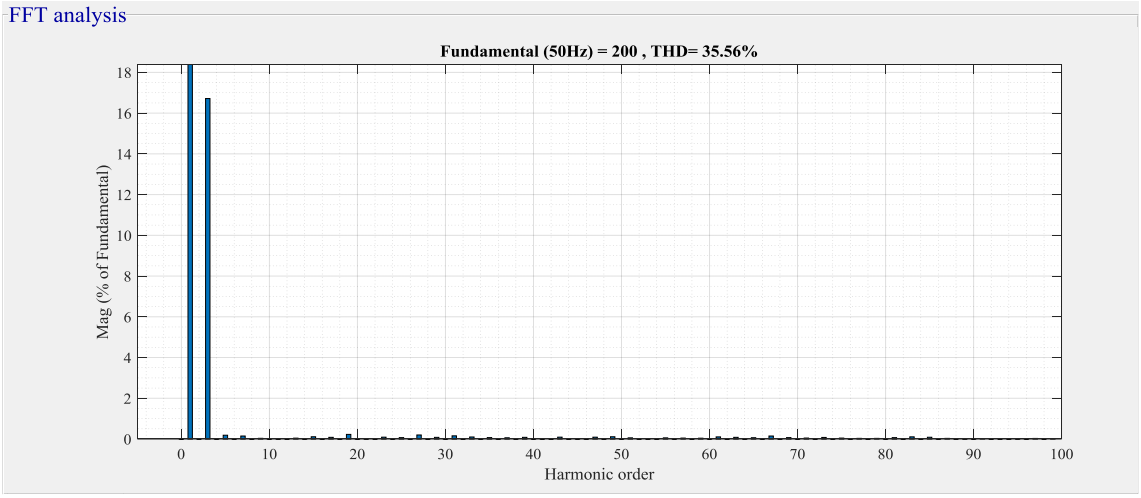


(b)

Figure (4-3): Inverter phase *a* voltage (a): before zero-sequence injection, (b): FFT analysis.



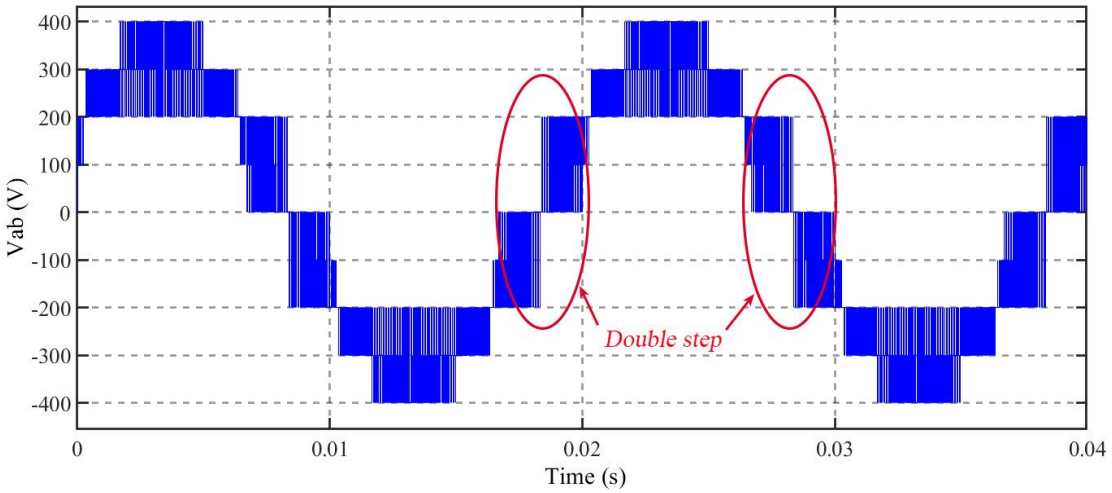
(a)



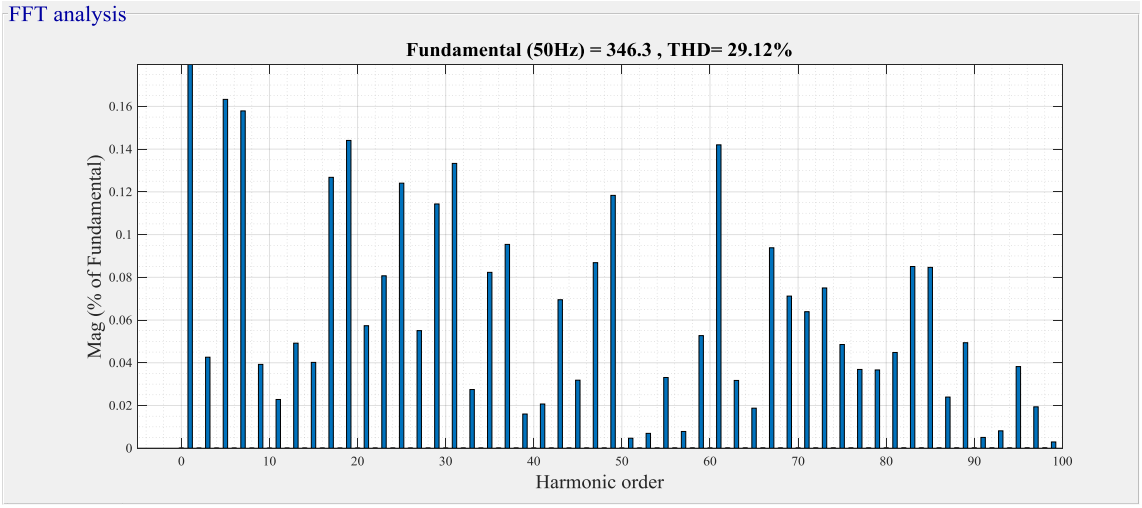
(b)

Figure (4-4): Inverter phase *a* voltage (a): after zero-sequence injection, (b): FFT analysis.

The line to line voltage of the inverter between phase *a* and phase *b* and its FFT analysis before the injection of the zero-sequence signal is shown in figure (4-5), and after the injection is shown in figure (4-6). It is clear that the double step in the line to line voltage is reduced after the injection of the zero-sequence.



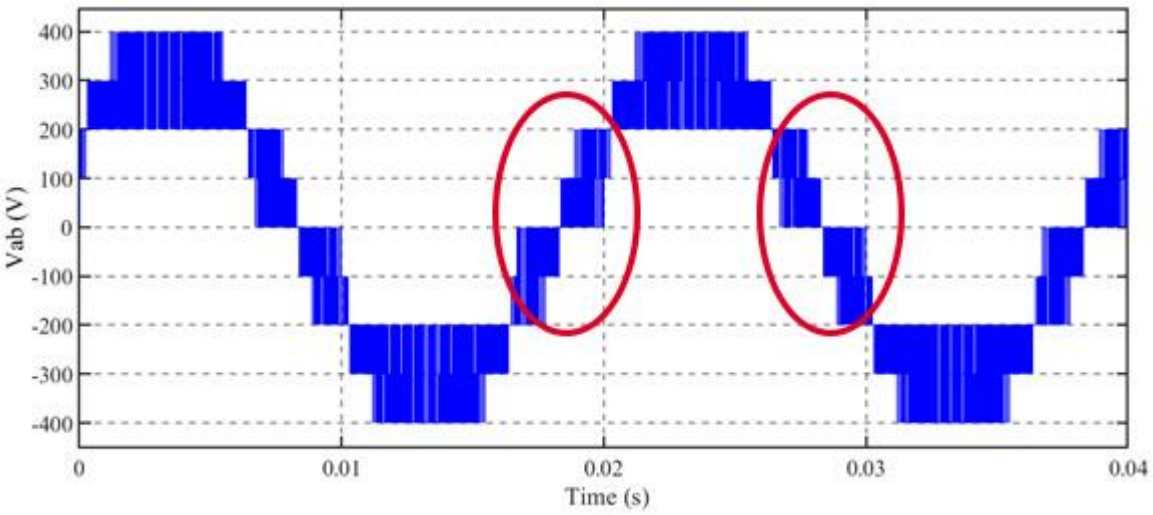
(a)



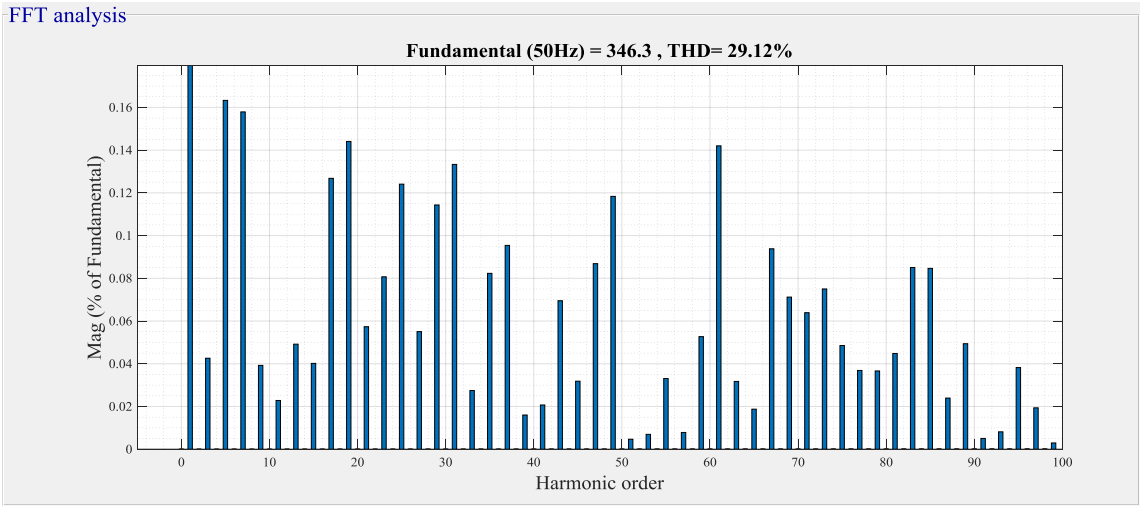
(b)

Figure (4-5): Inverter line to line voltage

(a): before zero-sequence injection, (b): FFT analysis.



(a)



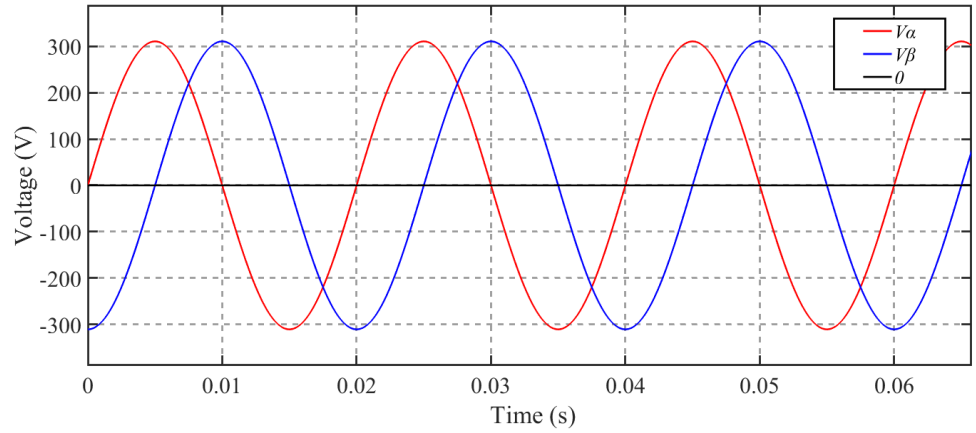
(b)

Figure (4-6): Inverter line to line voltage

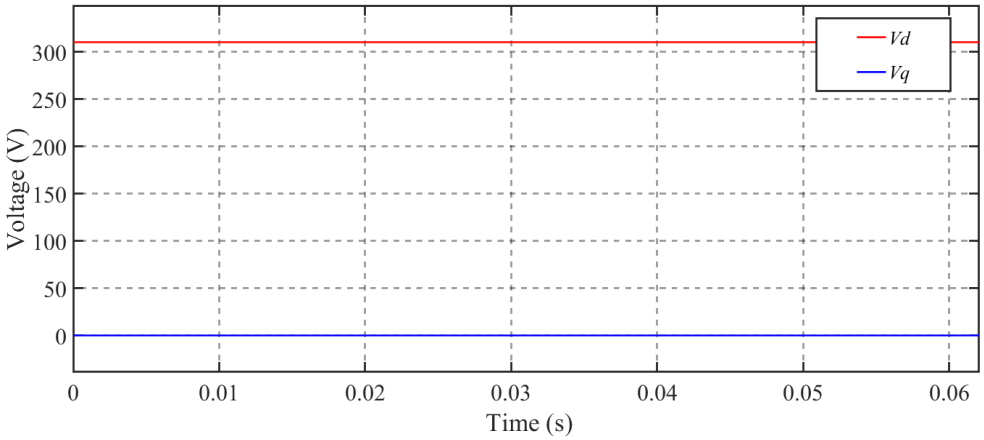
(a): after zero-sequence injection, (b): FFT analysis.

4.4 Phase Lock Loop (PLL) performance

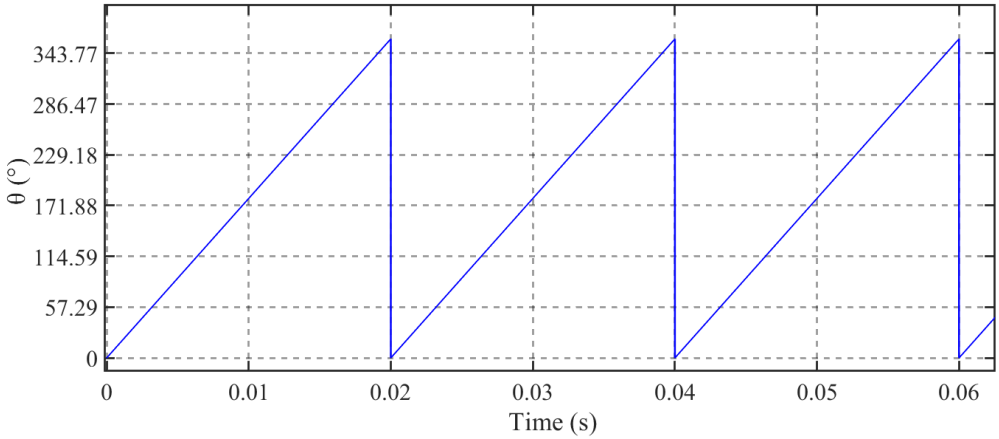
The performance of PLL is illustrated in figure (4-7), it illustrates the grid voltage V_α and V_β in α-β frame and the grid voltage V_d and V_q in d-q frame. It is observing that the value of V_q is kept at (zero) which is proportional to the phase difference between the *abc* signal and the internal oscillator rotating frame, the PLL calculate the grid voltage angle θ as shown in (c).



(a)



(b)



(c)

Figure (4-7): PLL performance: (a) grid voltage in α-β frame, (b) grid voltage in d-q frame, (c) grid voltage angle θ.

4.5 Current loop performance

Figure (4-8) shows the transient response of the current difference (error) between reference current I^*_d which is obtained from voltage loop and the actual current value I_d which is obtained from the current measurement of the inverter after its transformation from (*abc* form) to (*d-q*). It is clear that the error between them became (zero) at time (0.1 s).

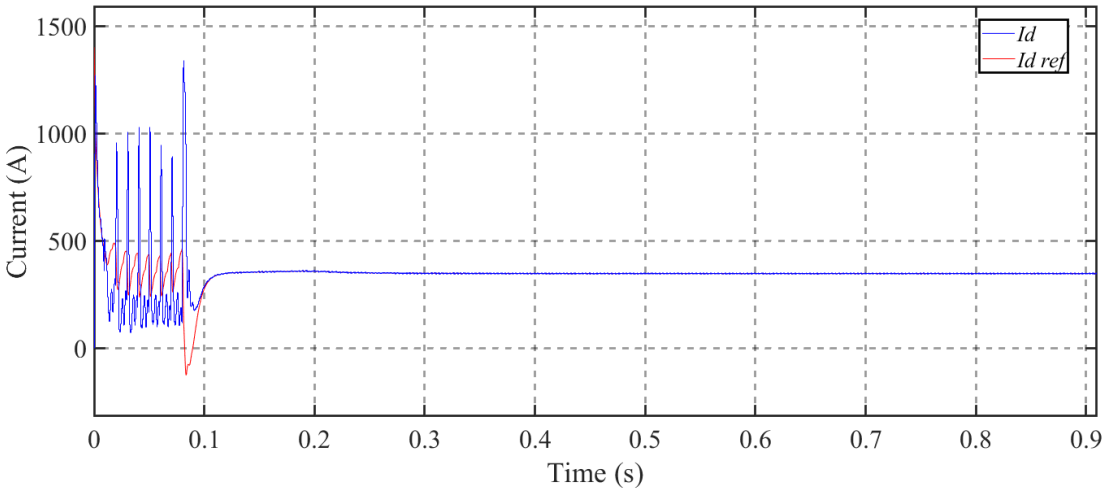


Figure (4-8): Current error (I^*_d - I_d).

4.6 Voltage loop performance

The voltage loop controls the error signal (e_t) results from the comparator between the summation of DC voltages of PV arrays and the summation of MPP voltages from MPPT algorithm units. Figure (4-9) shows that the error between them, this error is (zero) at time (3.54 s).

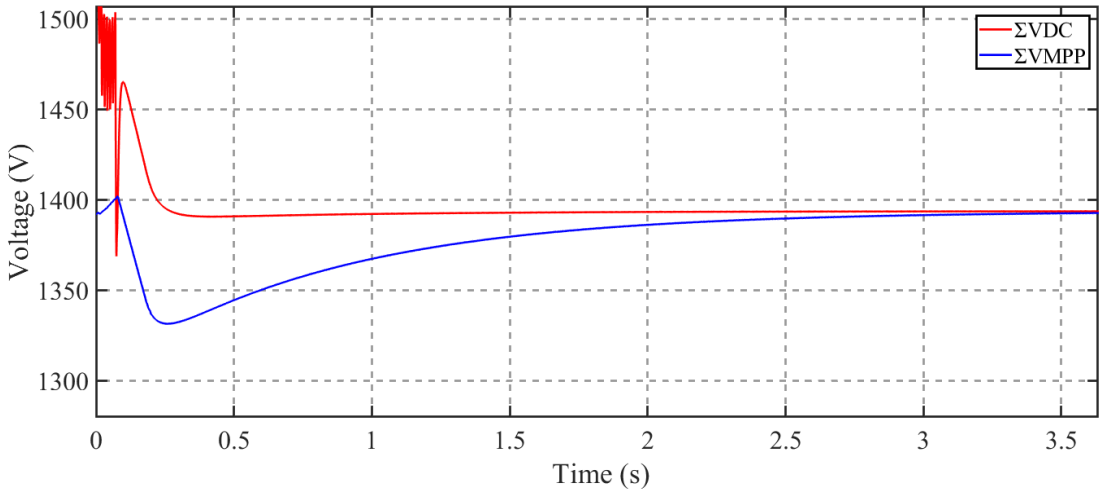


Figure (4-9): Voltage error (ΣV_{DC}- ΣV^{*}_{DC}).

4.7 Per-phase and per-cell compensation performance

The efficiency of per-phase and per-cell compensation, which was previously discussed in chapter three is tested in simulation work. The compensation is not active if all HB unit of the inverter work with same DC-link voltage and it will give the same output power. As a result, the reference voltages are not adjusted and are supplied directly to the modulator. However, only the per-cell compensation supposed to apply to the reference voltages if all HB units of the inverter work with DC-link voltages, but its' upper cells *HB-a1*, *HB-b1*, and *HB-c1* that produce a power different from the power produced by the lower cells *HB-a2*, *HB-b2*, and *HB-c2*. Thus, a balanced power is injected into the grid.

If the power produced by each cell of a single-phase is asymmetrical, this means that unbalanced power is injected to the grid. Therefore, in this case, both compensation circuits will operate to rebalance the injected power to the grid by redistributing power between the two cells in the same phase.

The temperature of the PV arrays in this simulation is set to be constant at (25°C) and the rated DC voltage that generated form the PV at MPP is (232 V) while the rated power obtained from each PV arrays is (27.28 kW) at sun irradiation (1000 W/m ^{2}). The grid line to line voltage V_{L1L2} is (380 V RMS), so that the minimum acceptable DC voltage for each phase that transfer power to the grid must be (311 V) according to the equations (3-20) and (3-21). The system is designed to produce total power injected to the grid about (163 kW).

The behavior of grid connection PV system is tested by simulation that based on these setups through seven cases of operation condition which were discussed in table (3-1) in chapter three.

Case 1: operating with all PV arrays work at rated power

In this operating case, the PV arrays is worked at rated sun irradiance and produces rated power. Which can be consider as operating at balance where all PV arrays for each inverter HB unit work at rated sun irradiance (1000 W/m^2), the produced power will be at maximum power point.

Case 2: operating with single HB unit unbalance

One of the upper PV arrays of any phase works at minimum sun irradiance (200 W/m^2) as the partial shading effects on it, thus the generated power by this PV is reduced to almost (20%) of its rated value. While the other two phases work at the rated power.

Case 3: operating with double HB unbalance units

In this case two upper PV arrays work at minimum sun irradiance. Therefore, the power produced by both PV arrays is reduced to almost (20%) of their rated value, while a single-phase remained working at its rated power.

Case 4: operating in single phase unbalance

Operating with one phase that the power of the PV arrays that connected to its HB units reduced in different ratio from its rated value, it means that the upper PV working at power is about (70%) of the rated power, and the lower PV produces power is about (20%) of the rated power. While the other two phases keep working at rated power.

Case 5: minimum power of the upper three PV arrays and rated power of the lower three PV arrays

In this operating case, all the three PV arrays are connected to the upper HB units (*HB-a1*, *HB-b1*, and *HB-c1*) are operated at minimum power operation (20%) of their rated power that is produced by the effect of reduced sun irradiance to (200 W/m^2), while the three PV arrays are connected to the lower HB units (*HB-a2*, *HB-b2*, and *HB-c2*) worked at rated power produced at the maximum power point.

Case 6: minimum power of all PV arrays

In this case of operation, all PV arrays are connected to the six HB units of the inverter worked at its' minimum power which is at (20%) of the rated power.

Case 7: no power in one of the upper PV arrays and rated power for the rest of PV arrays

In this case of operation, one of the three PV arrays is connected to the upper HB units let's (*HB-a1*) generates no power as technical problems, while the three PV arrays are connected to the lower HB units (*HB-a2*, *HB-b2*, and

HB-c2) and the other two upper (*HB-b1*, and *HB-c1*) operating at a rated power produced at the maximum power point.

Case 8: no power in one of the upper PV arrays and minimum power for the rest of PV arrays

This case similar to case 7 except that the power generated from the active PV arrays is at minimum value.

Case 7 and case 8 were infrequent, but these effect on system efficiency and effectiveness, which should be considered in simulation work.

Case 9: no power produced in all PV

In this case, all PV arrays connected to the six HB unit of inverter produced no power at night or cloudy weather.

Table (4-3) shows the current and the voltage produced by each HB unit of the inverter and its power generation under different operation cases. As well as the inverter current injected into the grid and the total generated power for the system in each case.

Table (4-3): Operating cases of the PV system grid connection.

Parameter	Unit	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6	Case 7	Case 8
$V_{HB\text{-}a1}$	V	232	230	230	231.8	230	230	0	0
$V_{HB\text{-}b1}$	V	232	232	230	232	230	230	232	230
$V_{HB\text{-}c1}$	V	232	232	232	232	230	230	232	230
$V_{HB\text{-}a2}$	V	232	232	232	230	232	230	232	230
$V_{HB\text{-}b2}$	V	232	232	232	232	232	230	232	230
$V_{HB\text{-}c2}$	V	232	232	232	232	232	230	232	230
$I_{HB\text{-}a1}$	A	117.6	23.5	23.5	82.5	23.5	23.5	0	0
$I_{HB\text{-}b1}$	A	117.6	117.6	23.5	117.6	23.5	23.5	117.6	23.5
$I_{HB\text{-}c1}$	A	117.6	117.6	117.6	117.6	23.5	23.5	117.6	23.5
$I_{HB\text{-}a2}$	A	117.6	117.6	117.6	23.5	117.6	23.5	117.6	23.5
$I_{HB\text{-}b2}$	A	117.6	117.6	117.6	117.6	117.6	23.5	117.6	23.5
$I_{HB\text{-}c2}$	A	117.6	117.6	117.6	117.6	117.6	23.5	117.6	23.5
$P_{HB\text{-}a1}$	kW	27.28	5.435	5.435	19.28	5.435	5.435	0	0
$P_{HB\text{-}b1}$	kW	27.28	27.28	5.435	27.28	5.435	5.435	27.28	5.435
$P_{HB\text{-}c1}$	kW	27.28	27.28	27.28	27.28	5.435	5.435	27.28	5.435

Parameter	Unit	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6	Case 7	Case 8
$P_{HB\text{-}a2}$	kW	27.28	27.28	27.28	5.435	27.28	5.435	27.28	5.435
$P_{HB\text{-}b2}$	kW	27.28	27.28	27.28	27.28	27.28	5.435	27.28	5.435
$P_{HB\text{-}c2}$	kW	27.28	27.28	27.28	27.28	27.28	5.435	27.28	5.435
Total power generated P_{Total}	kW	163.68	141.835	119.99	133.835	98.145	32.61	136.4	27.175
Total injected power P_{Inj}	kW	161.91	139.62	116.35	132.162	97.734	31.647	136	26.98
Inverter line current I_a	A	246	212.132	176.77	200.8	148.49	48	207	41
Power reduction		0%	13.34%	26.69%	18.23%	40%	80%	16.66%	83.39%

4.7.1 Simulation results for case 1 (in balance operation)

The results of balance operating case 1 will be the reference for other modes and cases as the simulation results focused on compensation technique. Figure (4-10) shows the reference voltages $V_{ref\,a}$, $V_{ref\,b}$, and $V_{ref\,c}$ which are obtained from current loop of VOC and will be sent to the compensation stage. Figure (4-11) shows these reference voltages after compensation $V'_{ref\,a}$, $V'_{ref\,b}$, and $V'_{ref\,c}$. It is obvious that the max-min of the zero-sequence still straight and kept unchanged because the per-phase compensation circuit is not working due to the balance in the three phases.

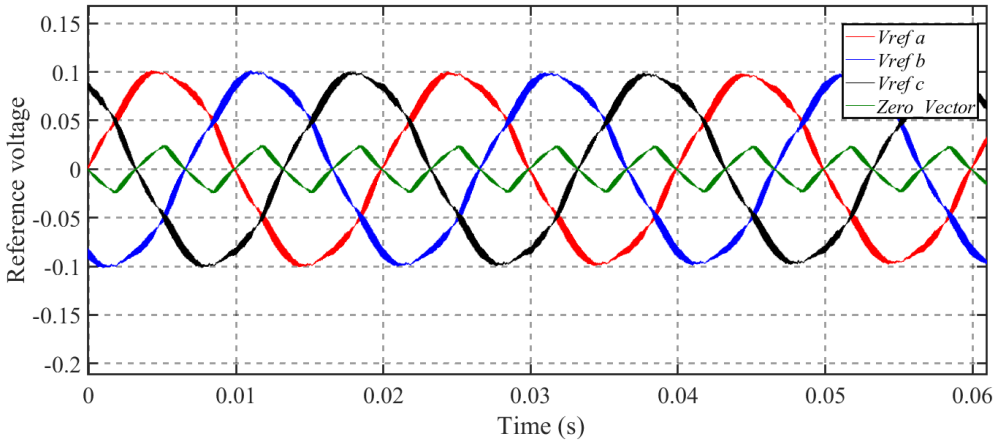


Figure (4-10): Reference voltages for case 1 before per-phase compensation.

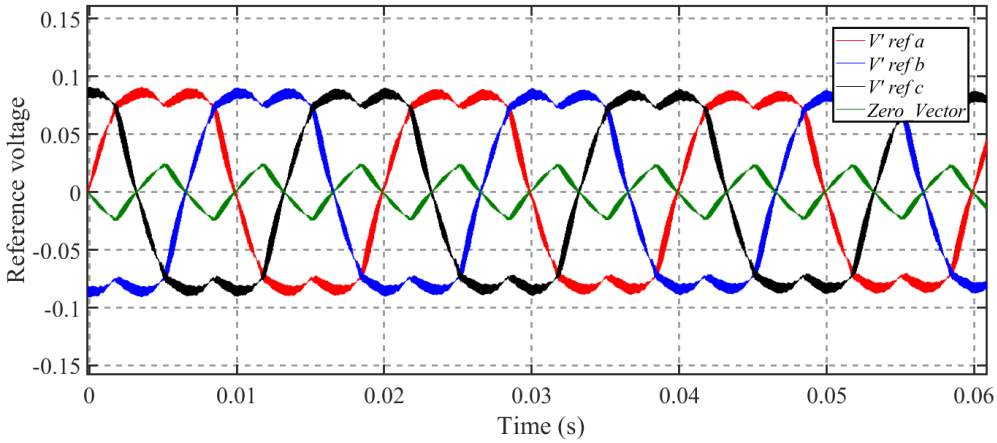


Figure (4-11): Reference voltages for case 1 after per-phase compensation.

Figure (4-12) explains the reference voltage of phase *a* which is in red color before the per-cell compensation $V'_{ref\,a}$, and there are two signals $V''_{ref\,a1}$, $V''_{ref\,a2}$ which refer to the reference voltage of HB1 and HB2 of phase *a*. These signals are matched and compensate in the same manner since PV arrays have the same DC-link voltage (232 V) and generate an equal power (27.28 kW). The compensation process has increased the modulation index from (0.1) to (0.6) according to the voltage generated from each HB unit.

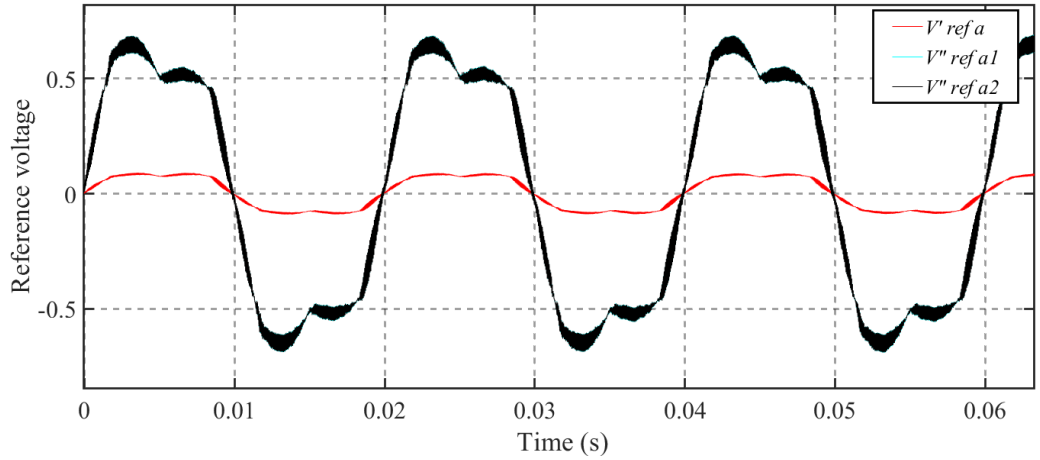


Figure (4-12): Phase *a* reference voltage for case 1 before and after per-cell compensation.

The inverter rated line current is shown in figure (4-13), which will be injected to the grid. i_a, i_b, and i_c are balanced and have a value of (246 A) RMS. The inverter phase voltages V_a, V_b, and V_c with the grid voltage V_{L1N}, V_{L2N}, and V_{L3N} are shown in figure (4-14) (a) and their Fast Fourier Transform (FFT) analysis is shown if part (b). It is clear from these figures that the inverter voltage is synchronized with the grid voltage in frequency and in phase angle and the fundamental value is (313.8 V) which is allowable value to transfer power to the grid. Figure (4-15) (a) illustrates line to line voltage of the inverter V_{ab}, V_{bc}, and V_{ca} and in part (b) the Fast Fourier Transform analysis for V_{ab} and it is the same for V_{bc} and V_{ca}.

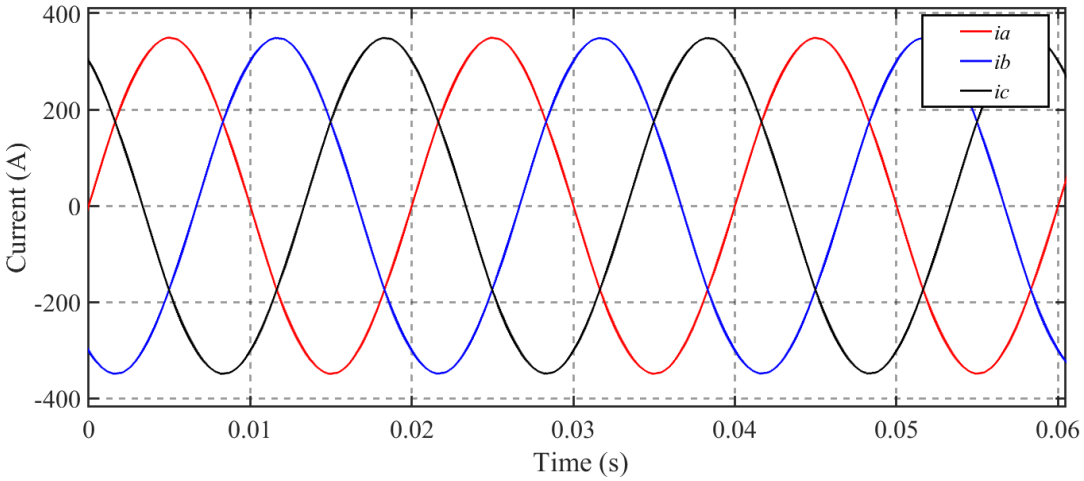
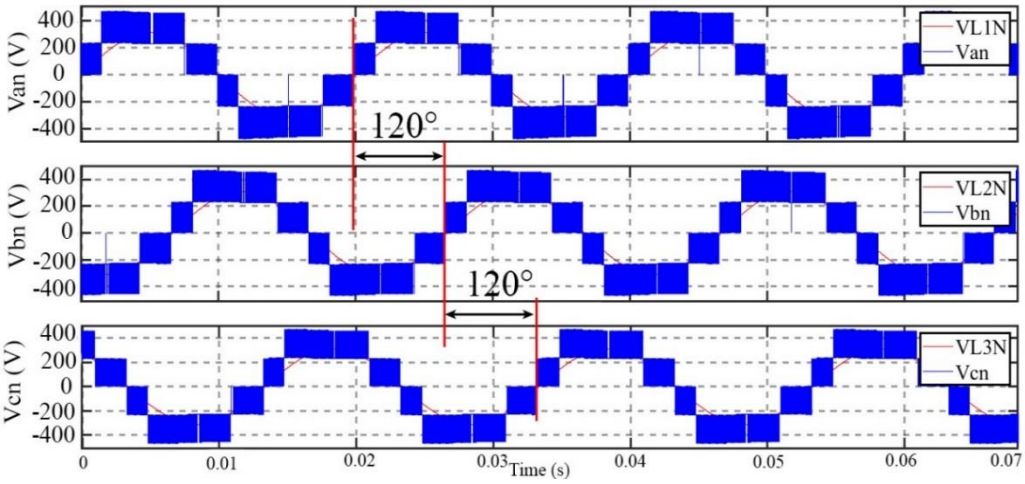
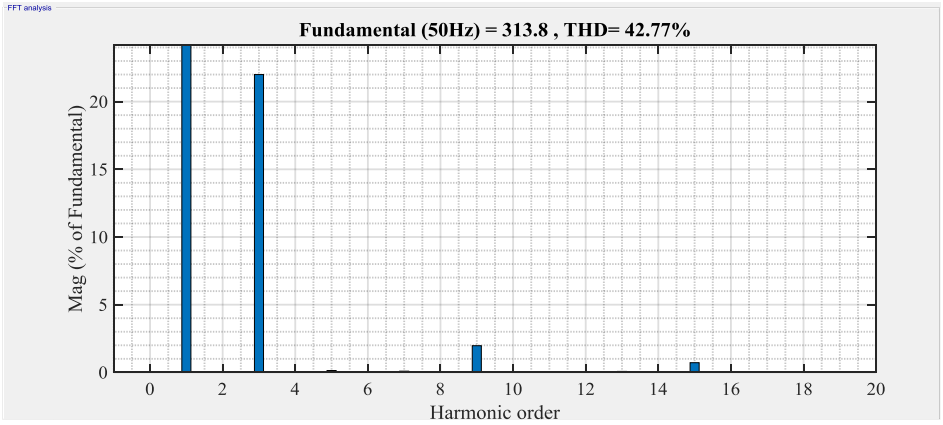


Figure (4-13): Grid injected current for case 1.

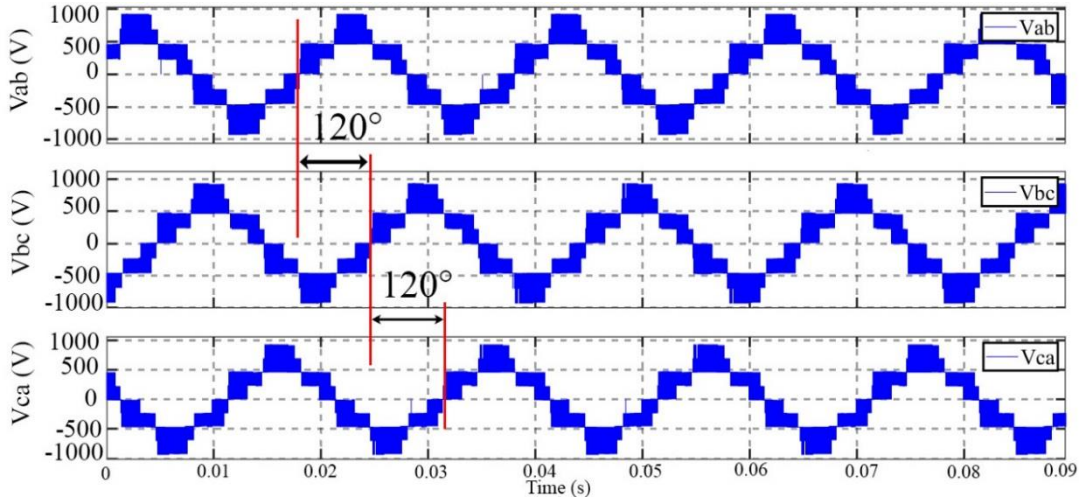


(a)

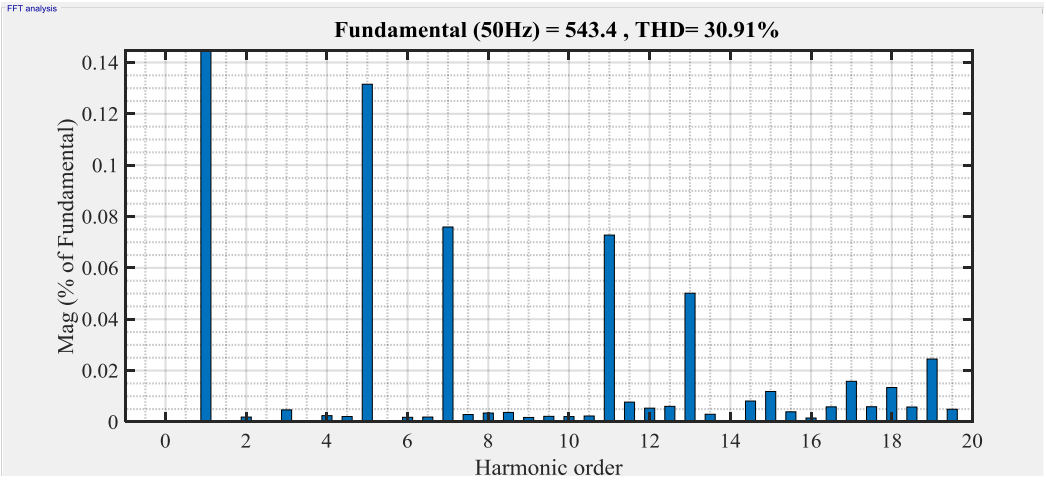


(b)

Figure (4-14): (a) Output phase voltages of the inverter with the corresponding grid phase voltages in case 1 (b) FFT analysis for phase *a*.



(a)



(b)

Figure (4-15): (a) Line to line voltages of the inverter for case 1 (b) FFT analysis for V_{ab}.

Figure (4-16) shows the inverter currents i_a, i_b, and i_c that are injected to the grid with unity power factor which is in red color while the signal in blue color represents the corresponding grid phase voltages. It is clear that the inverter current is synchronized in frequency and phase angle with the grid phase voltage V_{L1N}, V_{L2N}, and V_{L3N}.

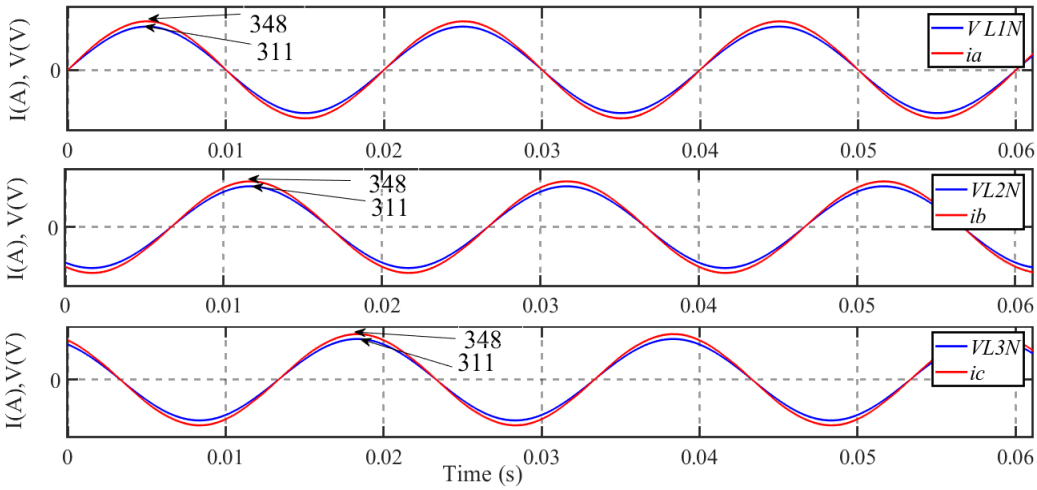


Figure (4-16): Inverter current with grid voltage for case 1.

4.7.2 Simulation results for case 2 (in single HB unit unbalance operation)

Unbalanced condition occurs in case 2 of operation according to table (4-3) due to a drop in the power produced by HB unit *a1* from (27.28 kW) to (5.435 kW). As shown in figure (4-17) the reference voltages $V_{ref\,a}$, $V_{ref\,b}$, and $V_{ref\,c}$ before per-phase compensation almost have an amplitude of (0.1). Figure (4-18) shows the reference voltages $V'_{ref\,a}$, $V'_{ref\,b}$, and $V'_{ref\,c}$ after compensation process, where the variance between the power processed by the phases (P_a, P_b, and P_c) and the average power P_{av} is compensated by changing the max-min of the zero-sequence. The reference voltages of phase *b* and *c* is adjusted to redistribute power as phase *a* produces less power and the zero-sequence *zero-vector* is in phase with its reference voltage.

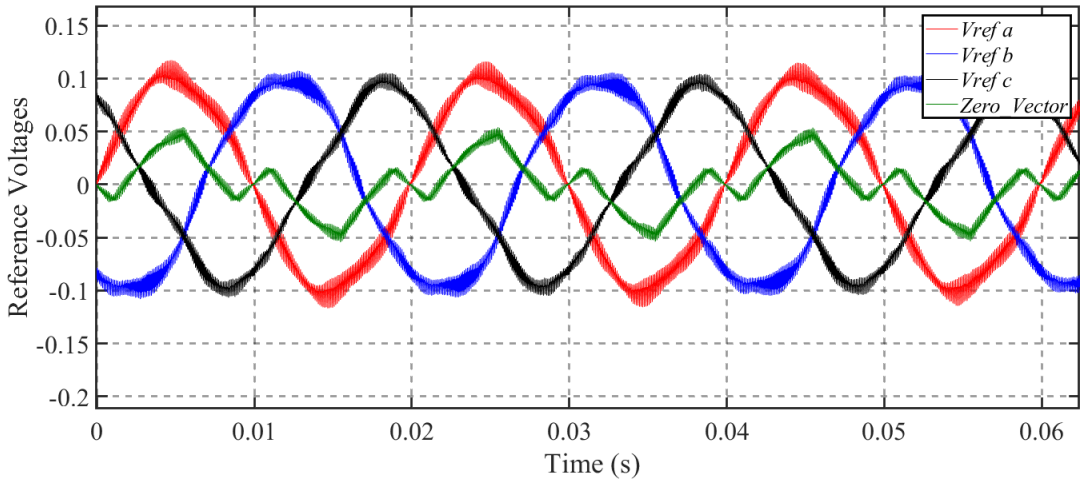


Figure (4-17): Reference voltages for case 2 before per-phase compensation.

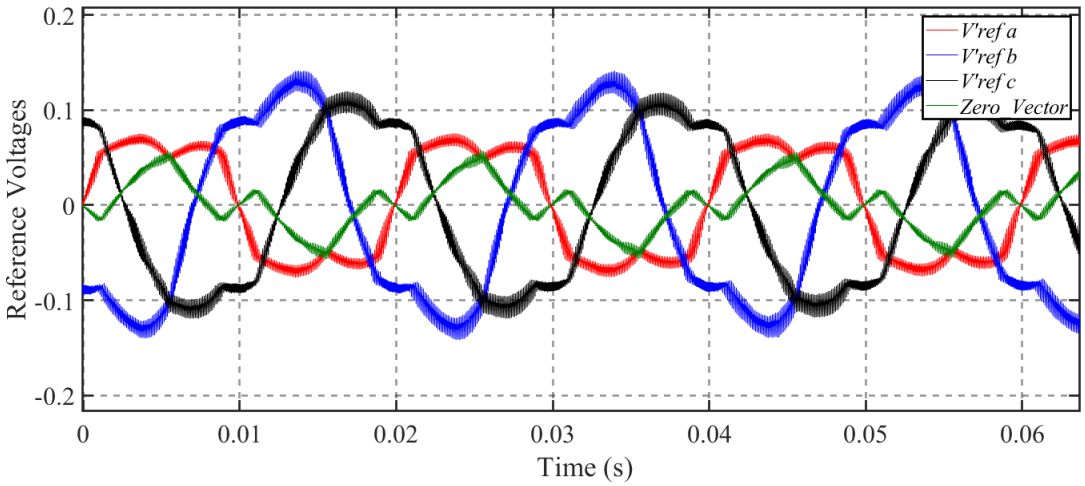
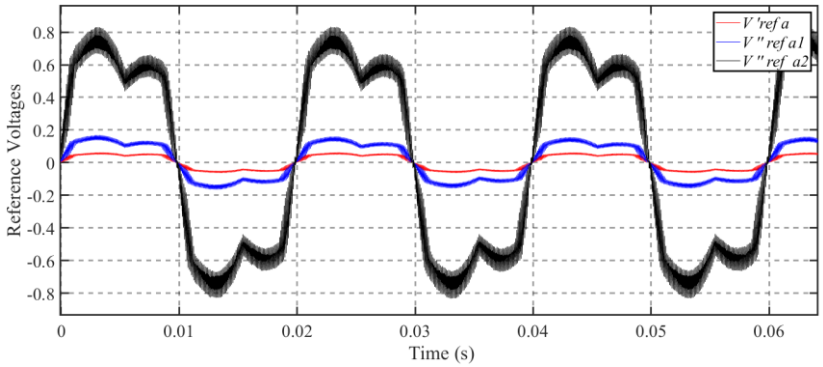


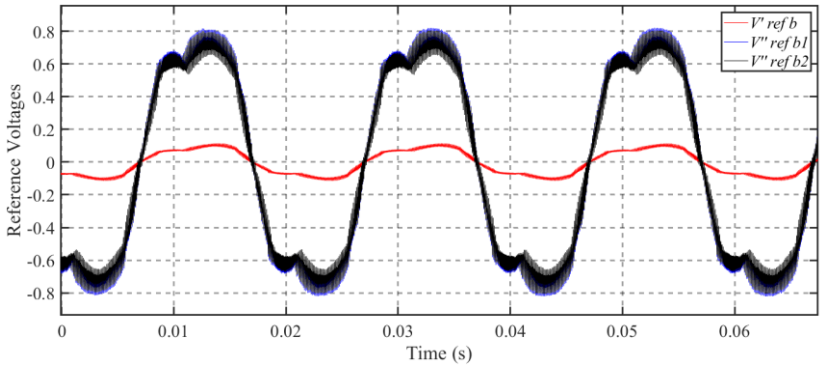
Figure (4-18): Reference voltages for case 2 after per-phase compensation.

After redistribution of the power between the three phases, the modification that occurs in the amplitude of the reference voltages for each cell as shown in figure (4-19) in order to reallocate the ON/OFF times of the cell in accordance with the generated power, ensuring that the PV array of HB-*a1* still operates at maximum power. The reference for cell HB-*a1* has reduced to roughly (0.14) since its radiation has reduced to (20%) of its rated value, while the reference voltage of HB-*a2* rise to approximately (0.8) to compensate for the shortfall in power in HB-*a1* as illustrated in

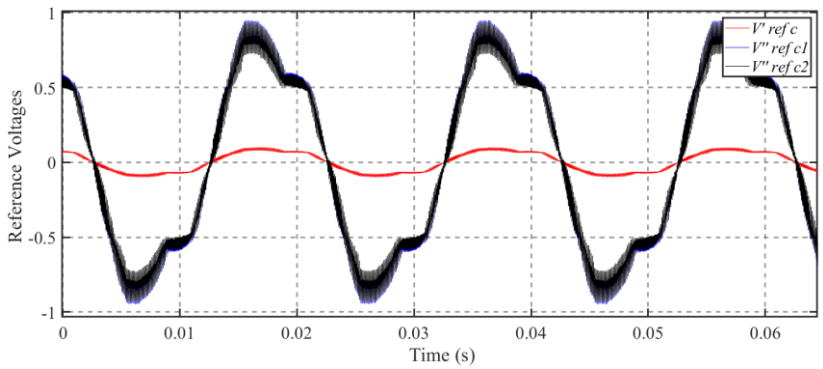
figure (4-19) (a). Figure (4-19) (b and c) illustrate the reference voltages for phase *b* and *c* before and after per-cell compensation respectively. where the amplitude of these reference voltages of each HB units has changed while the ratio between the reference voltages of upper units and the lower ($V''_{ref\ b1}$, $V''_{ref\ b2}$), ($V''_{ref\ c1}$, $V''_{ref\ c2}$) maintained constant to compensate for the reduction in phase *a*'s total power, which results in the rebalancing of the power injected to the grid.



(a)



(b)



(c)

Figure (4-19): Reference voltages of the three phases before and after per-cell compensation case 2 (a): phase *a*, (b): phase *b*, (c): phase *c*.

The inverter line currents are shown in figure (4-20). The current value in this unbalance operation is reduced to (212.132 A) RMS but it is remained balanced among the three phases.

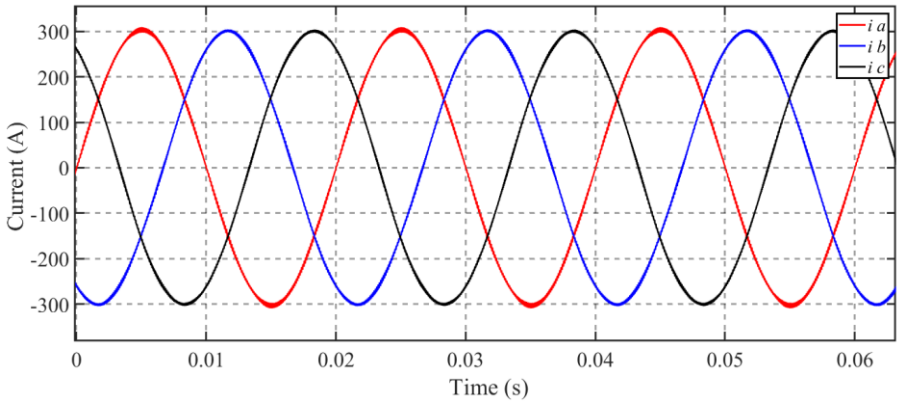
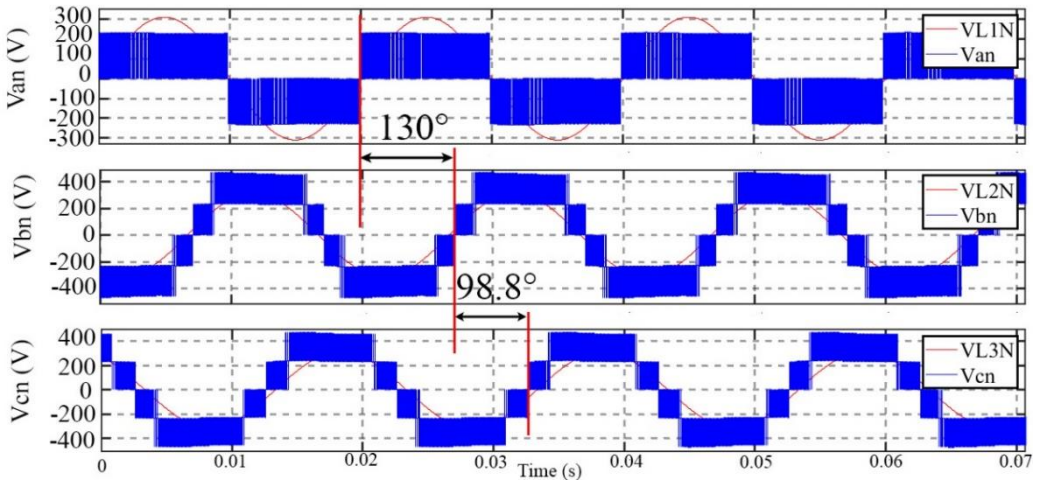
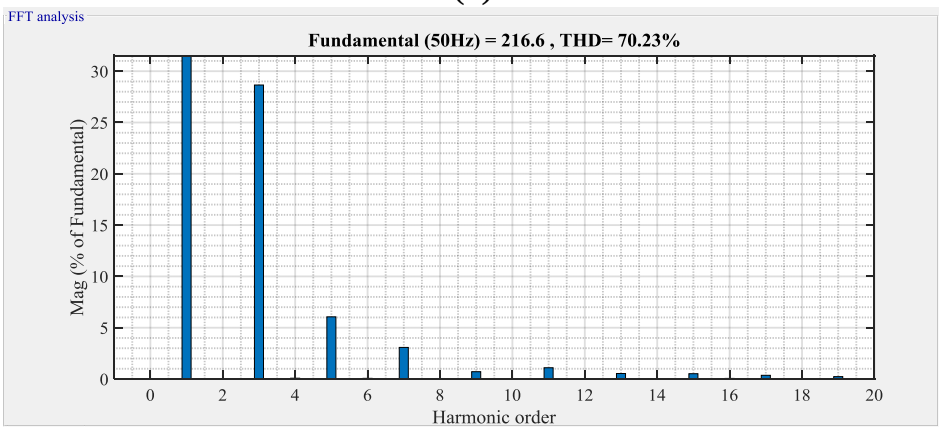


Figure (4-20): Grid injected current for case 2.

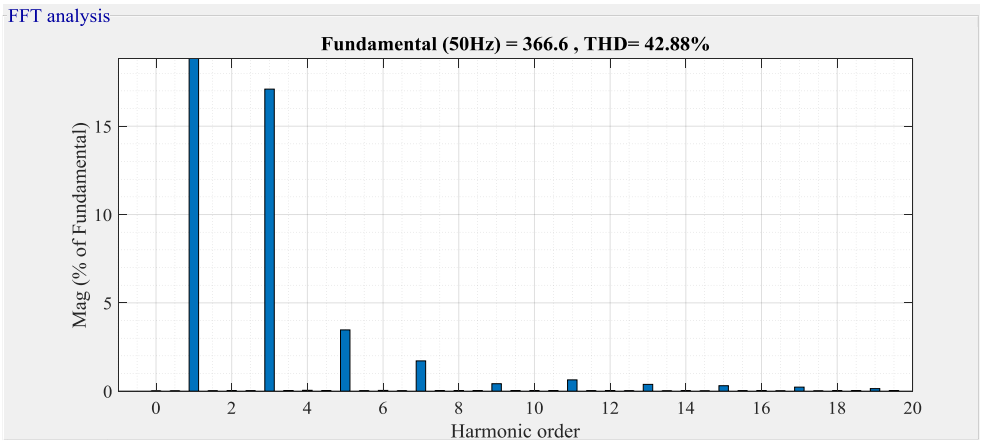
Figure (4-21) shows the effect of reducing modulation index that reduces the number of output voltage levels, Where the number of levels of phase *a* output voltage has been reduced to three levels and the fundamental component in this phase is reduced to (216.6 V), while other phases *b* and *c* still operated in a five-level and their fundamental component increased to (366.6 V). In addition, the phase angles between the inverter phase voltages are not equal to compensate the power between them.



(a)



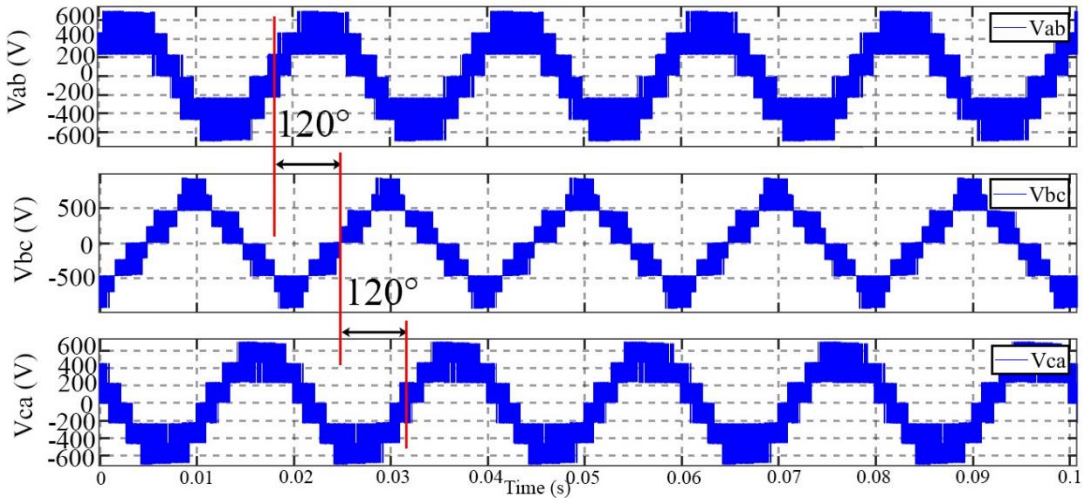
(b)



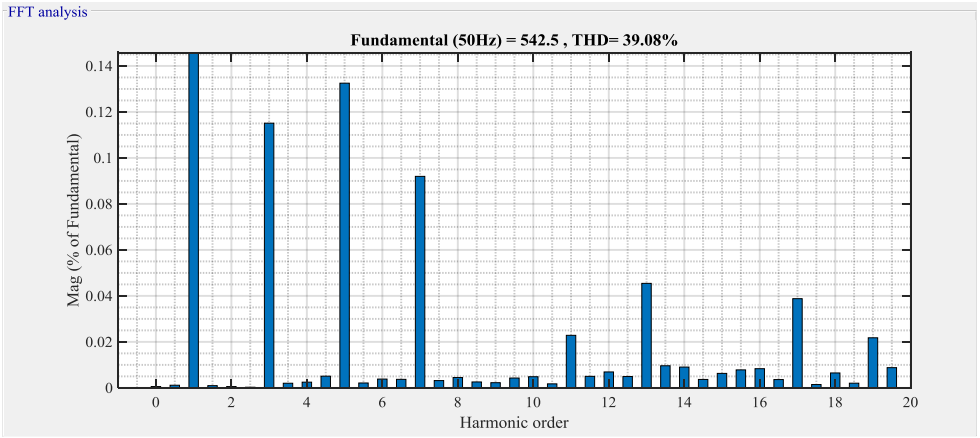
(c)

Figure (4-21): Inverter output phase voltage with the corresponding grid phase voltage for case 2 (b) FFT analysis for phase *a* (c) FFT analysis for phase *b*,*c*.

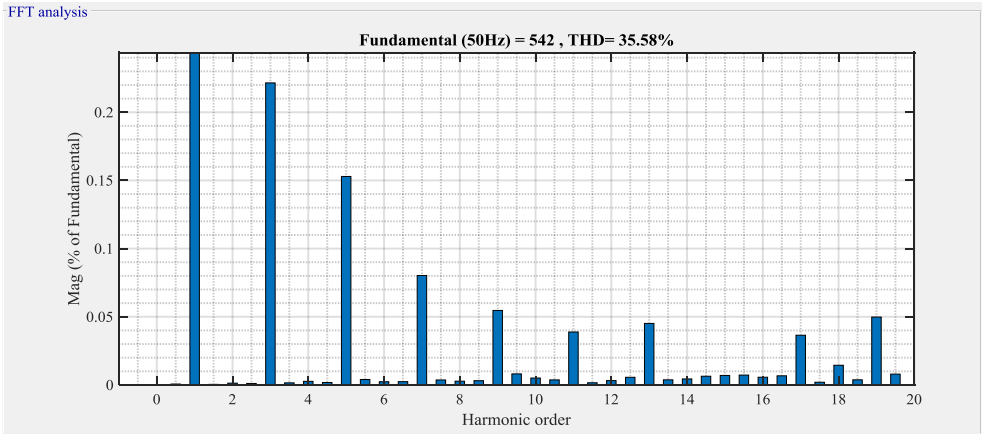
The inverter line to line voltages are shown in figure (4-22) (a). It can be seen from this figure that the amplitude of V_{ab} and V_{ca} are reduced by two levels as a result for the shortfall in phase *a* voltage while the phase angle remains constant at 120° and the fundamental component shown in part (b) also remains balance because of the per-phase compensation performance dose not effects on line to line voltages. The inverter line current still injected with a unity power factor as shown in figure (4-23).



(a)



(b)



(c)

Figure (4-22): (a) Line to line voltages of inverter for case 2 (b) FFT analysis for V_{ab} (c) FFT analysis for V_{bc} or V_{ac}.

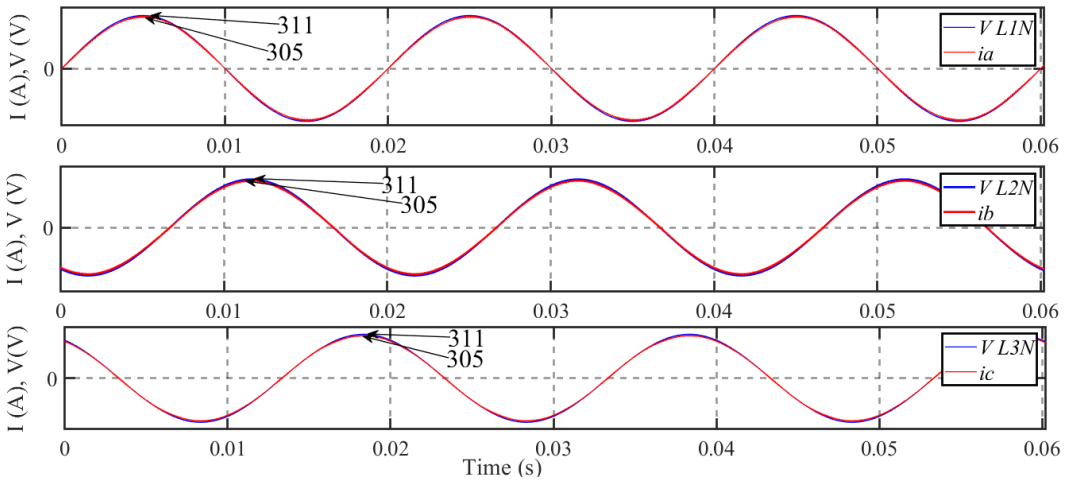


Figure (4-23): Inverter current with grid voltage for case 2.

4.7.3 Simulation results for case 3 (in double HB unit unbalance operation)

In case 3 operating is according to the values in table (4-3), the unbalance happens because the produced power in HB-a1 and HB-b1 is reduced to 20% of its rated value. Figure (4-24) shows the reference voltages $V_{ref\ a}$, $V_{ref\ b}$, and $V_{ref\ c}$ before compensation where $V_{ref\ a}$, $V_{ref\ b}$ slightly increase according to the reduction in power in these phases.

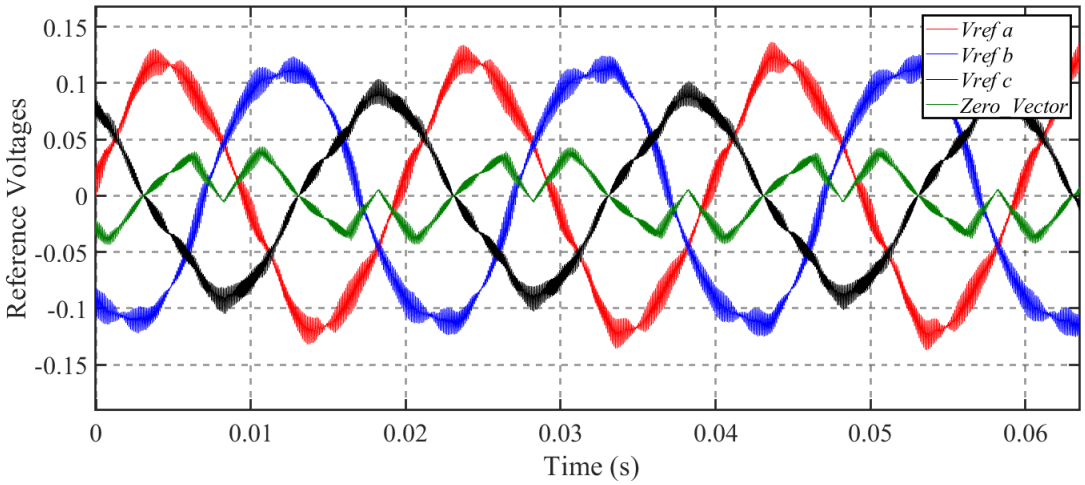


Figure (4-24): Reference voltages for case 3 before per-phase compensation.

The reference voltages after per-phase correction are given in figure (4-25). The max-min of the zero-sequence *zero-vector* is modified as in mode 2 to obtain attain per-phase compensation due to the difference in power produced among the three phases. Figure (4-26) shows the reference voltages of the three phases before and after per-cell compensation, where in (a) and (b) the reference voltages have been modified to provide the redistribution of the unbalance power that is delivered from the cells of phase *a* and phase *b* respectively. As a result, the ON/OFF time of each cell will also be redistributed to ensure that the PV arrays of HB-a1 and HB-b1 still operate at maximum power point. In part (c) the reference voltages in each HB unit phase *c* are increased in amplitude in same manner to redistribute the power and rise the current in phase *a* and phase *b*.

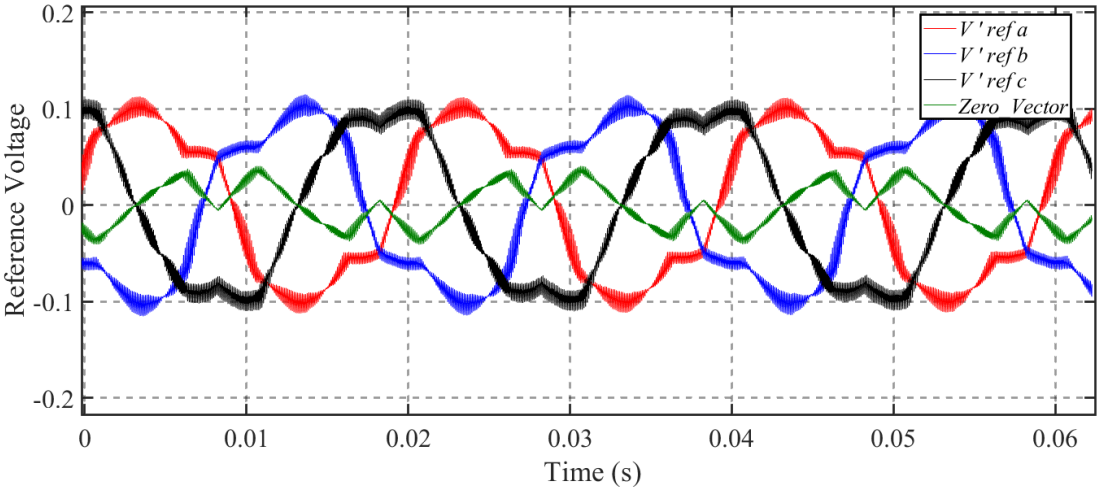
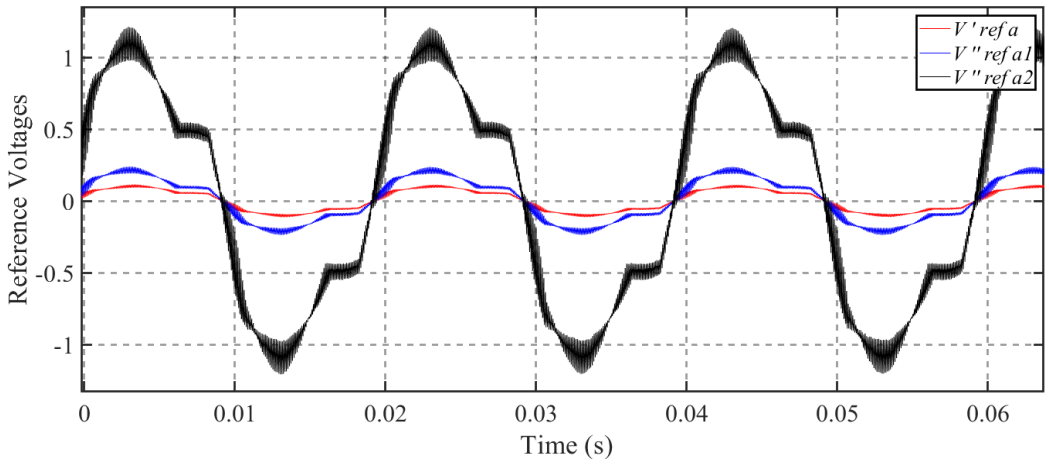
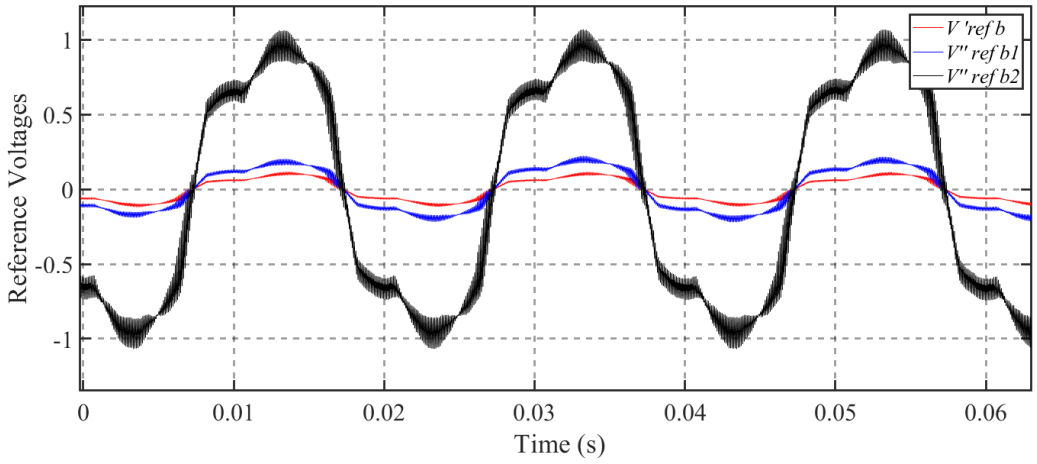


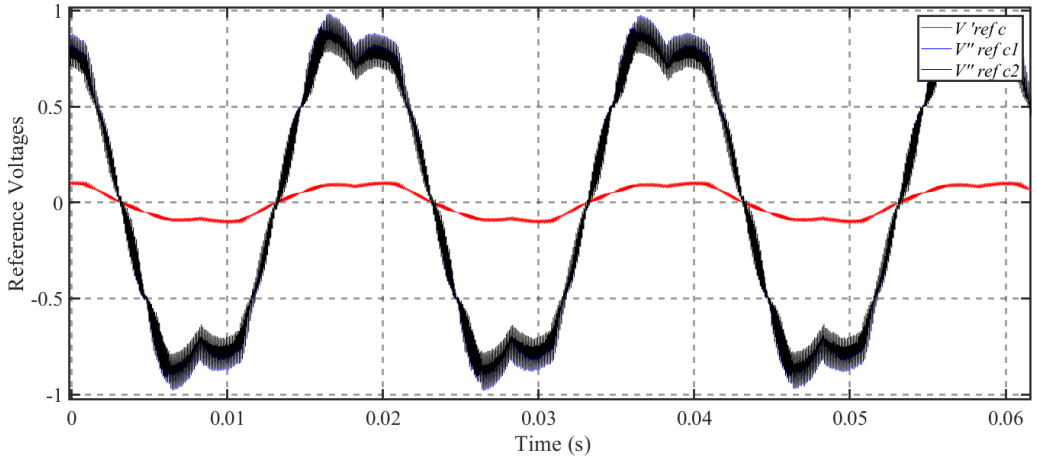
Figure (4-25): Reference voltages for case 3 after per-phase compensation



(a)



(b)



(c)

Figure (4-26): Reference voltages of the three phases before and after per-cell compensation case 3 (a): phase *a*, (b): phase *b*, (c): phase *c*.

The inverter line currents shown in figure (4-27) are balanced and have a value of (176.77 A) RMS which is lower than the rated value in case

1 and the current in case 2 because the total generated power in the three phases is reduced to (119.99 kW).

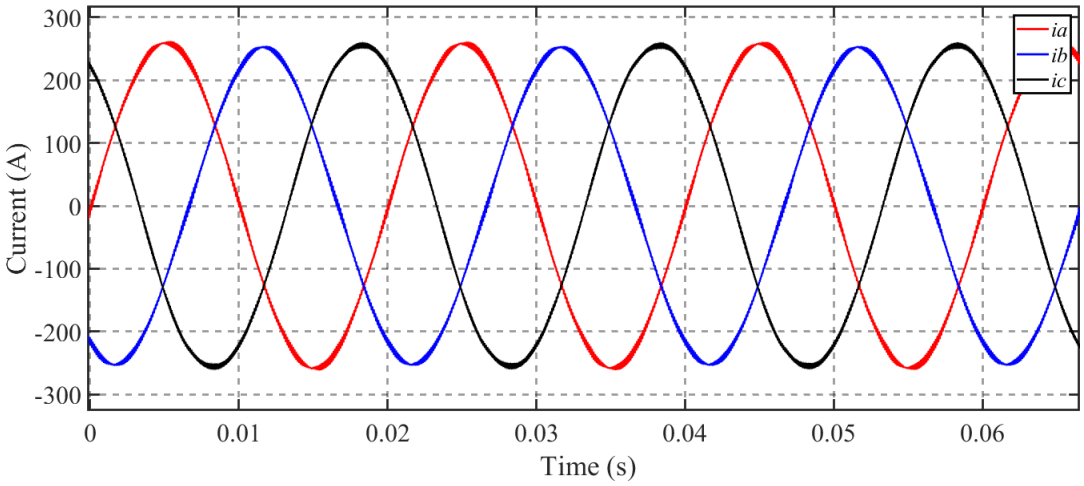
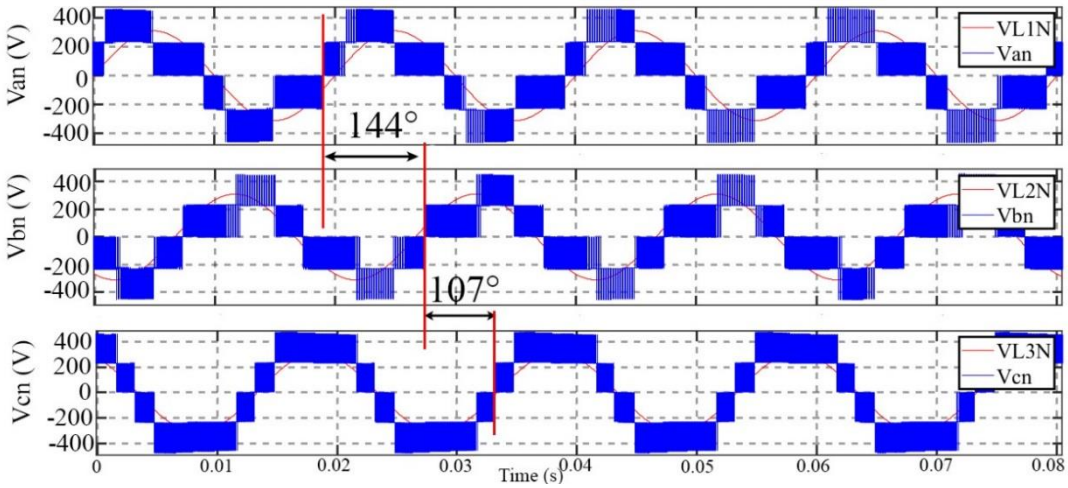
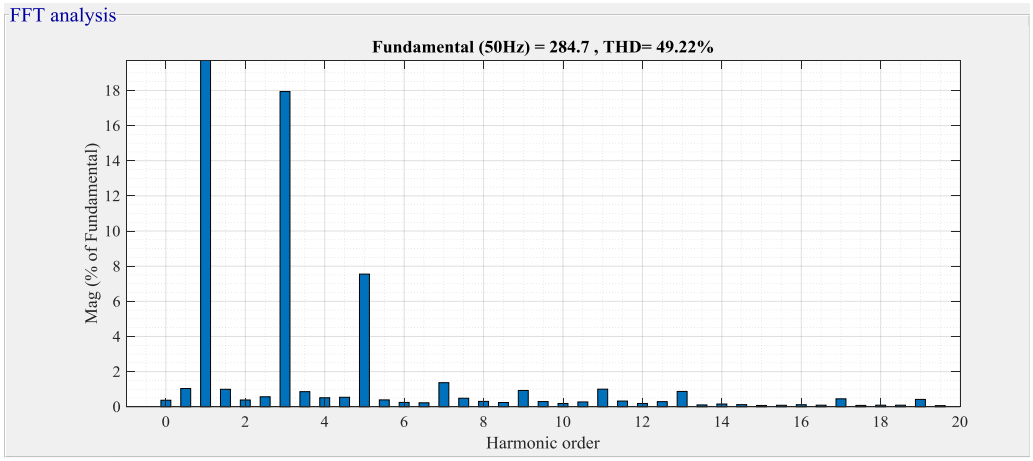


Figure (4-27): Grid injected current for case 3.

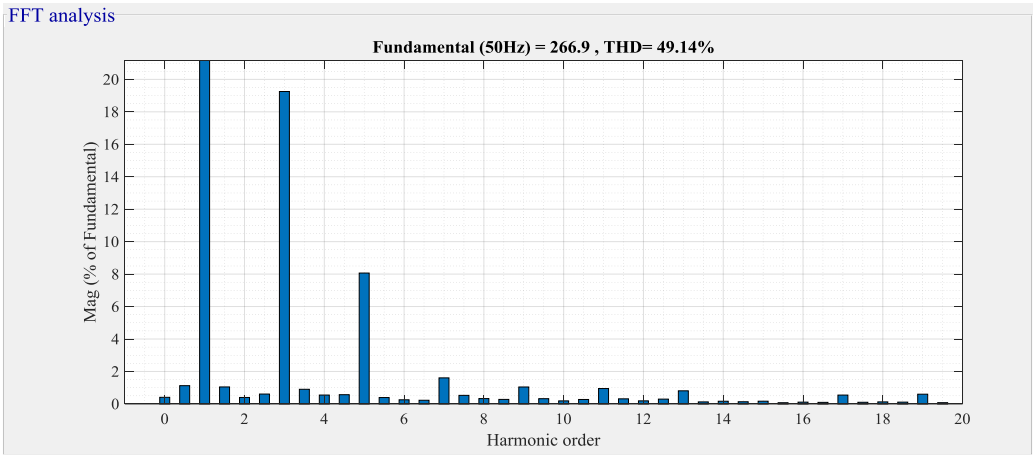
The inverter phase voltages are shown in figure (4-28) (a). As in the previous case, the phase angle between the three phases is not symmetrical and the fundamental component reduced in phase *a* and *b* but increased in phase *c* as shown in part (b), (c), (d) due to the shifting in neutral point position, however, this shifting keeps the phase angle among the line to line voltages constant as shown in figure (4-29). The injected current is kept with unity power factor as shown in figure (4-30).



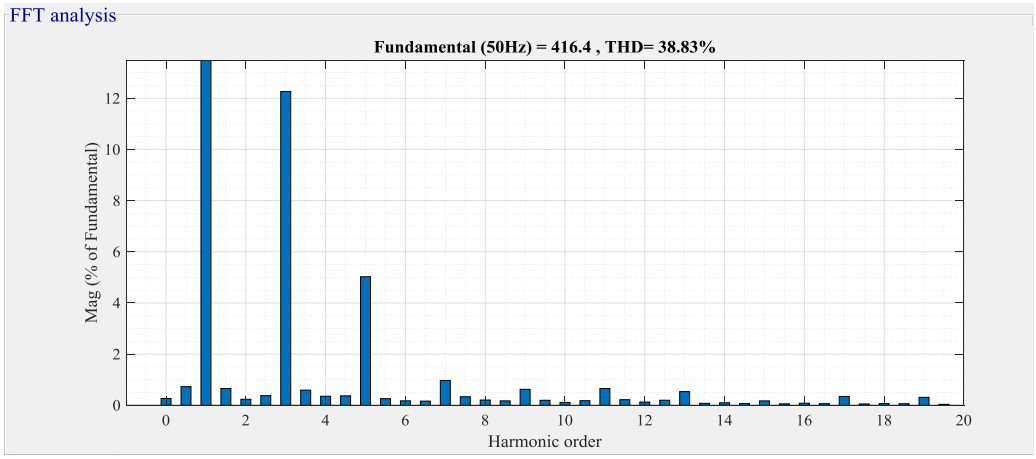
(a)



(b)

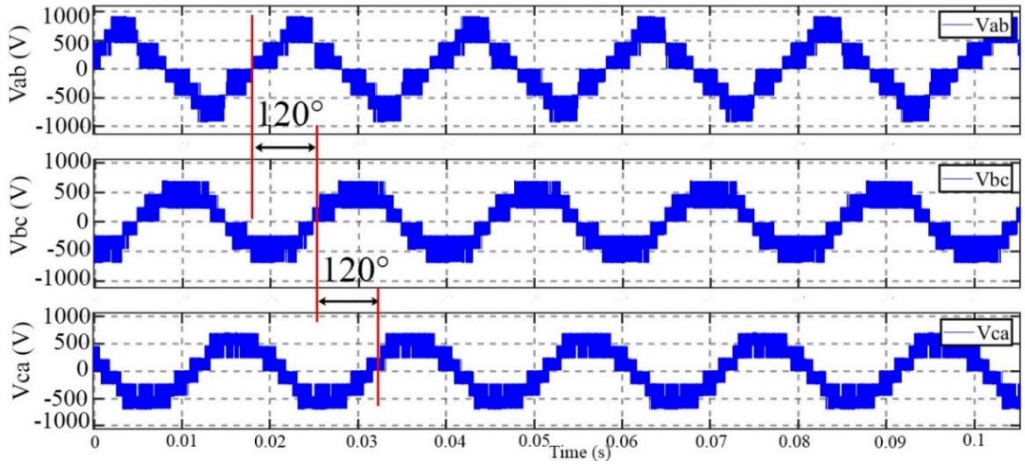


(c)

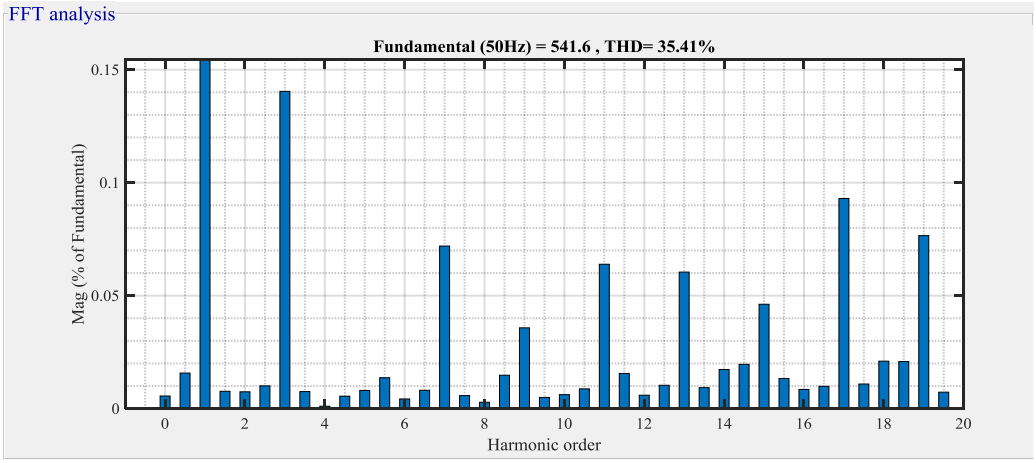


(d)

Figure (4-28): (a) Inverter output phase voltage with the corresponding grid phase voltage for case 3 (b) FFT analysis for phase *a* (c) FFT analysis for phase b (d) FFT analysis for phase *c*.



(a)



(b)

Figure (4-29): (a) Line to line voltages of inverter for case 3 (b) FFT analysis for V_{ab}.

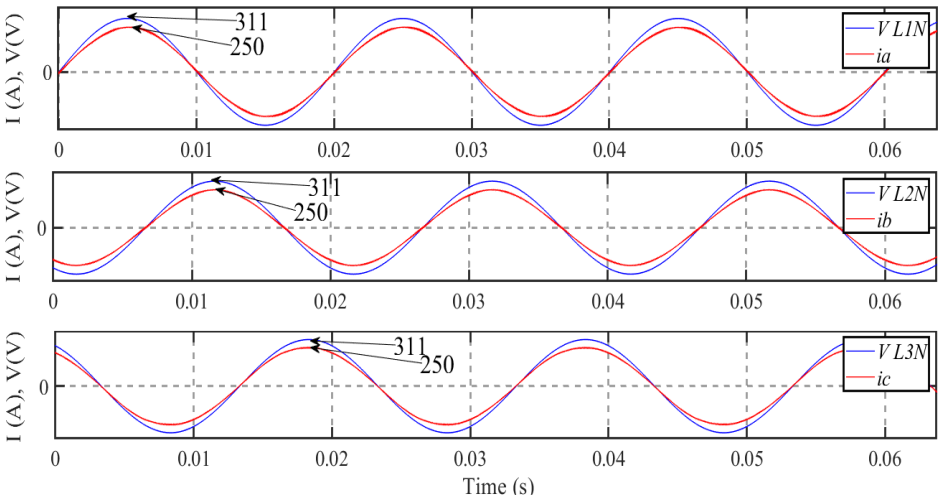


Figure (4-30): Inverter current with grid voltage for case 3.

4.7.4 Simulation results for case 4 (in single-phase unbalance operation)

According to table (4-3), the unbalance operation in the case 4, occurs as the PV array fed the upper bridge HB1 of phase *a* by a power reduced to (19.28 kW) which is equal to 70% of the rated power, while the PV fed the HB2 in the same phase produced power about 20% of the rated power having a value of (5.435 kW), while the power in phase *b* and phase *c* kept in (27.28 kW) which is the rated power value. Although the two units produced a different ratio of power, the system performance acted as in case 2, and the inverter line current had a value of (200.8 A) RMS as shown in figure (4-31).

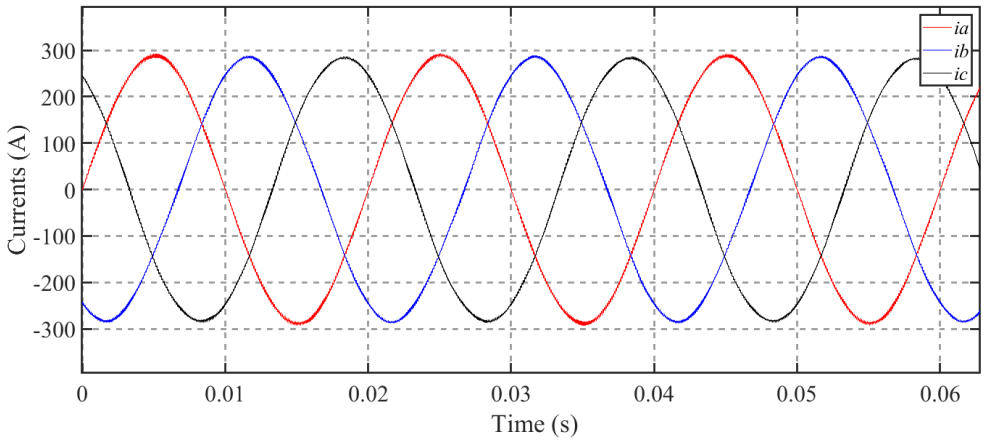


Figure (4-31): Grid injected current for case 4.

4.7.5 Simulation results for case 5 (minimum power for upper PV arrays and rated power for lower PV arrays)

In case 5 of operation according to table (4-3), the PV arrays are connected to the upper HB units of the three phases of the inverter produced power reduced form (27.28 kW) to (5.345 kW), but this power was equal among the three phases. Figure (4-32) shows the reference voltages $V_{ref\,a}$, $V_{ref\,b}$, and $V_{ref\,c}$ before compensation which were identical in amplitude at about (0.12). The reference voltages after compensation

process $V'_{ref\,a}$, $V'_{ref\,b}$, and $V'_{ref\,b}$ with the max-min of zero-sequence is shown in figure (4-33). The max-min remained without changing as case 1 (mode 1), because there is no unbalance among the three phases. As a result, the per-phase compensation is deactivated.

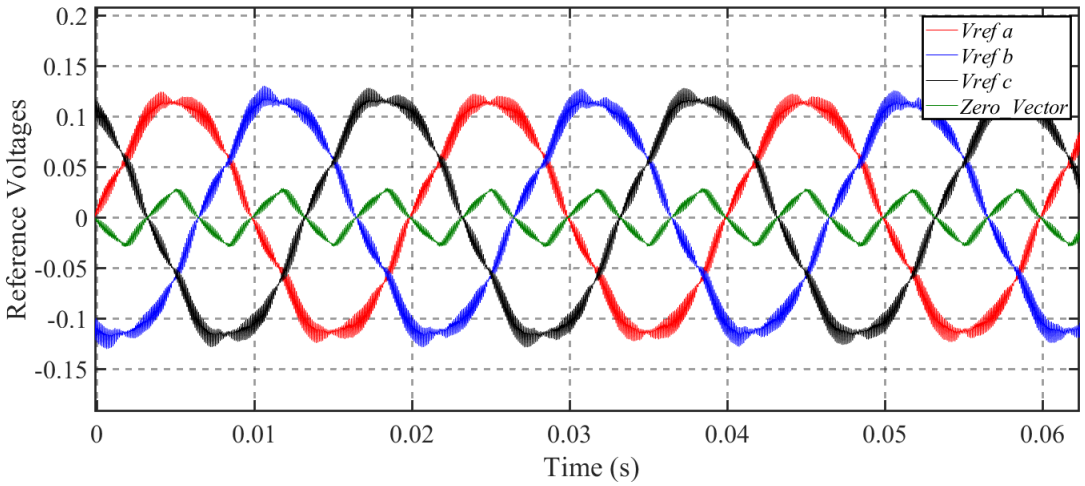


Figure (4-32): Reference voltages for case 5 before per-phase compensation.

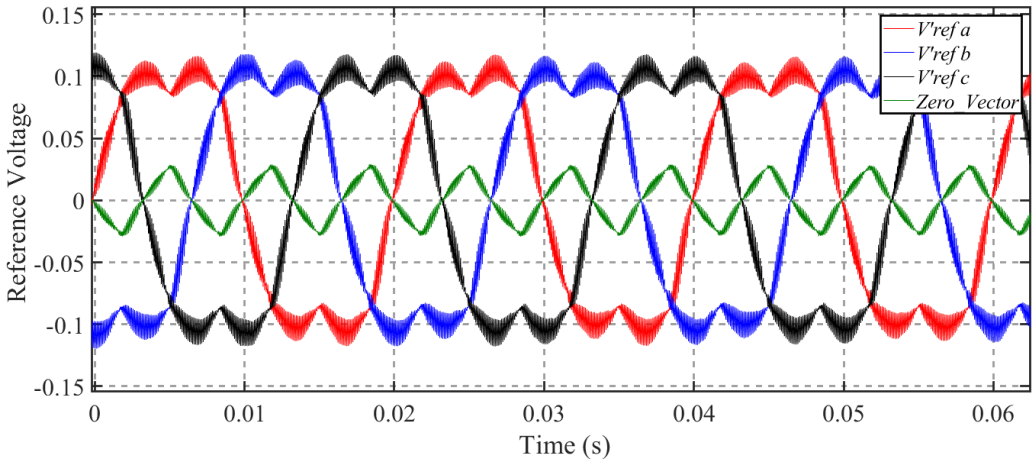


Figure (4-33): Reference voltages for case 5 after per-phase compensation.

Figure (4-34) illustrates phase *a* reference voltage before and after per-cell compensation. The compensation is performed by rising the reference voltage $V'_{ref\,a2}$ for HB-a2 as the reference voltage $V''_{ref\,a1}$ of HB-a1 is dropped to approximately (0.2) due to the reduction in the produced power to 20% of rated value. Similarly, the same procedure is applied for

phase *b* and phase *c*. However, the modified amplitude affects the redistribution of ON/OFF time of each unit according to the produced power to ensure that all upper PV arrays still operate at their maximum power point.

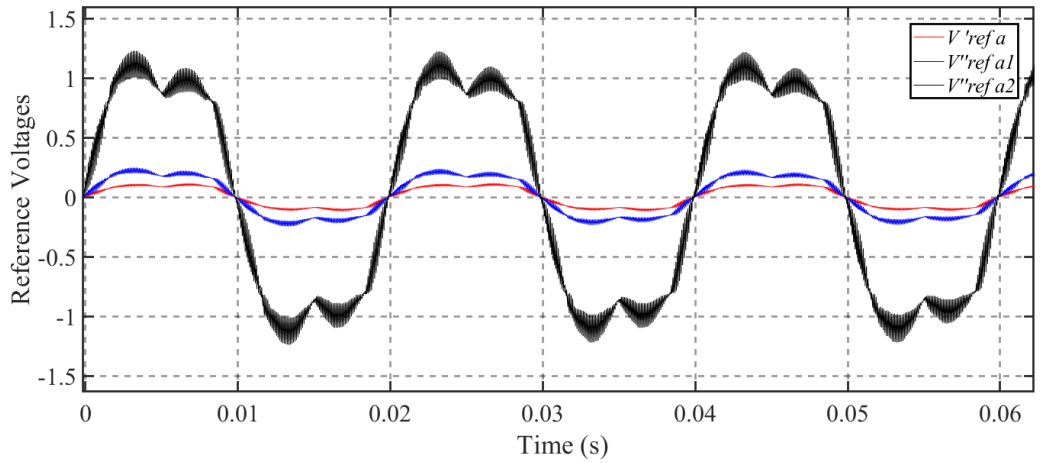


Figure (4-34): Phase *a* reference voltage for case 5 before and after per-cell compensation.

The inverter line currents that shown in figure (4-35) are balanced injected in to the grid and have a value of (148.49 A) RMS that are dropped below the rated value in case 1 because of the reduction in upper PV arrays power. As a result, the total generated power in the three phases become (98.145 kW).

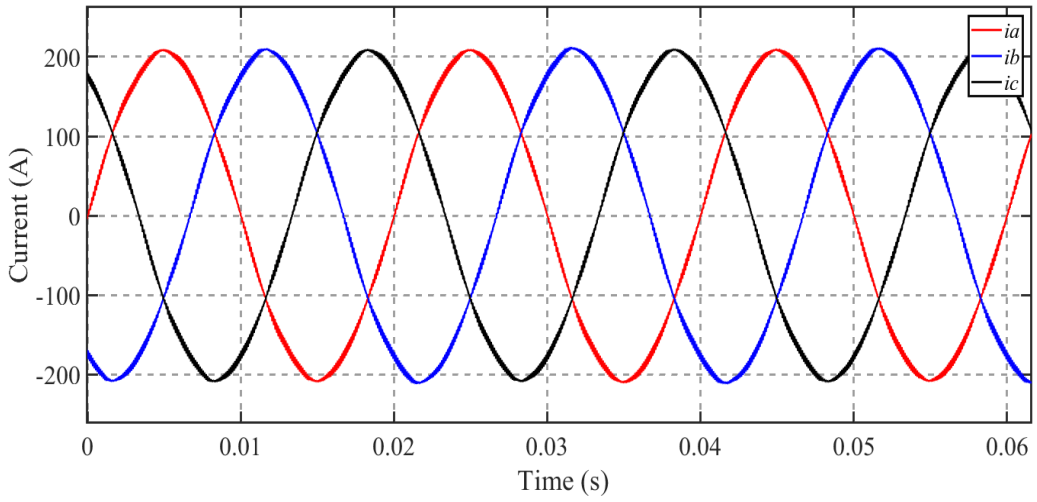
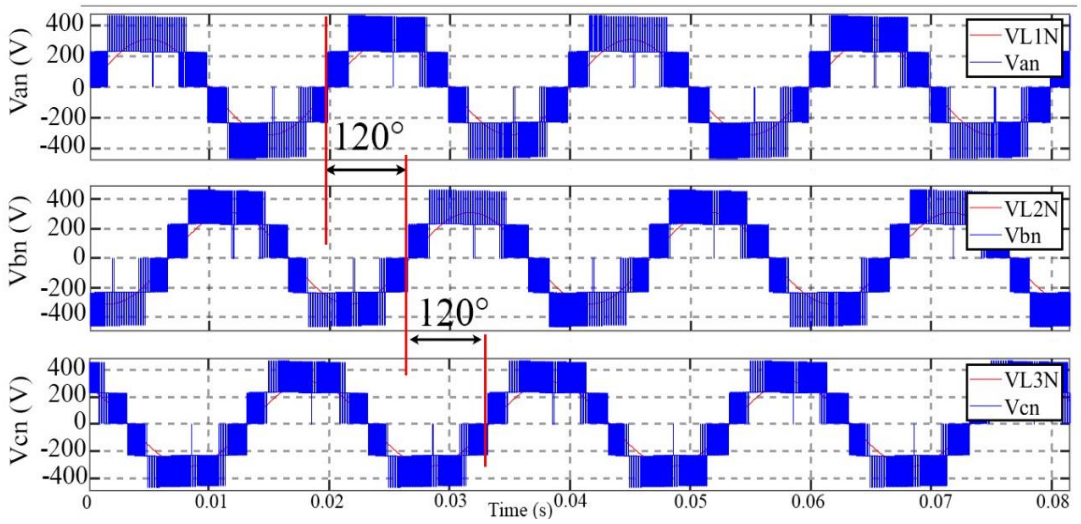
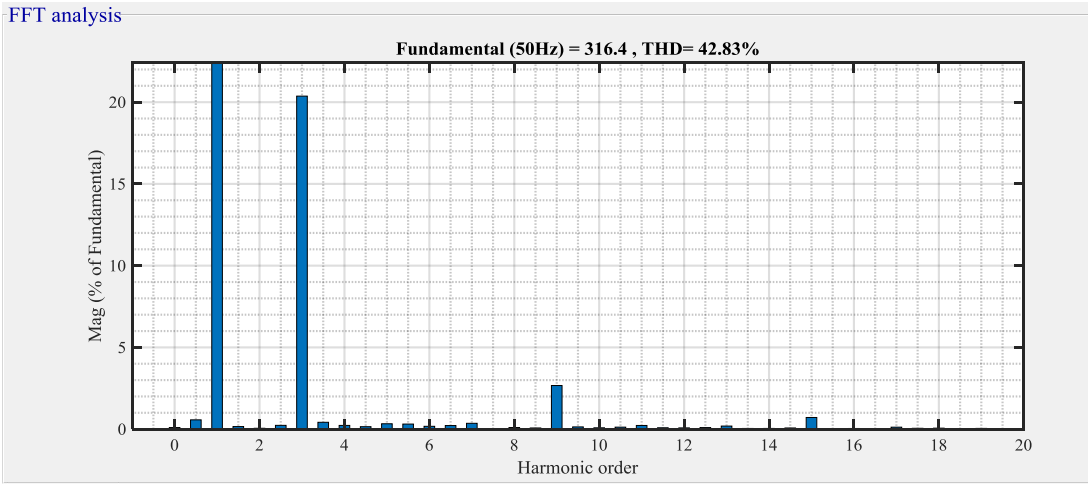


Figure (4-35): Grid injected current for case 5.

The inverter output phase voltages are shown in figure (4-36). As illustrated in the figure, the voltages are balanced in amplitude and in phase angle because there is no unbalance power among the three phases. Figure (4-37) explains the inverter line to line voltages which are also balanced because the neutral point is kept in the original point.

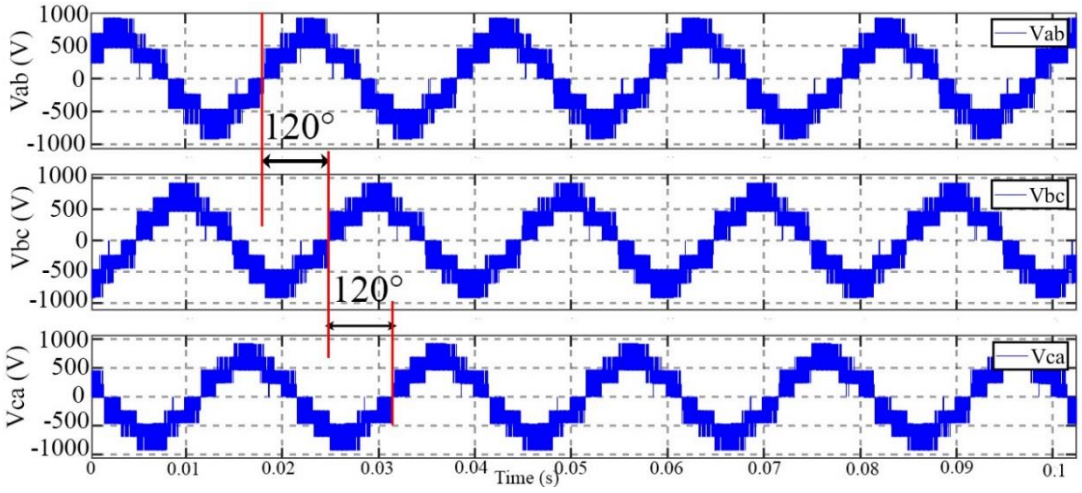


(a)

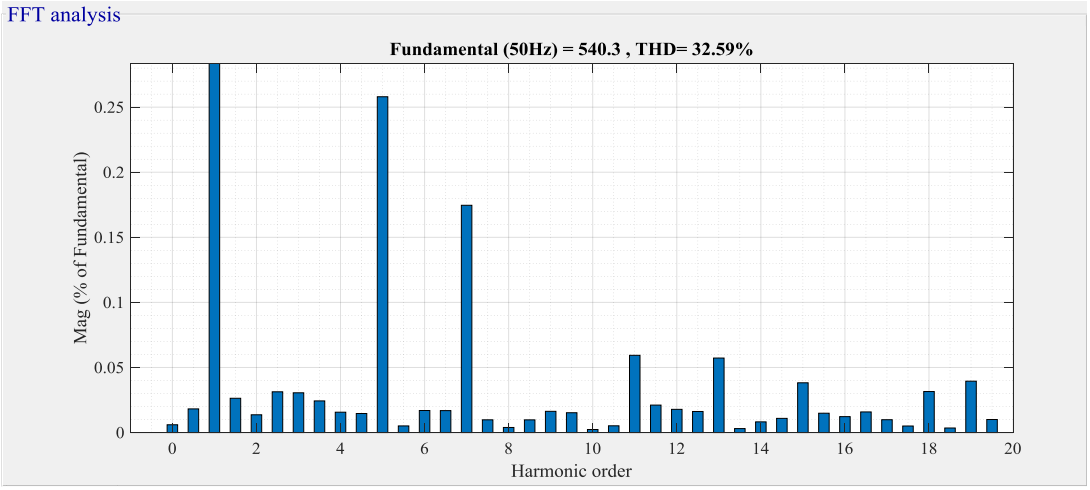


(b)

Figure (4-36): (a) Inverter output phase voltage with the corresponding grid phase voltage for case 5 (b) FFT analysis for phase *a*.



(a)



(b)

Figure (4-37): (a) Line to line voltages of Inverter for case 5 (b) FFT analysis for V_{ab}.

4.7.6 Simulation results for case 6 (minimum power of all PV arrays)

In case 6 of operation according to table (4-3), similarly to case 1, the system is balanced not only among the three phases but also among the cells in each phase, therefore, the system works in the same manner as case 1, in another words, the per-phase and per-cell compensation are deactivated, except that all PV arrays work at its minimum value. As a result, the inverter line current is reduced to (48 A) RMS as shown in figure

(4-38). Whereas the total injected power is reduced to (80%) from its rated value.

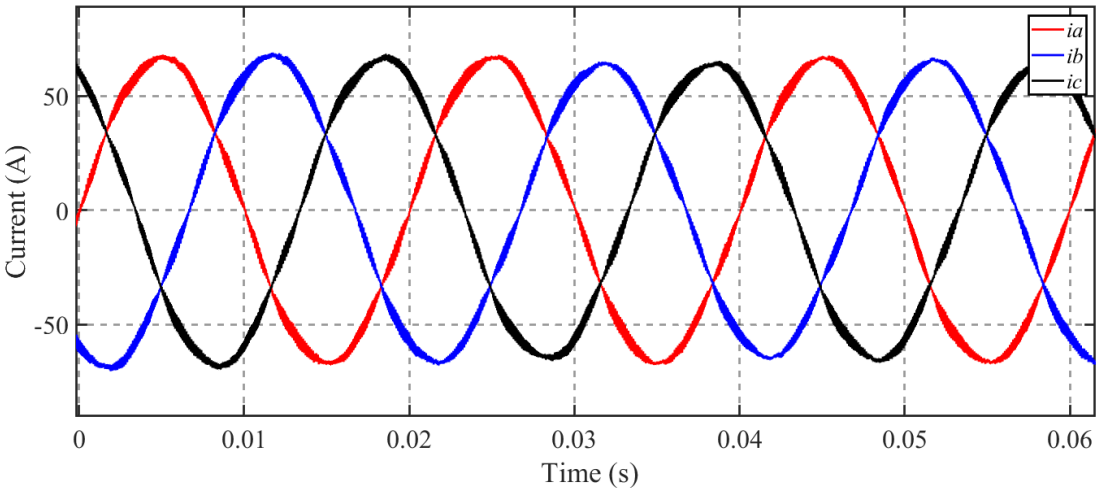


Figure (4-38): Grid injected current for case 6.

4.7.7 Simulation results for case 7 (no power for one of upper PV and rated power for the rest)

In case 7 operation according to table (4-3), the system is operating with one PV produces no power, which means that the total generated power is (136.4 kW) as the power of PV connected to the HB-a1 is (zero). Therefore, there is unbalance condition between the phases and between the cells in single-phase, the system works as case 2 so both compensation circuits will operate. The reference voltage for phase *a* after per-phase and per-cell compensation is shown in figure (4-39). It is clear from this figure that the reference voltage $V''_{ref\,a1}$ is reduced to (zero) while the reference voltages for phase *b* and phase *c* are kept without change because of the power is balanced in their HB unit. Figure (4-40) illustrates the inverter output phase voltages and its phase angle shift between phases due to no power produced in HB-a1 and the fundamental component of phase *a* reduced to (195.1V) while fundamental components of phase *b* and *c* increased, while the phase angle in inverter line to line voltages is kept

without change because of the effects of per-phase compensation as mentioned in case 2. The inverter line current that will be injected into the grid is shown in figure (4-41).

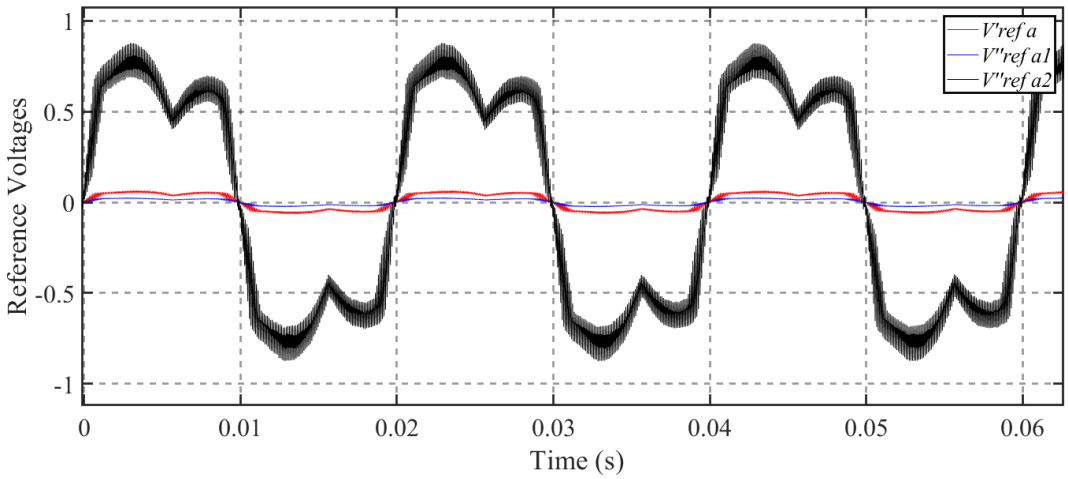
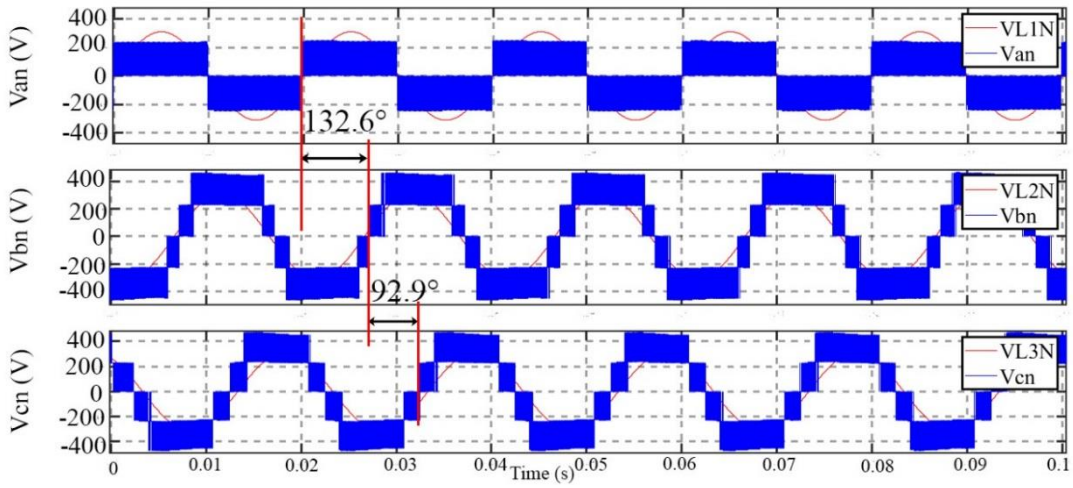
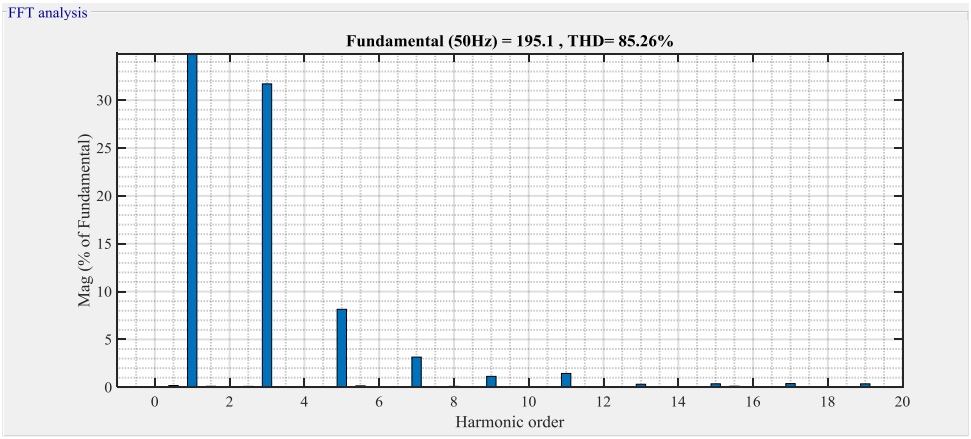


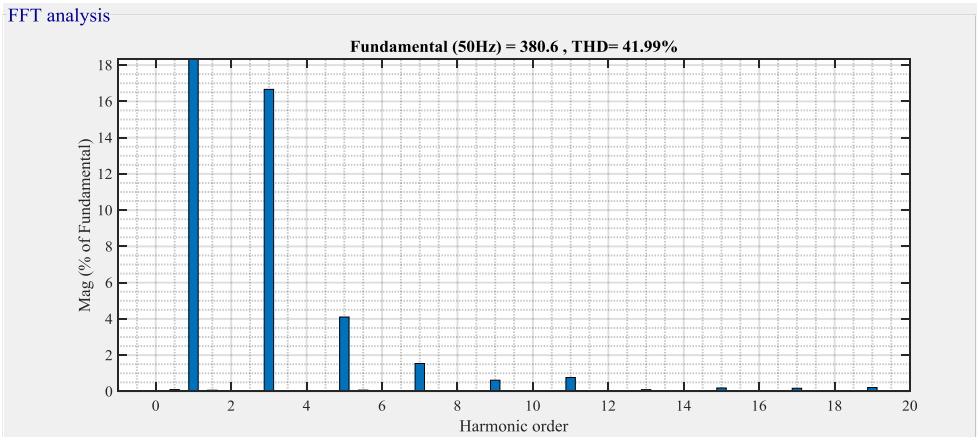
Figure (4-39): Reference voltages of phase *a* for case 7 before and after per-cell compensation.



(a)



(b)



(c)

Figure (4-40): (a) Inverter output phase voltage with the corresponding grid phase voltage for case 7 (b) FFT analysis for phase *a* (c) FFT analysis for phase *b* (d) FFT analysis for phase *c*.

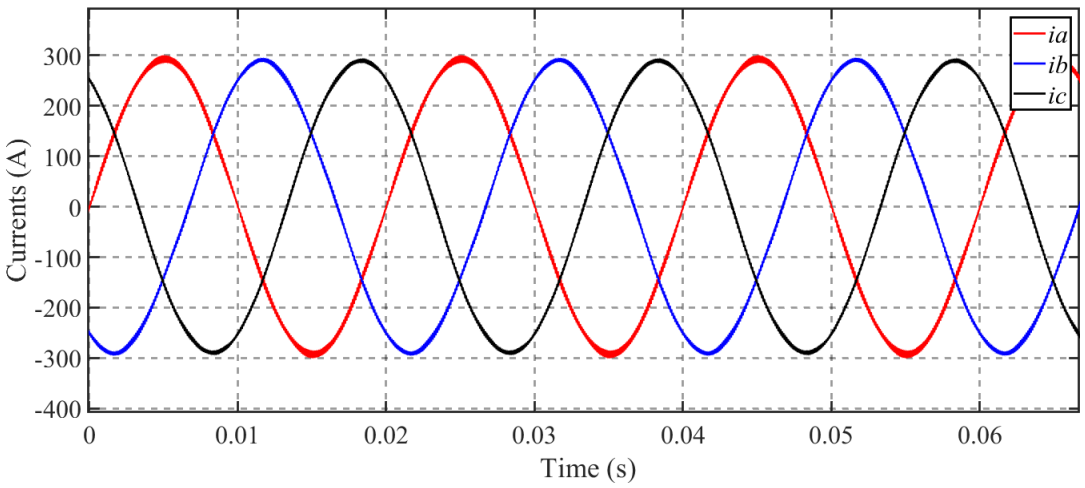


Figure (4-41): Grid injected current for case 7.

4.7.8 Simulation results for case 8 (no power for one of upper PV and minimum power for the rest)

In case 8 according to the table (4-3), the system behaves as in case 7 except that the operating PV arrays work at their minimum power generation. The injected line currents of the inverter are shown in figure (4-42) which is having a value of (41 A) RMS due to the reduction in total generating power to (27.175 kW).

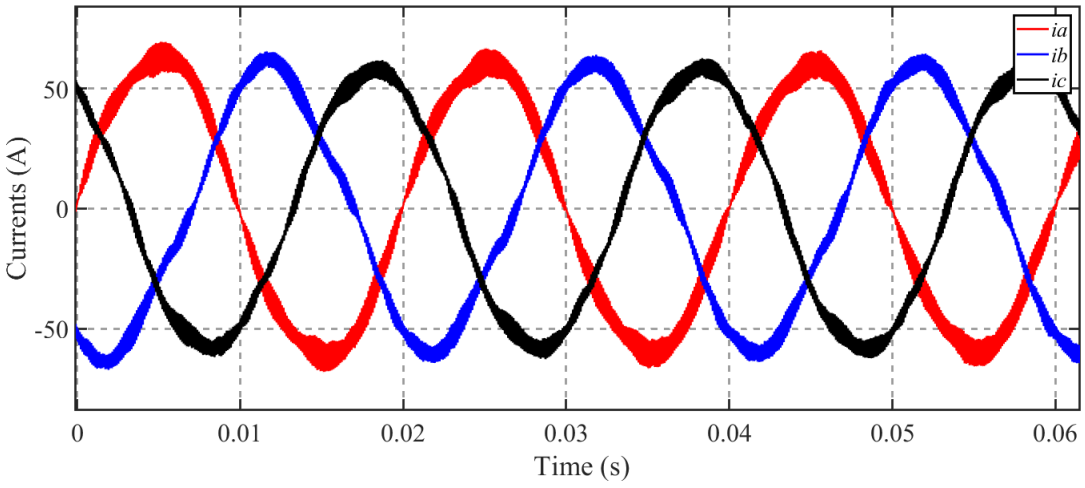


Figure (4-42): Grid injected current for case 8.

CHAPTER FIVE

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

5.1 Conclusions

The main purpose of this work was to investigate the use of a cascaded H-bridge VSI as an applicable power electronics approach that is used in solar energy source grid connections. The solar energy grid connection was investigated and simulated to examine the control scheme as well as the behavior of the entire system in maximum power point operating without the need to use extra dc-dc converters as it is used in standard systems.

The simulation procedure was performed by employing the three-phase (5L-CHB-VSI) each HB unit fed by a separated PV array. As well as, the designed system was controlled using the scheme of voltage oriented control (VOC) to regulate the process of injecting the active and reactive power into the grid independently. In addition, two feedforward compensation methods were applied. The first was accomplished by injecting a zero-sequence signal into reference voltage to obtain balanced power flow to the grid at unbalancing conditions. Whereas, the second was to independently modify the amplitude of each HB unit of the inverter's reference voltage signal to track the maximum power point of each connected PV.

The effectiveness of these methods was utilized in this proposed system, and was investigated through simulation work for five different operating cases, in which the generated power from the PV varies due to changing sun irradiations.

balanced case which is case 1, was tested under rated power generation for all H-bridge units, followed by unsymmetrical power generation among the three phases in case 2 by reducing the power of one from the upper PV arrays to 20% of its rated power. In case 3 two of upper PV array reduced its power to 20% of its rated value. In case 4 both cells (the upper and the lower) in one phase varied in different percentage of sun irradiation. case 2, case 3, case 4 where the system works in unbalance condition the output current and power is still in balance.

Case 5 was tested be reducing the power of the three upper cells to (20%) of its rated value, the unbalance occurs among the cell in the phase only and the total power reduced to about (40%) from the total injected power in balance case.

However, case 6 where all the PV works at minimum power, so the total power injected was reduced to (80%) from the power in balance condition.

Case 7 and case 8 examine the system performance if one of the PV break down, in both of rated and minimum operation condition, the system able to rebalance the injected power.

Simulation results performed for these operations cases demonstrate the system's flexibility when operating with independent MPPT for each H-bridge of the inverter without the need of dc-dc converters. Even in asymmetrical generation situations, a stable and balanced power injection to the grid is ensured. The topology of the cascaded H-bridge voltage source inverter is ideal for grid connection PV system.

5.2 Suggestions for future works

1. Study the influence of reactive power in the system performance if it is injected to the VOC as well as the active power injection.
2. Connect to this system a micro-inverter with a battery bank to utilize the solar energy in the villages and remote areas where the grid power is poor.
3. Utilize the CHB by connected it to a different renewable sources as wind turbine and large scale PV farm.

APPENDIX A

Filter design

The value of the filter inductance can be determined by [73]:

$$L_f = 2\frac{V_{DC}}{\sqrt{2} * 2 * \pi * f_{sw} * 3 * \Delta I}$$

Where L_f is the inductance value

V_{DC} is the DC voltage in each phase

f_{sw} is the switching frequency for the modulator

ΔI is the current ripple and it can be more than 5% [74]

$$L_f = 2\frac{232 + 232}{\sqrt{2} * 2 * \pi * 5000 * 3 * 0.06 * 348} = 0.33\ mH$$

The value of filter resistance is considered as the internal resistance of cables and it is small about (5 mΩ)

MPPT algorithm function

```
function Vref = RefGen(V, I)

Vrefmax =290.4;
Vrefmin = 0;
Vrefinit = 232;
deltaVref =0.0001;
persistent Vold Pold Vrefold;

dataType = 'double' ;

if isempty(Vold)
    Vold = 0;
    Pold = 0;
    Vrefold = Vrefinit;
end

P = V*I;
dV = V-Vold;
dP = P-Pold;

    if dP<0
        if dV<0
            Vref = Vrefold + deltaVref;
        else
            Vref = Vrefold - deltaVref;
        end
    else
        if dV<0
             Vref =  Vrefold - deltaVref;
        else
             Vref = Vrefold + deltaVref;
        end
    end

if Vref >= Vrefmax || Vref <= Vrefmin
    Vref = Vrefold;
end

Vrefold = Vref;
Vold = V;
Pold = P;
```

Proportional integral controller (PI) gain:

1. Current loop controllers

   $K_P = 0.002$

   $K_I = 1$

2. Voltage loop controller

   $K_P = 4$

   $K_I = 5$

3. Per-cell modulation index compensation controllers

   $K_P = 60$

   $K_I = 200$

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الخلاصة

هذه الدراسة تقترح نهجاً جديداً لربط الطاقة الشمسية بالشبكة الكهربائية. ومن اجل ذلك يستخدم النظام المقترح طوبولوجيا العاكس ذا المستويات الخمسة (5L-CHB) الذي يتمتع بمزايا من حيث الكلفة القليلة وسهولة الصيانة، إضافة الى ذلك، استمرار توليد الطاقة في ظل ظروف جوية مختلفة، فان النظام يسمح بحالات تشغيل مختلفة على أساس شدة الاشعاع الشمسي المؤثر على الخلية الشمسية التي تؤخذ في الاعتبار في جميع تفاصيل العمل. يعتبر هذا النظام حل جيد لدمج أنظمة التوليد الصغيرة الى الشبكة في البلدان النامية.

يتألف كل طور من اطوار العاكس من وحدتين H-Bridge مربوطتين على التوالي كل واحدةٍ منهما تُغذى بمصدر فولتية منفرد. تم استخدام الخلايا الشمسية في هذه الدراسة كمصدر للفولتية، وأيضا تم استخدم نظام السيطرة التقليدي Voltage Oriented Control (VOC) والذي يعمل على تنظيم ربط العاكس مع الشبكة متضمناً دائرتين اضافيتين لمعالجة مؤشر التضمين.

هناك طريقتان للتعويض تم استخدامهما في هذا العمل كل واحدة منها تقوم بوظيفة معينة في النظام، الأولى تعتمد على حقن المتسلسل الصفري (Zero-sequence injection) الى فولتية المرجع، وذلك من اجل موازنة الطاقة بين الاطوار الثلاثة في حالة حدوث أي حالة نقص في تولد الطاقة عند الخلايا الشمسية المربوطة على العاكس بسبب الظلال الجزئية او بسبب الأعطال الفنية.

اما الطريقة الثانية فهي تهتم بتتبع اقصى نقطة للطاقة Maximum Power Point Tracking (MPPT)من الخلية الشمسية في جميع الحالات ومن ثم وحقنها الى الشبكة بأعظم قدرة من دون الحاجة الى ربط محولات dc-dc بين الخلايا الشمسية والعاكس، وهذا يقلل من تعقيد النظام كما يقلل من كلفة تنصيبه.

في هذه الدراسة تم استخدمت برمجيات الحاسوب MATLAB/ Simulink لمحاكاة النظام، أظهرت نتائج المحاكاة وثوقيه النظام ومرونة التشغيل نتيجةً للوحدات الخاصة بتتبع اقصى نقطة للطاقة MPPT للخلايا الشمسة المنفصلة. كذلك أظهرت نتائج الدراسة ان القدرة المحقونة للشبكة تكون دائما متوازنة حتى في حالة عدم توازن الطاقة المتولدة من الخلايا الشمسية.

جـامعـة نينوى

كلية هندسة الالكترونيات

قسم الإلكترونيك

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هديل سعد طاهر معروف

رسالة ماجستير في هندسة الإلكترونيك

بإشراف

الدكتور أحمد ذنون يونس

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رسالة تقدمت بها

هديل سعد طاهر معروف

إلى

مجلس كلية هندسة الالكترونيات –جامعة نينوى

وهي جزء من متطلبات نيل شهادة الماجستير

علوم في هندسة الالكترونيك

بإشراف

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