Ninevah University
College of Electronics Engineering
Department of Systems and Control

Electronic I I
Lecture 3 part 2

Voltage-Divider Bias

by
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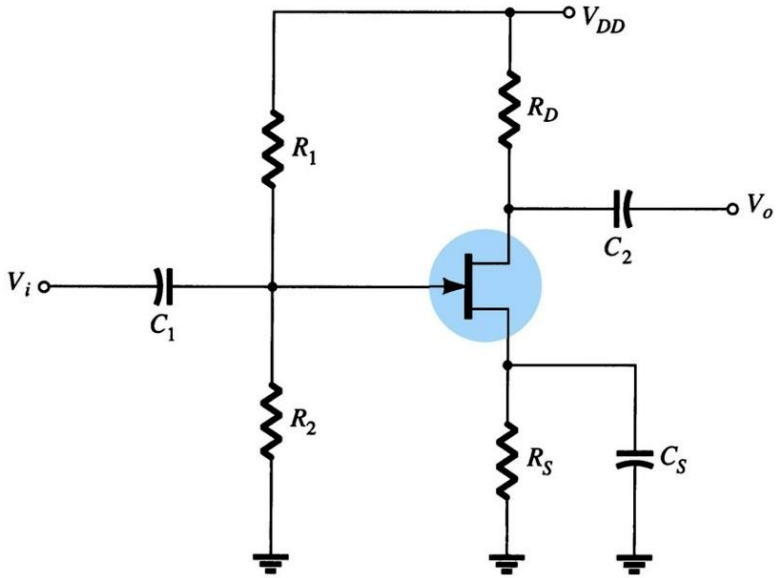
2nd Class

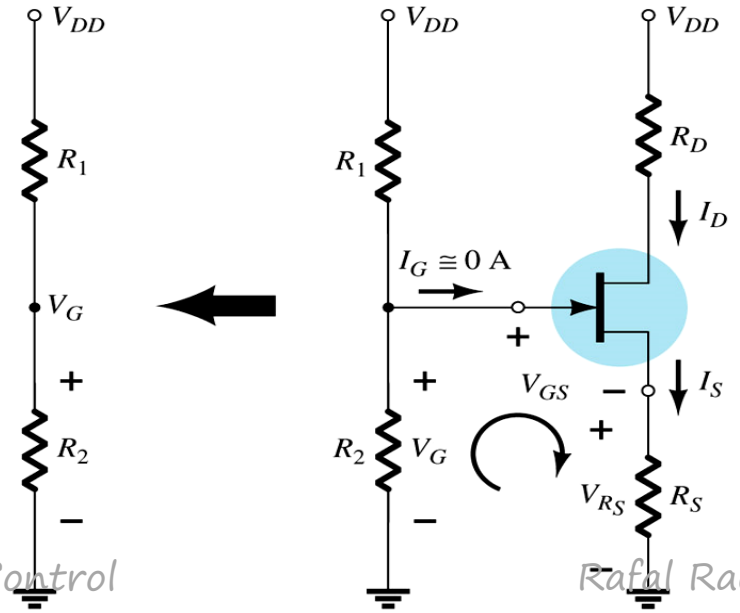
Voltage-Divider Bias

- The arrangement is the same as BJT but the DC analysis is different
- In BJT, I_B provide link to input and output circuit, in FET V_{GS} does the same



Voltage-Divider Bias

- The source V_{DD} was separated into two equivalent sources to permit a further separation of the input and output regions of the network.
- I_G = 0A ,Kirchoff's current law requires that I_{R1}= I_{R2} and the series equivalent circuit appearing to the left of the figure can be used to find the level of V_G.



Voltage-Divider Bias

- V_G can be found using the voltage divider rule :

$$\mathbf{V_G = \frac{R_2 V_{DD}}{R_1 + R_2}}$$

- Using Kirchoff's Law on the input loop:

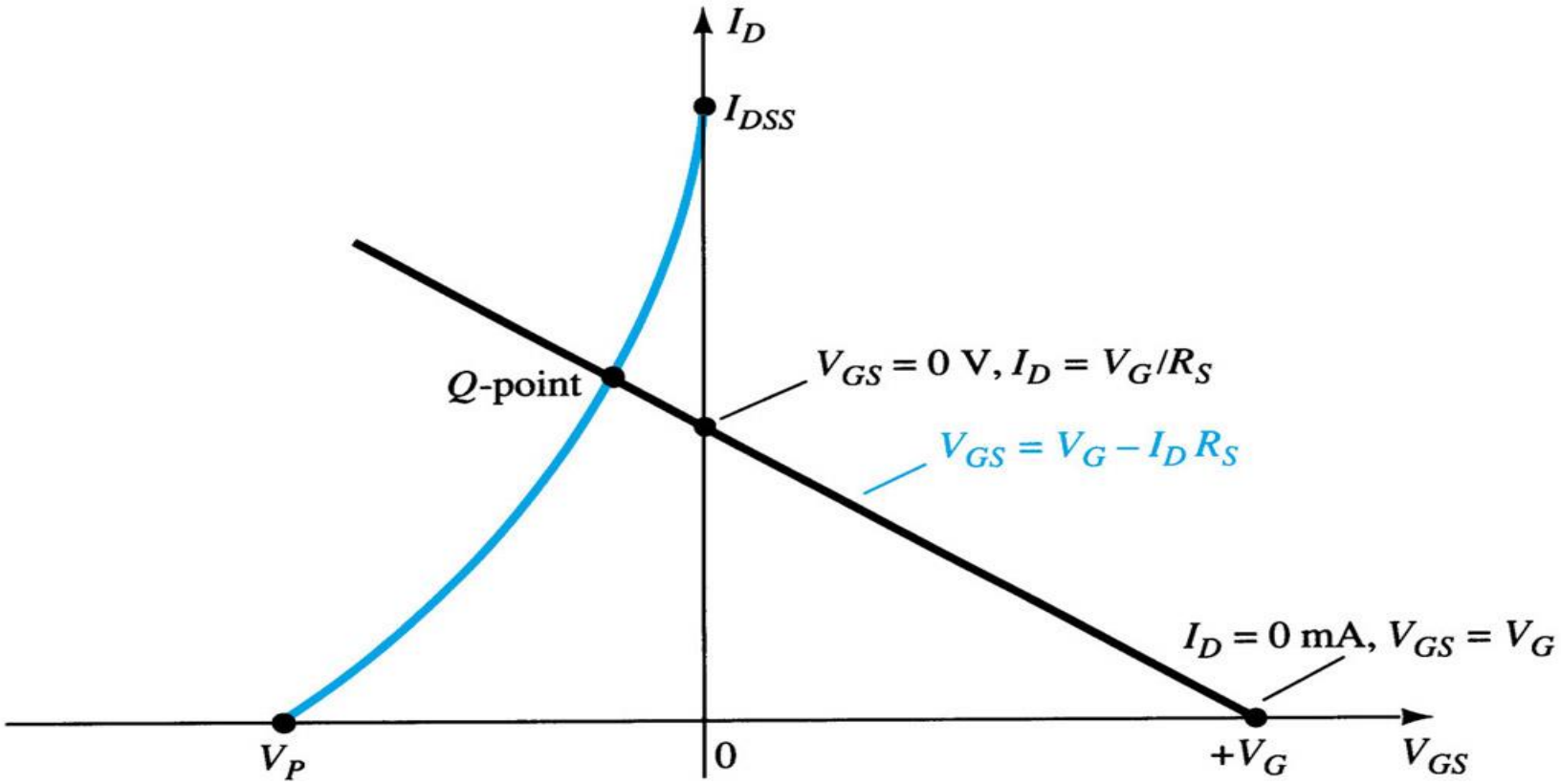
$$V_G - V_{GS} - V_{RS} = 0$$

- Rearranging and using $I_D = I_S$:

$$V_{GS} = V_G - I_D R_S$$

- Again the Q point needs to be established by plotting a line that intersects the transfer curve.

Procedures for plotting



1. Plot the line: By plotting two points: $V_{GS} = V_G$, $I_D = 0$ and $V_{GS} = 0$, $I_D = V_G/R_S$
2. Plot the transfer curve by plotting I_{DSS}, V_P and calculated values of I_D.
3. Where the line intersects the transfer curve is the Q point for the circuit.

- Once the quiescent values of I_{DQ} and V_{GSQ} are determined, the remaining network analysis can be found.

$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$

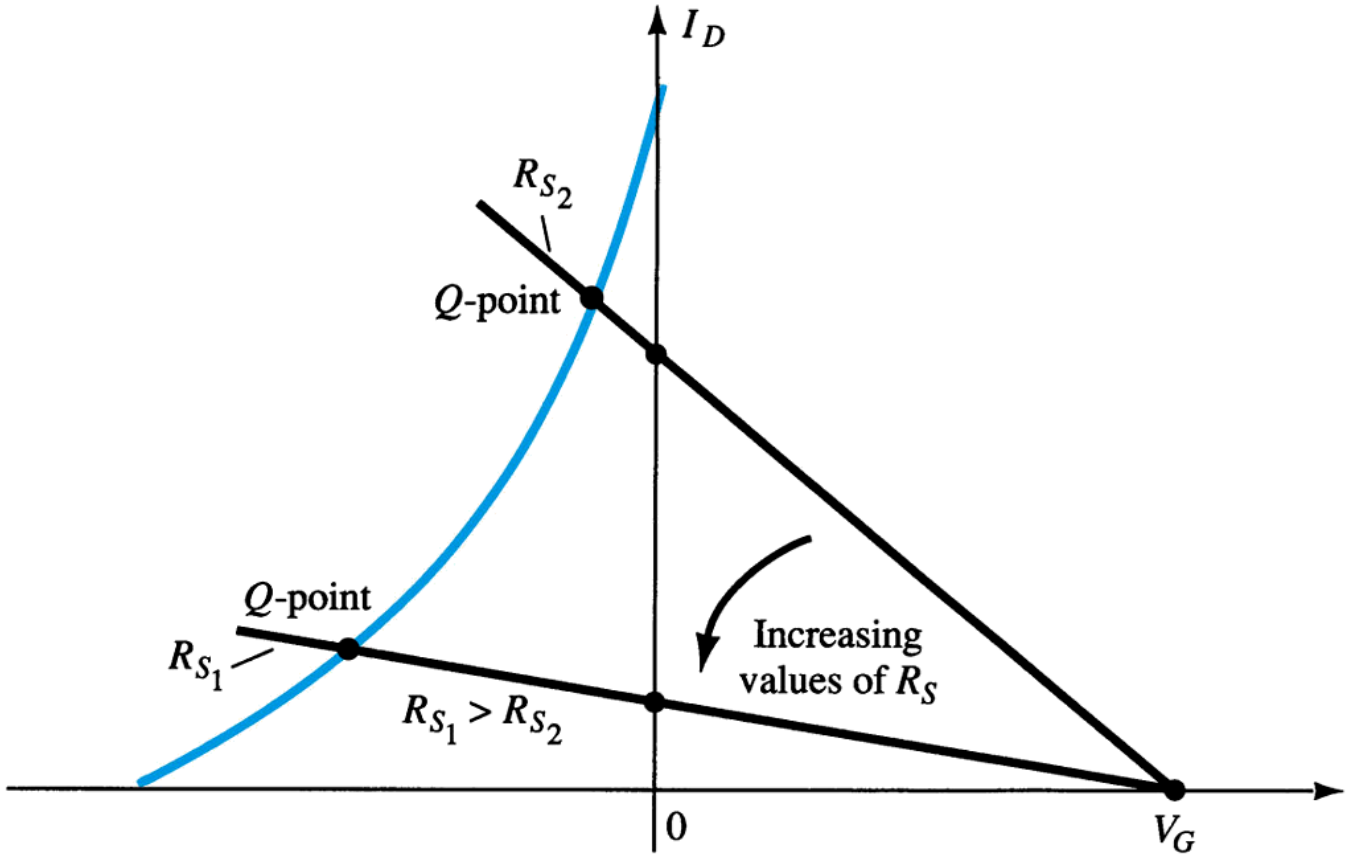
- Output loop:

$$V_{DS} = V_{DD} - I_D(R_D + I_D R_S)$$

$$V_D = V_{DD} - I_D R_D$$

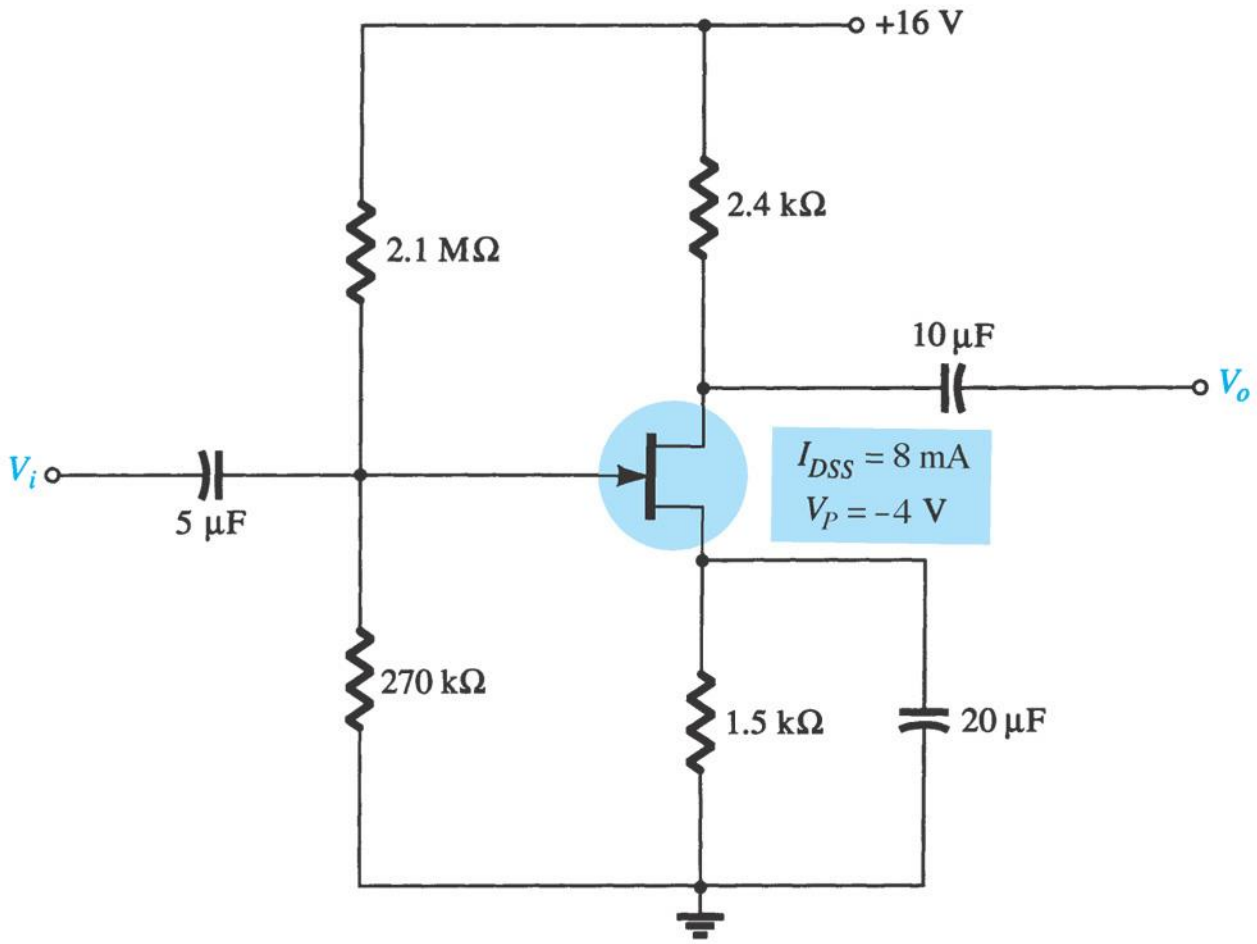
$$V_S = I_D R_S$$

Effect of increasing values of R_S

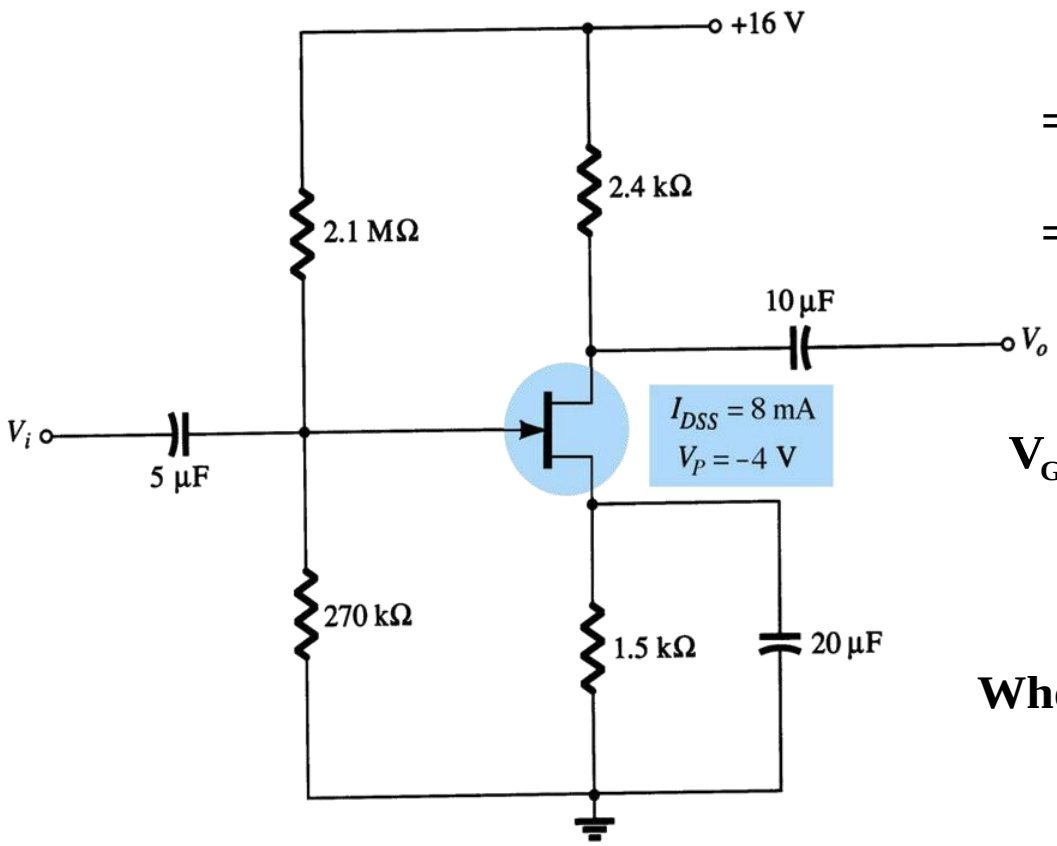


Example

- Determine I_{DQ}, V_{GSQ}, V_D, V_S, V_{DS} and V_{DG} .



Solutions



$$V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$

$$= \frac{(270k\Omega)(16V)}{2.1M\Omega + 0.27M\Omega_2} V_{DD}$$

$$= 1.82V$$

$$V_{GS} = V_G - I_D R_S$$

$$= 1.82V - I_D (1.5k\Omega)$$

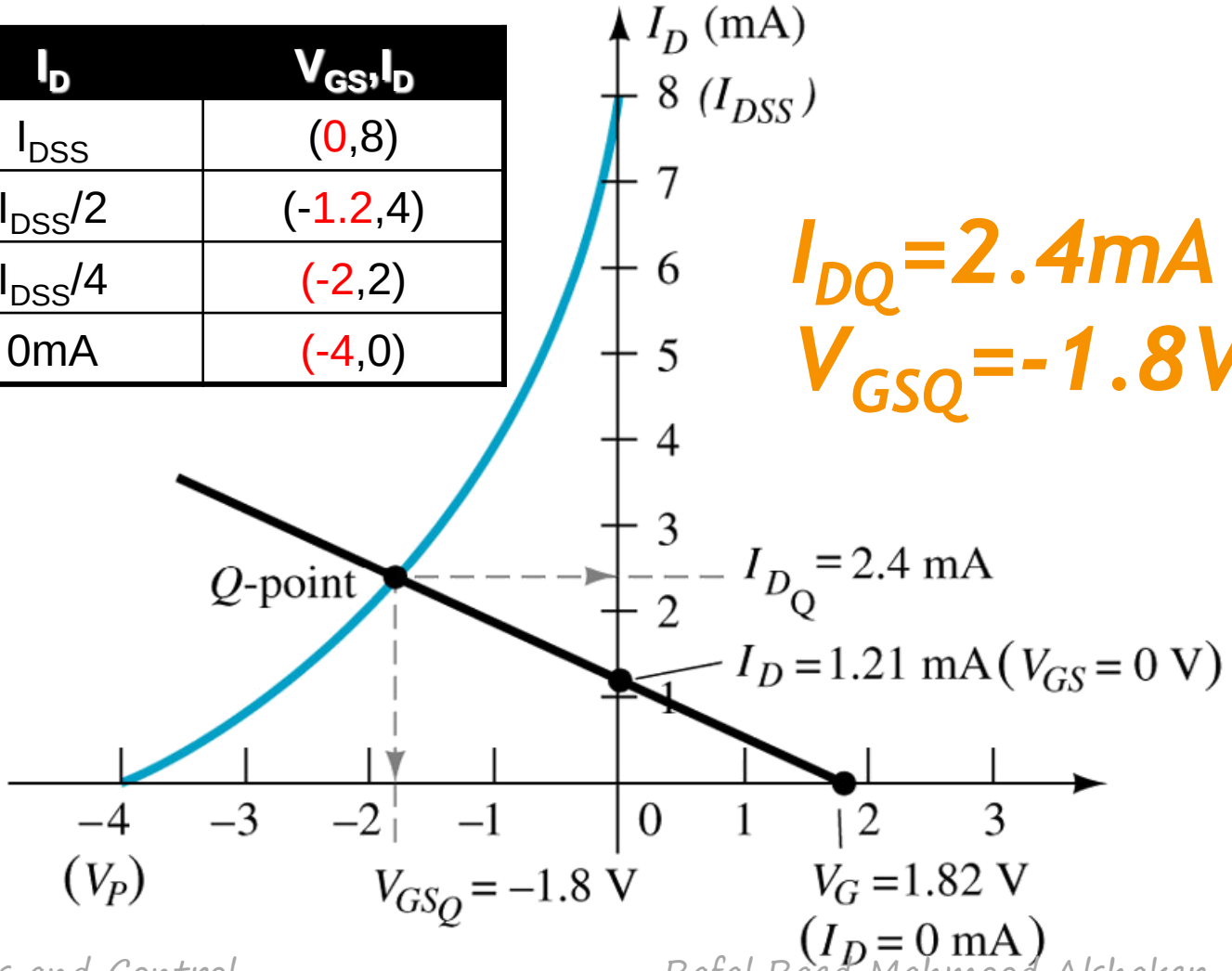
When $I_D = 0mA$, $V_{GS} = +1.82V$

When $V_{GS} = 0V$, $I_D = \frac{+1.82V}{1.5k\Omega} = 1.21mA$

Determining the *Q*-point for the network

$$V_{GS} = 1.82V - I_D\,(1.5k\Omega)$$

V_{GS}	I_D	V_{GS},I_D
0	I_{DSS}	(0,8)
$0.3V_P$	$I_{DSS}/2$	(-1.2,4)
$0.5V_P$	$I_{DSS}/4$	(-2,2)
V_P	0mA	(-4,0)



$I_{DQ}=2.4mA$

$V_{GSQ}=-1.8V$

b. $V_D = V_{DD} - I_D R_D$

$= 16\,\text{V} - (2.4\,\text{mA})(2.4\,\text{k}\Omega)$

$= \mathbf{10.24\,V}$

c. $V_S = I_D R_S = (2.4\,\text{mA})(1.5\,\text{k}\Omega)$

$= \mathbf{3.6\,V}$

d. $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 16\,\text{V} - (2.4\,\text{mA})(2.4\,\text{k}\Omega + 1.5\,\text{k}\Omega)$

$= \mathbf{6.64\,V}$

or $V_{DS} = V_D - V_S = 10.24\,\text{V} - 3.6\,\text{V}$

$= \mathbf{6.64\,V}$

Mathematical solutions

- How to get I_{DS}, V_{GS} and V_{DS} for voltage-divider bias configuration by using mathematical solutions?

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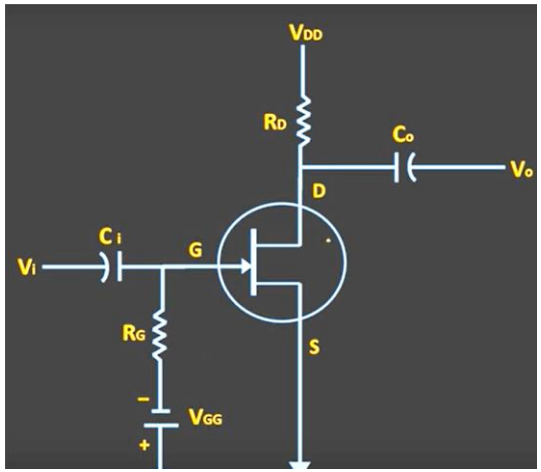
Electronic I I
Lecture 3 part 1

Field Effect Transistor (FET) Biasing



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EXAMPLE: The datasheet for a 2N7002 E-MOSFET gives $I_{D(on)}$=500mA (minimum) at V_{GS}=10V and $V_{GS(th)}$=1V. Determine the drain current for V_{GS}= 5 V.

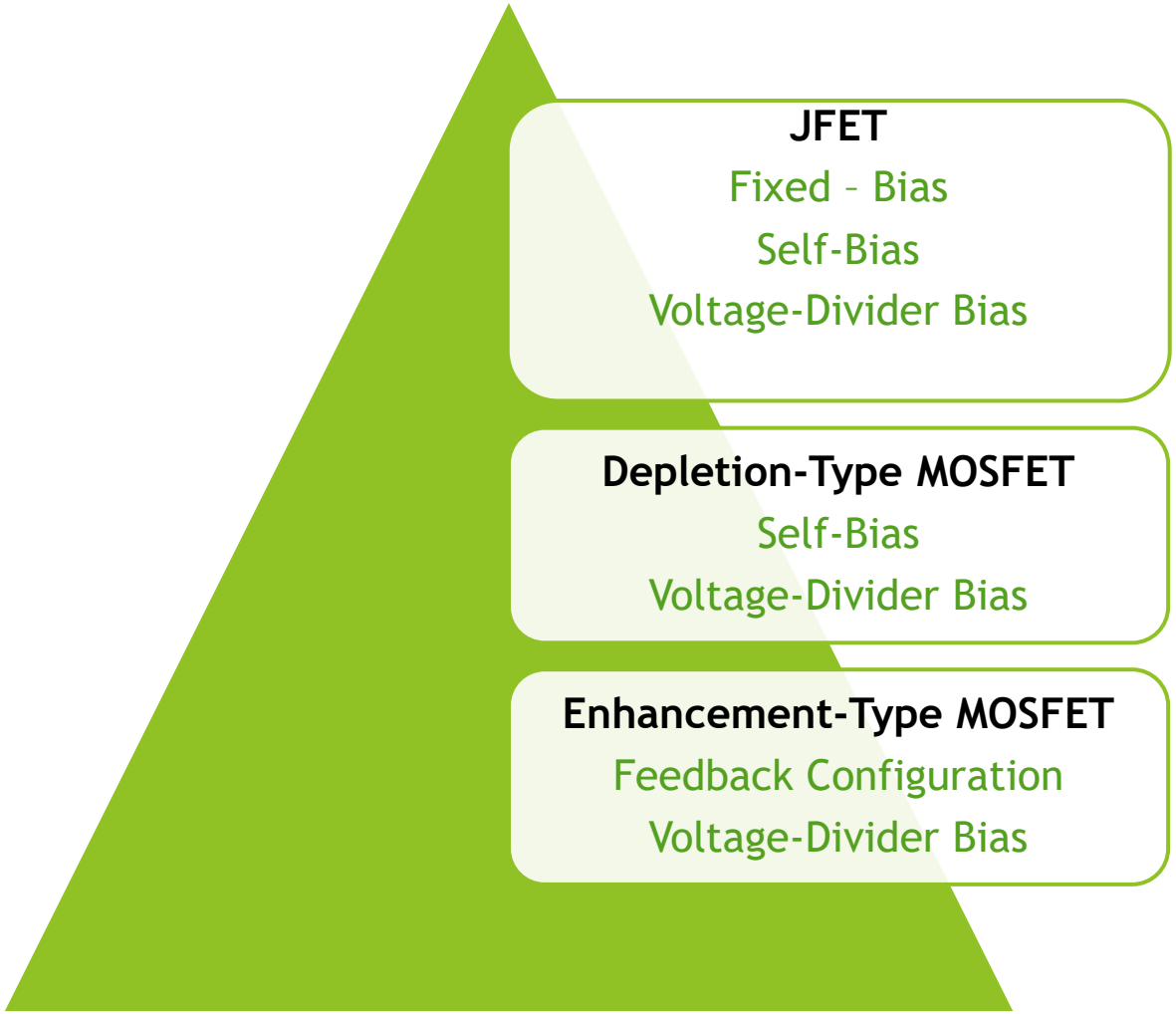
Solution:

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{500\text{ mA}}{(10\text{ V} - 1\text{ V})^2} = \frac{500\text{ mA}}{81\text{ V}^2} = 6.17\text{ mA/V}^2$$

Next, using the value of K, calculate I_D for $V_{GS} = 5$ V.

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (6.17\text{ mA/V}^2)(5\text{ V} - 1\text{ V})^2 = \mathbf{98.7\text{ mA}}$$

Common FET Biasing Circuits



Common FET Biasing Circuits

Common FET Biasing Circuits

- JFET
  - Fixed – Bias
  - Self-Bias
  - Voltage-Divider Bias

- Depletion-Type MOSFET
  - Self-Bias
  - Voltage-Divider Bias

- Enhancement-Type MOSFET
  - Feedback Configuration
  - Voltage-Divider Bias

General Relationships

- For all FETs:

$$I_G \approx 0A$$

$$I_D = I_S$$

- For JFETs and Depletion-Type MOSFETs:

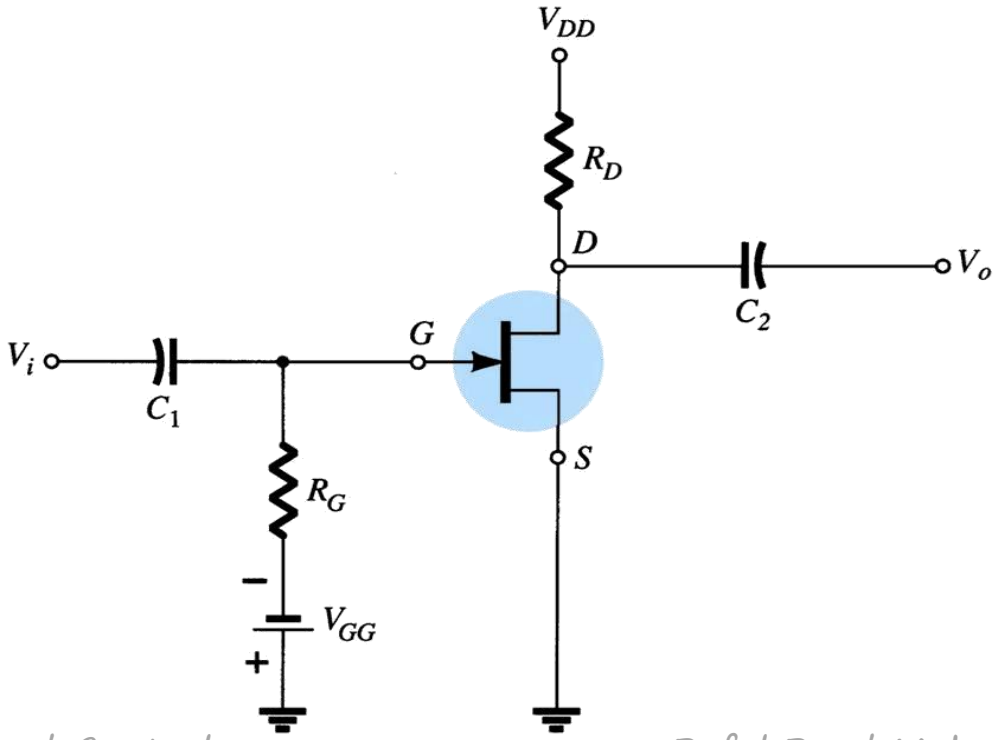
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

- For Enhancement-Type MOSFETs:

$$I_D = k(V_{GS} - V_T)^2$$

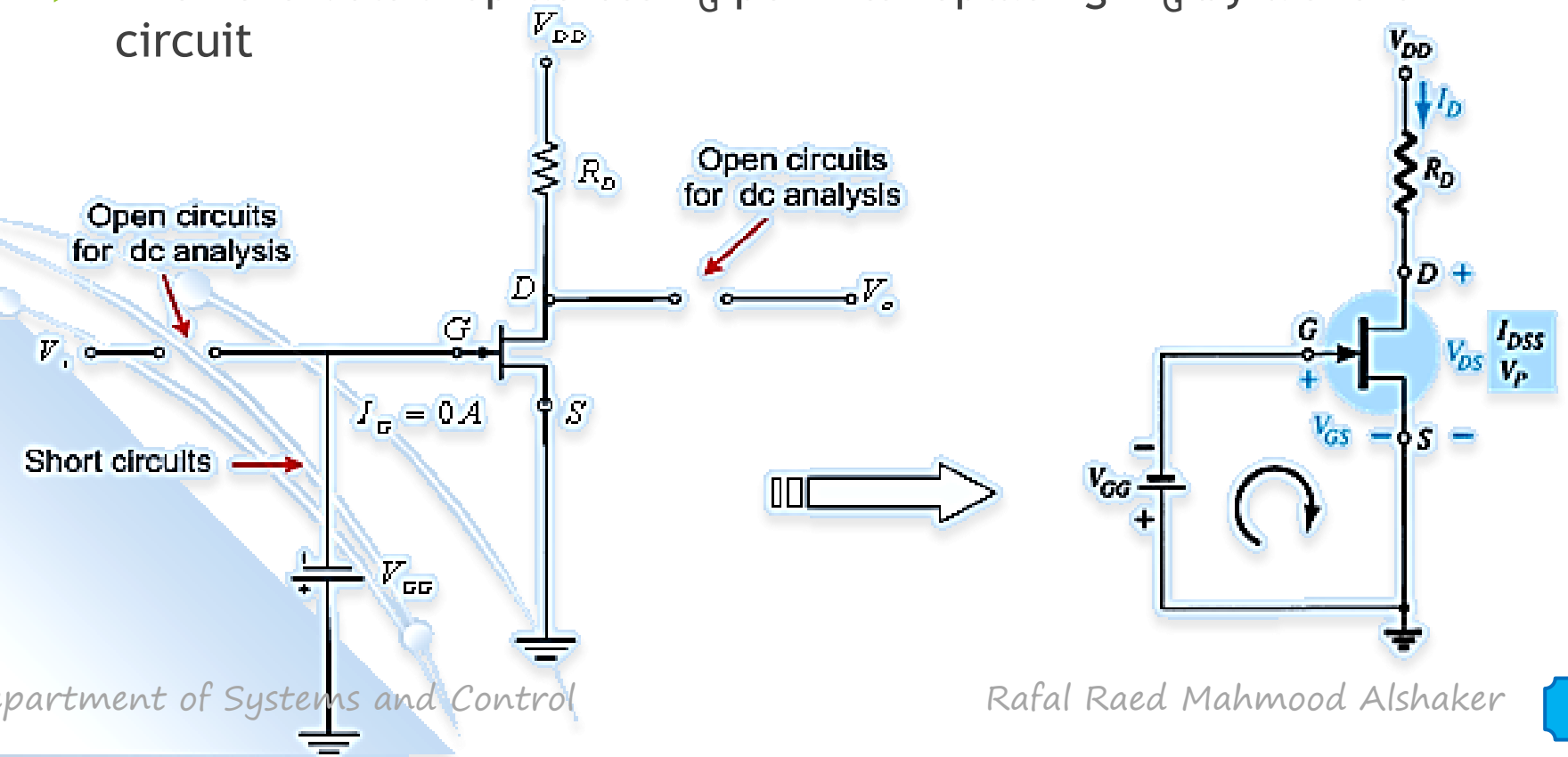
Fixed-Bias Configuration

- The configuration includes the ac levels Vi and Vo and the coupling capacitors.
- The resistor is present to ensure that Vi appears at the input to the FET amplifier for the AC analysis.



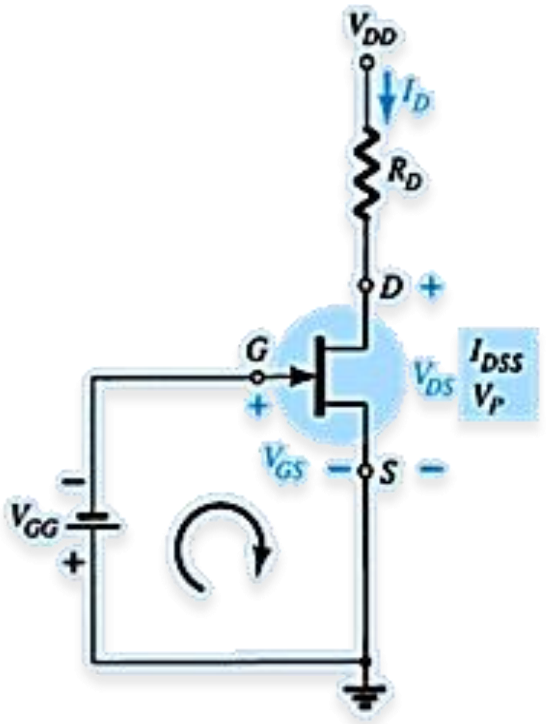
Fixed-Bias Configuration

- For the **DC analysis**,
  - Capacitors are open circuits
  - $I_G \cong 0A$ and $V_{RG} = I_G R_G = (0A)R_G = 0V$
- The zero-volt drop across R_G permits replacing R_G by a short-circuit



Fixed-Bias Configuration

1. Mathematical approach



Investigating the input loop

- I_G=0A, therefore

  $V_{RG}=I_G R_G=0V$

- Applying KVL for the input loop,

  $-V_{GG}-V_{GS}=0$

  $V_{GG}=-V_{GS}=-V_{GSQ}$

- It is called *fixed-bias configuration* due to V_{GG} is a fixed power supply so V_{GS} is fixed

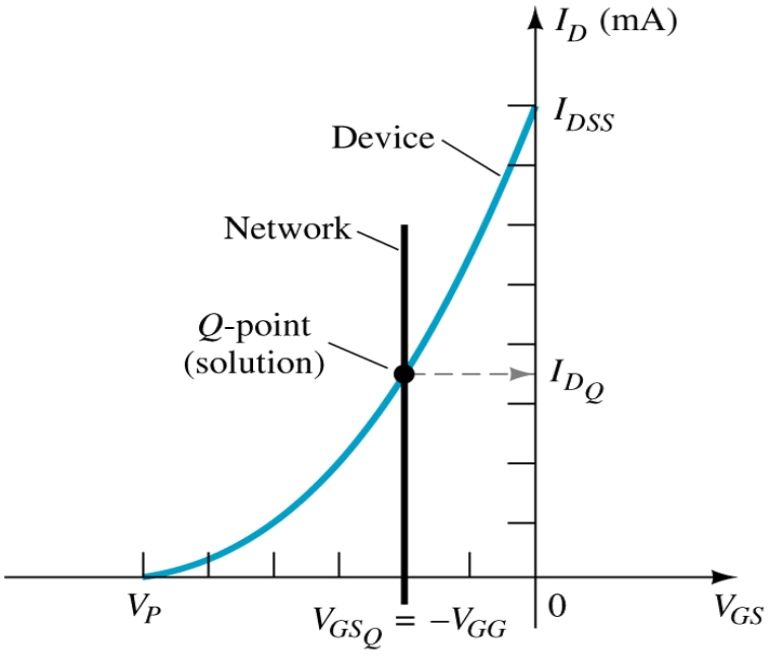
- The resulting current, $$I_D = I_{DSS}(1-\frac{V_{GS}}{V_P})^2$$

Fixed-Bias Configuration

2.Graphical Approach

- Using below table, Investigate the graphical approach. then draw the graph

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0mA



Fixed-Bias Configuration

2.Graphical Approach

- The fixed level of V_{GS} has been superimposed as a vertical line at $V_{GS} = -V_{GG}$
- At any point on the vertical line, the level of V_G is $-V_{GG}$--- the level of I_D must simply be determined on this vertical line.
- The point where the two curves intersect is the common solution to the configuration – commonly referred to as the **quiescent** or operating point.
- The quiescent level of I_D is determined by drawing a horizontal line from the Q-point to the vertical I_D axis.

- Output loop

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_S = 0V$$

$$V_{DS} = V_D - V_S$$

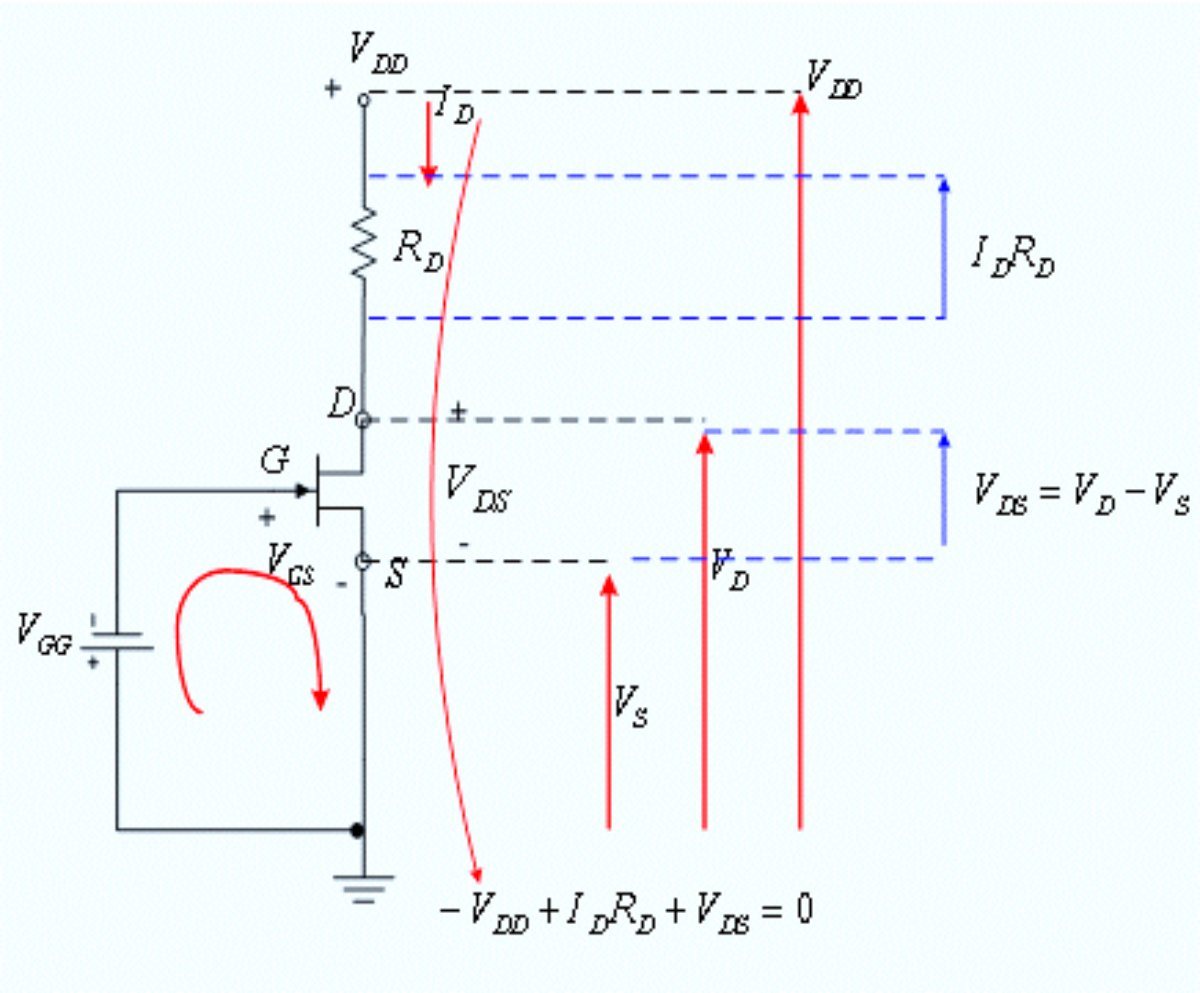
$$V_D = V_{DS} + V_S \qquad V_S = 0$$

$$V_D = V_{DS}$$

$$V_{GS} = V_G - V_S$$

$$V_G = V_{GS} + V_S \qquad V_S = 0$$

$$V_G = V_{GS}$$



Example

Determine the following for the network of Fig.

a. V_{GSQ}.

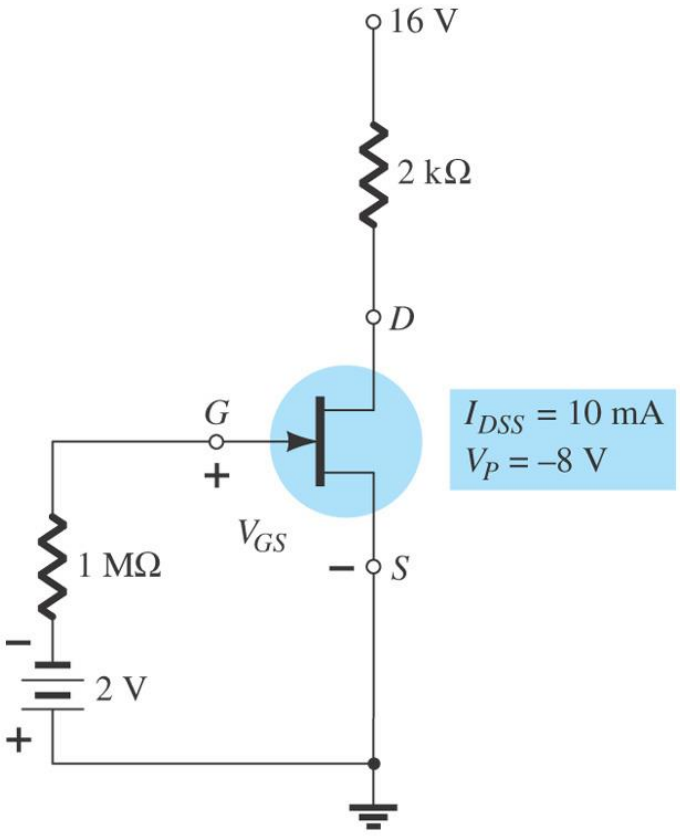
b. I_{DQ}.

c. V_{DS}.

d. V_D.

e. V_G.

f. V_S.



Solution:

Mathematical Approach

a. $V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$

b. $I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\ \text{mA}\left(1 - \frac{-2\ \text{V}}{-8\ \text{V}}\right)^2$

$= 10\ \text{mA}(1 - 0.25)^2 = 10\ \text{mA}(0.75)^2 = 10\ \text{mA}(0.5625)$

$= \mathbf{5.625\ mA}$

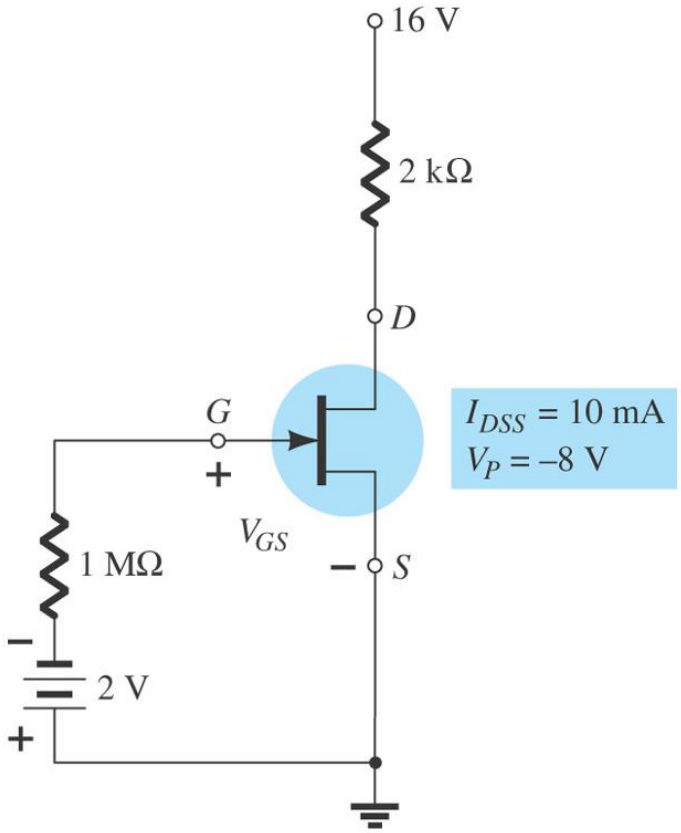
c. $V_{DS} = V_{DD} - I_D R_D = 16\ \text{V} - (5.625\ \text{mA})(2\ \text{k}\Omega)$

$= 16\ \text{V} - 11.25\ \text{V} = \mathbf{4.75\ V}$

d. $V_D = V_{DS} = \mathbf{4.75\ V}$

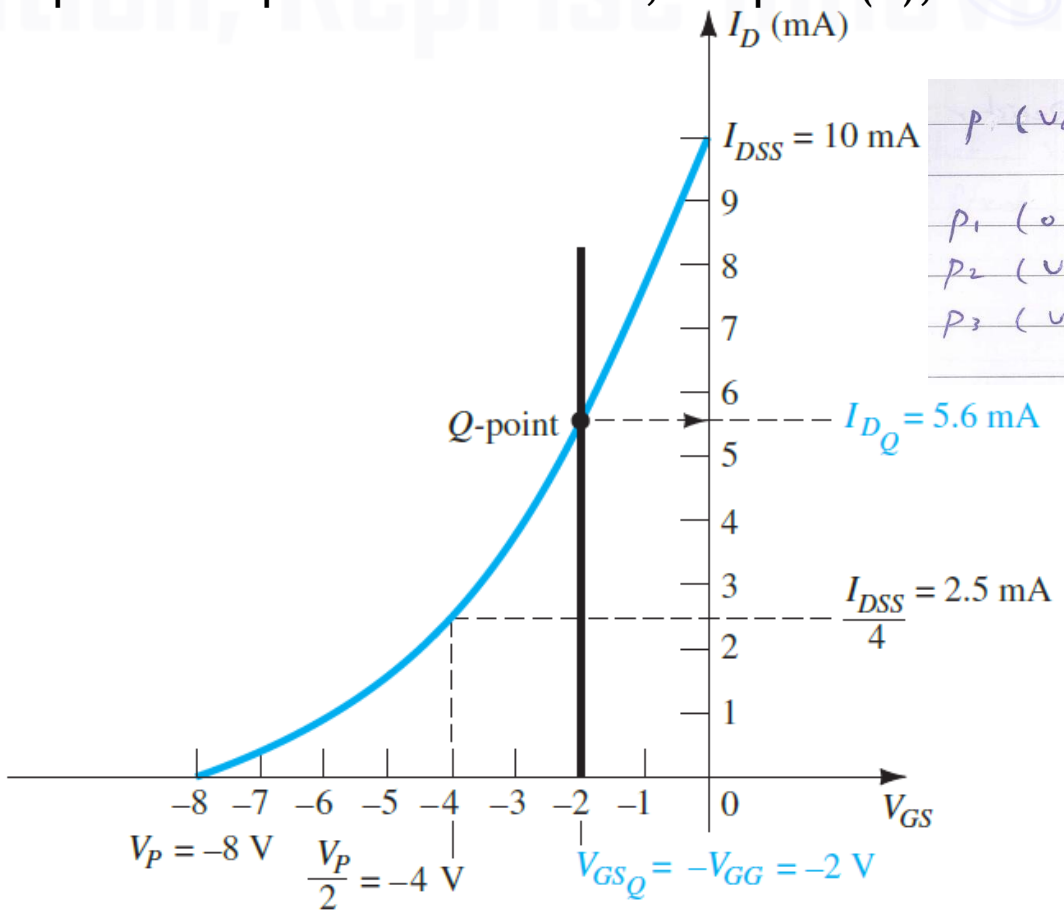
e. $V_G = V_{GS} = \mathbf{-2\ V}$

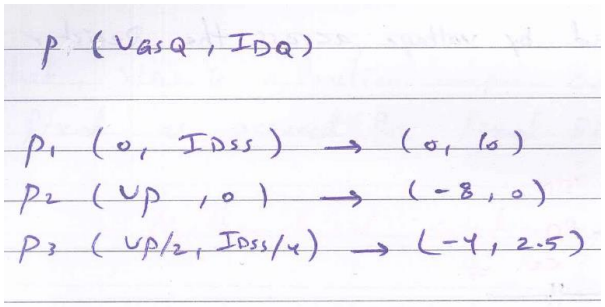
f. $V_S = \mathbf{0\ V}$



Graphical approach

The resulting Shockley curve and the vertical line at VGS=- 2 V are provided in Fig. below It is certainly difficult to read beyond the second place without significantly increasing the size of the figure, but a solution of 5.6 mA from the graph of Fig. is quite acceptable. Therefore, for part (a),





a. Therefore,

$$V_{GS_Q} = -V_{GG} = \mathbf{-2\,V}$$

b. $I_{D_Q} = \mathbf{5.6\,mA}$

c. $V_{DS} = V_{DD} - I_D R_D = 16\,\text{V} - (5.6\,\text{mA})(2\,\text{k}\Omega)$
$= 16\,\text{V} - 11.2\,\text{V} = \mathbf{4.8\,V}$

d. $V_D = V_{DS} = \mathbf{4.8\,V}$

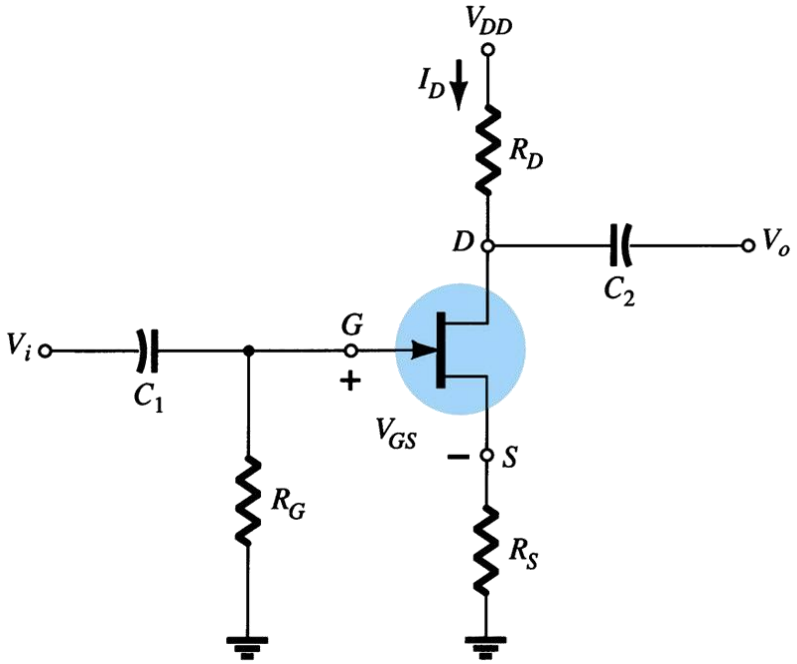
e. $V_G = V_{GS} = \mathbf{-2\,V}$

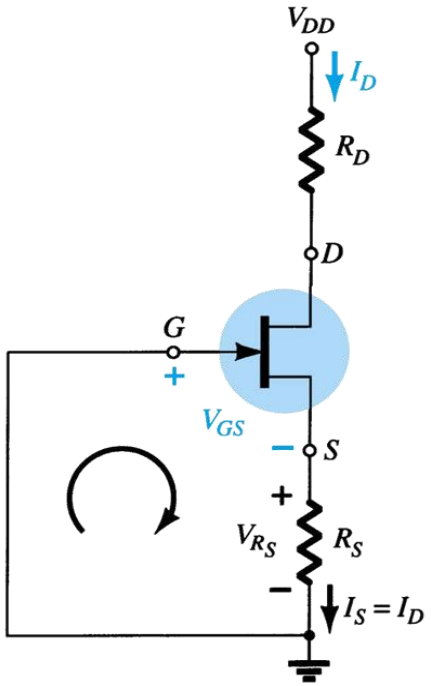
f. $V_S = \mathbf{0\,V}$

The results clearly confirm the fact that the mathematical and graphical approaches generate solutions that are quite close.

Self Bias Configuration

- The self-bias configuration eliminates the need for two dc supplies.
- The controlling V_{GS} is now determined by the voltage across the resistor R_S
- the capacitors should be replaced by “open circuits” and The resistor R_G should be replaced by a short-circuit equivalent since I_G =0 A.





- For the indicated input loop:

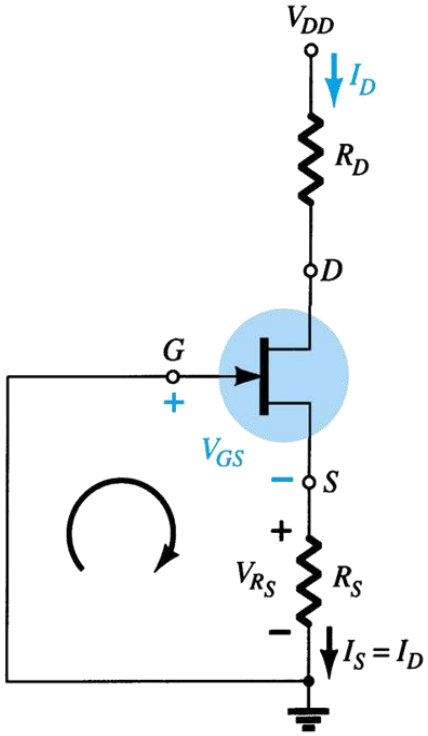
$$V_{GS} = -I_D R_S$$

- Mathematical approach:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1 - \frac{I_D R_S}{V_P}\right)^2$$

  - rearrange and solve.



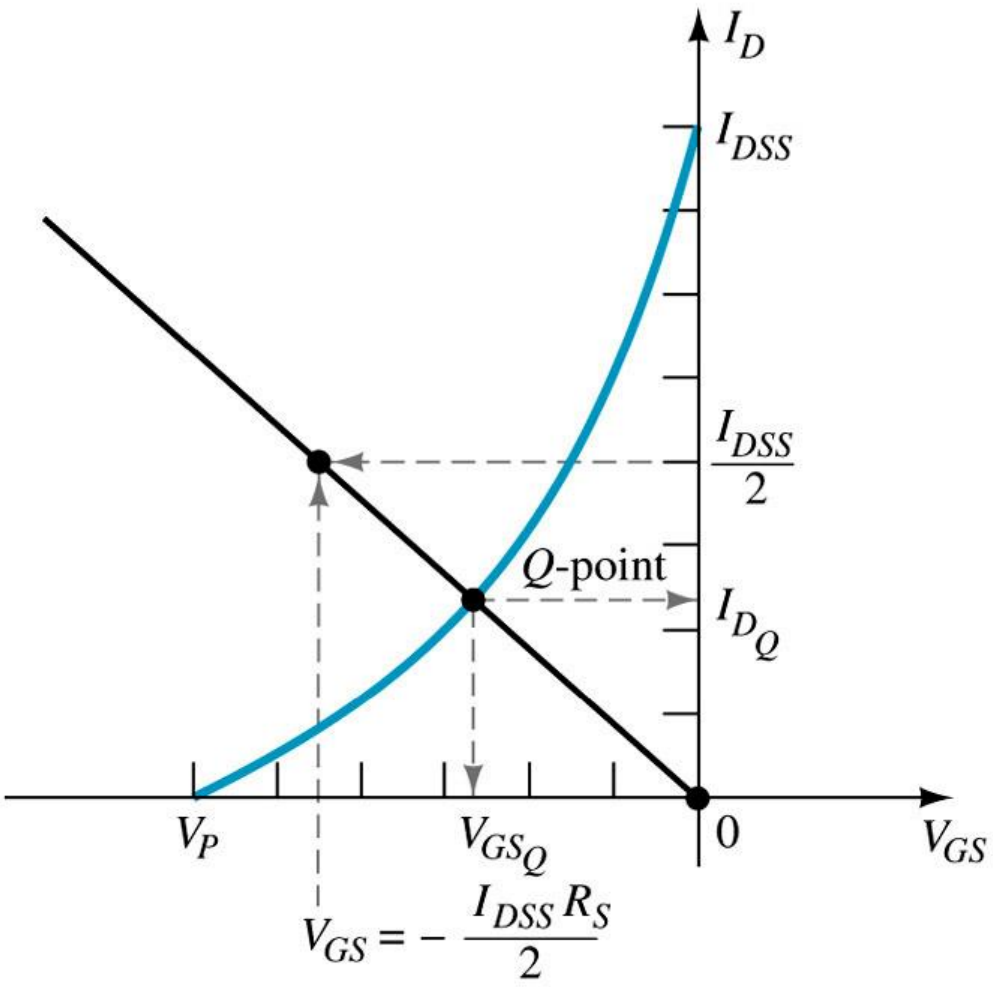
Graphical approach

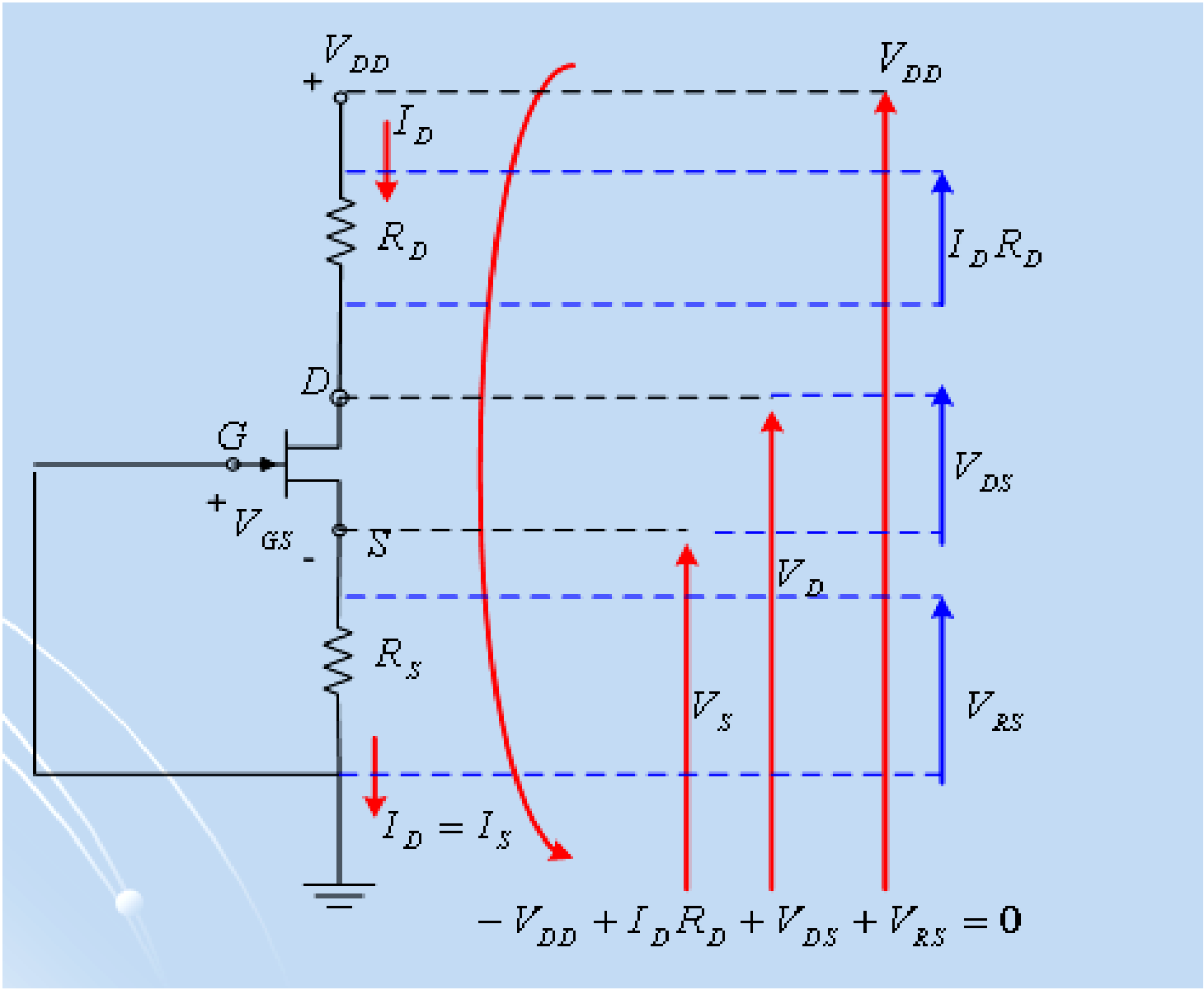
- Draw the device transfer characteristic
- Draw the network load line
  - Use $V_{GS} = -I_D R_S$ to draw straight line.
  - First point, $I_D = 0, \quad V_{GS} = 0$
  - Second point, any point from $I_D = 0$ to $I_D = I_{DSS}$. Choose

$$I_D = \frac{I_{DSS}}{2} \; then$$

$$V_{GS} = -\frac{I_{DSS} R_S}{2}$$

- the quiescent point obtained at the intersection of the straight line plot and the device characteristic curve.
- The quiescent value for I_D and V_{GS} can then be determined and used to find the other quantities of interest.


I_D
I_{DSS}
$\frac{I_{DSS}}{2}$
Q-point
I_{D_Q}
V_P
V_{GS_Q}
0
V_{GS}
$V_{GS} = -\frac{I_{DSS} R_S}{2}$

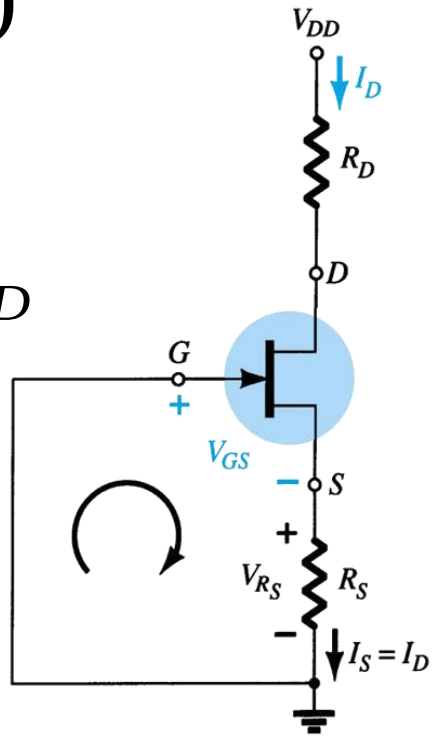

V_{DD}
I_D
R_D
D
G
V_{GS}
S
R_S
$I_D = I_S$
V_{DD}
$I_D R_D$
V_{DS}
V_D
V_S
V_{RS}
$-V_{DD} + I_D R_D + V_{DS} + V_{RS} = 0$

- **For output loop**
  - Apply KVL of output loop
  - Use $I_D = I_S$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

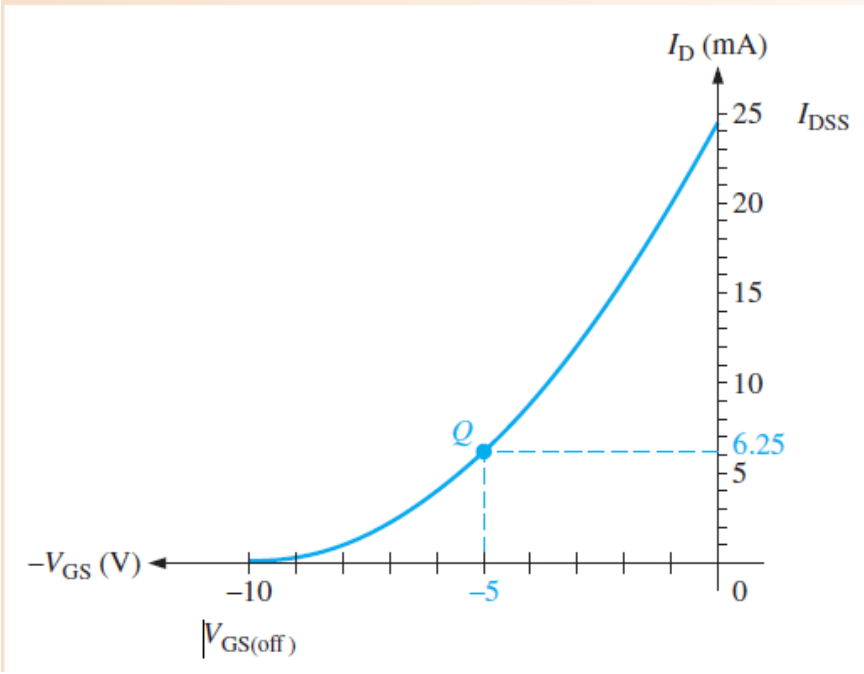
$$V_S = I_D R_S$$

$$V_D = V_{DS} + V_S = V_{DD} - V_{RD}$$



EXAMPLE:

Determine the value of R_S required to self-bias an *n*-channel JFET that has the transfer characteristic curve shown in Figure below at V_{GS} = -5 V.



Solution From the graph, $I_D = 6.25$ mA when $V_{GS} = -5$ V. Calculate R_S.

$$R_S = \left|\frac{V_{GS}}{I_D}\right| = \frac{5\text{ V}}{6.25\text{ mA}} = \mathbf{800\ \Omega}$$

EXAMPLE:

Determine the following for the network of Figure below

a. V_{GSQ}.

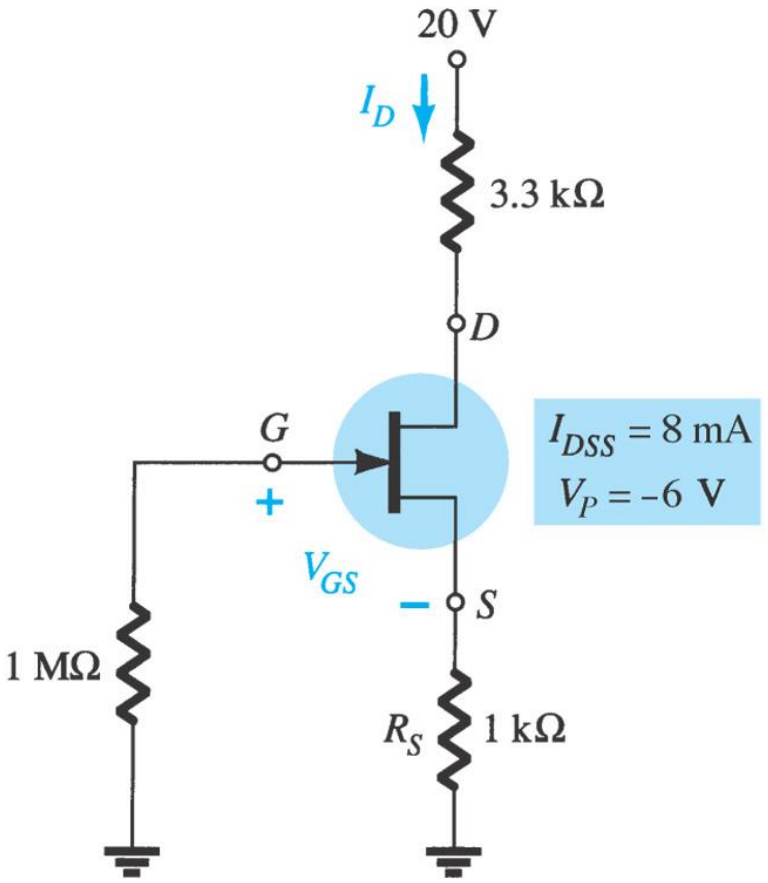
b. I_{DQ}.

c. V_{DS}.

d. V_D.

e. V_G.

f. V_S.

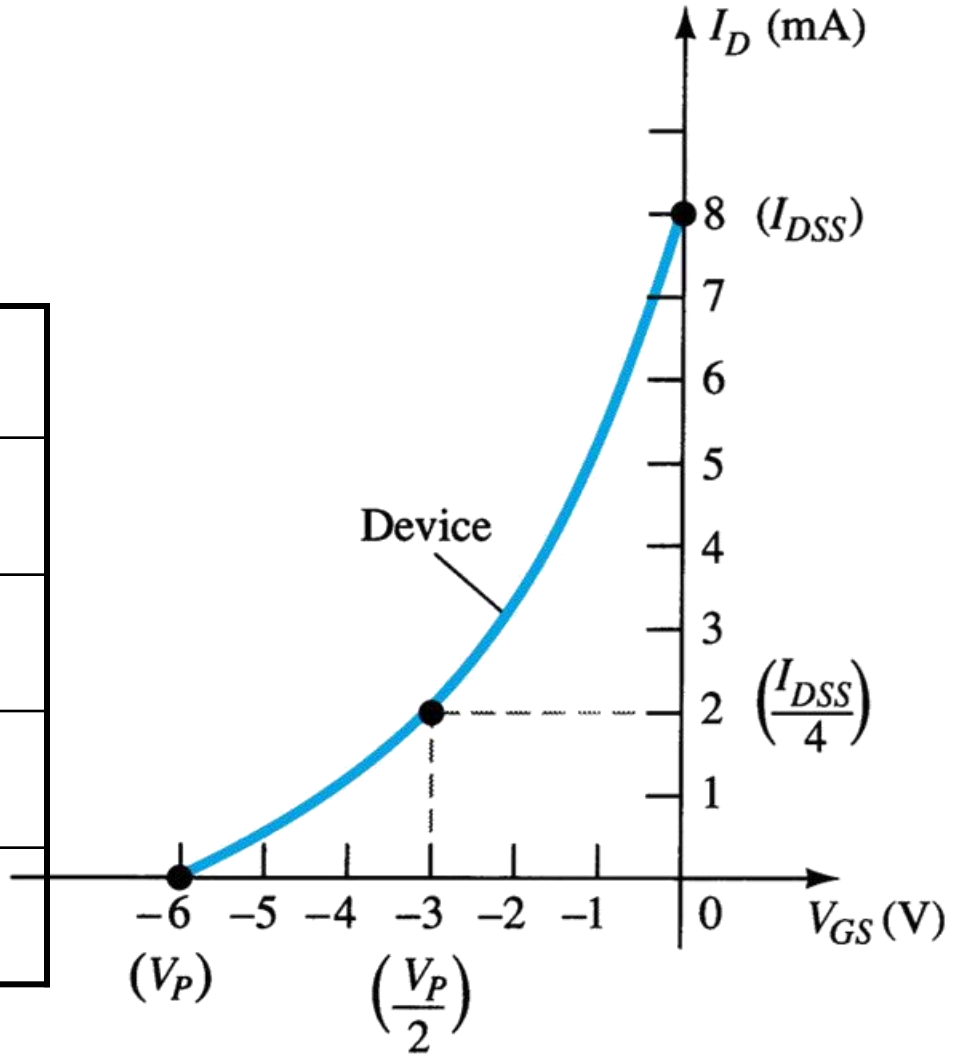


Graphical Solutions:

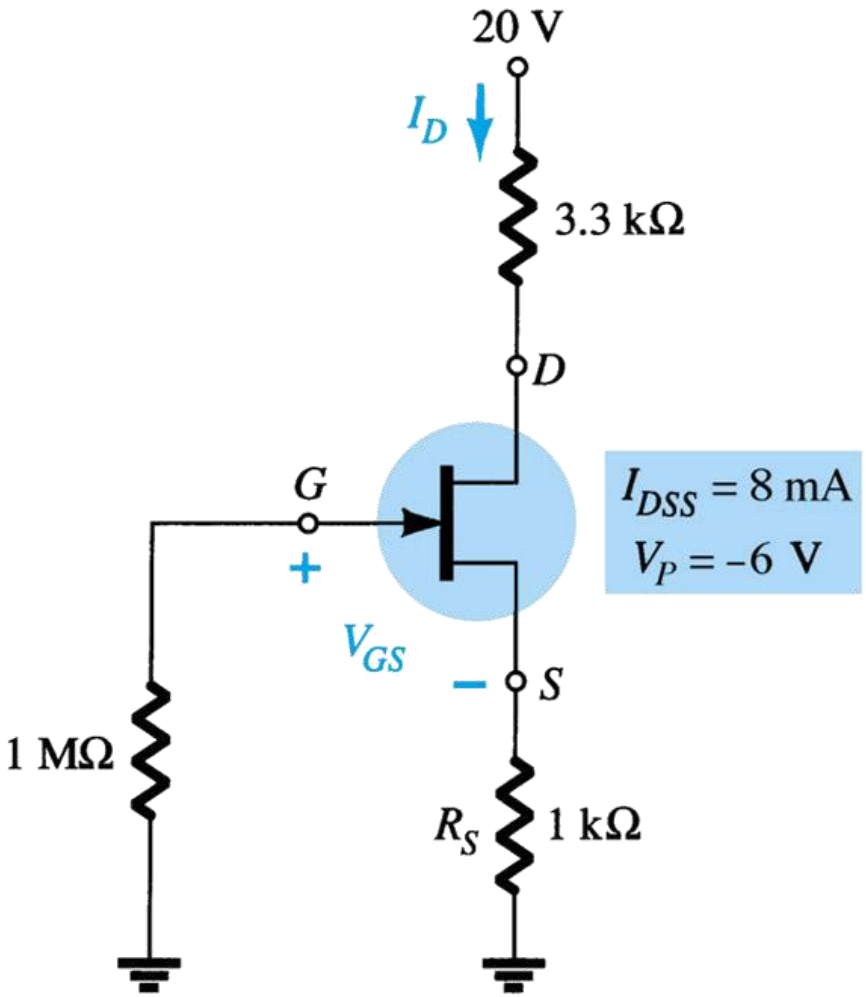
Sketching the transfer characteristics curve

$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$$

V_{GS}	I_D
0	I_{DSS}
0.3Vp	$I_{DSS}/2$
0.5Vp	$I_{DSS}/4$
Vp	0 mA



Graphical Solutions:



$$V_{GS} = -I_D R_s$$

When $I_D = 4mA$,

$$V_{GS} = -I_D R_s$$

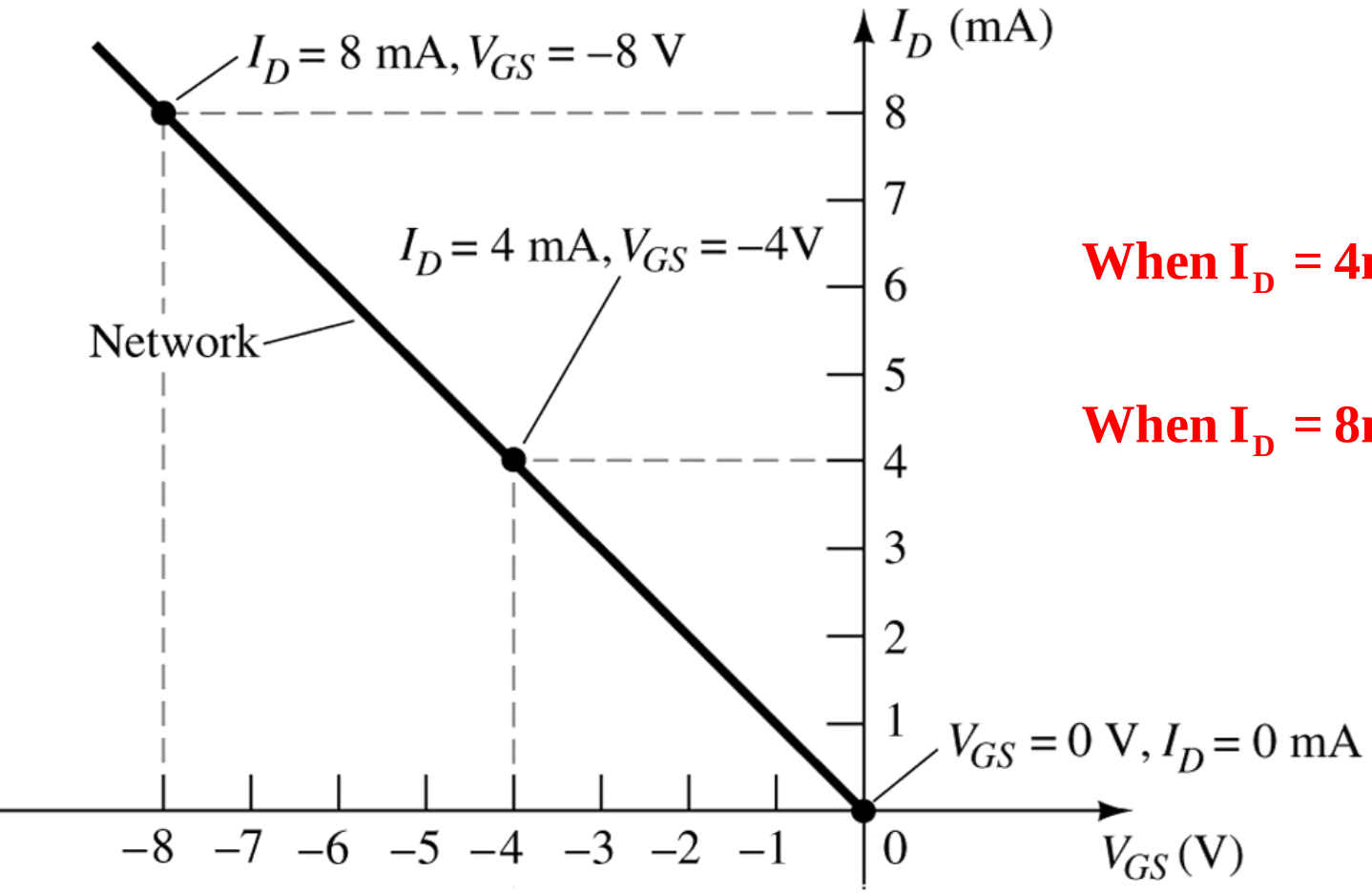
$$= -(4mA)(1k\Omega) = -4V$$

When $I_D = 8mA$, $V_{GS} = -I_D R_s$

$$V_{GS} = -I_D R_s$$

$$= -8 \quad mA \quad (1k\Omega) = -8V$$

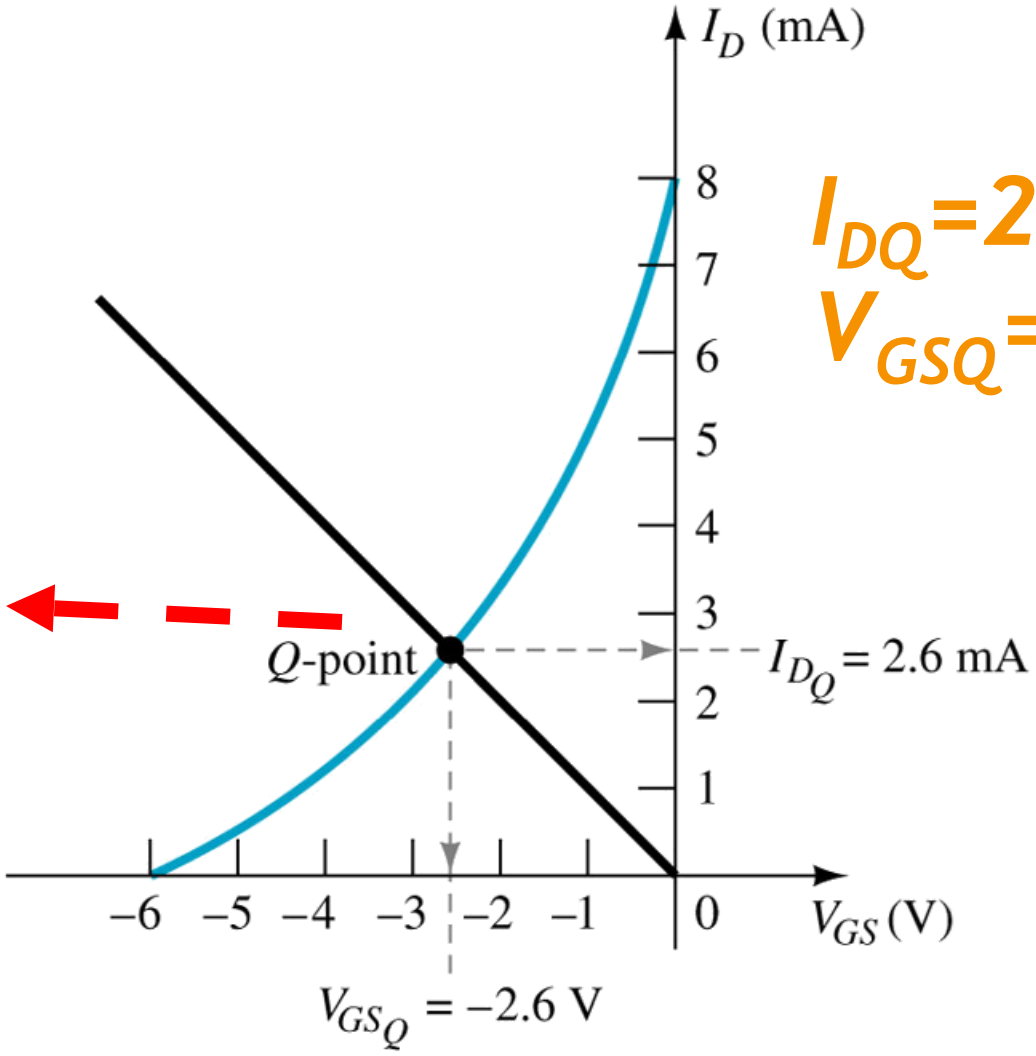
Sketching the self-bias line



When I_D = 4mA, V_{GS} = - 4V

When I_D = 8mA, V_{GS} = - 8V

Graphical Solutions: Determining the Q-point



Q-point

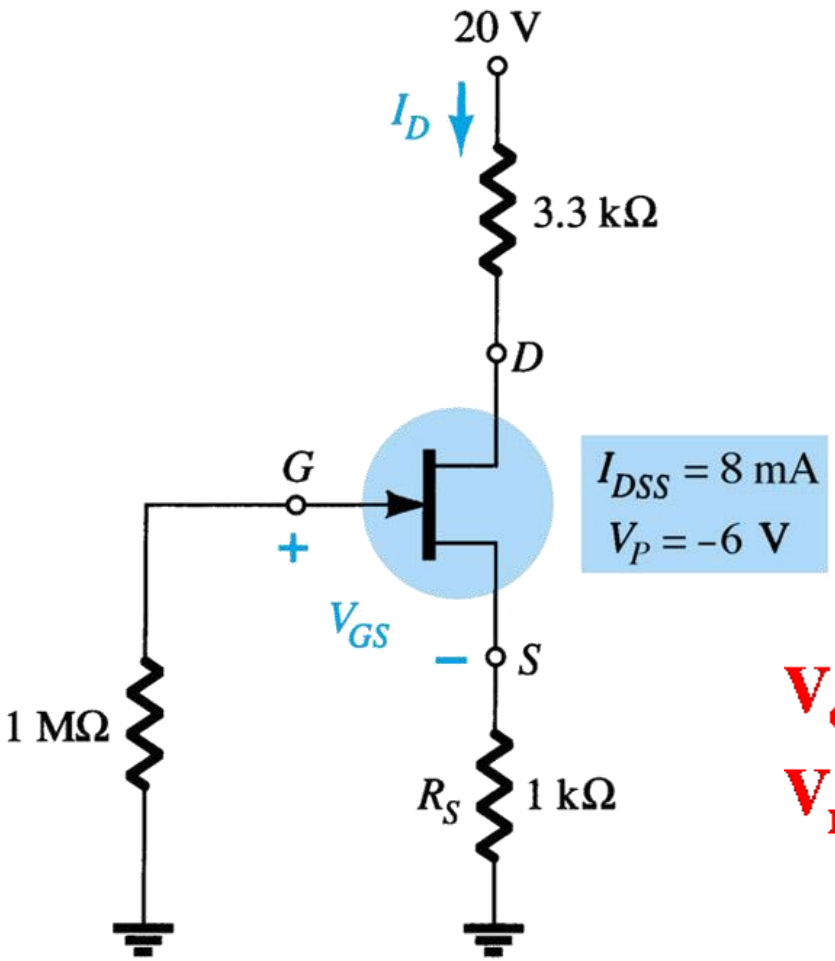
I_{DQ}=2.6mA

V_{GSQ}=-2.6mV

Solutions

$V_{GSQ} = -2.6V$

$I_{DQ} = 2.6mA$



$I_D = I_S$

$V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 20V - 2.6mA(4.3k\Omega)$

$= 8.82V$

$V_s = I_s R_s = (2.6mA)(1k\Omega)$

$= 2.6V$

$V_G = V_{GS} + V_s = 0V$

$V_D = V_{DS} + V_s$ or $V_D = V_{DD} - I_D R_D$

$= V_{DS} + V_s = 8.82V + 2.6V = 11.42V$

Mathematical Solutions

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 \qquad recall \;\; V_{GS} = -I_D R_S$$

$$= I_{DSS}\left(1-\frac{(-I_D R_S)}{V_P}\right)^2$$

$$I_D = 8m\left(1+\frac{I_D(1k)}{-6}\right)^2 = 8m\left(\frac{-6+I_D(1k)}{-6}\right)^2$$

$$= \frac{8m}{36}\left(36-6kI_D-6kI_D+1MI_D{}^2\right)$$

$$36I_D = 0.288-96I_D+8kI_D{}^2$$

$$8kI_D{}^2-132I_D+0.288=0$$

$$I_{D_1} = 13.9mA \qquad I_{D_{21}} = 2.588mA$$

$$V_{GS} = -I_D R_S \qquad V_{GS} = -I_D R_S$$

$$= -13.9mA(1k) \qquad = -2.588mA(1k)$$

$$= -13.9V \qquad = -2.6V$$

$$therefore, \;\; choose \; I_D = 2.588mA \;\; and \;\; V_{GS} = -2.6V$$

Home Work

- Determine the value of R_S required to self-bias a *p*-channel JFET with datasheet values of I_{DSS} =25 mA and V_{GS} (off) = 15 V. V_{GS} is to be 5 V.

Ninevah University
College of Electronics Engineering
Department of Systems and Control

Electronic I I
Lecture 4

Field Effect Transistor (FET) Biasing

by
Rafal Raed Mahmood Alshaker

2nd Class

Depletion-Type MOSFETs

The DC Analysis

- **Same as the FET calculations**
  - Plotting the transfer characteristics of the device
  - Plotting the at a point that V_{GS} exceeds the 0V or more positive values
  - Plotting point when V_{GS}=0V and I_D=0A
  - The intersection between Shockley characteristics and linear characteristics defined the Q-point of the MOSFET

- **The problem is that how long does the transfer characteristics have to be draw?**
  - We have to analyze the input loop parameter relationship.
  - As R_S become smaller, the linear characteristics will be in narrow slope therefore needs to consider the extend of transfer characteristics for example of voltage divider MOSFET,

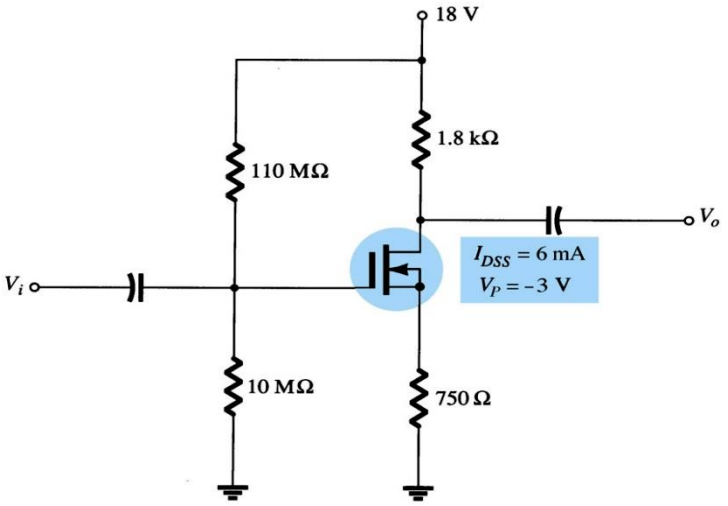
$$V_G - V_{GS} - V_{RS} = 0$$

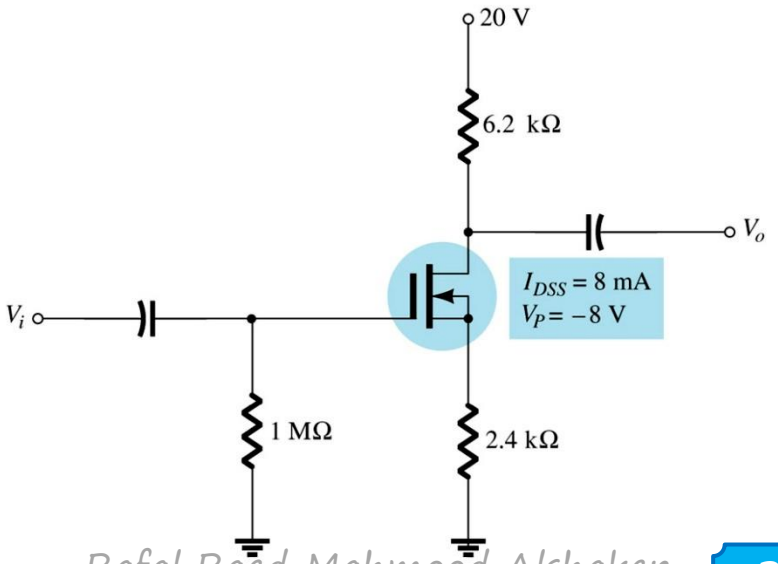
$$V_{GS} = V_G - I_D R_S$$

  - The bigger values of V_P the more positive values we should draw for the transfer characteristics

Analyzing the MOSFET circuit for DC analysis

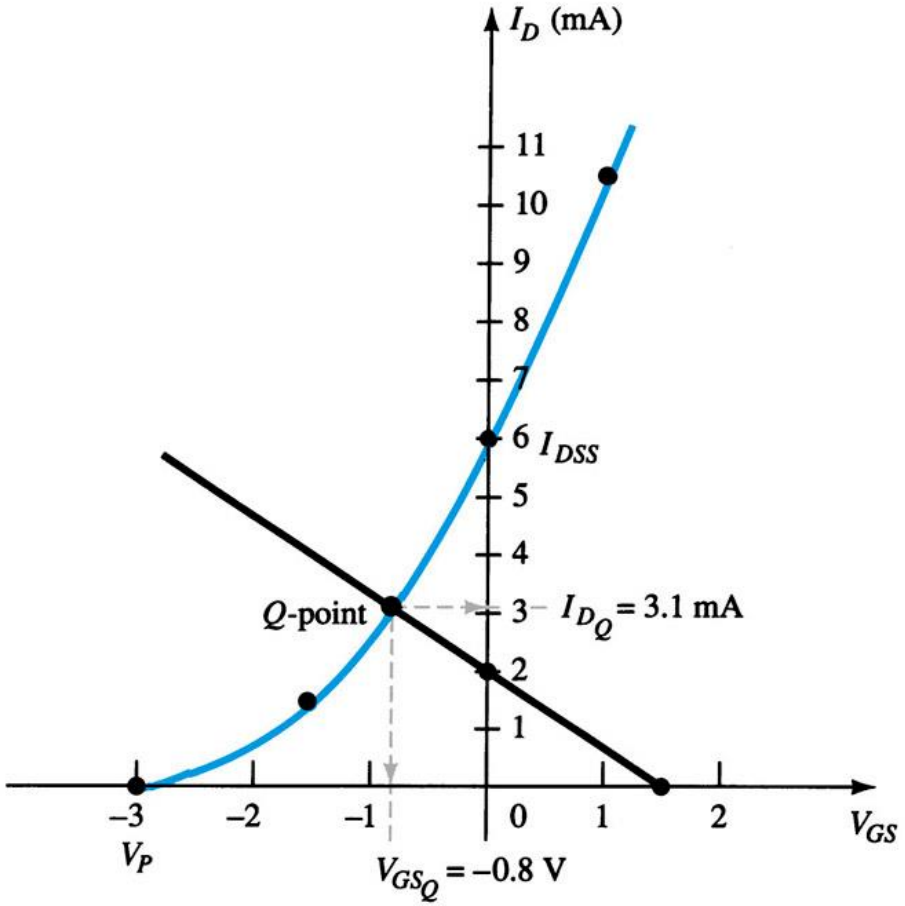
- How to analyze dc analysis for the shown network?
  - It is a …. Type network
  - Find V_G or V_{GS}
  - Draw the linear characteristics
  - Draw the transfer characteristics
  - Obtain V_{GSQ} and I_{DQ} from the graph intersection





1. Plot line for $V_{GS} = V_G$, $I_D = 0$ and $I_D = V_G/R_S$, $V_{GS} = 0$
2. Plot the transfer curve by plotting I_{DSS}, V_P and calculated values of I_D.
3. Where the line intersects the transfer curve is the Q-point.

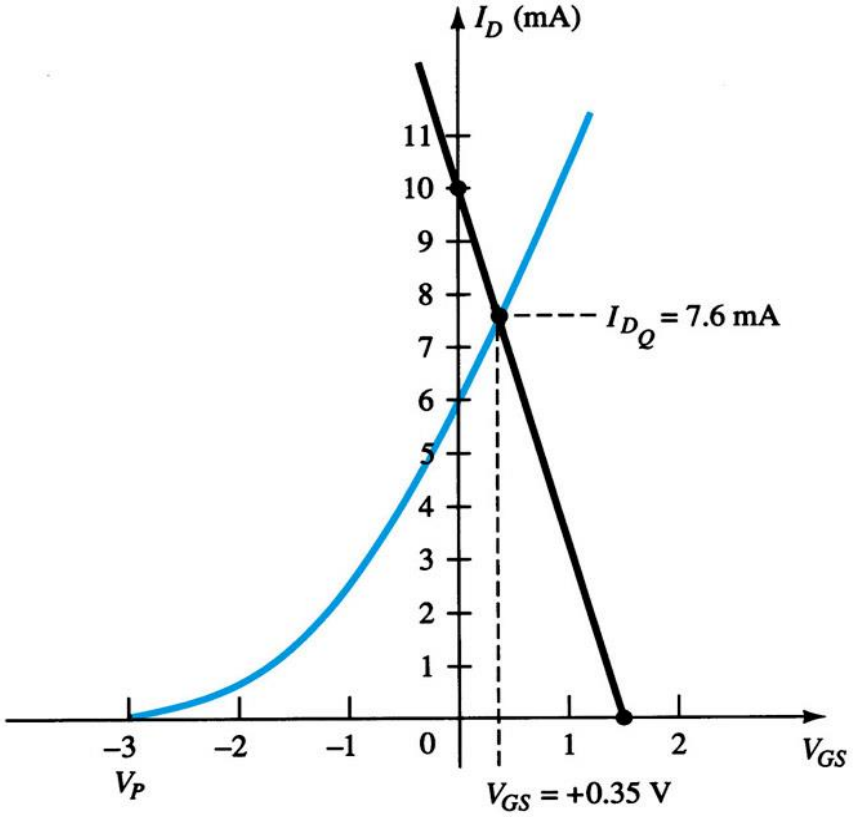
Use the I_D at the Q-point to solve for the other variables in the voltage-divider bias circuit. These are the same calculations as used by a JFET circuit.



When R_S change…the linear characteristics will change..

1. Plot line for $V_{GS} = V_G$, $I_D = 0$ and $I_D = V_G/R_S$, $V_{GS} = 0$
2. Plot the transfer curve by plotting I_{DSS}, V_P and calculated values of I_D.
3. Where the line intersects the transfer curve is the Q-point.

Use the I_D at the Q-point to solve for the other variables in the voltage-divider bias circuit. These are the same calculations as used by a JFET circuit.



Depletion-Type MOSFETs

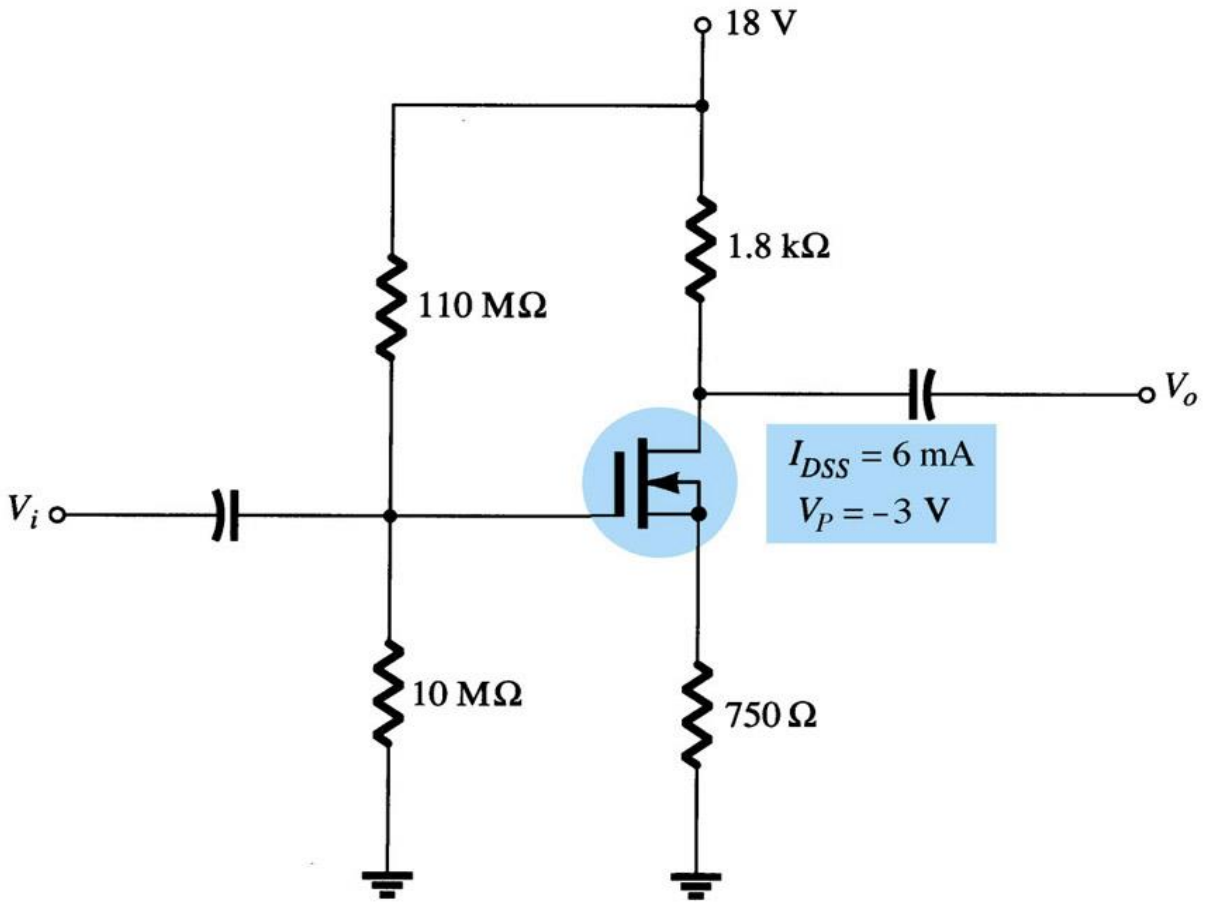
Depletion-type MOSFET bias circuits are similar to JFETs. The only difference is that the depletion-Type MOSFETs can operate with positive values of V_{GS} and with I_D values that exceed I_{DSS}.

Example

For the *n*-channel depletion-type MOSFET of Figure below, determine:

a. I_{DQ} and V_{GSQ}.

b. V_{DS}.



Solution:

a. For the transfer characteristics, a plot point is defined by $I_D = I_{DSS}/4 = 6\text{ mA}/4 = 1.5\text{ mA}$ and $V_{GS} = V_P/2 = -3\text{ V}/2 = -1.5\text{ V}$. Considering the level of V_P and the fact that Shockley's equation defines a curve that rises more rapidly as V_{GS} becomes more positive, a plot point will be defined at $V_{GS} = +1\text{ V}$. Substituting into Shockley's equation yields

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

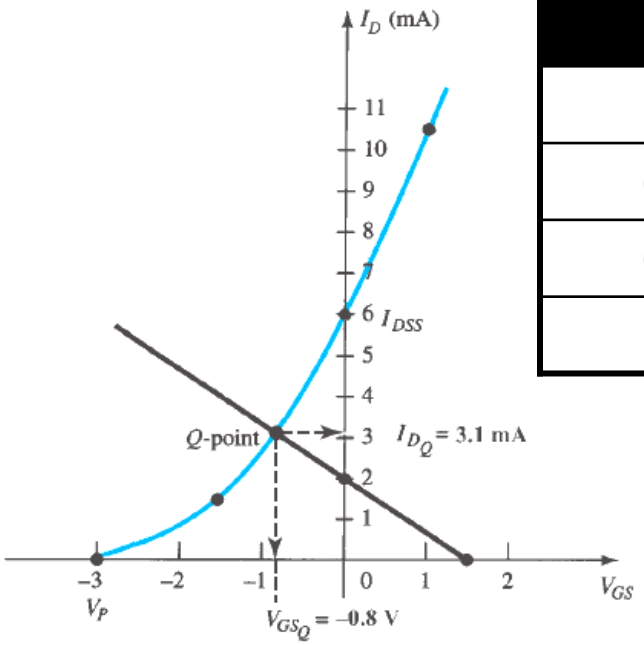
$$= 6\text{ mA}\left(1 - \frac{+1\text{ V}}{-3\text{ V}}\right)^2 = 6\text{ mA}\left(1 + \frac{1}{3}\right)^2 = 6\text{ mA}\,(1.778)$$

$$= 10.67\text{ mA}$$

The resulting transfer curve appears in Fig. 7.31. Proceeding as described for JFETs, we have

$$\text{Eq. (7.15):}\quad V_G = \frac{10\text{ M}\Omega(18\text{ V})}{10\text{ M}\Omega + 110\text{ M}\Omega} = 1.5\text{ V}$$

$$\text{Eq. (7.16):}\quad V_{GS} = V_G - I_D R_S = 1.5\text{ V} - I_D(750\ \Omega)$$



V_{GS}	I_D	V_{GS},I_D
0	I_{DSS}	(0,6)
$0.3V_P$	$I_{DSS}/2$	(-0.9,3)
$0.5V_P$	$I_{DSS}/4$	(-1.5,1.5)
V_P	0mA	(-3,0)

Setting $I_D = 0$ mA results in

$$V_{GS} = V_G = 1.5\text{ V}$$

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5\text{ V}}{750\ \Omega} = 2\text{ mA}$$

The plot points and resulting bias line appear in Fig. 7.31. The resulting operating point is given by

$$I_{D_Q} = \mathbf{3.1\text{ mA}}$$
$$V_{GS_Q} = \mathbf{-0.8\text{ V}}$$

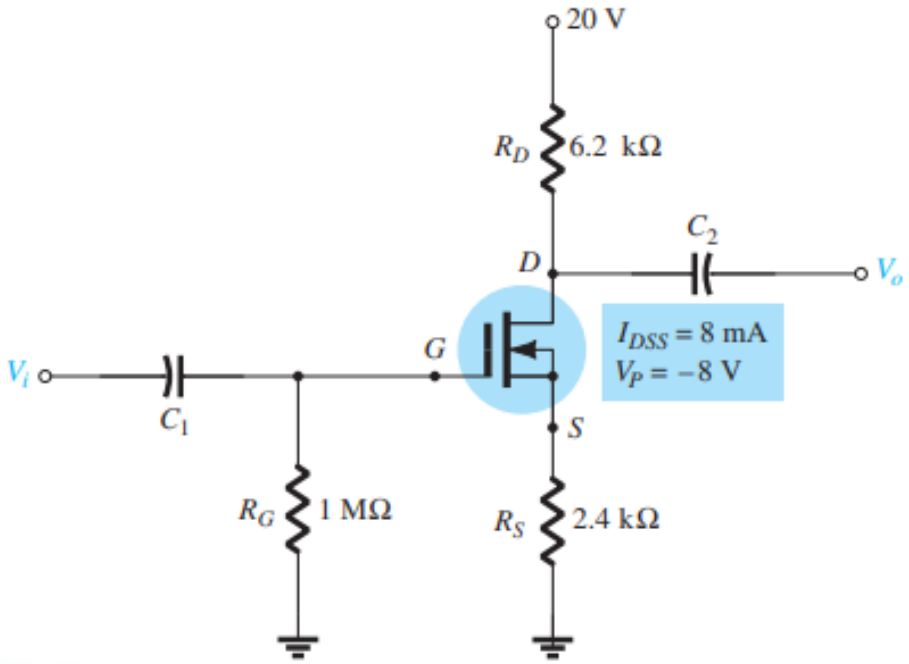
b. Eq. (7.19):

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$= 18\text{ V} - (3.1\text{ mA})(1.8\text{ k}\Omega + 750\ \Omega)$$
$$\cong \mathbf{10.1\text{ V}}$$

Example

Determine the following for the network of Fig.

a) I_{DQ} and V_{GSQ}.
b) V_D .



Solution:

a. The self-bias configuration results in

$$V_{GS} = -I_D R_S$$

as obtained for the JFET configuration, establishing the fact that V_{GS} must be less than 0 V. There is therefore no requirement to plot the transfer curve for positive values of V_{GS}, although it was done on this occasion to complete the transfer characteristics. A plot point for the transfer characteristics for $V_{GS} < 0$ V is

$$I_D = \frac{I_{DSS}}{4} = \frac{8\text{ mA}}{4} = 2\text{ mA}$$

and

$$V_{GS} = \frac{V_P}{2} = \frac{-8\text{ V}}{2} = -4\text{ V}$$

and for $V_{GS} > 0$ V, since $V_P = -8$ V, we will choose

$$V_{GS} = +2\text{ V}$$

and

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 8\text{ mA}\left(1 - \frac{+2\text{ V}}{-8\text{ V}}\right)^2$$

$$= 12.5\text{ mA}$$

The resulting transfer curve appears in Fig. 7.34. For the network bias line, at $V_{GS} = 0$ V, $I_D = 0$ mA. Choosing $V_{GS} = -6$ V gives

$$I_D = -\frac{V_{GS}}{R_S} = -\frac{-6\text{ V}}{2.4\text{ k}\Omega} = 2.5\text{ mA}$$

The resulting Q-point is given by

$$I_{D_Q} = \mathbf{1.7\text{ mA}}$$
$$V_{GS_Q} = \mathbf{-4.3\text{ V}}$$

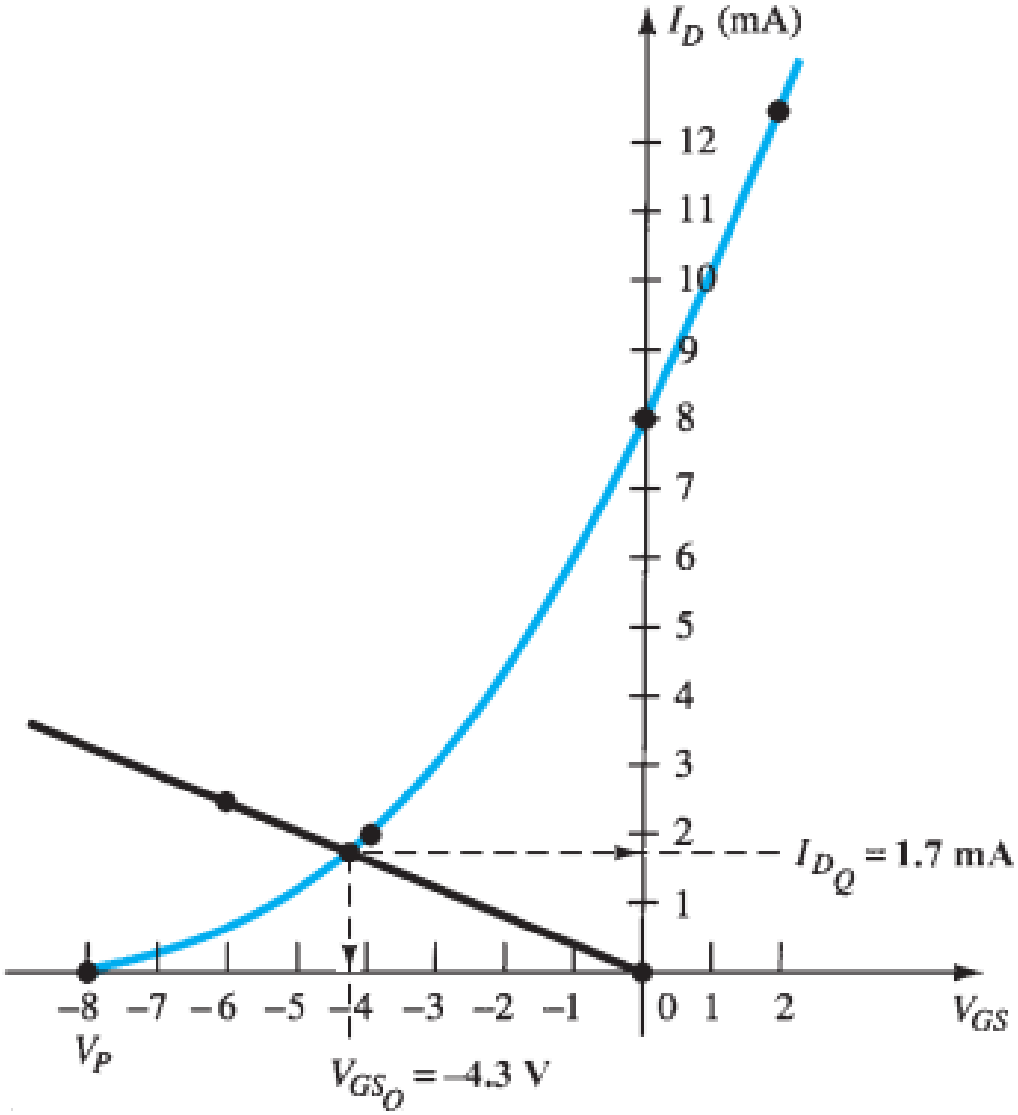
b. $V_D = V_{DD} - I_D R_D$

$= 20\text{ V} - (1.7\text{ mA})(6.2\text{ k}\Omega)$

$= \mathbf{9.46\text{ V}}$

The example to follow employs a design that can also be applied to JFET transistors. At first impression it appears rather simplistic, but in fact it often causes some confusion when first analyzed due to the special point of operation.

V_{GS}	I_D	V_{GS},I_D
0	I_{DSS}	(0,8)
$0.3V_P$	$I_{DSS}/2$	(-2.4,4)
$0.5V_P$	$I_{DSS}/4$	(-4,2)
V_P	0mA	(-8,0)



V_{GS}	I_D	V_{GS},I_D
0	I_{DSS}	(0,8)
$0.3V_P$	$I_{DSS}/2$	(-2.4,4)
$0.5V_P$	$I_{DSS}/4$	(-4,2)
V_P	0mA	(-8,0)

Example

Sketch the transfer characteristics for an *n* -channel depletion-type MOSFET with I_{DSS}= 10 mA and V_P= -4 V.

Solution:

$$\text{At } V_{GS} = 0\text{ V}, \quad I_D = I_{DSS} = 10\text{ mA}$$

$$V_{GS} = V_P = -4\text{ V}, \quad I_D = 0\text{ mA}$$

$$V_{GS} = \frac{V_P}{2} = \frac{-4\text{ V}}{2} = -2\text{ V}, \quad I_D = \frac{I_{DSS}}{4} = \frac{10\text{ mA}}{4} = 2.5\text{ mA}$$

and at $I_D = \frac{I_{DSS}}{2}$,

$$V_{GS} = 0.3V_P = 0.3(-4\text{ V}) = -1.2\text{ V}$$

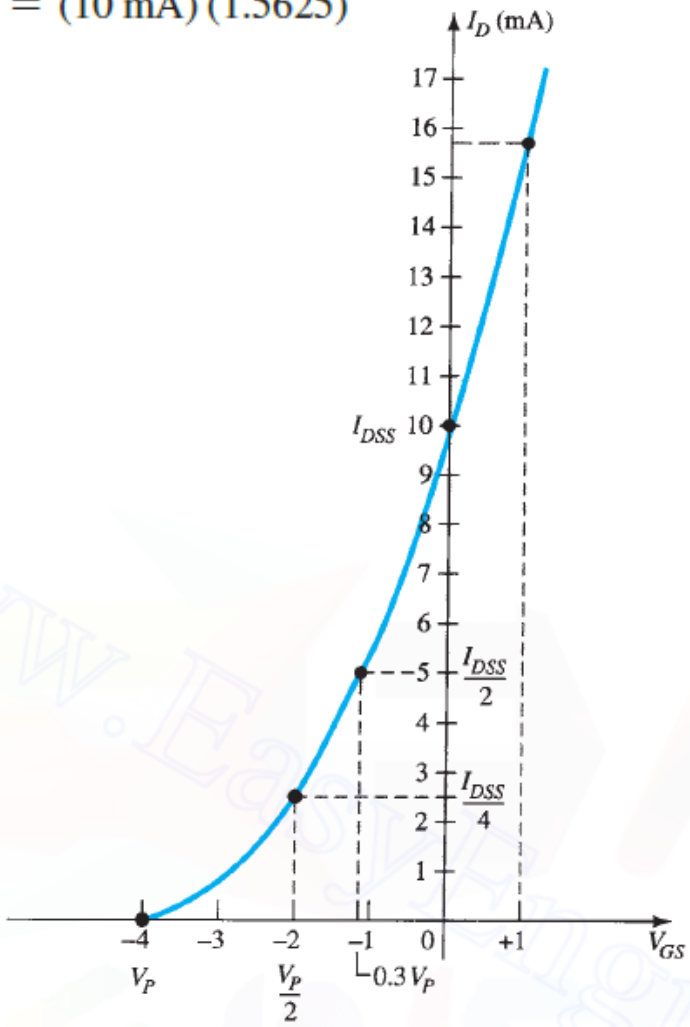
all of which appear in Fig. 6.28.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= (10\text{ mA})\left(1 - \frac{+1\text{ V}}{-4\text{ V}}\right)^2 = (10\text{ mA})\,(1 + 0.25)^2 = (10\text{ mA})\,(1.5625)$$

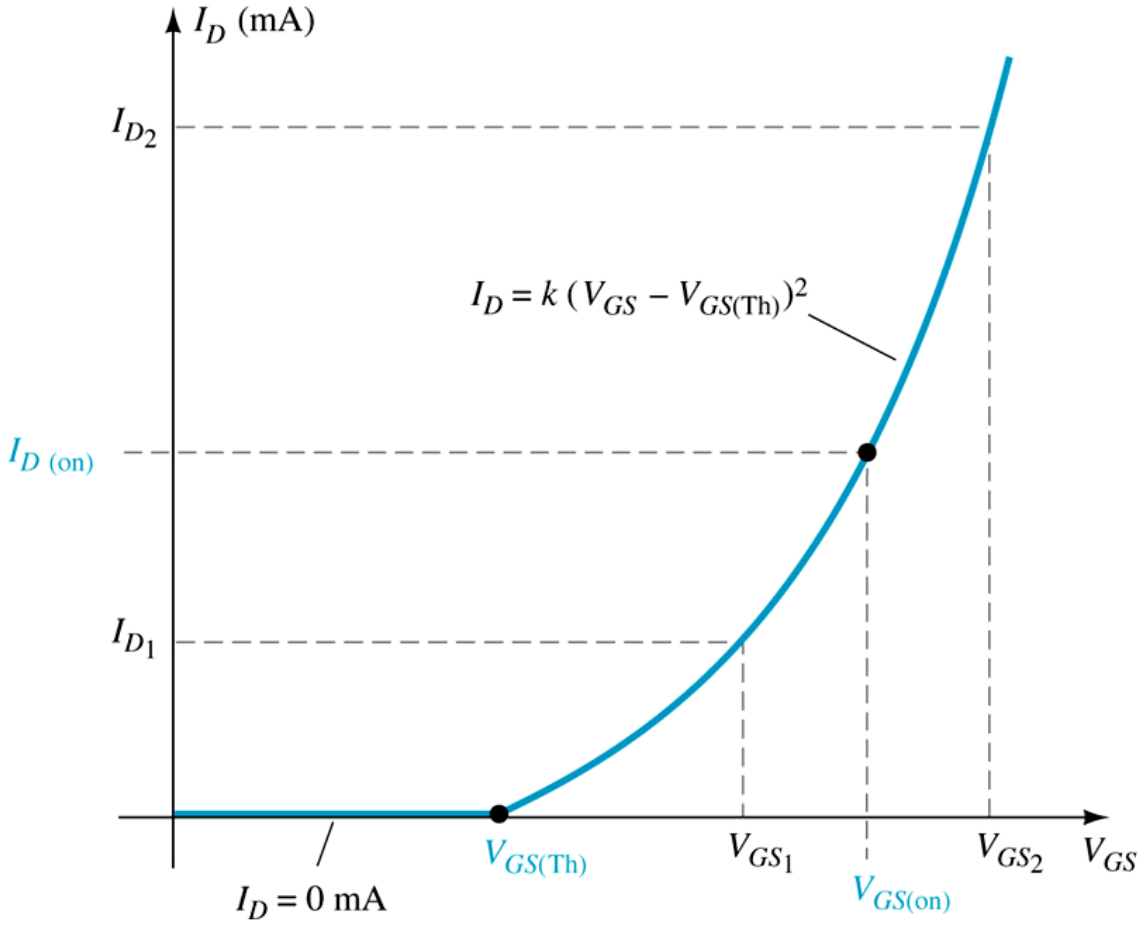
$$\cong 15.63\text{ mA}$$

which is sufficiently high to finish the plot.



Enhancement-Type MOSFET

The transfer characteristic for the enhancement-type MOSFET is very different from that of a simple JFET or the depletion-type MOSFET.

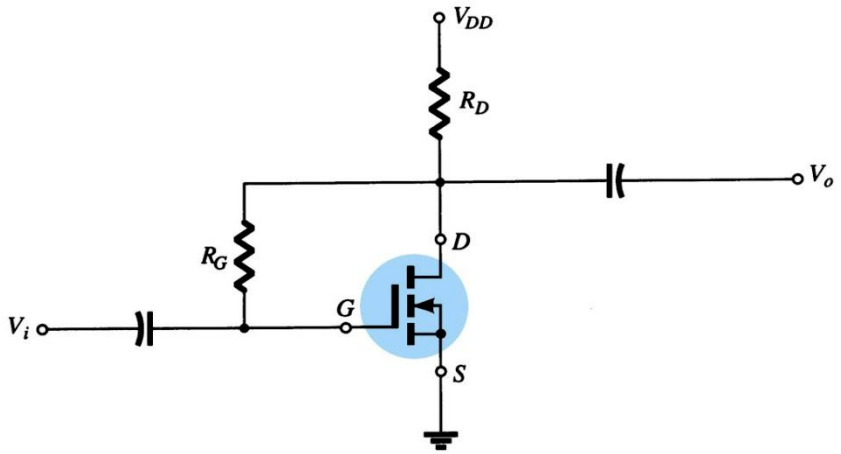


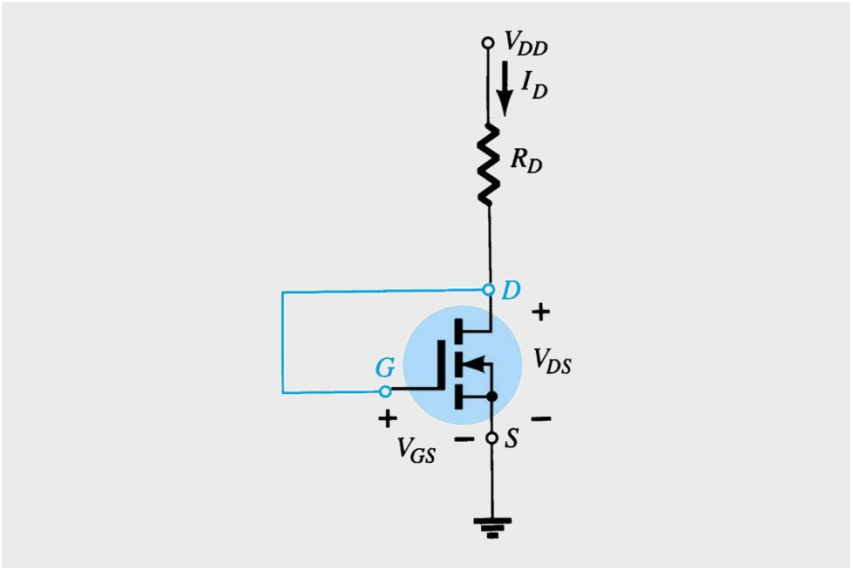
- Transfer characteristic for E-MOSFET

and $$I_D = k(V_{GS} - V_{GS(Th)})^2$$

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$

Feedback Biasing





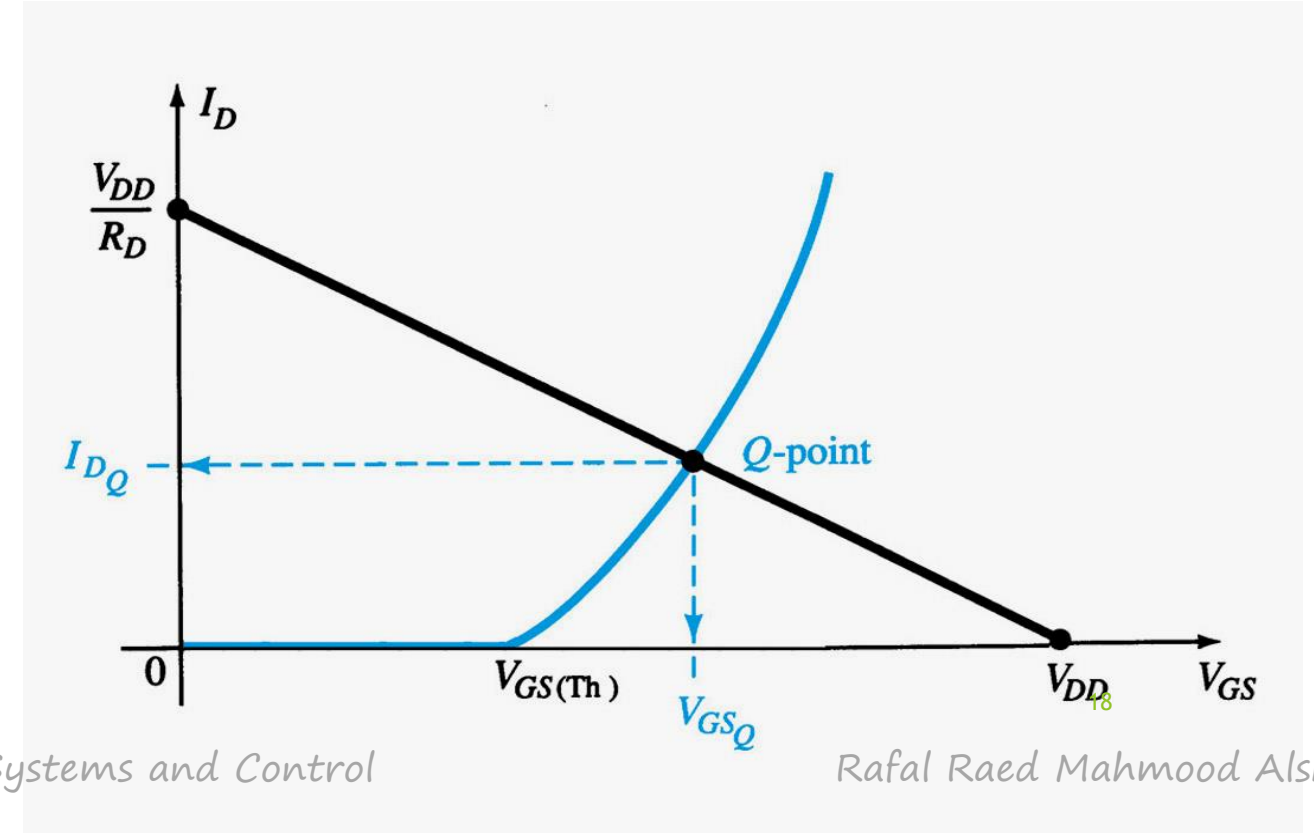
I_G =0A, therefore V_{RG} = 0V

Therefore: $V_{DS} = V_{GS}$

Which makes $$V_{GS} = V_{DD} - I_D R_D$$

Feedback Biasing Q-Point

1. Plot the line using $V_{GS} = V_{DD}$, $I_D = 0$ and $I_D = V_{DD} / R_D$ and $V_{GS} = 0$
2. Plot the transfer curve using V_{GSTh} , $I_D = 0$ and $V_{GS(on)}$, $I_{D(on)}$; all given in the specification sheet.
3. Where the line and the transfer curve intersect is the Q-Point.
4. Using the value of I_D at the Q-point, solve for the other variables in the bias circuit.

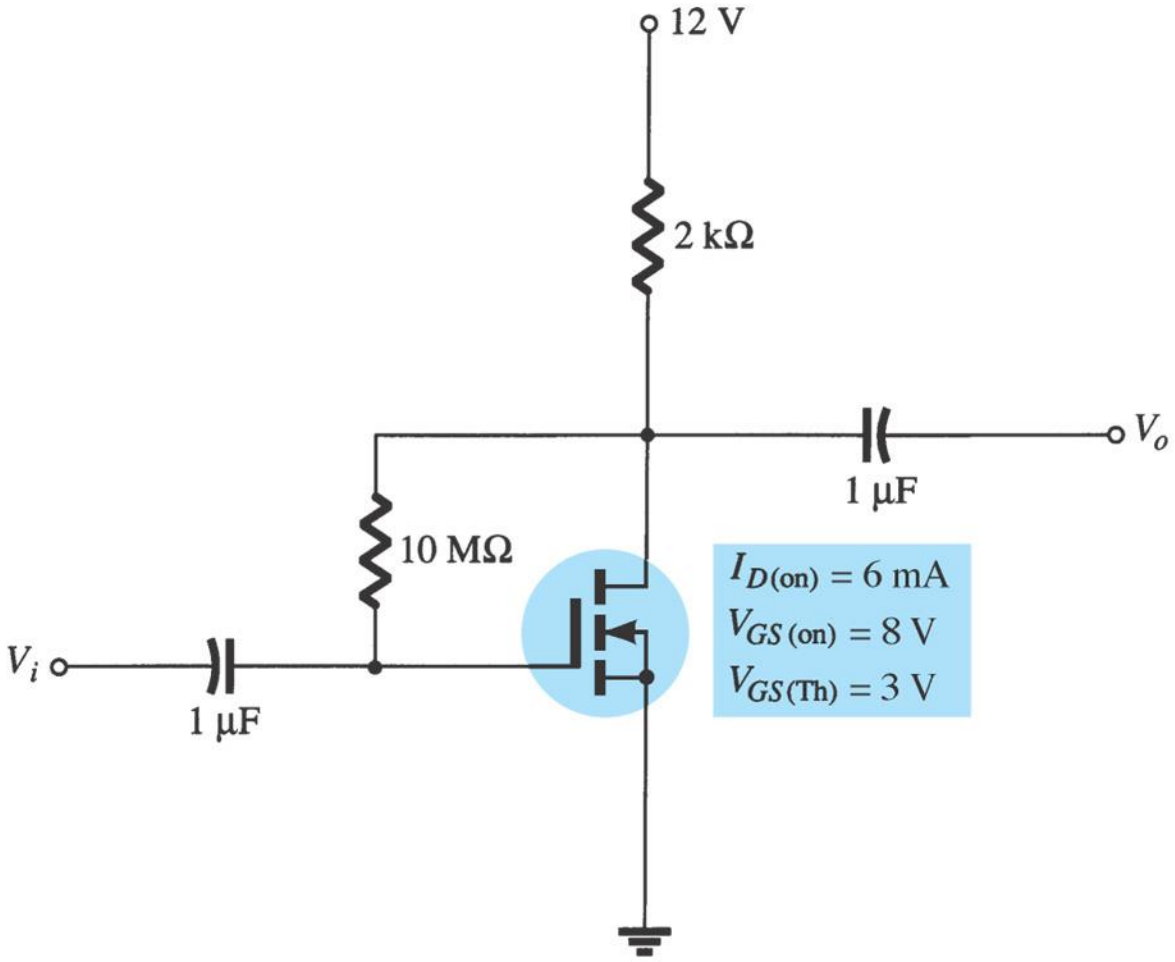


DC analysis step for Feedback Biasing Enhancement type MOSFET

- Find k using the datasheet or specification given;
  ex: $V_{GS(ON)}$,$V_{GS(TH)}$
- Plot transfer characteristics using the formula
  $I_D=k(V_{GS} - V_T)^2$. Three point already defined that is $I_{D(ON)}$, $V_{GS(ON)}$ and $V_{GS(TH)}$
- Plot a point that is slightly greater than V_{GS}
- Plot the linear characteristics (network bias line)
- The intersection defines the Q-point

Example

Determine I_{DQ} and V_{DSQ} for the enhancement-type MOSFET



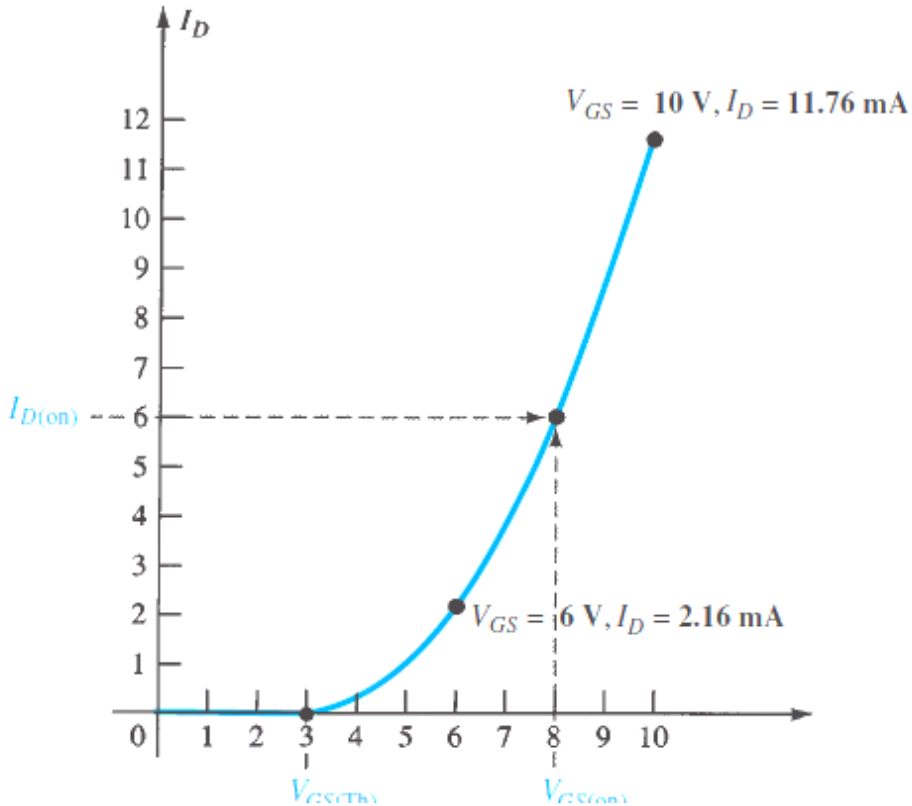
Solution:

Plotting the Transfer Curve Two points are defined immediately as shown in Fig. Solving for k, we obtain

$$\text{Eq. (7.34):} \quad k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$

$$= \frac{6\ \text{mA}}{(8\ \text{V} - 3\ \text{V})^2} = \frac{6 \times 10^{-3}}{25}\ \text{A/V}^2$$

$$= \mathbf{0.24 \times 10^{-3}\ A/V^2}$$



For $V_{GS} = 6$ V (between 3 and 8 V):

$$I_D = 0.24 \times 10^{-3}(6\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(9)$$
$$= 2.16\text{ mA}$$

as shown on Fig. 7.41. For $V_{GS} = 10$ V (slightly greater than $V_{GS(\text{Th})}$),

$$I_D = 0.24 \times 10^{-3}(10\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(49)$$
$$= 11.76\text{ mA}$$

as also appearing on Fig. 7.41. The four points are sufficient to plot the full curve for the range of interest as shown in Fig. 7.41.

For the Network Bias Line

$$V_{GS} = V_{DD} - I_D R_D$$
$$= 12\text{ V} - I_D(2\text{ k}\Omega)$$

Eq. (7.37): $$V_{GS} = V_{DD} = 12\text{ V}|_{I_D = 0\text{ mA}}$$

Eq. (7.38): $$I_D = \frac{V_{DD}}{R_D} = \frac{12\text{ V}}{2\text{ k}\Omega} = 6\text{ mA}|_{V_{GS} = 0\text{ V}}$$

The resulting bias line appears in Fig. 7.42.

At the operating point,

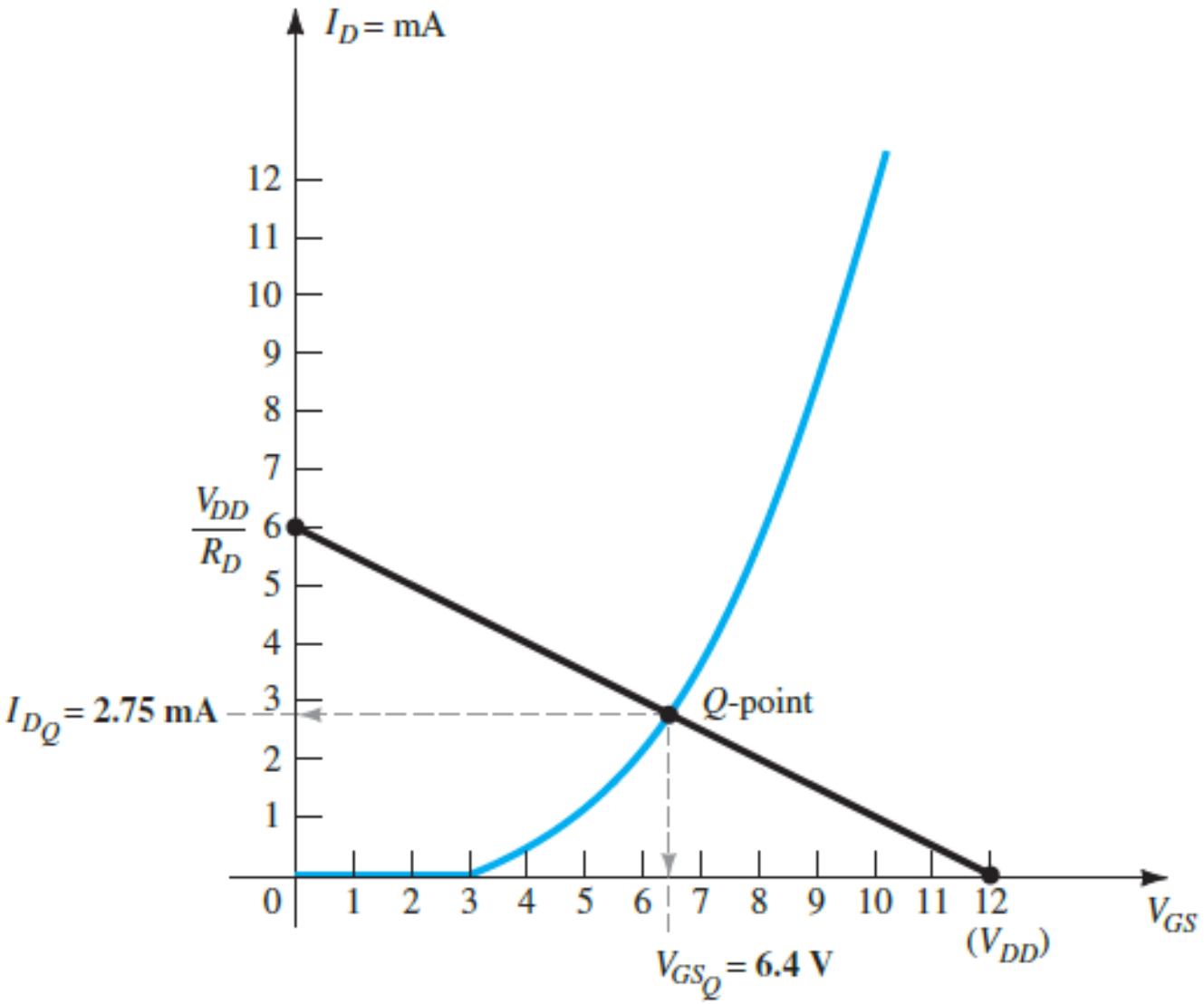
$$I_{D_Q} = \mathbf{2.75\text{ mA}}$$

and

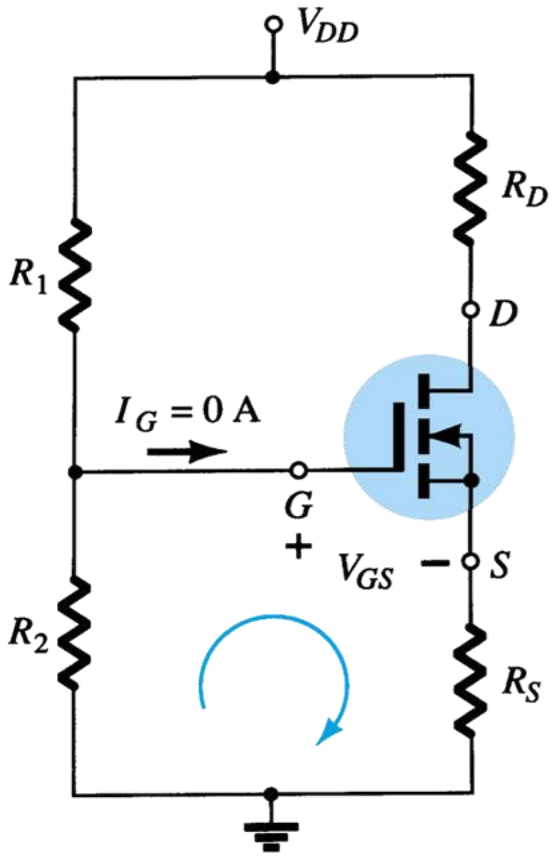
$$V_{GS_Q} = 6.4\text{ V}$$

with

$$V_{DS_Q} = V_{GS_Q} = \mathbf{6.4\text{ V}}$$


I_D = mA
12
11
10
9
8
7
$\frac{V_{DD}}{R_D}$
6
5
4
3
I_{D_Q} = 2.75 mA
2
1
0
1
2
3
4
5
6
7
8
9
10
11
12
(V_{DD})
V_{GS}
Q-point
V_{GS_Q} = 6.4 V

Voltage-Divider Biasing



Again plot the line and the transfer curve to find the Q-point.

Using the following equations:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Input loop : $V_{GS} = V_G - I_D R_S$

Output loop: $V_{DS} = V_{DD} - I_D (R_S + R_D)$

Voltage-Divider Bias Q-Point

1. Plot the line using $V_{GS} = V_G = (R_2V_{DD})/(R_1 + R_2)$, $I_D = 0$ and $I_D = V_G/R_S$ and $V_{GS} = 0$

2. Find k

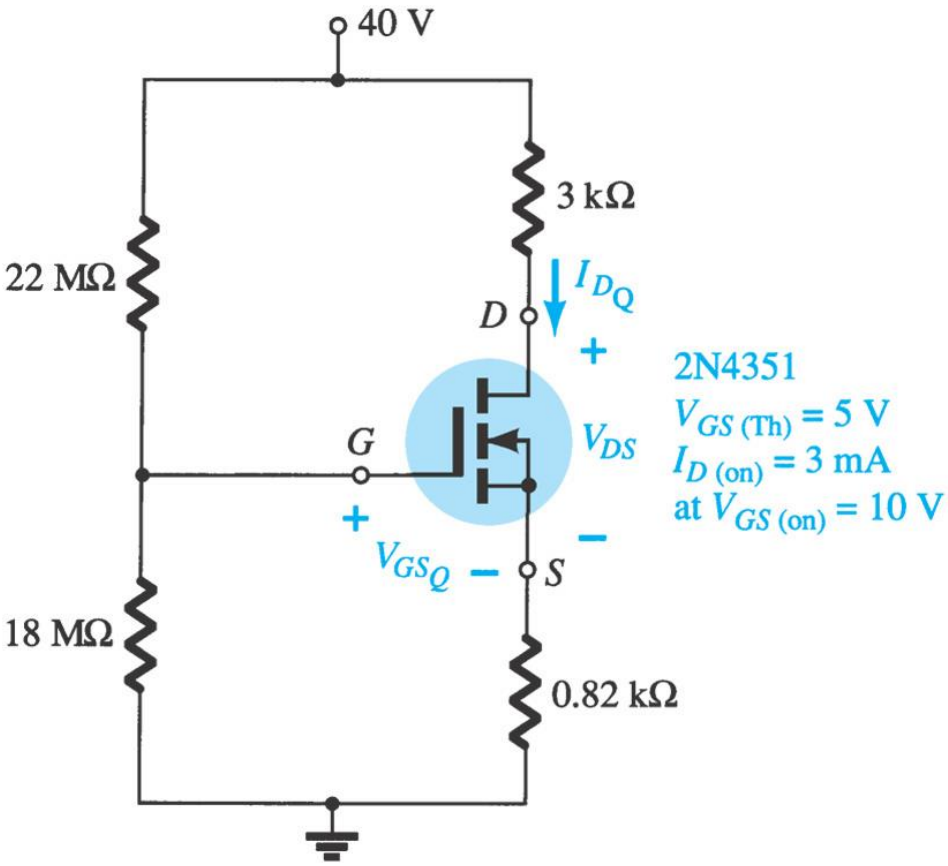
3. Plot the transfer curve using V_{GSTh}, $I_D = 0$ and $V_{GS(on)}$, $I_D(on)$; all given in the specification sheet.

4. Where the line and the transfer curve intersect is the Q-Point.

5. Using the value of I_D at the Q-point, solve for the other variables in the bias circuit.

Example

- Determine I_{DQ} and V_{GSQ} and V_{DS} for network below



Solution:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18\,\text{M}\Omega)(40\,\text{V})}{22\,\text{M}\Omega + 18\,\text{M}\Omega} = 18\,\text{V}$$

$$V_{GS} = V_G - I_D R_S = 18\,\text{V} - I_D(0.82\,\text{k}\Omega)$$

When $I_D = 0\,\text{mA}$,

$$V_{GS} = 18\,\text{V} - (0\,\text{mA})(0.82\,\text{k}\Omega) = 18\,\text{V}$$

When $V_{GS} = 0\,\text{V}$,

$$V_{GS} = 18\,\text{V} - I_D(0.82\,\text{k}\Omega)$$

$$0 = 18\,\text{V} - I_D(0.82\,\text{k}\Omega)$$

$$I_D = \frac{18\,\text{V}}{0.82\,\text{k}\Omega} = 21.95\,\text{mA}$$

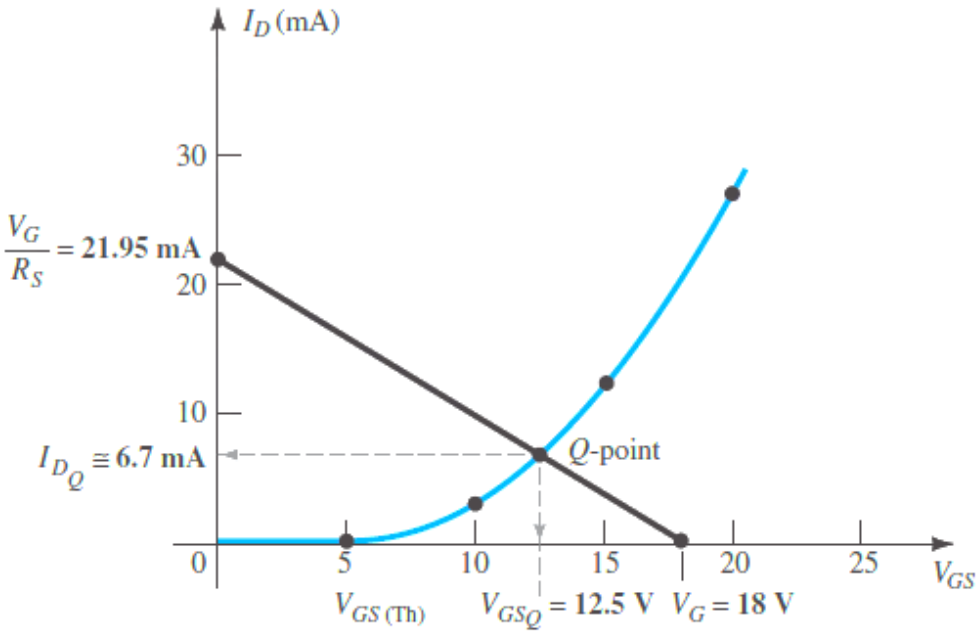


FIG. 7.45
Determining the Q-point for the network of Example 7.11.

Device

$$V_{GS(\text{Th})} = 5\ \text{V}, \quad I_{D(\text{on})} = 3\ \text{mA with } V_{GS(\text{on})} = 10\ \text{V}$$

Eq. (7.34):
$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$
$$= \frac{3\ \text{mA}}{(10\ \text{V} - 5\ \text{V})^2} = 0.12 \times 10^{-3}\ \text{A/V}^2$$

and
$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$
$$= 0.12 \times 10^{-3}(V_{GS} - 5)^2$$

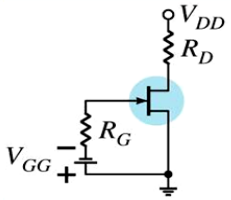
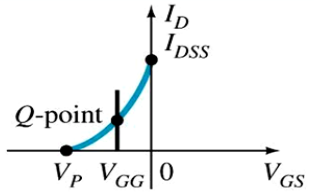
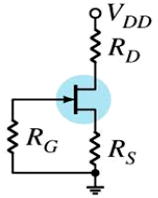
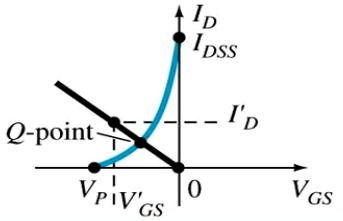
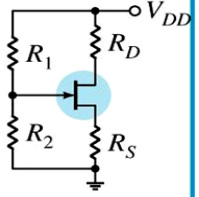
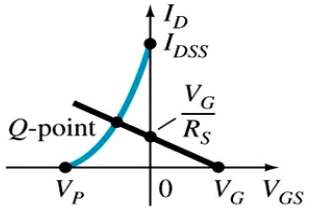
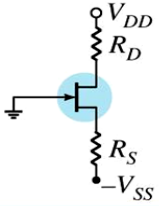
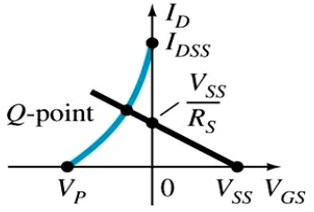
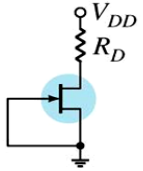
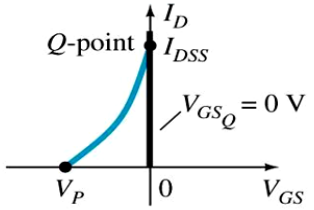
which is plotted on the same graph (Fig. 7.45). From Fig. 7.45,

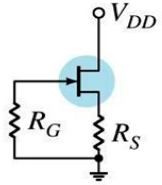
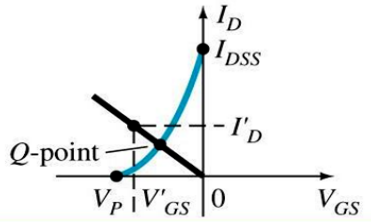
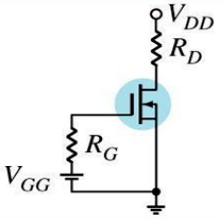
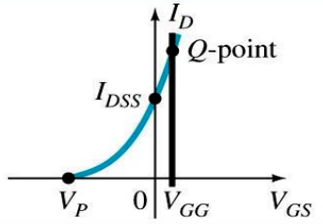
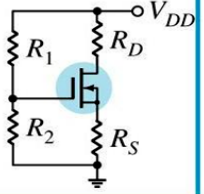
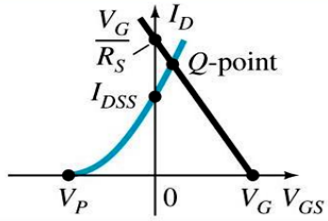
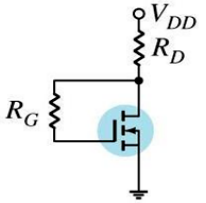
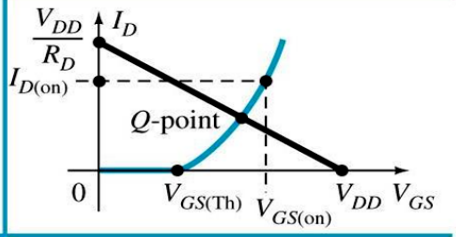
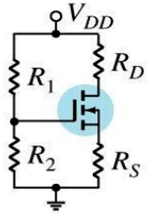
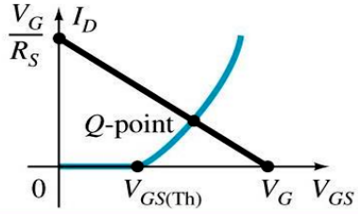
$$I_{D_Q} \cong \mathbf{6.7\ mA}$$

$$V_{GS_Q} = \mathbf{12.5\ V}$$

Eq. (7.41):
$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_S + R_D) \\ &= 40\ \text{V} - (6.7\ \text{mA})(0.82\ \text{k}\Omega + 3.0\ \text{k}\Omega) \\ &= 40\ \text{V} - 25.6\ \text{V} \\ &= \mathbf{14.4\ V} \end{aligned}$$

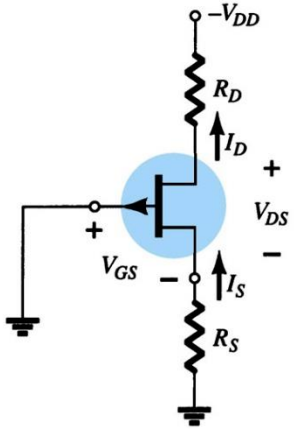
TABLE 6.1 FET Bias Configurations

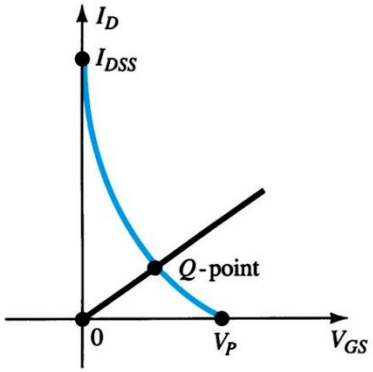
Type	Configuration	Pertinent Equations	Graphical Solution
JFET Fixed-bias		$V_{GS_Q} = -V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
JFET Self-bias		$V_{GS} = -I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Common-gate		$V_{GS} = V_{SS} - I_D R_S$ $V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$	
JFET $V_{GS_Q} = 0$ V		$V_{GS_Q} = 0$ V $\therefore I_{D_Q} = I_{DSS}$	

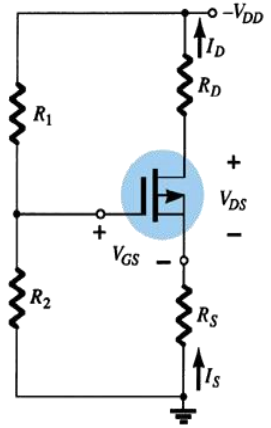
Type	Configuration	Pertinent Equations	Graphical Solution
JFET 1R$_D$ 5 0 V 2		$V_{GS} = -I_D R_S$ $V_D = V_{DD}$ $V_S = I_D R_S$ $V_{DS} = V_{DD} - I_S R_S$	
Depletion-type MOSFET Fixed-bias		$V_{GS} = -V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
Depletion-type MOSFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_S R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
Enhancement type MOSFET Feedback configuration		$V_{GS} = V_{DS}$ $V_{GS} = V_{DD} - I_D R_D$	
Enhancement type MOSFET Voltage-divider		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$	

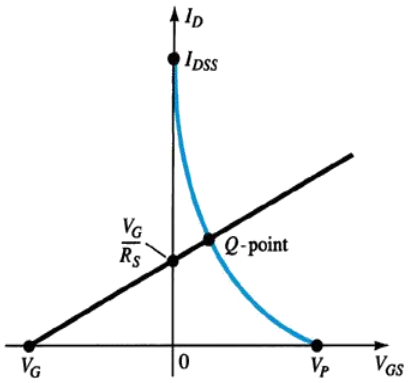
P-Channel FETs

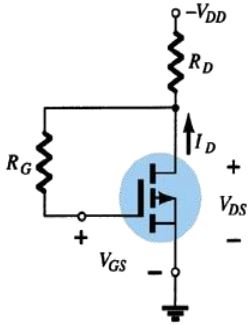
For p-channel FETs the same calculations and graphs are used, except that the voltage polarities and current directions are the opposite. The graphs will be mirrors of the n-channel graphs.

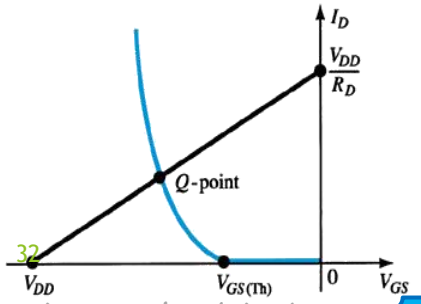










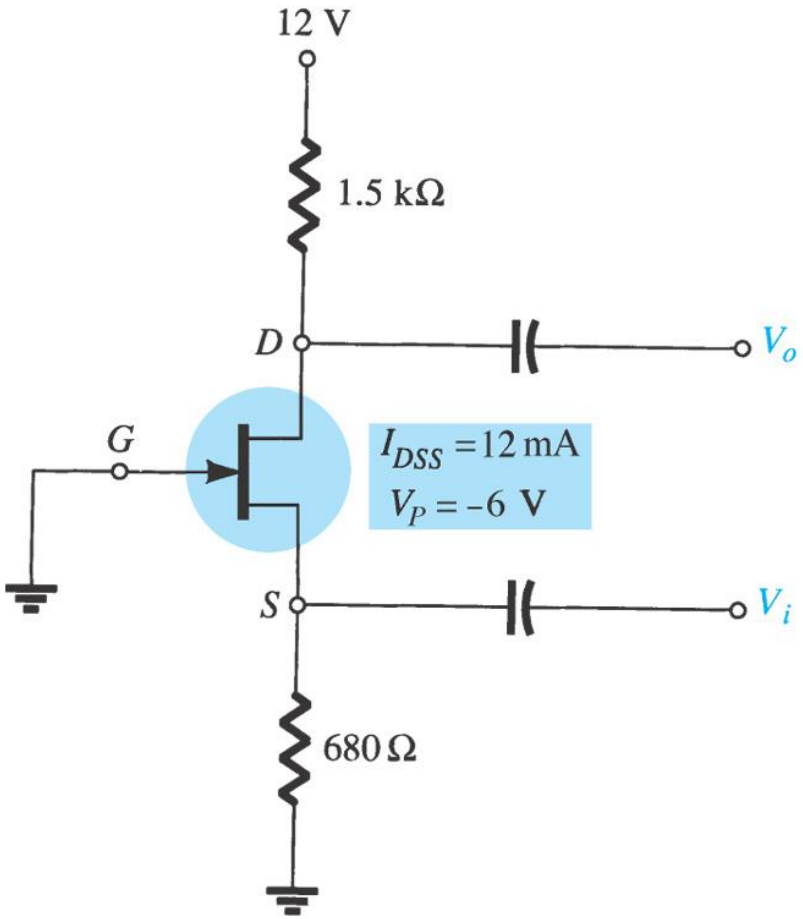


Advantages

- High Input impedance for isolation.
- Amount of power drawn from circuit under test is very small, so no loading effect.
- Very high sensitivity.
- Amplifier gain allows measurement in the mV range.
- No damage due to overload because of amplifier saturation.

Home Work

- Determine V_{GS} I_{DQ}, V_D , V_G , V_S , andV_{DS} .



Equations

JFET:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = I_{DSS}\big|_{V_{GS}=0\ V}, \quad I_D = 0\ \text{mA}\big|_{V_{GS}=V_P}, \quad I_D = \left.\frac{I_{DSS}}{4}\right|_{V_{GS}=V_P/2}, \quad V_{GS} \cong 0.3V_P\big|_{I_D=I_{DSS}/2}$$

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$P_D = V_{DS}I_D$$

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2}$$

MOSFET (enhancement):

$$I_D = k(V_{GS} - V_T)^2$$

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_T)^2}$$

Ninevah University
College of Electronics Engineering
Department of Systems and Control

Electronic I I
Lecture 5

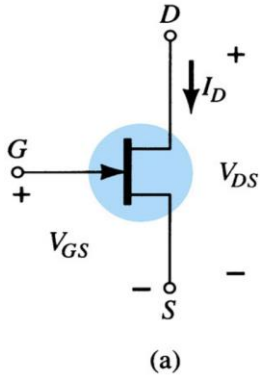
AC Equivelent Cct (FET)

by
Rafal Raed Mahmood Alshaker

2nd Class

FET Small-Signal Model

•FET amplifiers are similar to BJT amplifiers in operation. The purpose of the amplifier is the same for both FET amplifiers and BJT amplifiers. FET amplifiers have certain advantages over BJT amplifiers such as high input impedance. However, the BJT normally has a higher voltage gain.



(a)

•A major component of the ac model will reflect the fact that an ac voltage applied to the input gate-to-source terminals will control the level of current from drain to source.

•The relationship of V_{GS} (input) to I_D (output) is called transconductance, **gm**

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

As we known for FET, a dc gate-to source voltage controlled the level of dc drain current through a relationship known as Shockley's equation :

$$I_D = I_{DSS}\left(1 - V_{GS}/V_P\right)^2 .$$

The change in drain current that will result from a change in gate-to-source voltage can be determined using the transconductance factor g_m in the following manner

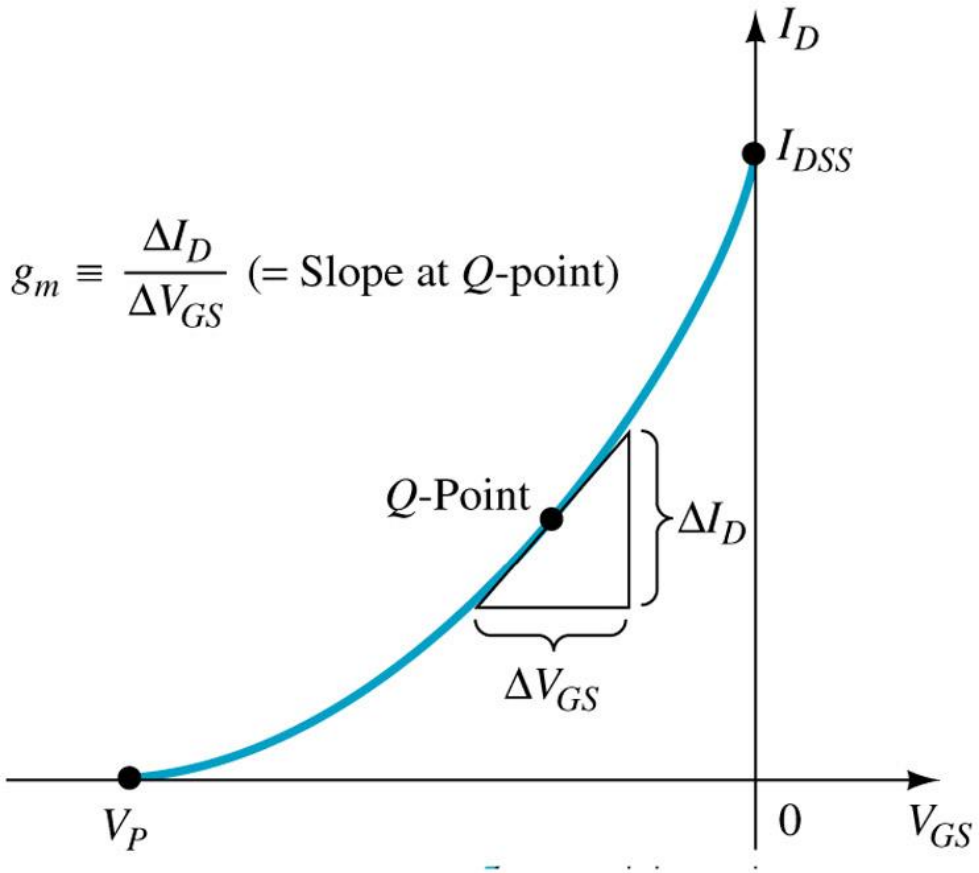
$$\Delta I_D = g_m \Delta V_{GS}$$

The prefix *tarns-* in terminology applied to g_m reveals that it establishes a relationship between an *output and input* quantity. The root word *conductance* was chosen because g_m is determined by a *voltage-to-current ratio* similar to the ratio that defines the conductance of a resistor $G = 1/R = I/V$.

Solving for g_m above, we have :

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Graphical Determination of gm



- The problem with the accuracy of the transfer plot

هذه الطريقة فيها مشكلة حيث تحتاج الي رسم عالي الدقة لحساب قيمتها بالإضافة لرسم موضح بشكل كبير للحصول على قيم دقيقة

Mathematical Definitions of g_m

The deviation of a function at a point is equal to the slope of the tangent line drawn at that point

$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{Q\text{-pt.}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right]$$

$$= I_{DSS}\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)$$

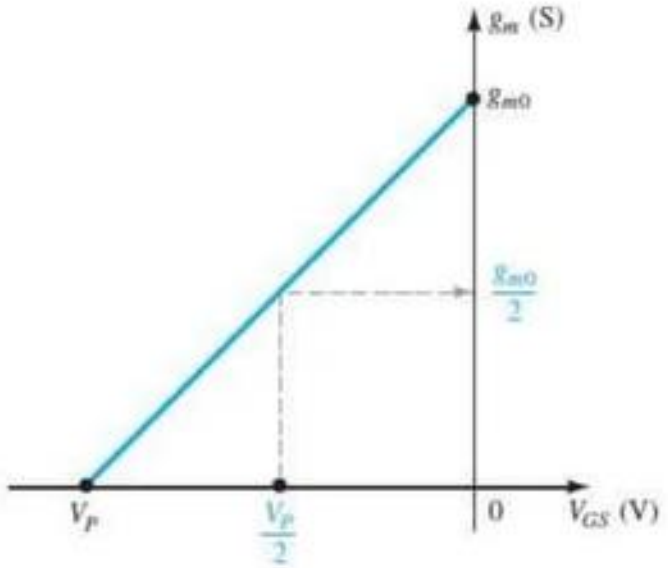
$$= 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[\frac{d}{dV_{GS}}(1) - \frac{1}{V_P}\frac{dV_{GS}}{dV_{GS}}\right] = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[0 - \frac{1}{V_P}\right]$$

$$\boxed{g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]}$$

On a specification sheet g_m is often provided us g_{fs} or , y_{fs} where y indicates it is part of an admittance equivalent circuit . The *f* signifies forward transfer conductance and that *s* Indicates that it is connected to the source terminal in equation form

$$g_m = g_{fs} = y_{fs}$$

In general , therefore the maximum value of g_m occurs where V_{GS} =0
and the minimum Value at $V_{GS} = V_P$ .The more negative the value of V_{GS} the less value of g_m



Plot of g_m versus V_{GS}.

Effect of I_D on g_m

- A mathematical relationship between $g\ m$ and the dc bias current $I\ D$ can be derived by noting that Shockley's equation can be written in the following form:

$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

determine g_m for a few specific values of I_D,

a. If $I_D = I_{DSS}$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}}{I_{DSS}}} = g_{m0}$$

b. If $I_D = I_{DSS}/2$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/2}{I_{DSS}}} = 0.707g_{m0}$$

c. If $I_D = I_{DSS}/4$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/4}{I_{DSS}}} = \frac{g_{m0}}{2} = 0.5g_{m0}$$

the highest values of g_m are obtained when V_{GS} approaches 0 V and I_D approaches its maximum value of I_{DSS}.

Mathematical Definition of gm

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

The derivative of I_D respect to V_{GS} using Shockley's Equation

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

magnitude only to ensure a positive value for g_m

for V_{GS} =0V:

$Zi = \infty\Omega$

As mentioned, the slope of the transfer curve is max at V_{GS} = 0 V,

g_m for V_{GS} =0V: $g_{m0} = \frac{2I_{DSS}}{|V_P|}$

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$Zo = r_d = \frac{1}{y_{os}}$

for

$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

Input Impedance Zi: $Zi = \infty\Omega$

Output Impedance Zo: $Zo = r_d = \frac{1}{y_{os}}$

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\Big/_{V_{GS}=\text{constant}}$$

yos: admittance equivalent circuit parameter listed on FET specification sheets.

FET Impedance

Input impedance:

$$Z_i = \infty\Omega$$

Output Impedance:

$$Z_o = r_d = \frac{1}{y_{os}}$$

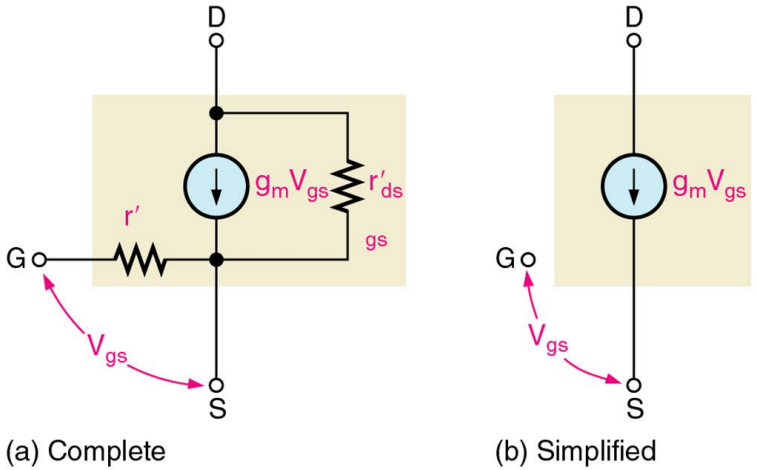
where:

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\bigg|_{V_{GS}=\text{constant}}$$

y_{os}= admittance parameter listed on FET specification sheets.

FET Amplification

- Let's first look at an equivalent FET circuit to better understand it's operation. The FET is basically a current source that is controlled by V_{GS}. Note that the resistance, r' from gate to source can be neglected since it is so large in value and in most cases the drain to source resistance (r'_{ds}) or (r_d) can be neglected as well.

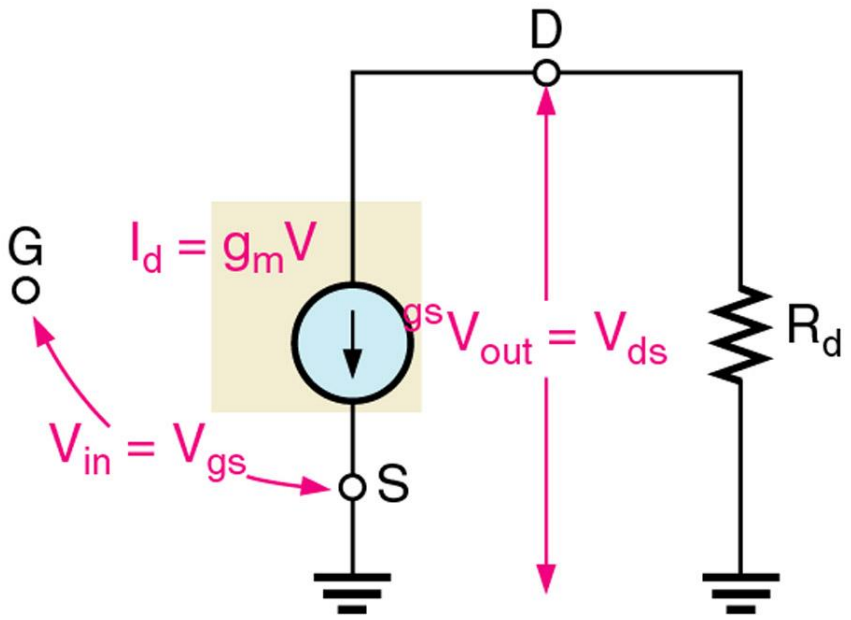


$$I_D = g_m V_{GS} \qquad (g_m \text{ is the symbol for transconductance})$$

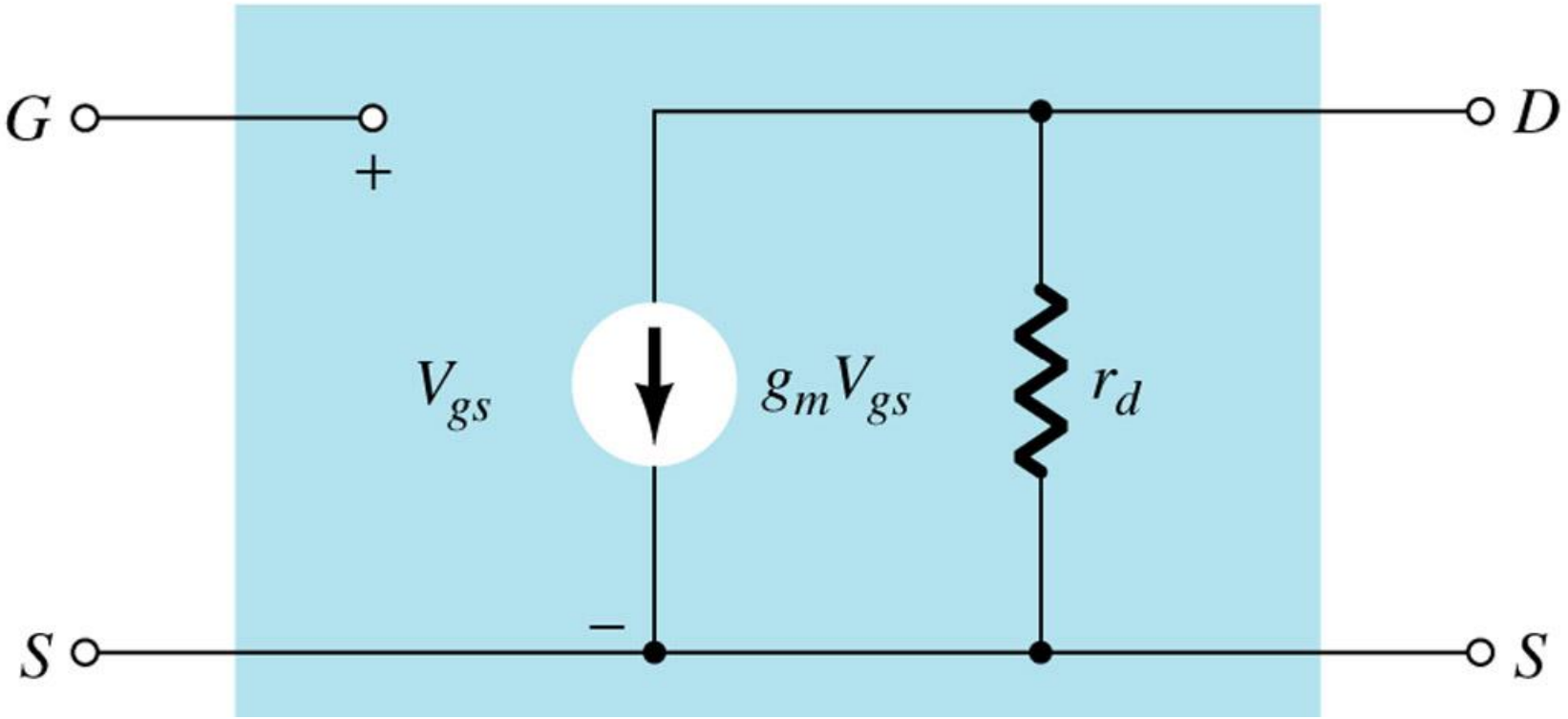
FET Amplification

Voltage gain (*Av*) for any amplifier can certainly be determined by the formula $A_V = V_{out}/V_{in}$ or in the case of an FET amplifier, $A_V = V_{ds}/V_{gs}$. A_V can also be determined by way of the transconductance and the drain resistor.

$$A_V = -g_m R_D$$

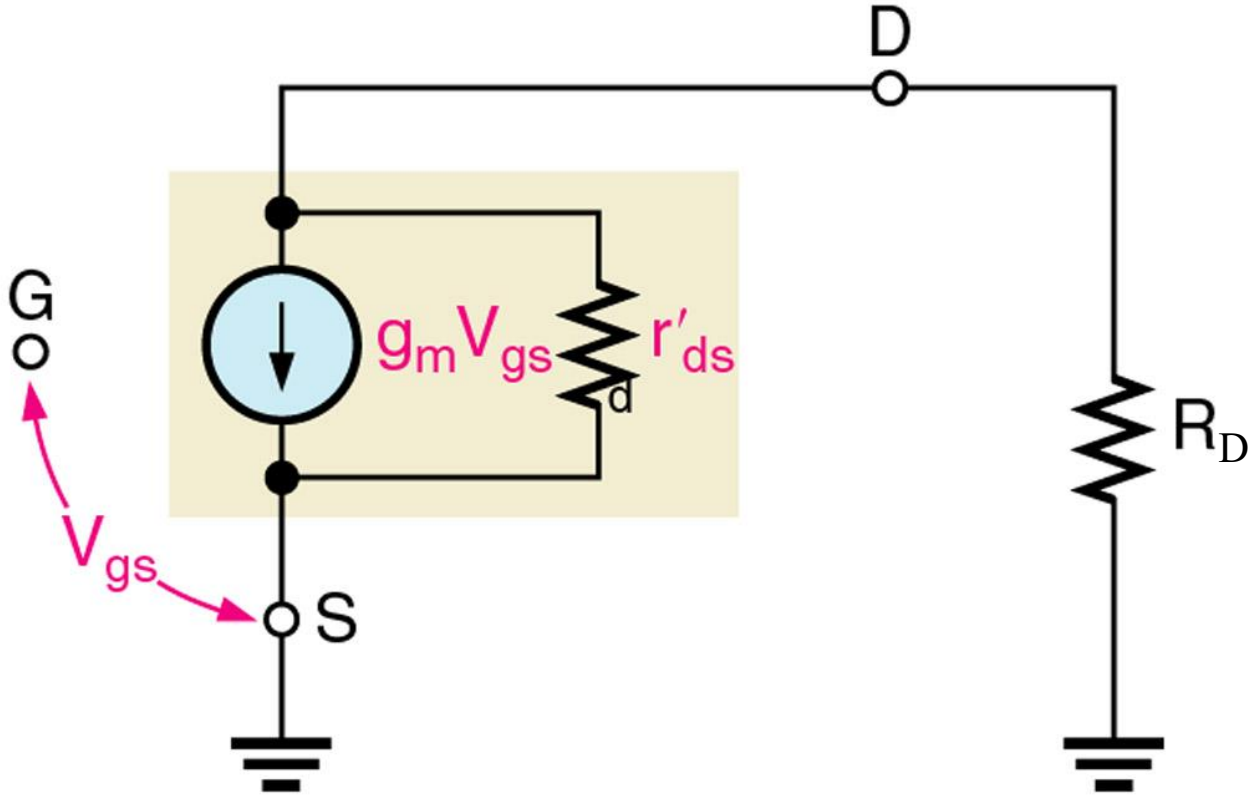


FET AC Equivalent Circuit



FET Amplification

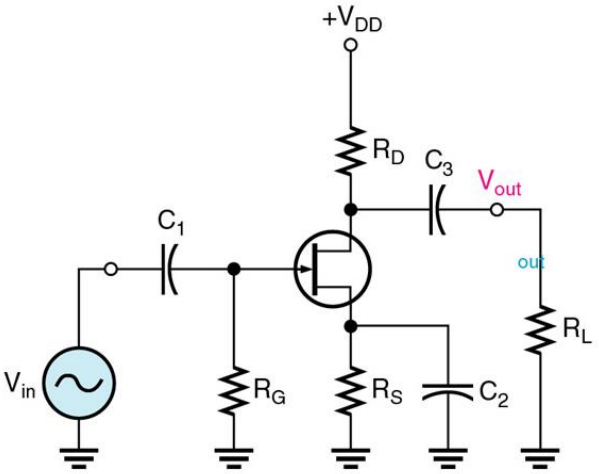
The r_{ds} can lower the gain if it is not sufficiently greater than R_D. Note that the two resistances are in parallel.



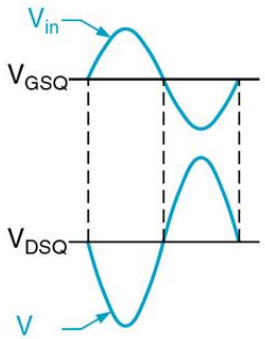
Common-Source Amplifiers

The common-source amplifier is biased such that the input stays within the linear range of operation.

The input signal voltage causes the gate to source voltage to swing above and below V_{GSQ} point, causing a corresponding swing in drain current. As the drain current increases, the voltage drop across R_D also increases, causing the drain voltage decrease. Clearly reveal a phase shift of 180^o between input and output voltages.



(a) Schematic



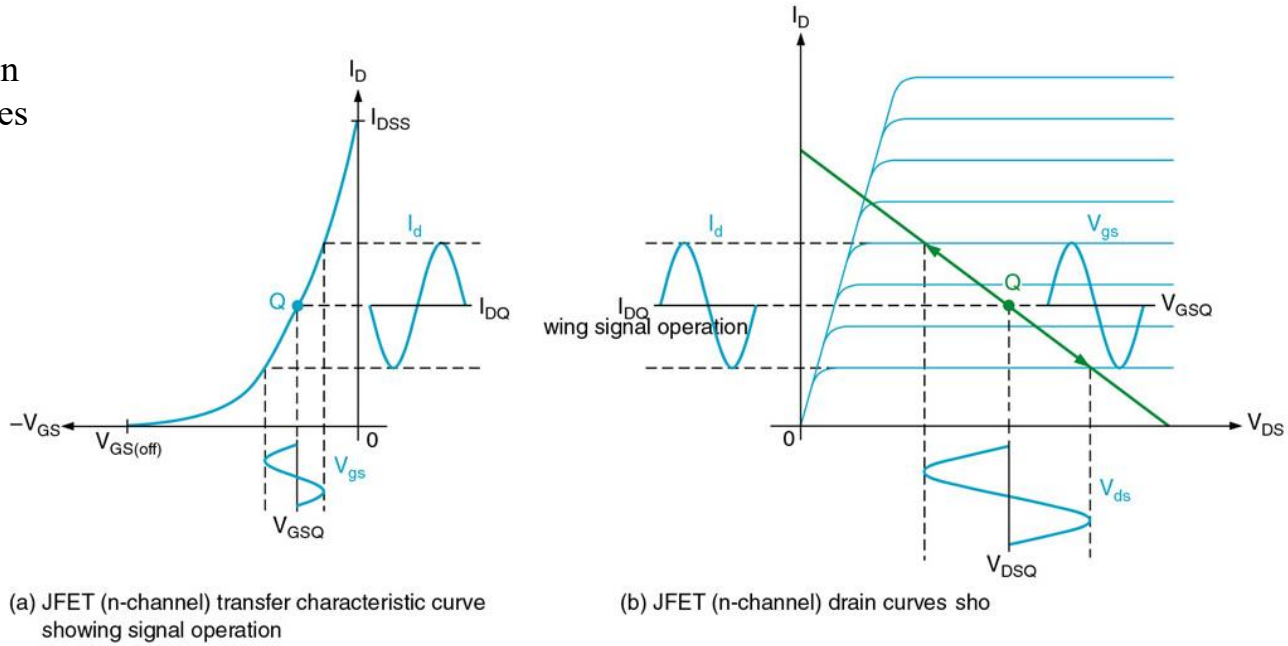
(b) Voltage waveform relationshi

Self biased common source amplifier. Note the source is at ac ground by way of C_2..

Common-Source Amplifiers

The transfer characteristic curve and drain curves with load line give us a graphical representation of how the input signal affects the drain current with relation to the Q-point.

a) The gate to source voltage swing above and below its V_{GS} value, when swing to negative value, ID decreases from its Q-point value and increase when swing to less negative value.



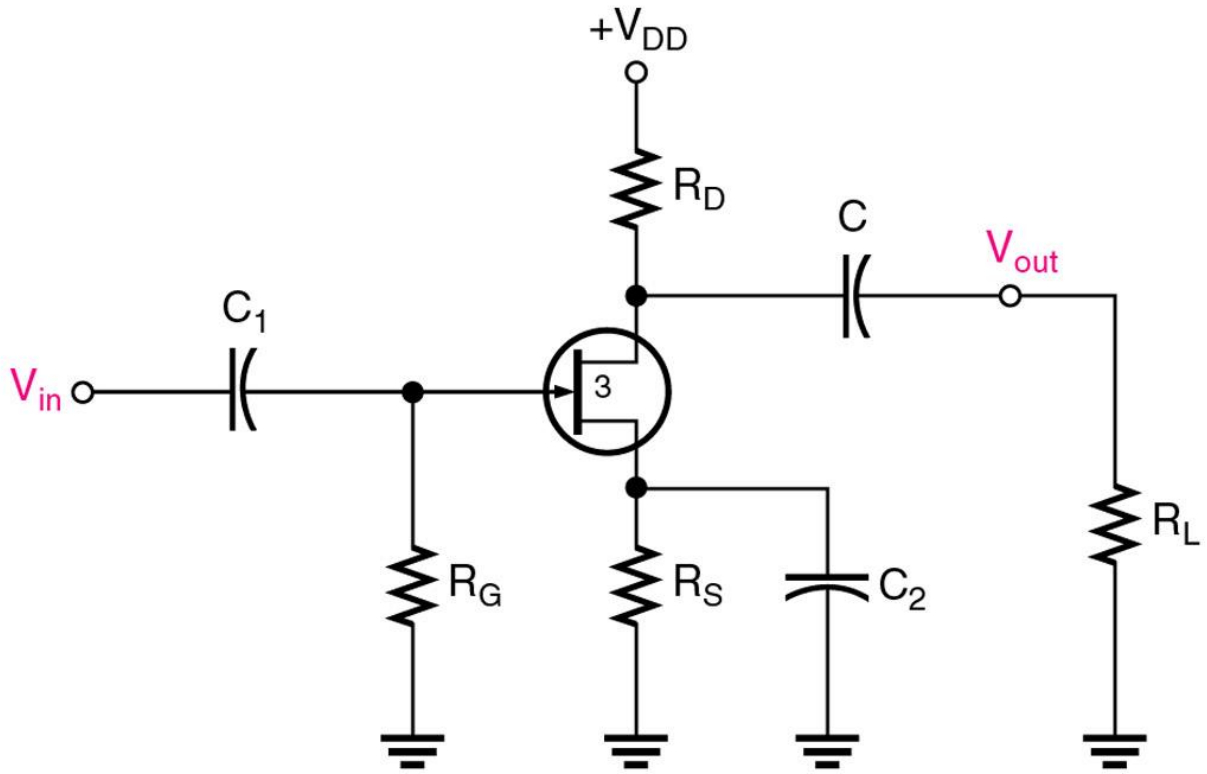
(a) JFET (n-channel) transfer characteristic curve showing signal operation

(b) JFET (n-channel) drain curves sho

b) View of the same operation using the drain curve. The signal at the gate drives the drain current equally above and below the Q-point on the load line, as indicate by arrows. Lines projected from the peak of the gate voltage across to I_D axis and down to the V_{DS} axis indicate the peak-to-peak variations of the drain current and the drain-to-source voltage.

Common-Source Amplifiers

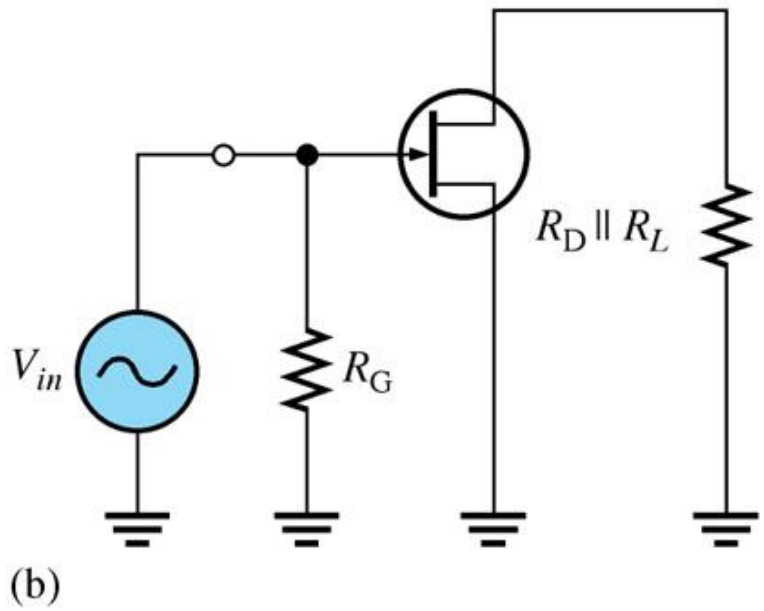
DC analysis of a common-source amplifier requires us to determine I_D. Biasing at midpoint is most common so I_D will be half of I_{DSS}. Note that the capacitors are viewed as open components when only dc is considered.



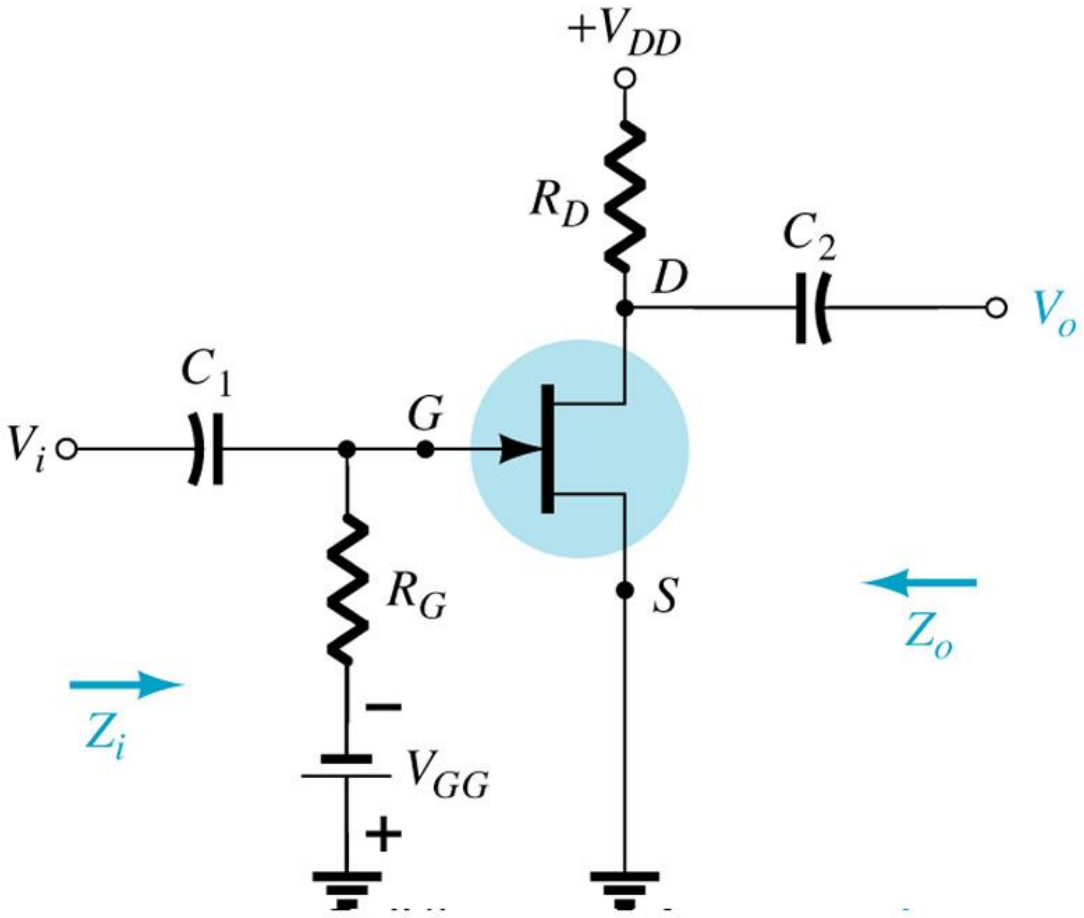
Common-Source Amplifiers

The load (R_L) must be considered when viewing the ac equivalent circuit of an FET amplifier, R_L is in parallel with the drain resistor (R_D). This will lower the gain by lowering the overall drain resistance which is represented by R_d. Calculation for R_d can be determined by parallel resistance calculation methods. Once R_d is determined the voltage gain can be determined by the familiar gain formula below.

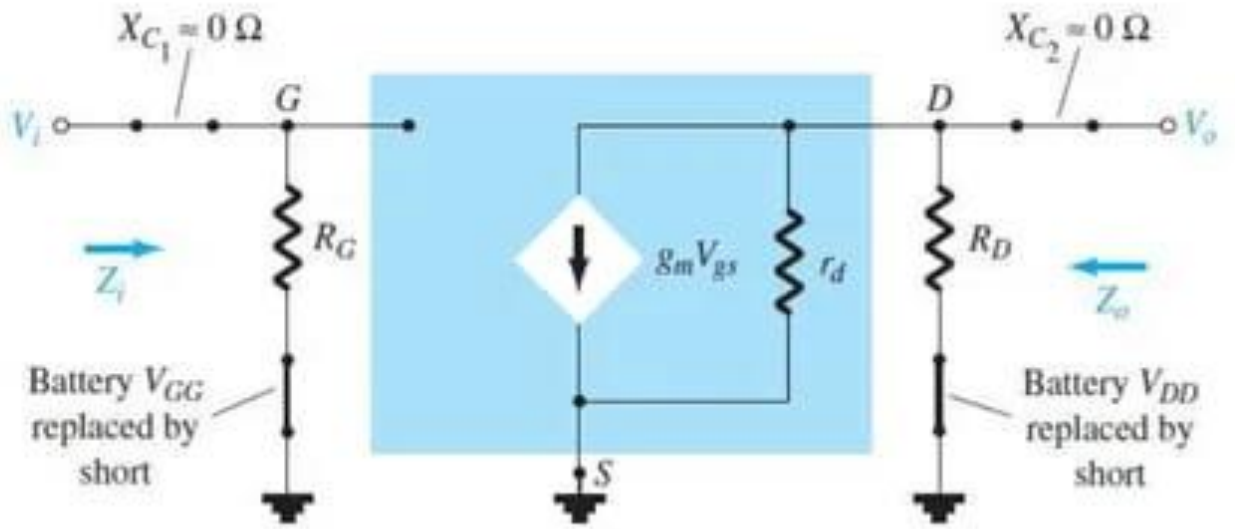
$$A_v = -g_m R_d$$

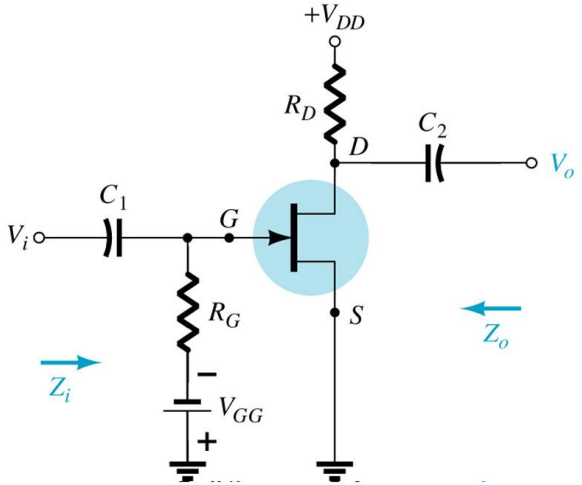


JFET Common-Source (CS) Fixed-Bias

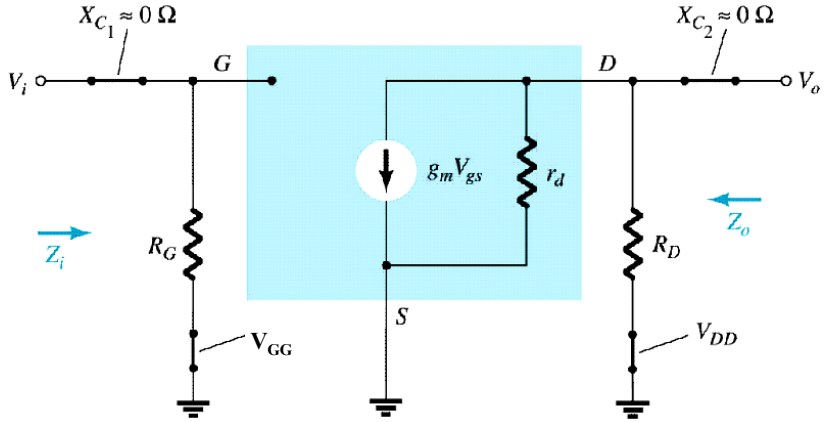


The input is on the gate and the output is on the drain.


$X_{C_1} \approx 0\ \Omega$
$X_{C_2} \approx 0\ \Omega$
V_i
V_o
G
D
S
R_G
R_D
$g_m V_{gs}$
r_d
Z_i
Z_o
Battery V_{GG} replaced by short
Battery V_{DD} replaced by short



JFET fixed-bias configuration

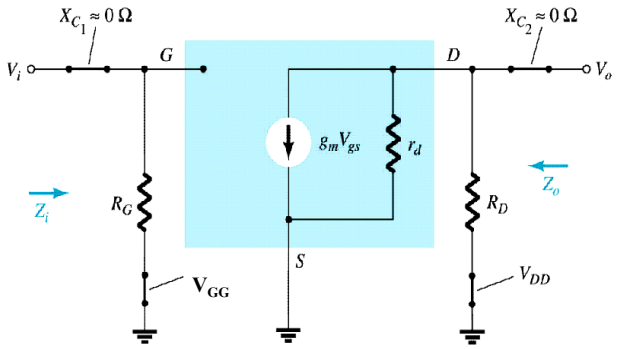


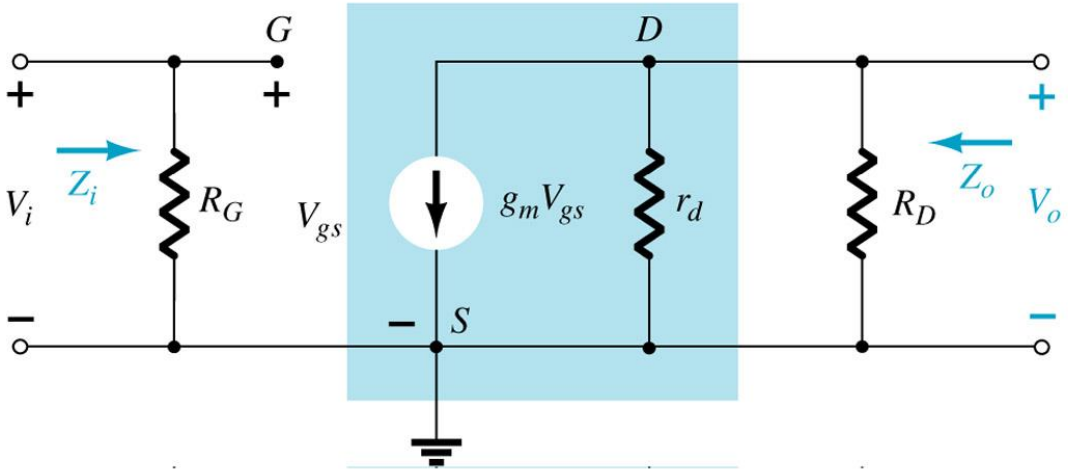
The JFET ac equivalent circuit

The *fixed-bias* configuration on fig. includes the coupling capacitors C1 and C2 that isolate the dc biasing arrangement from the applied signal and load; they act as short-circuit equivalents for the ac analysis.

Once the level of gm and rd are determined from the dc biasing arrangement, specification sheet, or characteristics, the ac equivalent model can be substituted between the appropriate terminals as shown in fig. Note that both capacitors have the short-circuit equivalent because the reactance Xc = $1/(2\pi fC)$ is sufficiently small compared to other impedance levels of the network, and the dc batteries V_{GG} and V_{DD} are set to zero volts by a short-circuit equivalent.

AC Equivalent Circuit





Input Impedance:

$$Zi = R_G$$

Output Impedance:

$$Zo = R_D \| r_d \qquad Zo \cong R_D \;\Big/_{r_d \geq 10R_D}$$

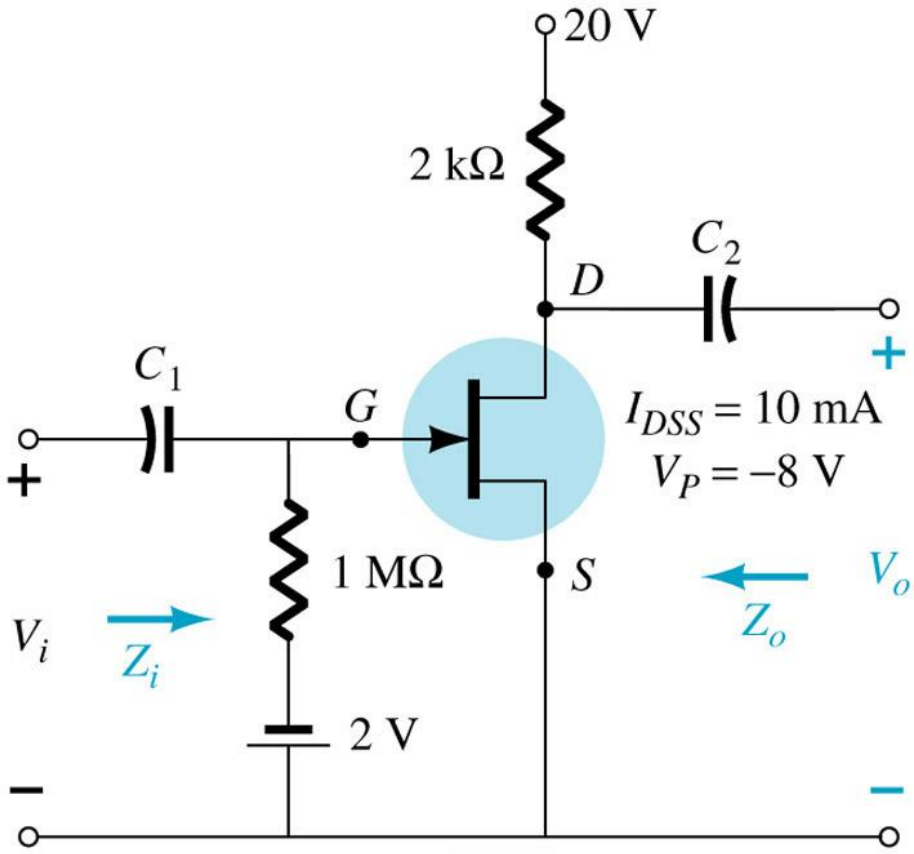
Voltage Gain:

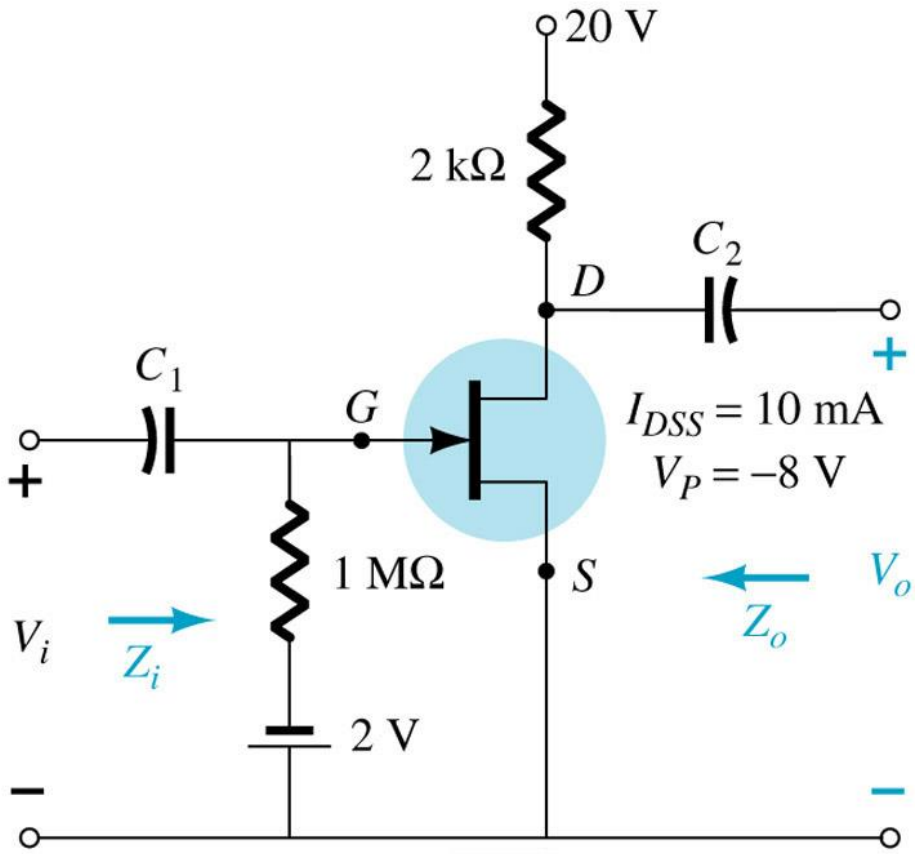
$$Av = \frac{Vo}{Vi} = -g_m(r_d \| R_D) \qquad Av = \frac{Vo}{Vi} = -g_m R_D \;\Big/_{r_d \geq 10R_D}$$

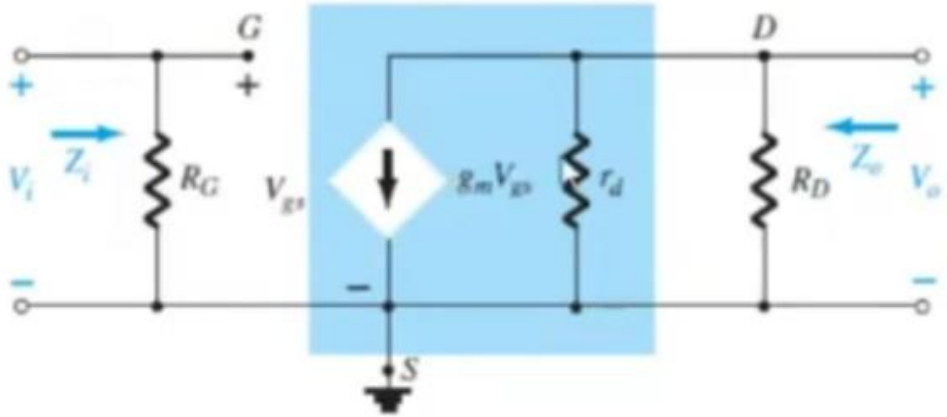
Phase Relationship: **CS amplifier configuration has a 180-degree phase shift between input and output.**

Example 1

The fixed-bias configuration of example had an operating point defined by $V_{GSQ} = -2$ V and $I_{DQ} = 5.625$ mA, with $I_{DSS} = 10$ mA and $V_P = -8$ V. The network is redrawn as Figure with an applied signal V_i . The value of y_{OS} is provided as 40 μS. Determine g_m, r_d, Z_i, Z_o, voltage gain A_v , A_v ignoring the effects of r_d.




20 V
2 kΩ
C_2
D
+
C_1
G
I_{DSS} = 10 mA
V_P = −8 V
+
1 MΩ
S
V_o
V_i
Z_i
Z_o
2 V
−
−

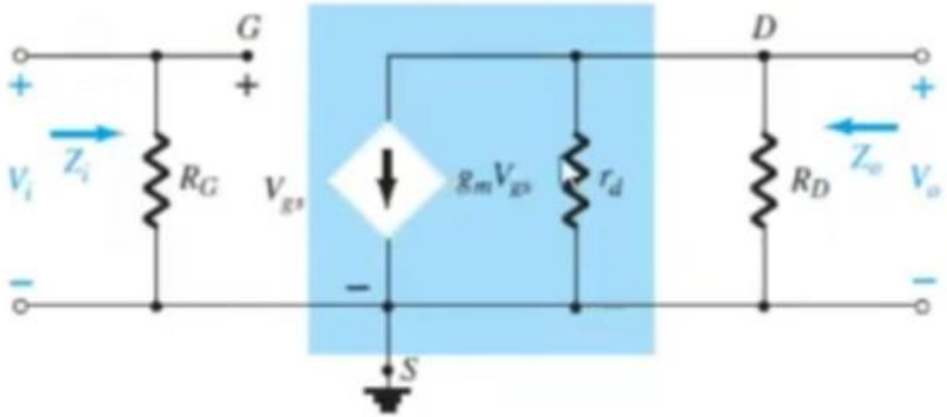

G
D
+
+
V_i
Z_i
R_G
V_{gs}
$g_m V_{gs}$
r_d
R_D
Z_o
V_o
−
−
S

Solution

(a) $$g_{mO} = \frac{21_{DSS}}{|V_P|} = \frac{2(10\text{mA})}{8\text{V}} = 2.5\text{mS}$$

$$g_m = g_{mo}\left(1 - \frac{V_{GS_Q}}{V_p}\right) = 2.5\,\text{mS}\left(1 - \frac{(-2\text{V})}{(-8\text{V})}\right) = 1.88\,\text{mS}$$

(b) $$r_d = \frac{1}{y_{os}} = \frac{1}{40\mu\text{S}} = 25\,\text{k}\Omega$$



(c) $Z_i = R_G = 1\ \text{M}\Omega$

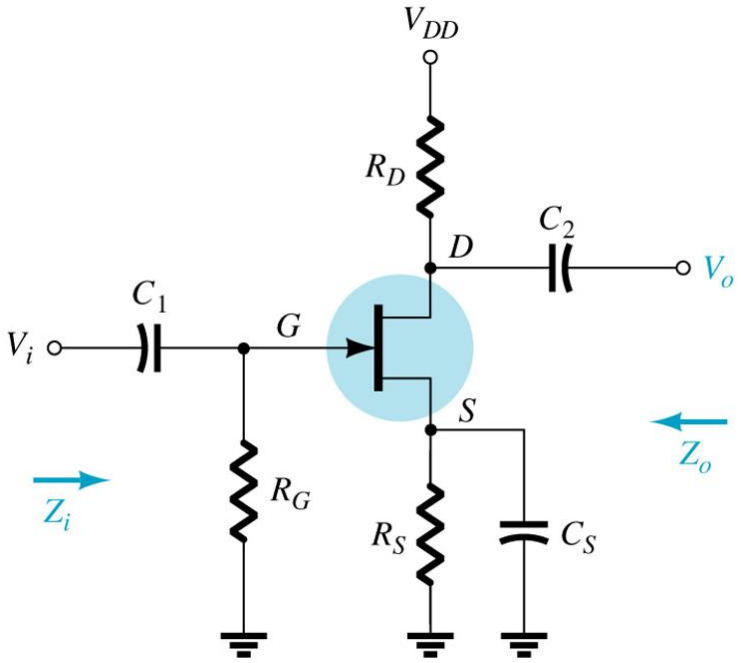
(d) $Z_o = R_D \,\|\, r_d = 2\text{k}\Omega \,\|\, 25\text{k}\Omega = 1.85\text{k}\Omega$

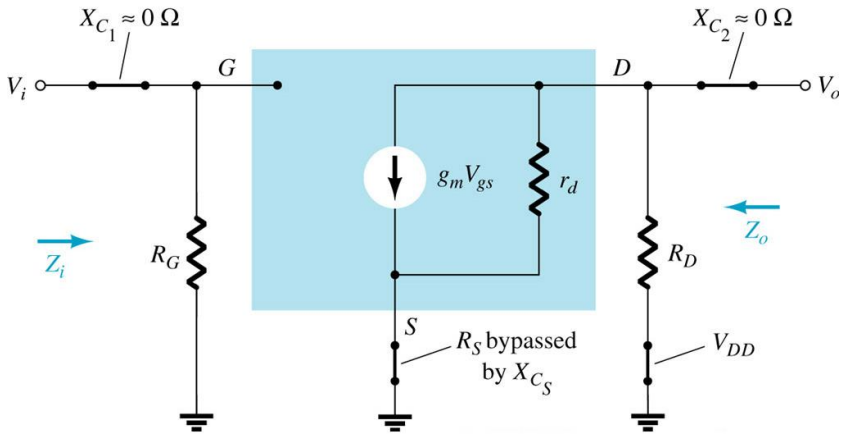
(e) $A_V = -g_m (R_D \,\|\, r_d) = -(1.88\,\text{mS})(1.85\,\text{k}\Omega) = -3.48$

(f) $A_V = -g_m R_D = -(1.88\ \text{mS})(2\ \text{k}\Omega) = -3.76$

As demonstrated in part (f), a ratio of 25 kΩ : 2 kΩ = 12.5 : 1 between rd and RD resulted in a difference of 8% in the solution.

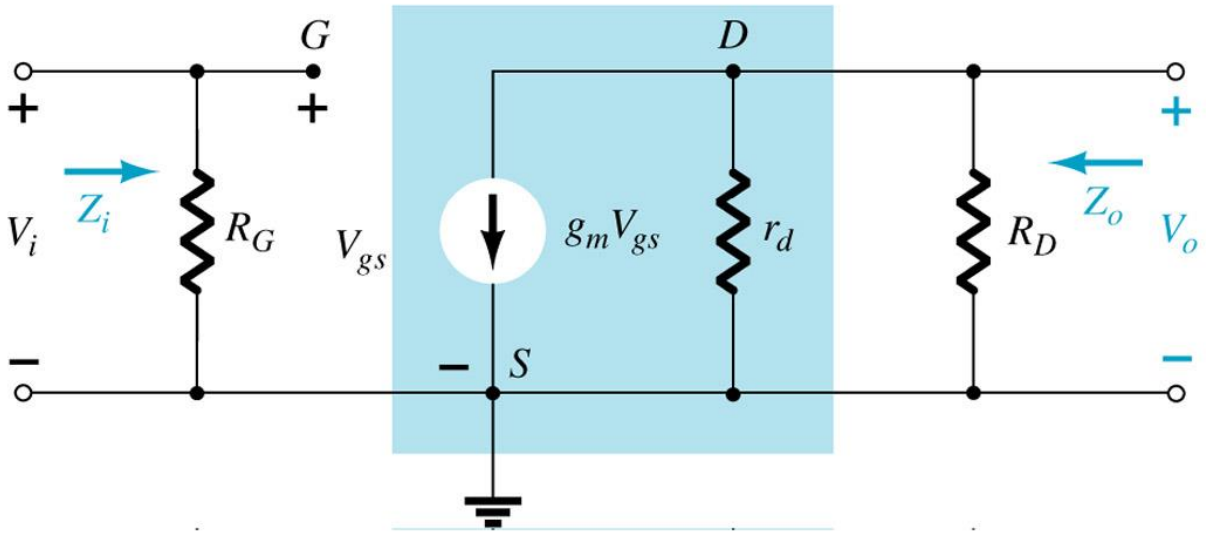
JFET CS Self-Bias Configuration





This is a CS amplifier configuration therefore the input is on the gate and the output is on the drain.

AC Equivalent Circuit



Input Impedance:

$$Zi = R_G$$

Output Impedance:

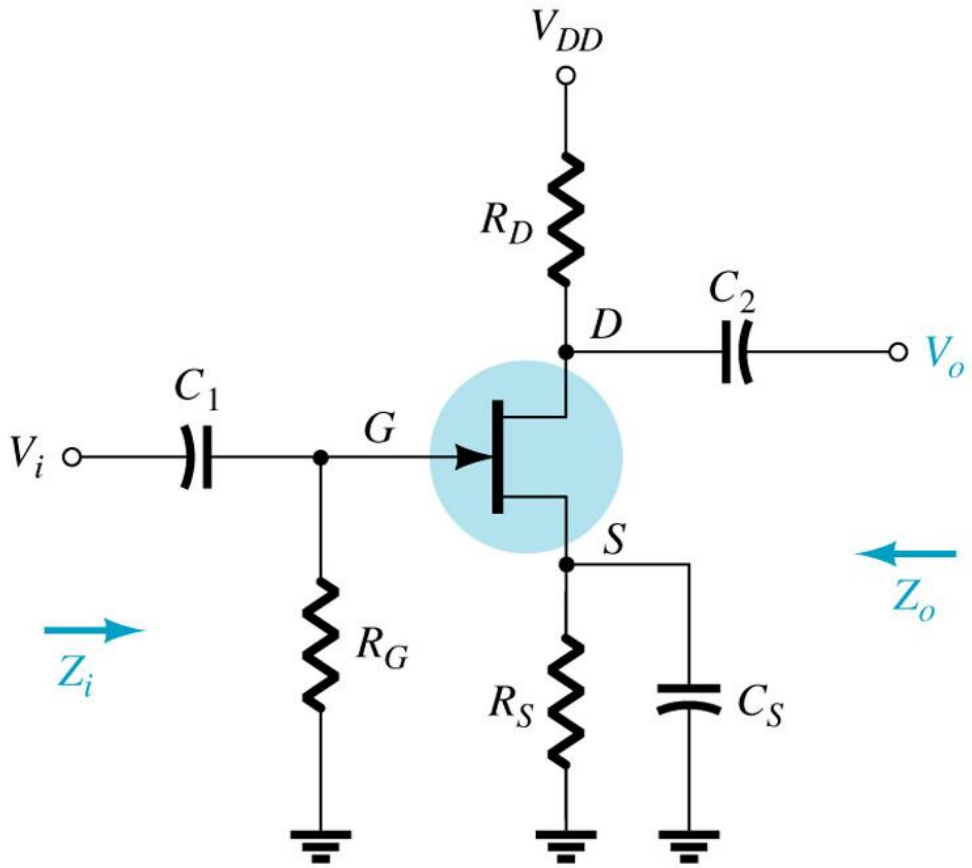
$$Zo = R_D \| r_d \qquad Zo \cong R_D \;\big/_{r_d \geq 10R_D}$$

Voltage Gain:

$$Av = \frac{Vo}{Vi} = -g_m(r_d \| R_D) \qquad Av = \frac{Vo}{Vi} = -g_m R_D \;\big/_{r_d \geq 10R_D}$$

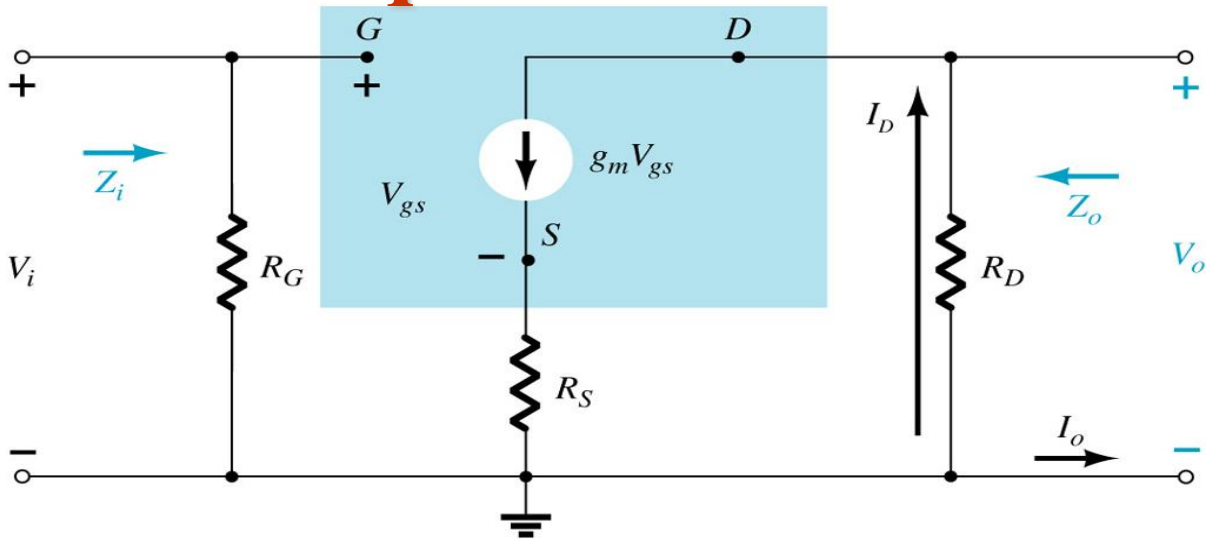
Phase Relationship: **CS amplifier configuration has a 180-degree phase shift between input and output.**

JFET CS Self-Bias Configuration – Unbypassed Rs



If Cs is removed, it affects the gain of the circuit.

AC Equivalent Circuit



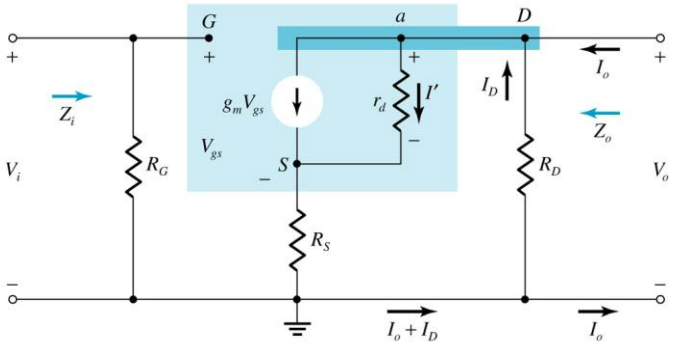
Input Impedance: $Zi = R_G$

Output Impedance: $Zo = R_D \,/\, r_d \geq 10R_D$

Voltage Gain:

$$Av = \frac{Vo}{Vi} = -\frac{g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$$

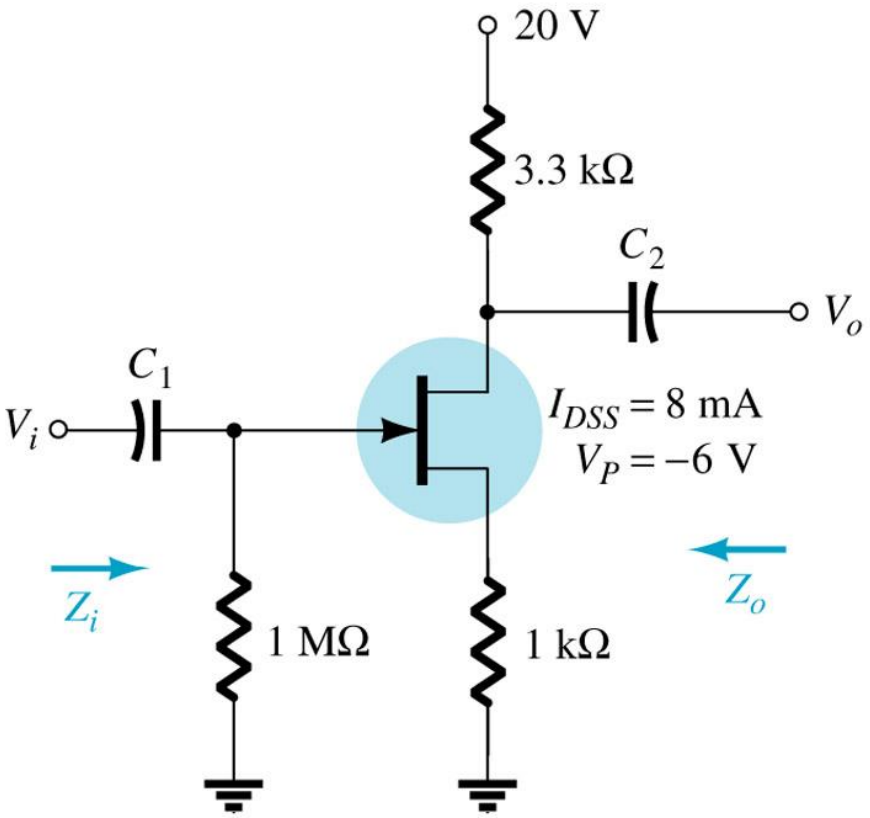
$$Av = \frac{Vo}{Vi} = -\frac{g_m R_D}{1 + g_m R_S} \,/\, r_d \geq 10(R_D + R_S)$$



If r_d is included in the network

Example 2

The self-bias configuration of example 2 has an operating point defined by V_{GSQ} = -2.6 V and I_{Dq} = 2.6 mA, with I_{DSS} = 8 mA and V_P = -6 V. The network is redrawn as figure with an applied signal V_i. The value of y_{OS} is given as 20 μS. Determine g_m, r_d, Z_i, Z_O with and without the effects of r_d. and A_V with and without the effects of r_d .

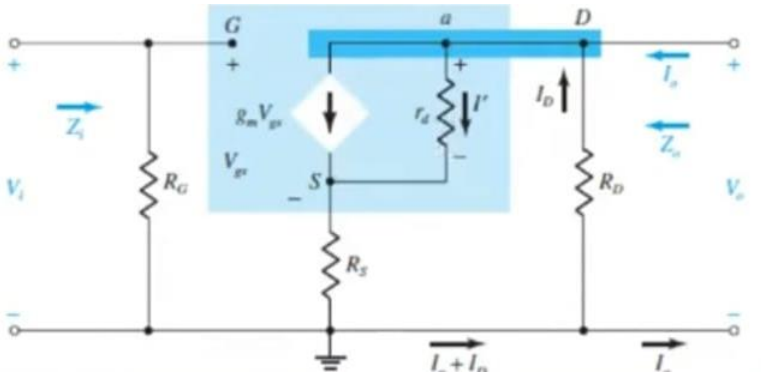


Solution

(a) $$g_{mo} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8\,\text{mA})}{6\,\text{V}} = 2.67\,\text{mS}$$

$$g_m = g_{mo}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.67\,\text{mS}\left(1 - \frac{(-2.6\,\text{V})}{(-6\,\text{V})}\right) = 1.51\,\text{mS}$$

(b) $$r_d = \frac{1}{y_{OS}} = \frac{1}{20\mu S} = 50\,\text{k}\Omega$$



(c) $Z_i = R_G = 1\,\text{M}\Omega$

(d) With r_d: $r_d = 50\,\text{k}\Omega > 10\,R_D = 33\,\text{k}\Omega$

therefore, $Z_o = R_D = 3.3\,\text{k}\Omega$

If $r_d = \infty\,\Omega$, $Z_o = R_D = 3.3\,\text{k}\Omega$

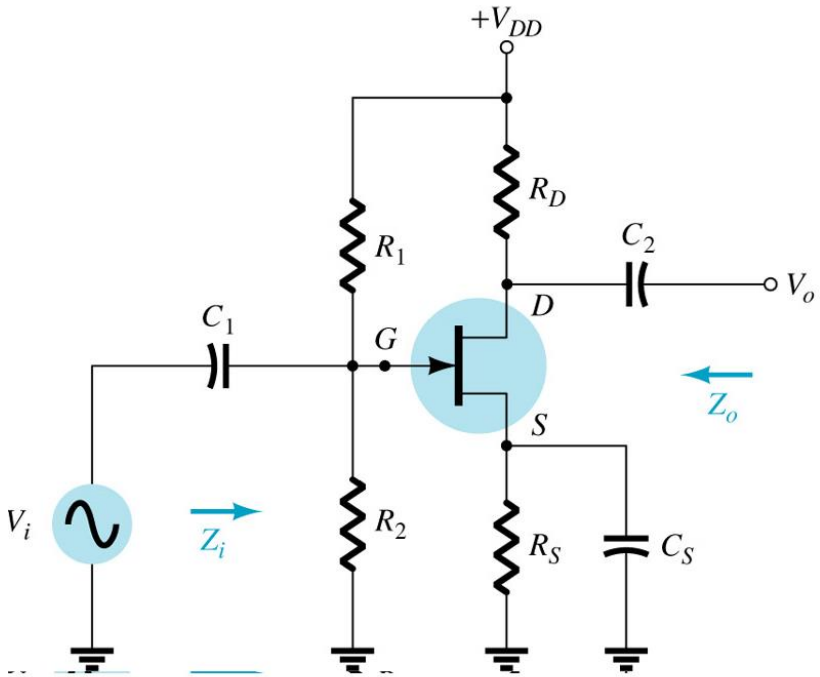
(e) With r_d : $$A_V = \frac{-g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

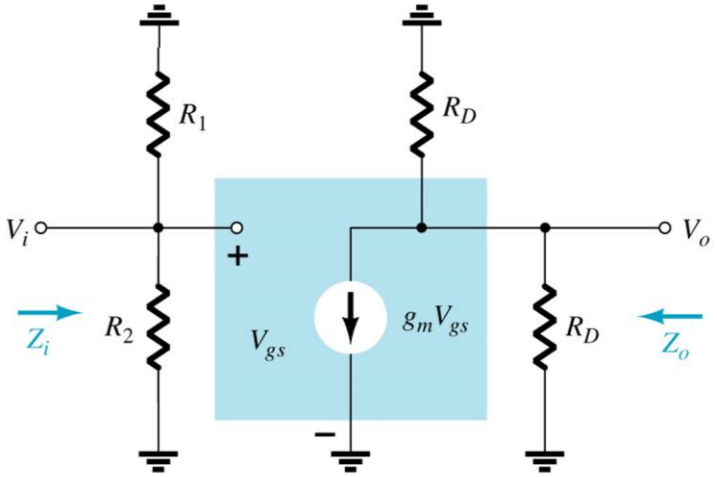
$$= \frac{-(1.51\,\text{mS})(3.3\,\text{k}\Omega)}{1 + (1.51\,\text{mS})(1\text{k}\Omega) + \frac{3.3\,\text{k}\Omega + 1\,\text{k}\Omega}{50\,\text{k}\Omega}} = -1.92$$

(f) Without r_d : $$A_V = \frac{-g_m R_D}{1 + g_m R_S} = \frac{-(1.51\,\text{mS})(3.3\,\text{k}\Omega)}{1 + (1.51\,\text{mS})(1\text{k}\Omega)}$$

$$= -1.98$$

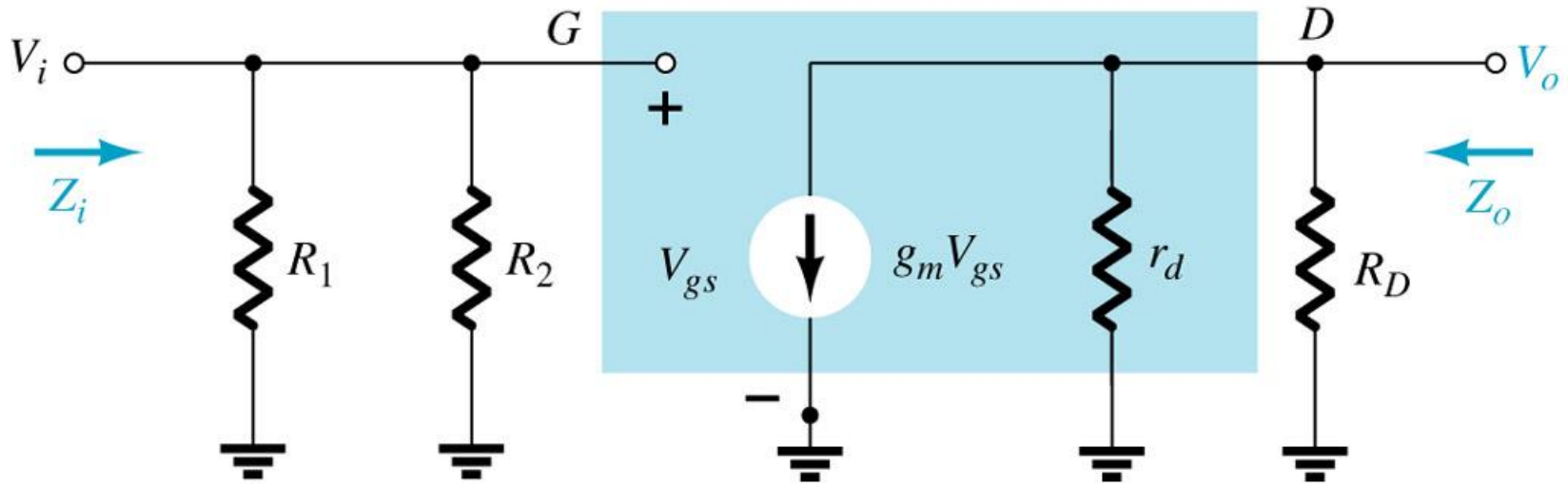
JFET CS Voltage-Divider Configuration





This is a CS amplifier configuration therefore the input is on the gate and the output is on the drain.

AC Equivalent Circuit



Input Impedance: $Zi = R_1 || R_2$

Output Impedance: $Zo = r_d || R_D$ $\quad Zo \cong R_D \;/_{r_d \geq 10R_D}$

Voltage Gain: $Av = -g_m(r_d || R_D)$ $\quad Av \cong -g_m R_D \;/_{r_d \geq 10R_D}$

Ninevah University
College of Electronics Engineering
Department of Systems and Control

Electronic I I
Lecture 5 Part 2

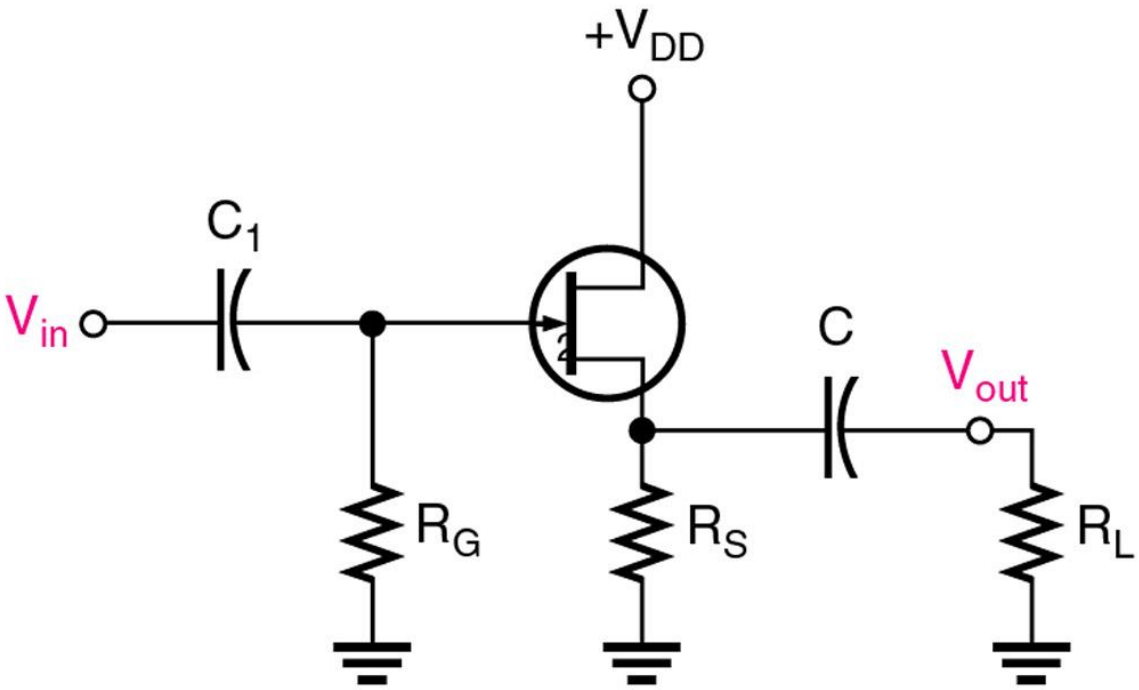
Common-DrainAmplifier

by
Rafal Raed Mahmood Alshaker

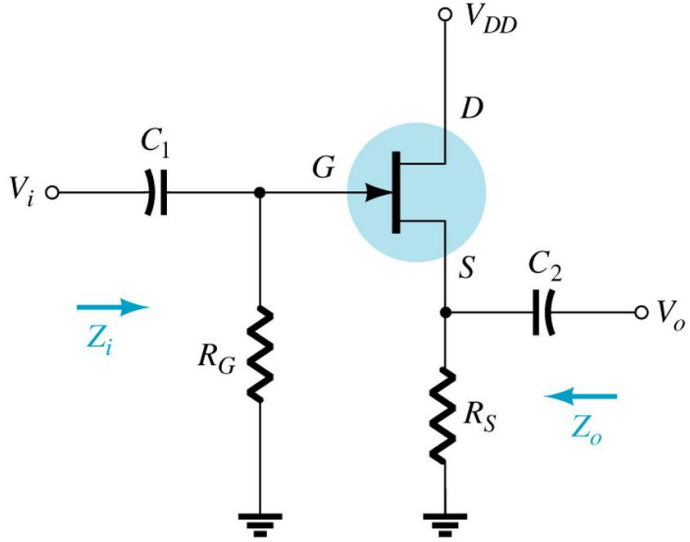
2nd Class

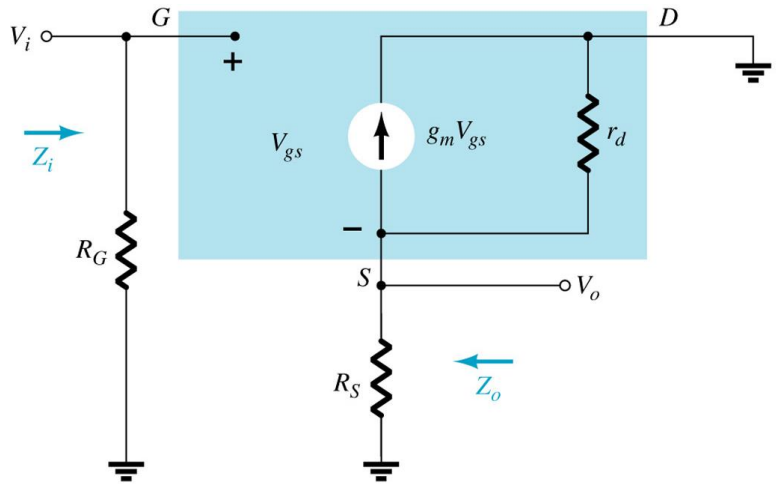
Common-Drain Amplifiers

The common-drain amplifier is similar to the common-collector BJT amplifier in that the V_{in} is the same as V_{out} with no phase shift. The gain is actually slightly less than 1. Note the output is taken from the source.



JFET Source Follower (Common-Drain) Configuration

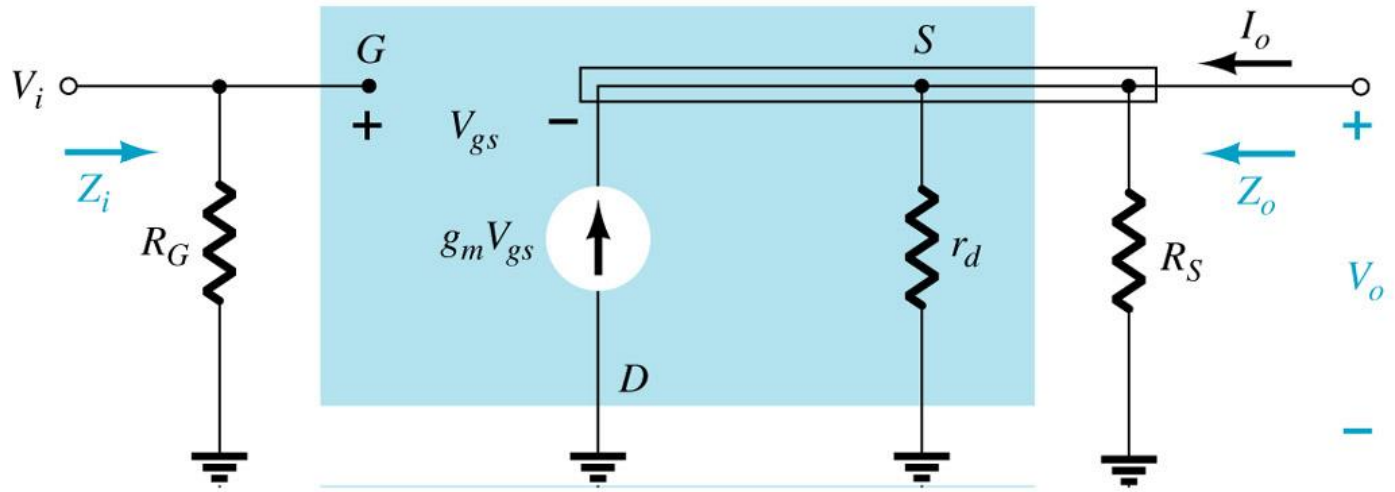




In a CD amplifier configuration, the input is on the gate, but the output is from the source.

The controlled source and terminal output impedance of the JFET are tied to ground at one end and R_S on the other, with VO across R_S. Since $g_m V_{gs}$, r_d and R_S are connected to the same terminal and ground they can all be placed in parallel. The current source reversed direction but V_{GS} is still defined between the gate and source terminals.

AC Equivalent Circuit



Input Impedance: $Zi = R_G$

Output Impedance: $Zo = r_d \| R_S \| \frac{1}{g_m}$

$Zo \cong R_S \| \frac{1}{g_m} \Big/ r_d \geq 10R_S$

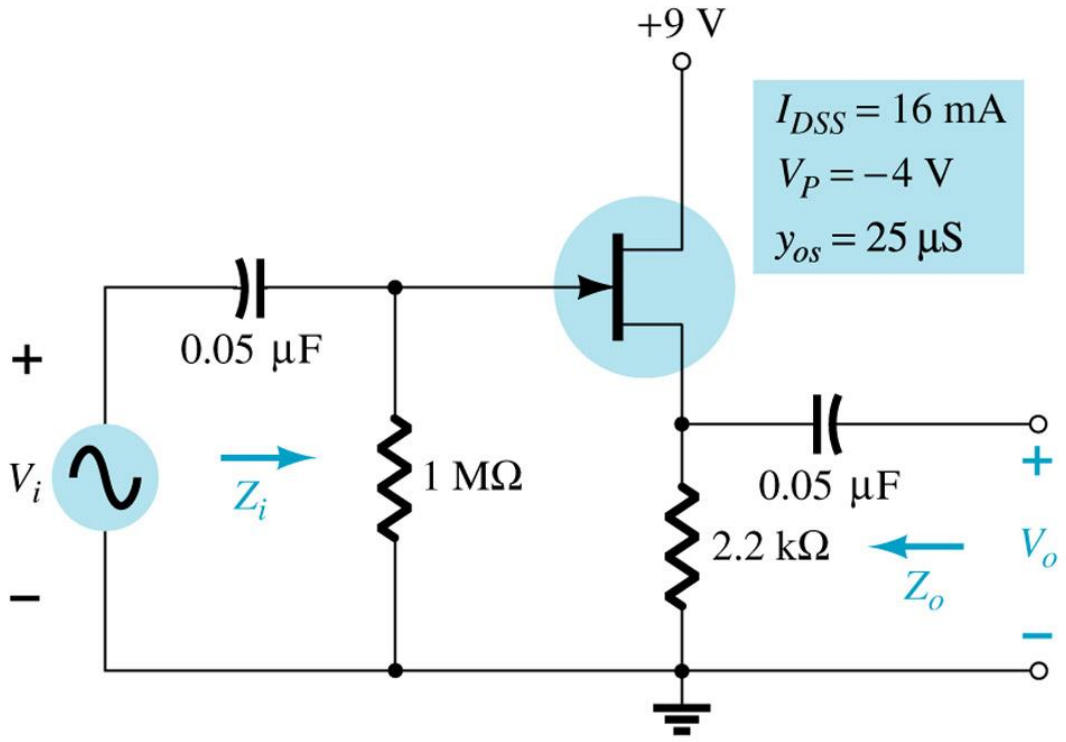
Voltage Gain: $Av = \frac{Vo}{Vi} = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}$

$Av = \frac{Vo}{Vi} = \frac{g_m R_S}{1 + g_m R_S} \Big/ r_d \geq 10R_S$

Phase Relationship: CD amplifier configuration has no phase shift between input and output.

Example 3

A dc analysis of the source-followed network of figure will result in V_{GSQ} = -2.86 V and I_{DQ} = 4.56 mA. Determine g_m , r_d, Z_i, Z_o with and without the effects of r_d and A_V with and without the effects of r_d.



Solution

(a) $$g_{mo} = \frac{2 I_{DSS}}{|V_P|} =$$

$$g_m = g_{mo}\left(1 - \frac{V_{GS_Q}}{V_P}\right) =$$

(b) $$r_d = \frac{1}{y_{os}} =$$

(c) $Z_i = R_G =$

(d) With r_d : $Z_O = r_d \| R_S \| 1/g_m =$

Without rd : $Z_O = R_S \| 1/g_m =$

(d) With rd : $$A_V = \frac{g_m (r_d \| R_S)}{1 + g_m (r_d \| R_S)} =$$

Without rd : $$A_V = \frac{g_m R_S}{1 + g_m R_S} =$$

Solution

(a) $$g_{mo} = \frac{2\,I_{DSS}}{|V_P|} = \frac{2(16\,\text{mA})}{4\text{V}} = 8\text{mS}$$

$$g_m = g_{mo}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 8\,\text{mS}\left(1 - \frac{(-2.86\,\text{V})}{(-4\,\text{V})}\right) = 2.28\,\text{mS}$$

(b) $$r_d = \frac{1}{y_{os}} = \frac{1}{25\,\mu S} = 40\,\text{k}\Omega$$

(c) $Z_i = R_G = 1\,\text{M}\Omega$

(d) With r_d ; $$Z_O = r_d \,\|\, R_S \,\|\, 1/g_m = 40\,\text{k}\Omega \,\|\, 22\,\text{k}\Omega \,\|\, 1/2.28\,\text{mS}$$

$$= 40\,\text{k}\Omega \,\|\, 22\,\text{k}\Omega \,\|\, 438.6\,\Omega$$

$$= 362.52\,\Omega$$

revealing that Z_O is often relatively small and determined primarily by $1/g_m$.

Without r_d ; $$Z_O = R_S \,\|\, 1/g_m = 2.2\,\text{k}\Omega \,\|\, 438.6\Omega = 365.69\,\Omega$$

revealing that r_d typically has little impact on Z_O

(e) With r_d ;

$$A_v = \frac{g_m (r_d \| R_s)}{1 + g_m (r_d \| R_s)} = \frac{(2.28\,\text{mS})(40\,\text{k}\Omega \| 2.2\,\text{k}\Omega)}{1 + (2.28\,\text{mS})(40\text{k}\Omega \| 2.2\text{k}\Omega)}$$

$$= \frac{(2.28\,\text{mS})(2.09\,\text{k}\Omega)}{1 + (2.28\,\text{mS})(2.09\,\text{k}\Omega)}$$

$$= \frac{4.77}{1 + 4.77}$$

$$= 0.83$$

which is less than 1 as predicted above.

Without r_d ;

$$A_v = \frac{g_m R_s}{1 + g_m R_s}$$

$$= \frac{(2.28\,\text{mS})(2.2\,\text{k}\Omega)}{1 + (2.28\,\text{mS})(2.2\,\text{k}\Omega)}$$

$$= \frac{5.02}{1 + 5.02}$$

$$= 0.83$$

revealing that r_d usually has little impact on the gain of the configuration.

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Electronic I I
Lecture 6

AC Configurations of (JFET) and (MOSFET) Amplifier

by
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2nd Class

Topics of this lecture

1 . **Common-Gate Amplifiers**

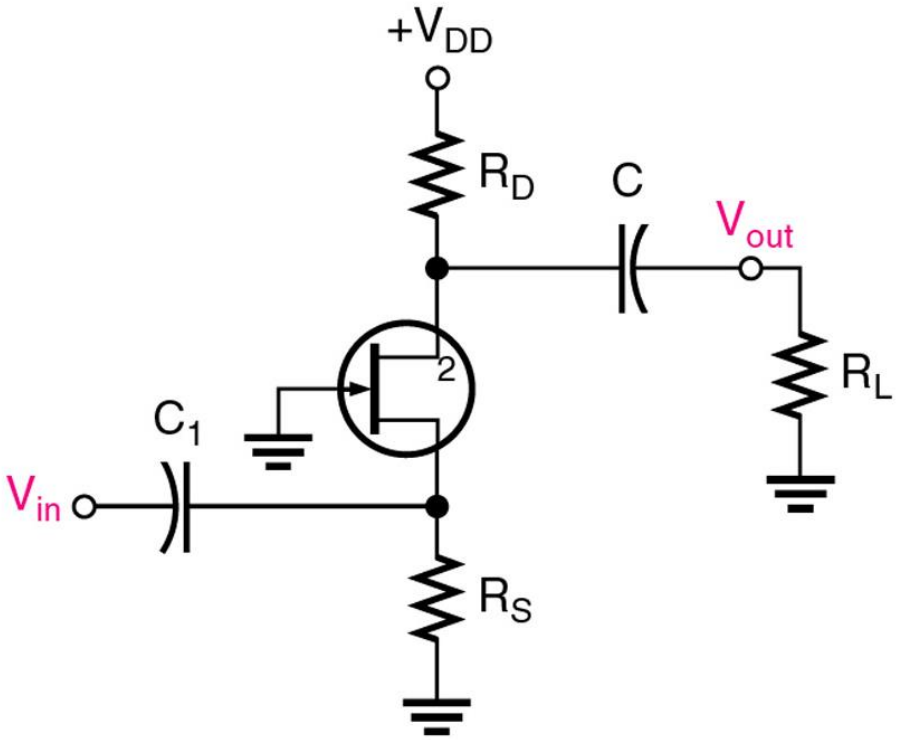
2. **D-MOSFET Amplifier**
Example

3. **E-MOSFET Amplifier**
Example

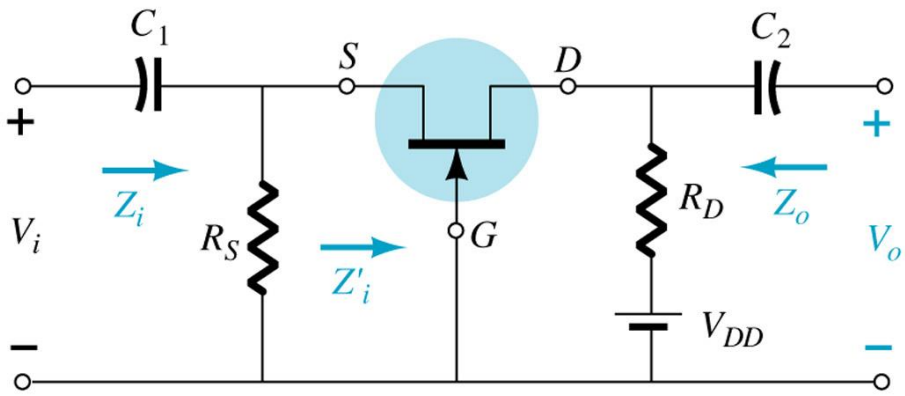
Common-Gate Amplifiers

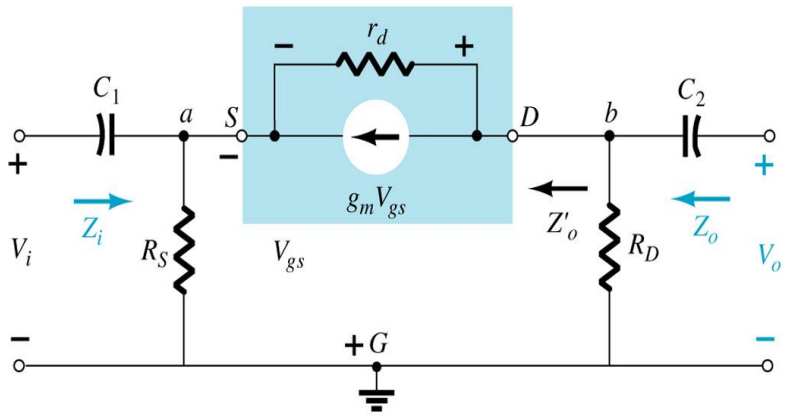
The common gate is similar to the common base BJT amplifier in that it has a low input resistance. The voltage gain can be determined by the same formula as used with the JFET common-source amplifier. The input resistance can be determined by the formula below.

$R_{in(source)} = 1/g_m$



JFET Common-Gate Configuration

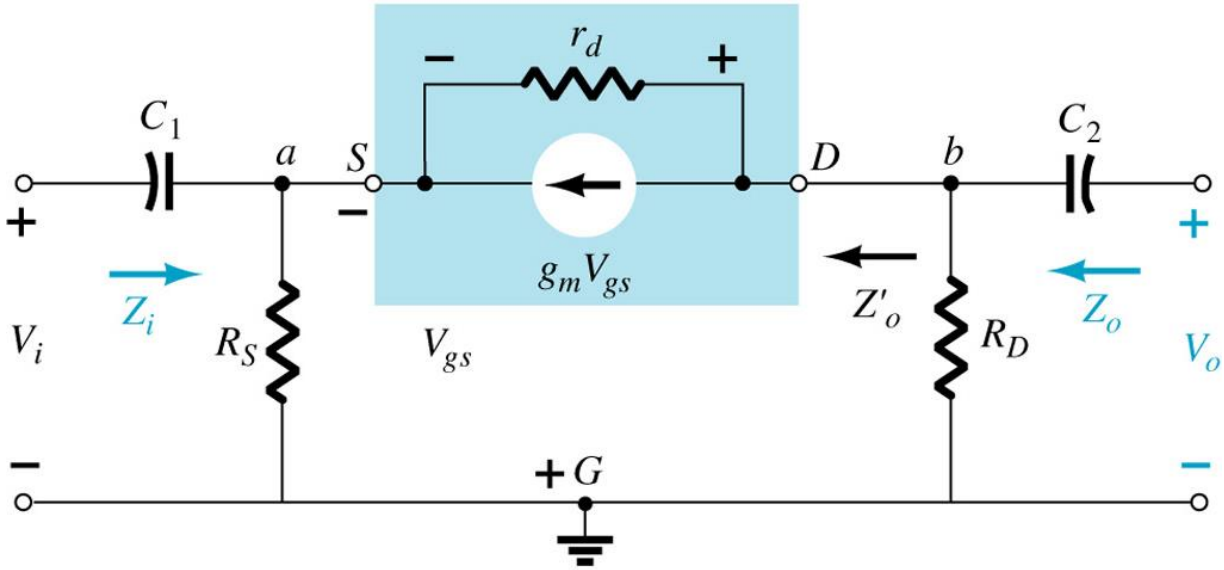




The input is on source and the output is on the drain.

Substituting the JFET equivalent circuit will result in Fig. Note the continuing requirement that the controlled source $g_m V_{gs}$ be connected from drain to source with r_d in parallel. The isolation between input and output circuits has obviously been lost since the gate terminals is now connected to the common ground of the network. In addition, the resistor connected between input terminals is no longer R_G but the resistor R_S connected from source to ground. Note also the location of the controlling voltage V_{gs} and the fact that it appears directly across the resistor R_S.

AC Equivalent Circuit



Input Impedance: $Zi = R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d} \right]$ $Zi \cong R_S \| (1/g_m) \;/\; r_d \geq 10R_D$

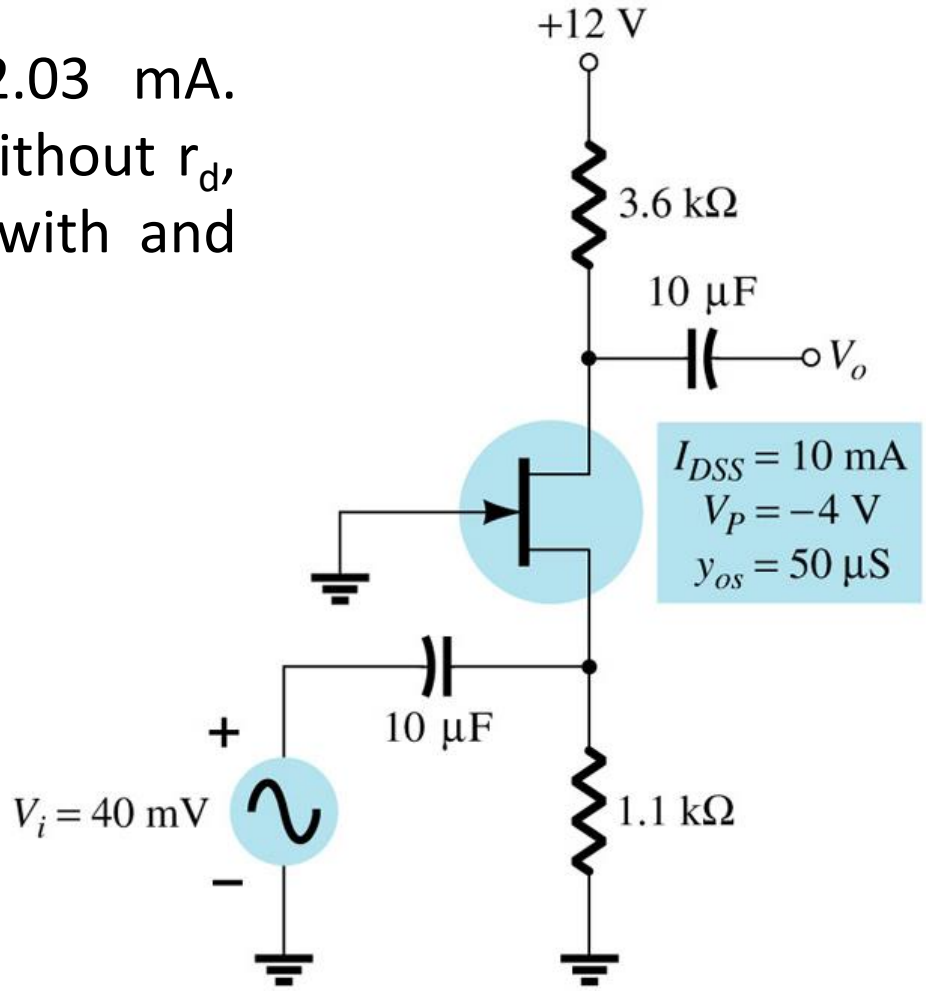
Output Impedance: $Zo = R_D \| r_d$ $Zo \cong R_D \;/\; r_d \geq 10R_D$

Voltage Gain: $Av = \frac{Vo}{Vi} = \frac{\left[g_m R_D + \frac{R_D}{r_d} \right]}{\left[1 + \frac{R_D}{r_d} \right]}$ $Av = g_m R_D \;/\; r_d \geq 10R_D$

Phase Relationship: CG amplifier configuration has no phase shift between input and output.

Example 4

If V_{GSQ} = -2.2 V and I_{DQ} = 2.03 mA. Determine g_m, r_d, Z_i with and without r_d, Z_o with and without r_d and V_o with and without r_d .



Solution

(a) $$g_{mO} = \frac{21_{DSS}}{|V_p|} = \frac{2(10\text{mA})}{4\text{V}} = 5\text{mS}$$

$$g_m = g_{mO}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 5\text{mS}\left(1 - \frac{(-2.2\text{V})}{(-4\text{V})}\right) = 2.25\text{mS}$$

(b) $$r_d = \frac{1}{y_{os}} = \frac{1}{50\mu\text{S}} = 20\text{k}\Omega$$

(c) With r_d ,

$$Z_i = R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d}\right] = 1.1\text{k}\Omega \| \left[\frac{20\text{k}\Omega + 3.6\text{k}\Omega}{1 + (2.25\text{ms})(20\text{k}\Omega\text{k}}\right]$$

$$= 1.1\,\text{k}\Omega \| 0.51\text{k}\Omega = 0.35\text{k}\Omega$$

Without r_d,

$$Z_i = R_s \| 1/g_m = 1.1\text{k}\Omega \| 1/2.25\text{ms} = 1.1\,\text{k}\Omega \| 0.44\text{k}\Omega$$

$$= 0.31\,\text{k}\Omega$$

Even though the condition,

$r_d \geq 10\, R_D = > 20k\Omega \geq 10(3.6\,k\Omega) = > 20\,k\Omega \geq 36\,k\Omega$

Is not satisfied, both equations result in essentially the same level of impedance. In this case, 1/gm was the predominant factor.

(d) With r_d,

$$Z_o = R_D \,\|\, r_d = 3.6\,k\Omega \,\|\, 20\,k\Omega = 3.05\,k\Omega$$

Without r_d,

$Z_O = R_D = 3.6\,k\Omega$

Again the condition $r_d \geq 10\, R_D$ is not satisfied, but both result are resonably close. R_D is certainly the prodominant factor in this example.

(e) With r_d,

$$A_v = \frac{\left[g_m R_D + \frac{R_D}{r_d} \right]}{\left[1 + \frac{R_D}{r_d} \right]} = \frac{\left[(2.25mS)(3.6k\Omega) + \frac{3.6k\Omega}{20k\Omega} \right]}{\left[1 + \frac{3.6k\Omega}{20k\Omega} \right]}$$

$$= \frac{8.1 + 0.18}{1 + 0.18} = 7.02$$

and $A_v = \frac{V_o}{V_i} \Rightarrow V_o = A_v V_i = (7.02)(40\,mV) = 280.8\,mV$

without r_d,

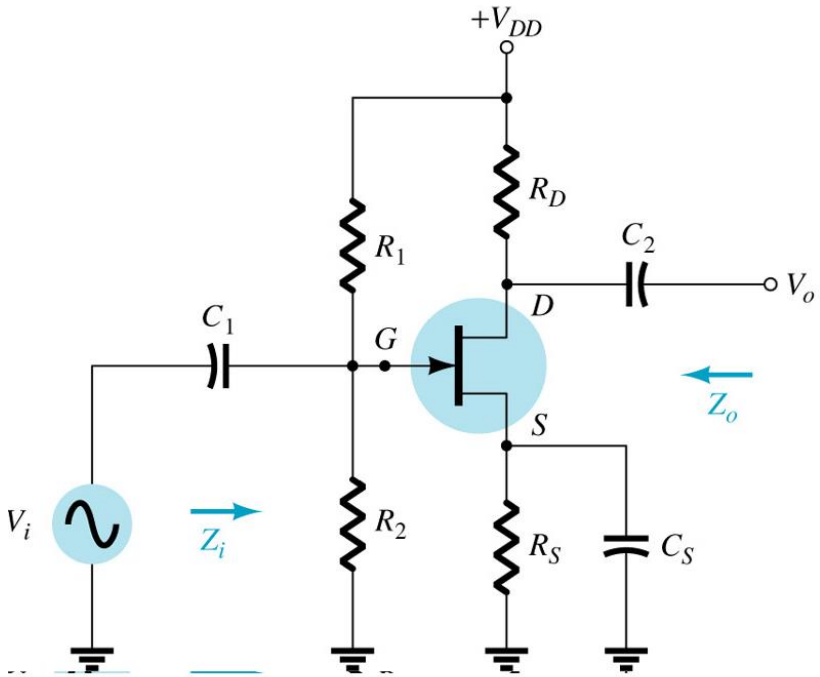
$$A_v = g_m R_D = (2.25\ \text{mS})(3.6\ \text{k}\Omega) = 8.1$$

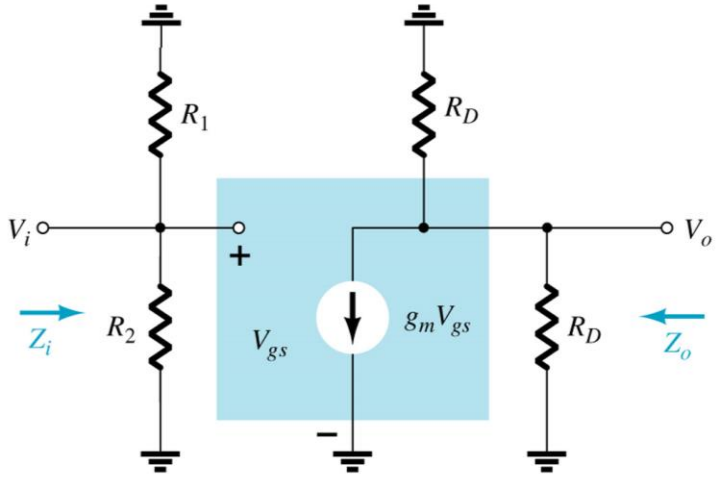
With

$$V_o = A_v V_i = (8.1)(40\ \text{mV}) = 324\ \text{mV}$$

In this case, the difference is a little more noticeable but not dramatically so.

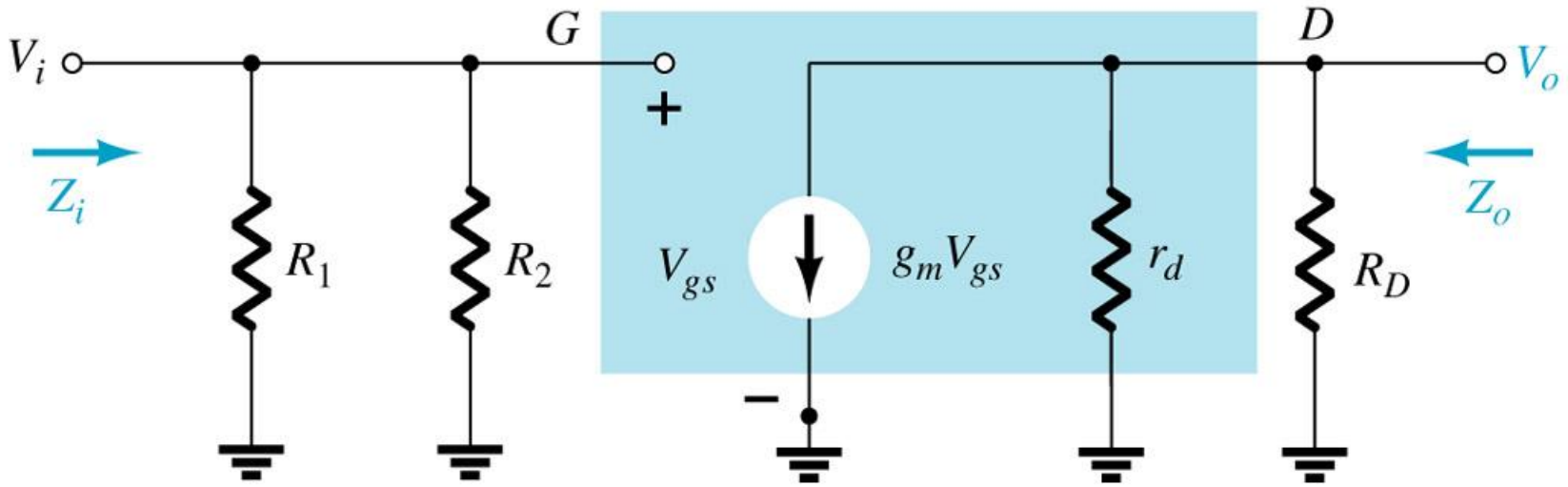
JFET CS Voltage-Divider Configuration





This is a CS amplifier configuration therefore the input is on the gate and the output is on the drain.

AC Equivalent Circuit



Input Impedance: $Zi = R_1 || R_2$

Output Impedance: $Zo = r_d || R_D$ $\quad Zo \cong R_D \;/_{r_d \geq 10R_D}$

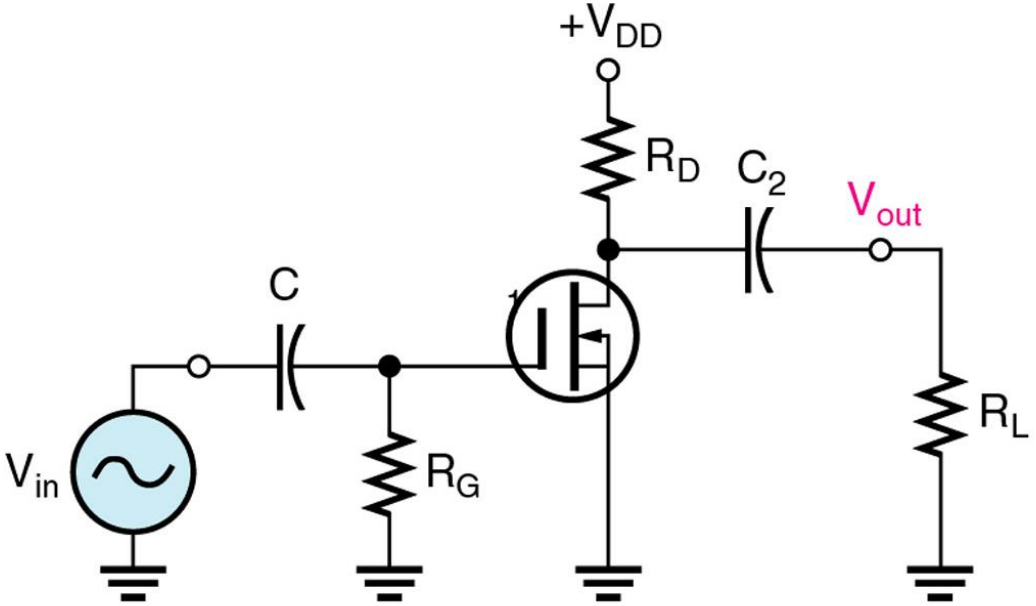
Voltage Gain: $Av = -g_m(r_d || R_D)$ $\quad Av \cong -g_m R_D \;/_{r_d \geq 10R_D}$

D-MOSFET Amplifier

With this zero biased D-MOSFET amplifier it is quite easy to analyze the drain circuit since

$I_D = I_{DSS}$ (at $V_{GS} = 0$).

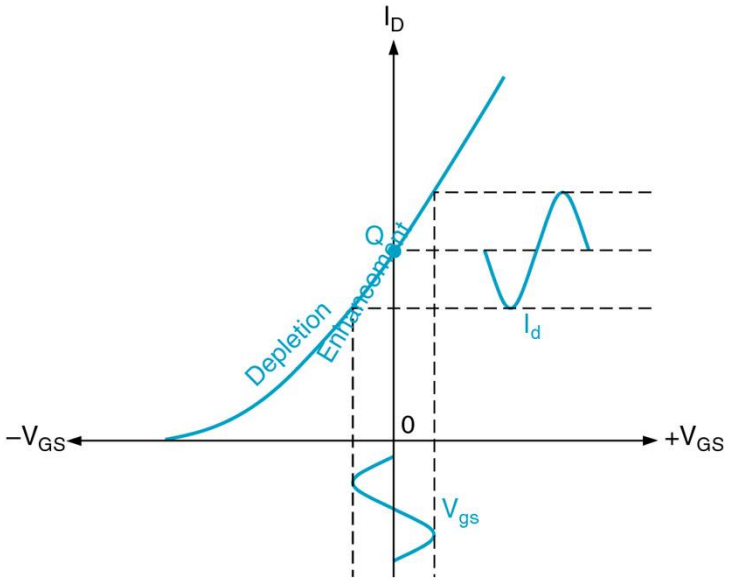
The analysis involves only, $V_D = V_{DD} - I_D R_D$.



Zero-bias D-MOSFET common-source amplifier

D-MOSFET Amplifier Operation

With a zero-biased D-MOSFET amplifier the swings occur in both depletion mode (negative swing in V_{GS} produces the depletion mode, I_D decreases) and enhancement mode (positive swing in V_{GS} produces the enhancement mode, I_D increases). The methods for ac analysis for the D-MOSFET amplifier is identical to the JFET amplifier discussed previously.



Depletion-enhancement operation of D_MOSFET shown on transfer characteristic curve.

Example 5

The network of Figure below was analyzed and resulting in V_{GSQ} =0.35 V and I_{DQ} =7.6 mA.

(a) Determine g_m and compare to g_{m0}.

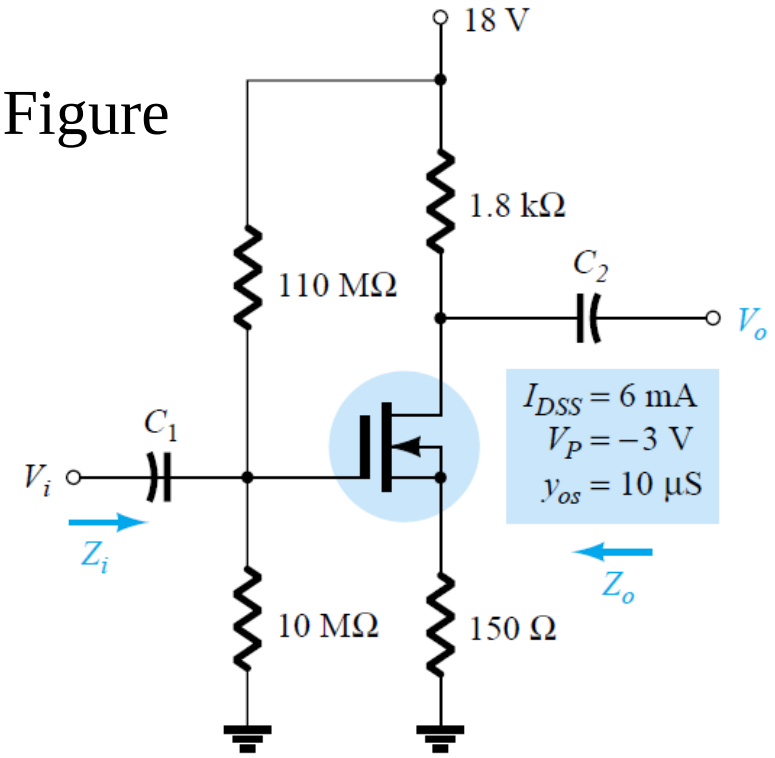
(b) Find r_d .

(c) Sketch the ac equivalent network for Figure

(d) Find Z_i .

(e) Calculate Z_o .

(f) Find A_v .



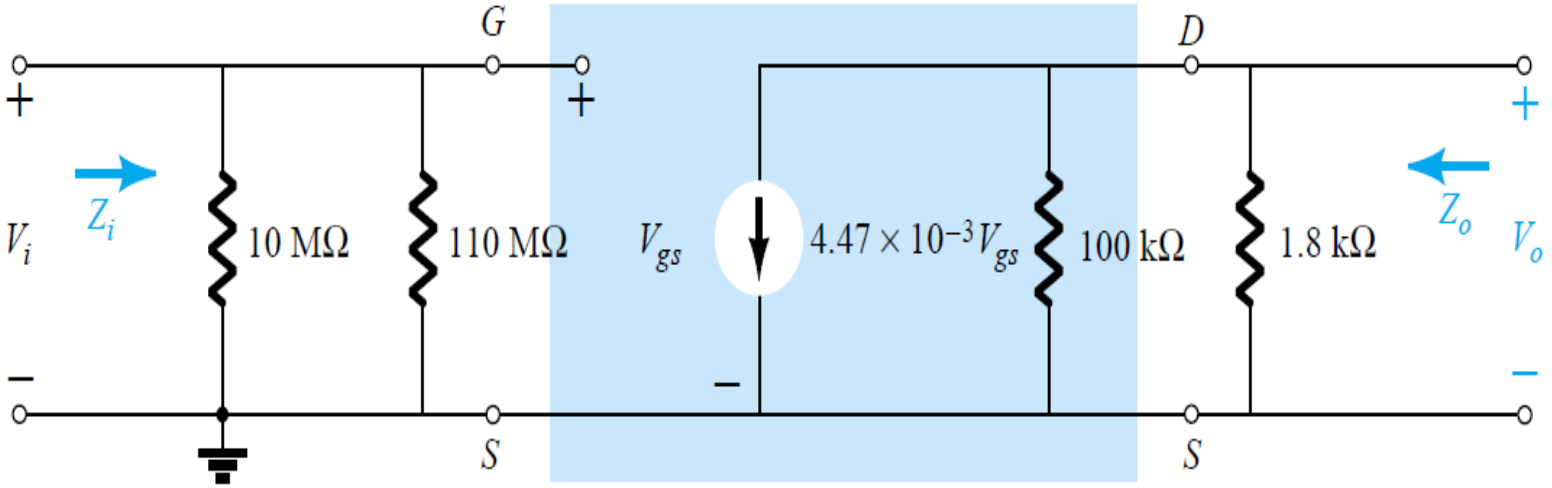
Solution

(a) $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(6\text{ mA})}{3\text{ V}} = 4\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 4\text{ mS}\left(1 - \frac{(+0.35\text{ V})}{(-3\text{ V})}\right) = 4\text{ mS}(1 + 0.117) = \mathbf{4.47\text{ mS}}$$

(b) $$r_d = \frac{1}{y_{os}} = \frac{1}{10\ \mu S} = \mathbf{100\ k\Omega}$$

(c)



(d) $$Z_i = R_1 \| R_2 = 10\text{ M}\Omega \| 110\text{ M}\Omega = \mathbf{9.17\ M\Omega}$$

(e) $$Z_o = r_d \| R_D = 100\text{ k}\Omega \| 1.8\text{ k}\Omega = \mathbf{1.77\ k\Omega} \cong R_D = \mathbf{1.8\ k\Omega}$$

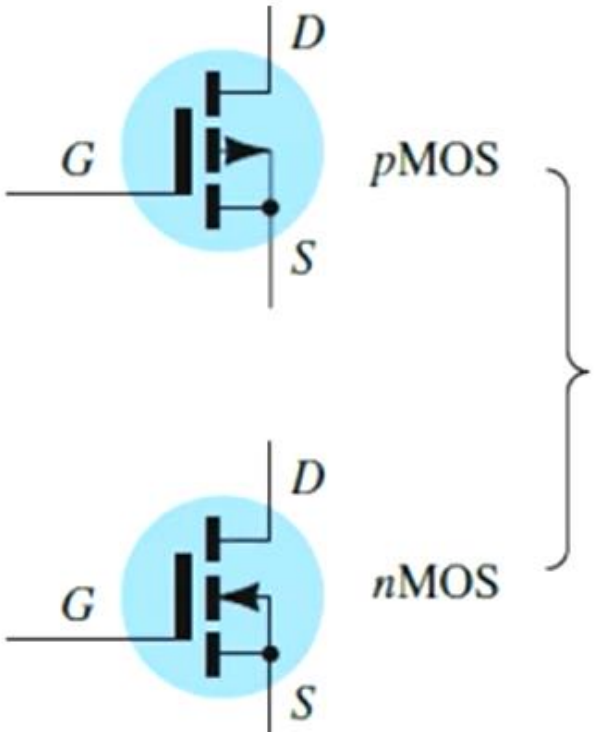
(f) $r_d \geq 10R_D \rightarrow 100\text{ k}\Omega \geq 18\text{ k}\Omega$

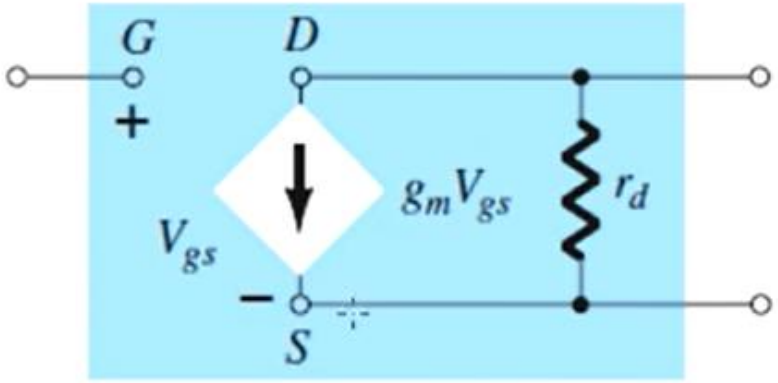
$$A_v = -g_m R_D = -(4.47\text{ mS})(1.8\text{ k}\Omega) = \mathbf{8.05}$$

AC analysis for Enhancement -type MOSFETs

The enhancement-type MOSFET (E-MOSFET) can be either an n -channel (n MOS) or p -channel (p MOS) device, as shown in Fig. below. The ac small-signal equivalent circuit of the device is revealing an open-circuit between gate and drain–source channel and a current source from drain to source having a magnitude dependent on the gate to- source voltage. The device trans-conductance gm is provided on specification sheets. For E-MOSFETs, the relationship between output current and controlling voltage is defined by

$$ID = k(VGS - VGS_{(Th)})^2$$





$$g_m = g_{fs} = |y_{fs}| r_d = \frac{1}{g_{os}} = \frac{1}{|y_{os}|}$$

E-MOSFET Amplifier

Since g_m is still defined by

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

we can take the derivative of the transfer equation to determine g_m as an operating point. That is,

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}} k(V_{GS} - V_{GS(\text{Th})})^2 = k\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})})^2$$

$$= 2k(V_{GS} - V_{GS(\text{Th})})\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})}) = 2k(V_{GS} - V_{GS(\text{Th})})(1 - 0)$$

and

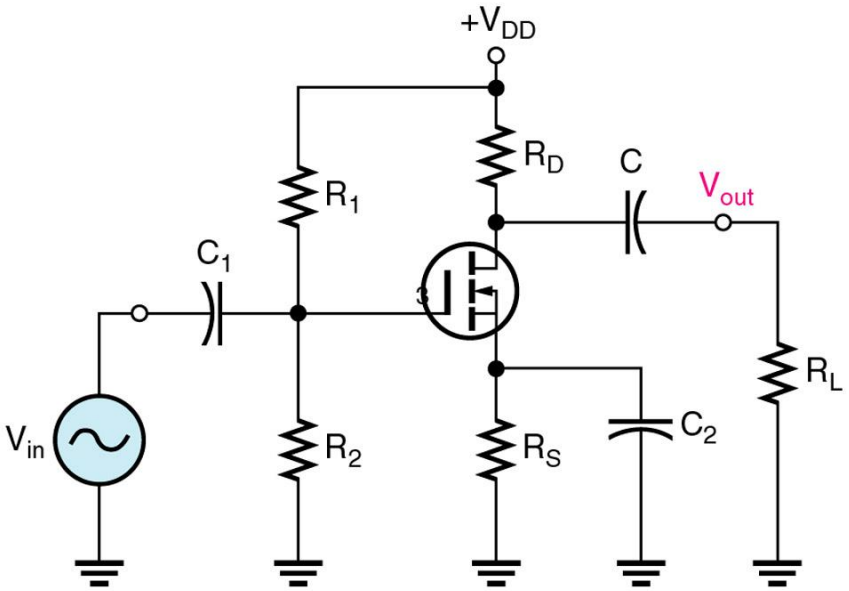
$$\boxed{g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})})}$$

E-MOSFET Amplifier

For a voltage-divider biased E-MOSFET circuit the voltage divider sets the V_{GS} needed to set the Q-point above the threshold. DC analysis of the drain circuit requires determination of the constant (K) from the formula discussed in the previous chapter.

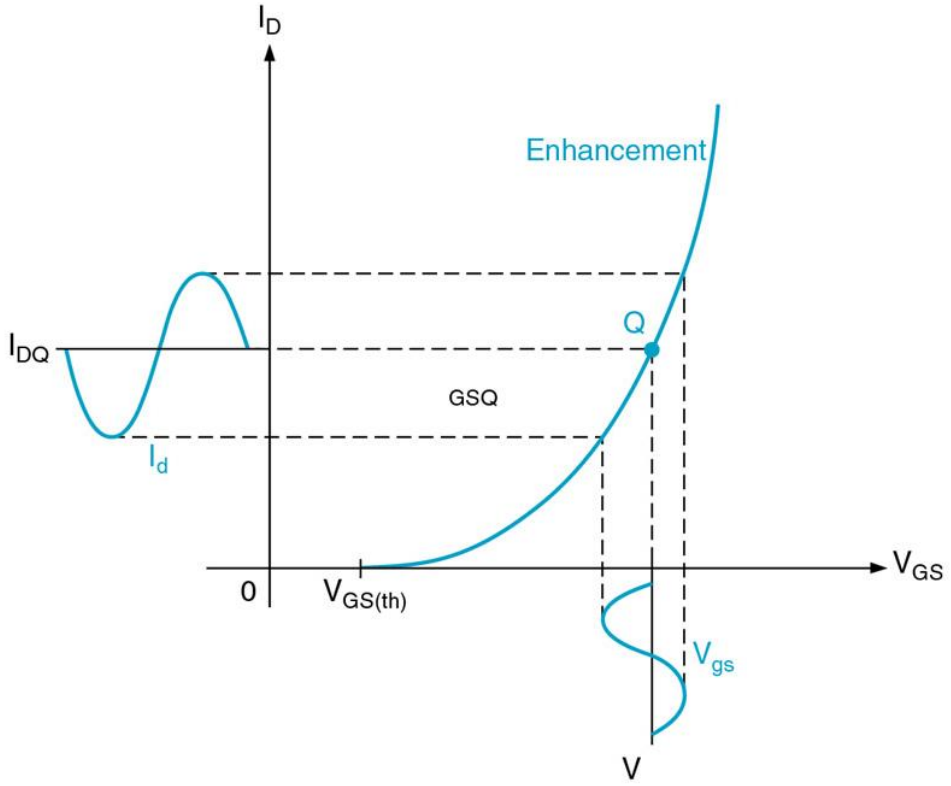
$$K = I_{D(on)} / (V_{GS} - V_{GS(th)})^2$$

$$I_D = K(V_{GS} - V_{GS(th)})^2$$



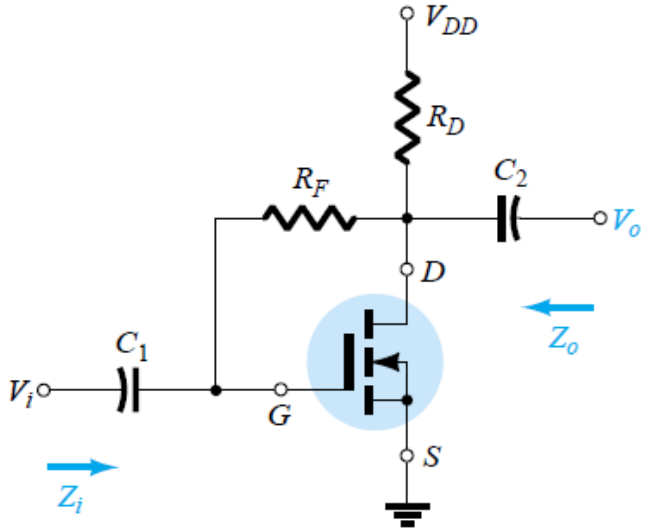
E-MOSFET Amplifier Operation

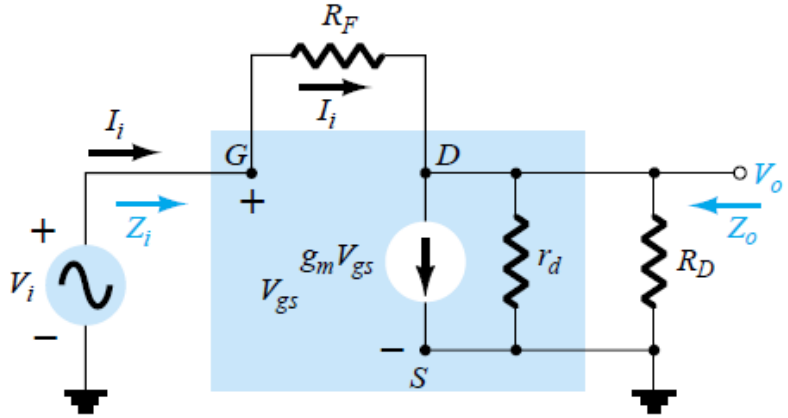
Notice that with the E-MOSFET amplifier operation occurs exclusively in the enhancement mode. Voltage gain calculation for the E-MOSFET amplifier is the same as the JFET and D-MOSFET.



E_MOSFET (n-channel) operation shown on transfer characteristic urve

E-MOSFET Drain-feedback Configuration





$$Z_i = \frac{V_i}{I_i} = \frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)}$$

$$Z_i \cong \frac{R_F}{1 + g_m R_D}$$

$R_F \gg r_d \| R_D,\ r_d \geq 10R_D$

so that

$$A_v = -g_m(R_F \| r_d \| R_D)$$

Since R_F is usually $>> r_d \| R_D$ and if $r_d \geq 10R_D$,

$$A_v \cong -g_m R_D$$

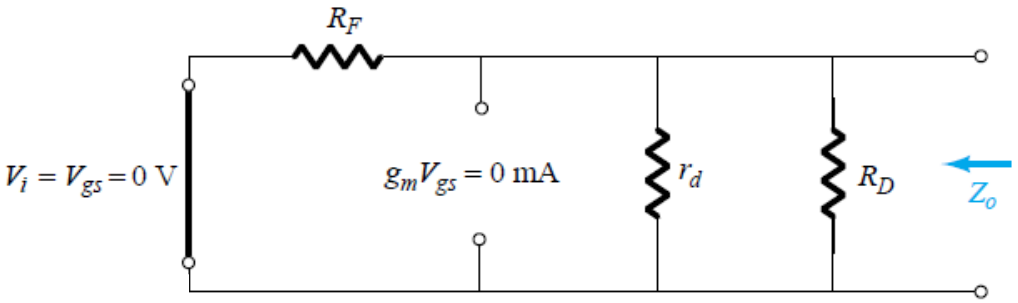
$R_F \gg r_d \| R_D,\ r_d \geq 10R_D$

Phase Relationship: The negative sign for A_v reveals that V_o and V_i are out of phase by 180°.

E-MOSFET Drain-feedback Configuration

Z_o: Substituting $V_i = 0$ V will result in $V_{gs} = 0$ V and $g_m V_{gs} = 0$, with a short-circuit path from gate to ground as shown in Fig. . R_F, r_d, and R_D are then in parallel and

$$Z_o = R_F \| r_d \| R_D$$



Determining Z_o for the network of Fig

Normally, R_F is so much larger than $r_d \| R_D$ that

$$Z_o \cong r_d \| R_D$$

and with $r_d \geq 10R_D$,

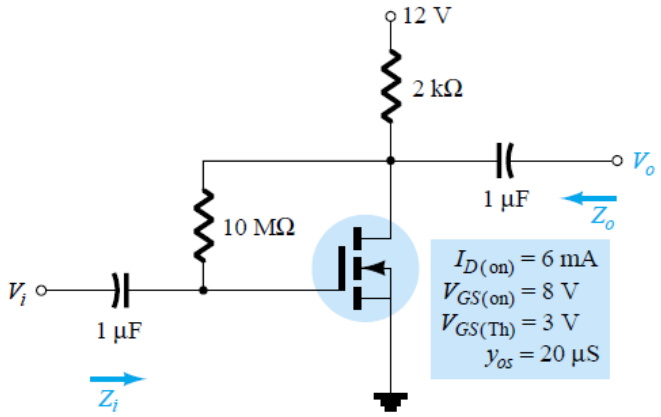
$$Z_o \cong R_D \qquad R_F \gg r_d \| R_D,\ r_d \geq 10R_D$$

Example 6

with the result that

$k = 0.24 \times 10^{-3}$ A/V^2, $V_{GS_Q} = 6.4$ V, and $I_{D_Q} = 2.75$ mA.

(a) Determine g_m.
(b) Find r_d.
(c) Calculate Z_i with and without r_d. Compare results.
(d) Find Z_o with and without r_d. Compare results.
(e) Find A_v with and without r_d. Compare results.



Solution

(a) $g_m = 2k(V_{GS_Q} - V_{GS(Th)}) = 2(0.24 \times 10^{-3}\ \text{A/V}^2)(6.4\ \text{V} - 3\ \text{V})$

$= \mathbf{1.63\ mS}$

(b) $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{20\ \mu\text{S}} = \mathbf{50\ k\Omega}$

(c) With r_d:

$$Z_i = \frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)} = \frac{10\ \text{M}\Omega + 50\ \text{k}\Omega \| 2\ \text{k}\Omega}{1 + (1.63\ \text{mS})(50\ \text{k}\Omega \| 2\ \text{k}\Omega)}$$

$$= \frac{10\ \text{M}\Omega + 1.92\ \text{k}\Omega}{1 + 3.13} = \mathbf{2.42\ M\Omega}$$

Without r_d:

$$Z_i \cong \frac{R_F}{1 + g_m R_D} = \frac{10\ \text{M}\Omega}{1 + (1.63\ \text{mS})(2\ \text{k}\Omega)} = \mathbf{2.53\ M\Omega}$$

revealing that since the condition $r_d \geq 10R_D = 50\ \text{k}\Omega \geq 40\ \text{k}\Omega$ is satisfied, the results for Z_o with or without r_d will be quite close.

(d) With r_d:

$$Z_o = R_F \| r_d \| R_D = 10\ \text{M}\Omega \| 50\ \text{k}\Omega \| 2\ \text{k}\Omega = 49.75\ \text{k}\Omega \| 2\ \text{k}\Omega$$
$$= \mathbf{1.92\ k\Omega}$$

Without r_d:

$$Z_o \cong R_D = \mathbf{2\ k\Omega}$$

again providing very close results.

(e) With r_d:

$$A_v = -g_m(R_F \| r_d \| R_D)$$
$$= -(1.63\ \text{mS})(10\ \text{M}\Omega \| 50\ \text{k}\Omega \| 2\ \text{k}\Omega)$$
$$= -(1.63\ \text{mS})(1.92\ \text{k}\Omega)$$
$$= \mathbf{-3.21}$$

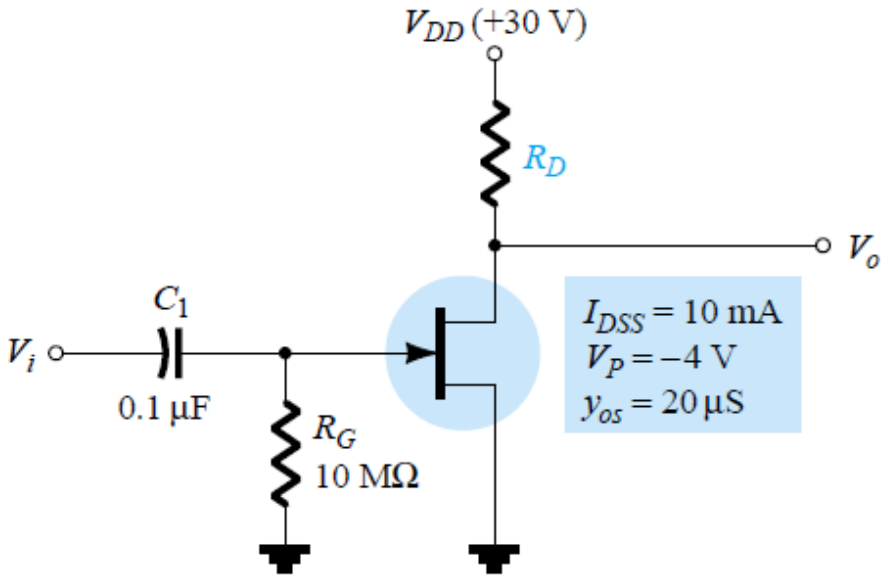
Without r_d:

$$A_v = -g_m R_D = -(1.63\ \text{mS})(2\ \text{k}\Omega)$$
$$= \mathbf{-3.26}$$

which is very close to the above result.

Example 7

Design the fixed-bias network of Figure below to have an ac gain of 10. That is, determine the value of R_D



Solution

Since $V_{GS_Q} = 0$ V, the level of g_m is g_{m0}. The gain is therefore determined by

$$A_v = -g_m(R_D \| r_d) = -g_{m0}(R_D \| r_d)$$

with

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10 \text{ mA})}{4 \text{ V}} = 5 \text{ mS}$$

The result is

$$-10 = -5 \text{ mS}(R_D \| r_d)$$

and

$$R_D \| r_d = \frac{10}{5 \text{ mS}} = 2 \text{ k}\Omega$$

From the device specifications,

$$r_d = \frac{1}{y_{os}} = \frac{1}{20 \times 10^{-6} \text{ S}} = 50 \text{ k}\Omega$$

Substituting, we find

$$R_D \| r_d = R_D \| 50 \text{ k}\Omega = 2 \text{ k}\Omega$$

and

$$\frac{R_D(50 \text{ k}\Omega)}{R_D + 50 \text{ k}\Omega} = 2 \text{ k}\Omega$$

or

$$50R_D = 2(R_D + 50 \text{ k}\Omega) = 2R_D + 100 \text{ k}\Omega$$

with

$$48R_D = 100 \text{ k}\Omega$$

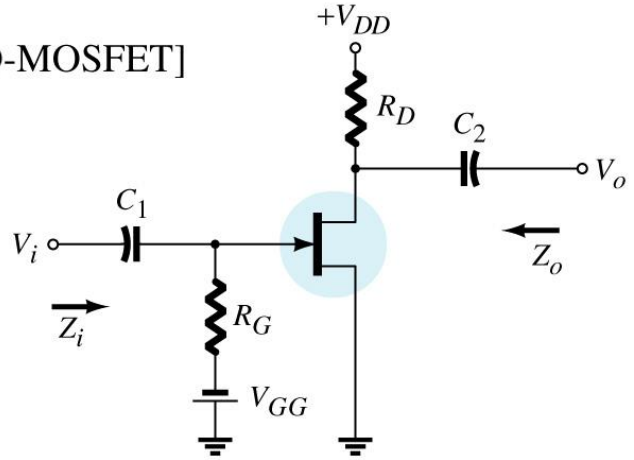
and

$$R_D = \frac{100 \text{ k}\Omega}{48} \cong 2.08 \text{ k}\Omega$$

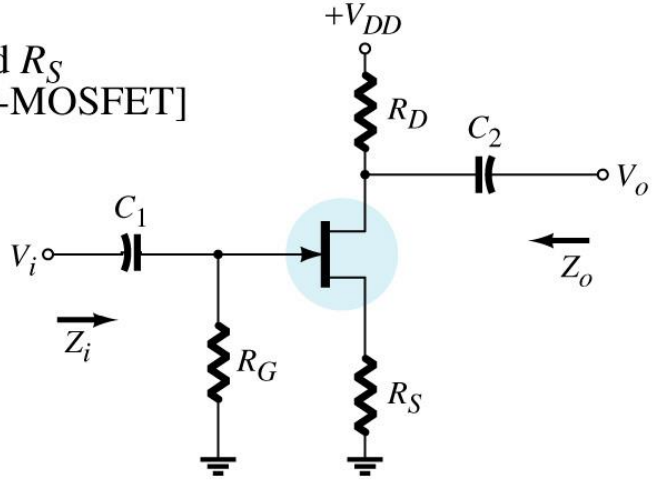
The closest standard value is **2 kΩ** (Appendix C), which would be employed for this design.

Summary Table

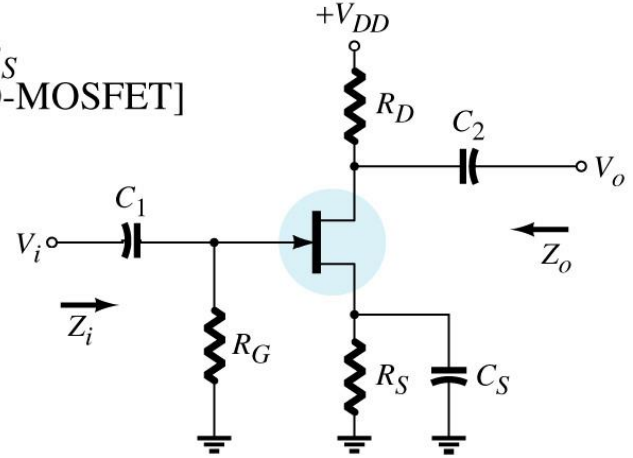
Fixed-bias
[JFET or D-MOSFET]



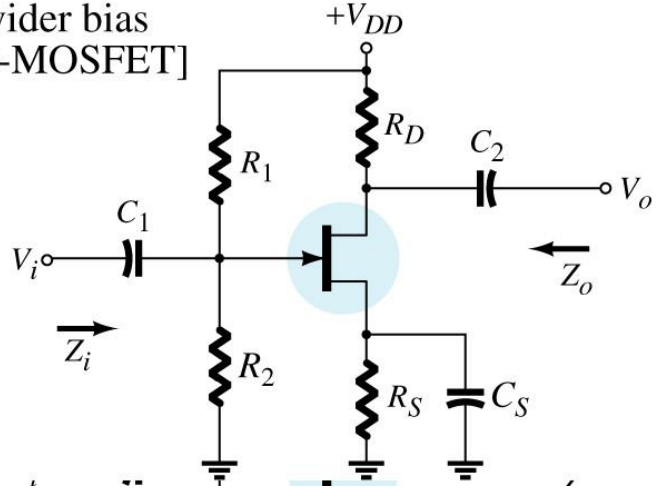
Self-bias
Unbypassed R_S
[JFET or D-MOSFET]



Self-bias
bypassed R_S
[JFET or D-MOSFET]

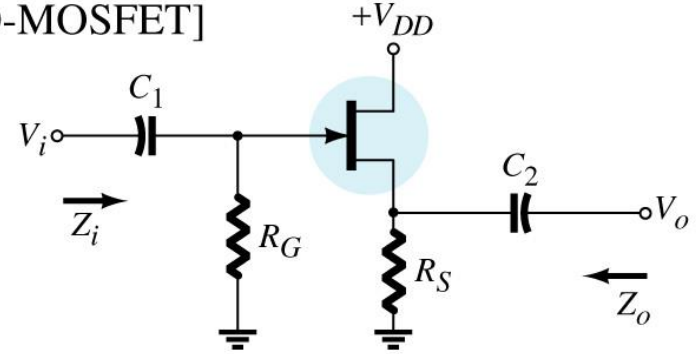


Voltage-divider bias
[JFET or D-MOSFET]

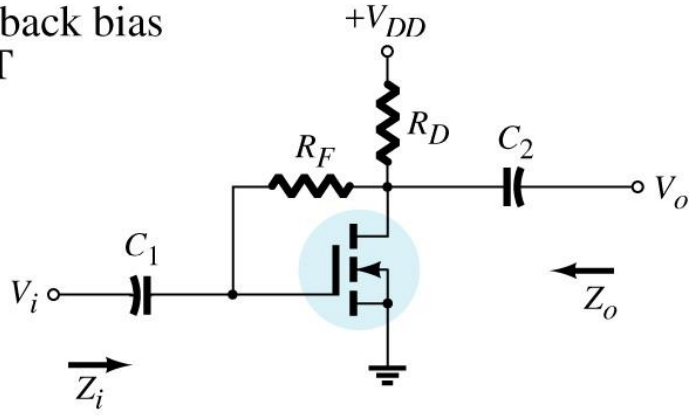


Summary Table

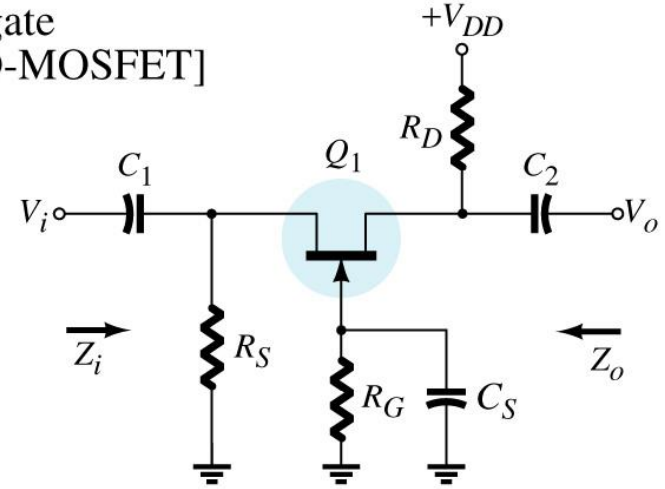
Source-follower
[JFET or D-MOSFET]



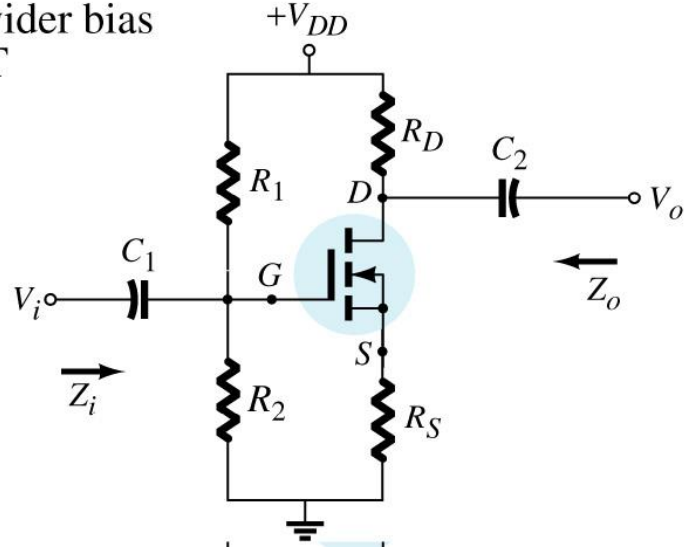
Drain-Feedback bias
E-MOSFET



Common-gate
[JFET or D-MOSFET]



Voltage-divider bias
E-MOSFET



Summary

- FET amplifier configuration operation are similar to BJT amplifiers.
- The transconductance (g_m) relates the drain current (ac output) to the ac input voltage (V_{gs})
- Gain can be affected by drain circuit resistance.
- The input resistance for a FET at the gate is extremely high
- The common-source is the most used type of FET amplifer and has a phase inversion is 180°.

Summary

- The common-drain has no phase shift, a gain slightly less than 1 and the output is taken from the source.
- The common-gate has no phase shift and low input resistance.

Ninevah University
College of Electronics Engineering
Department of Systems and Control

Electronic I I
Lecture 2

(MOSFET) Transistor

by
Rafal Raed Mahmood Alshaker

2nd Class

Topics of Second Lecture

1 . DEPLETION-TYPE MOSFET

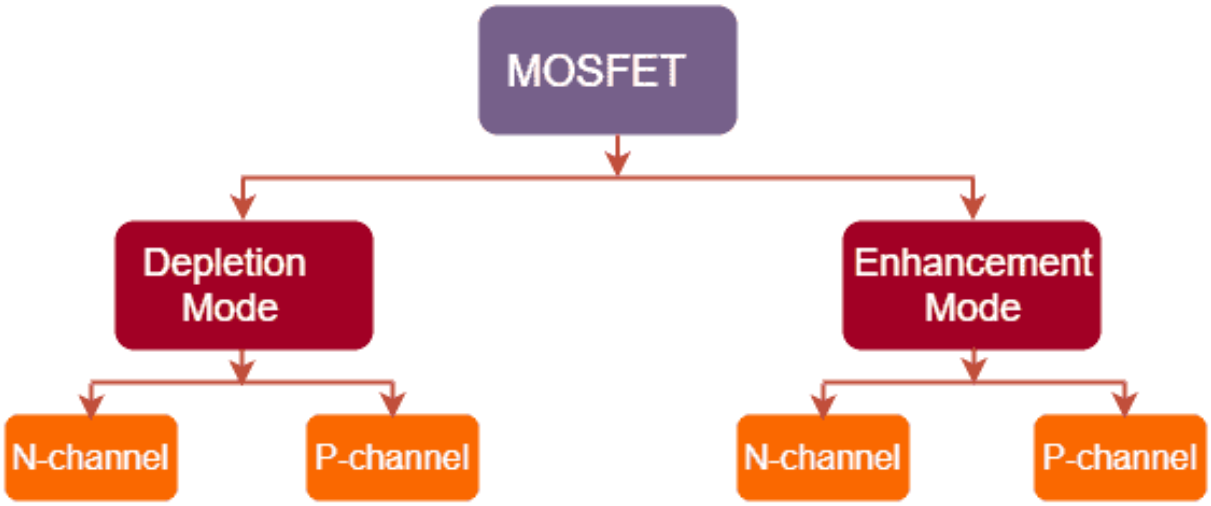
- Basic Construction
- Basic Operation and Characteristics

2. ENHANCEMENT-TYPE MOSFET

- Basic Construction
- Basic Operation and Characteristics

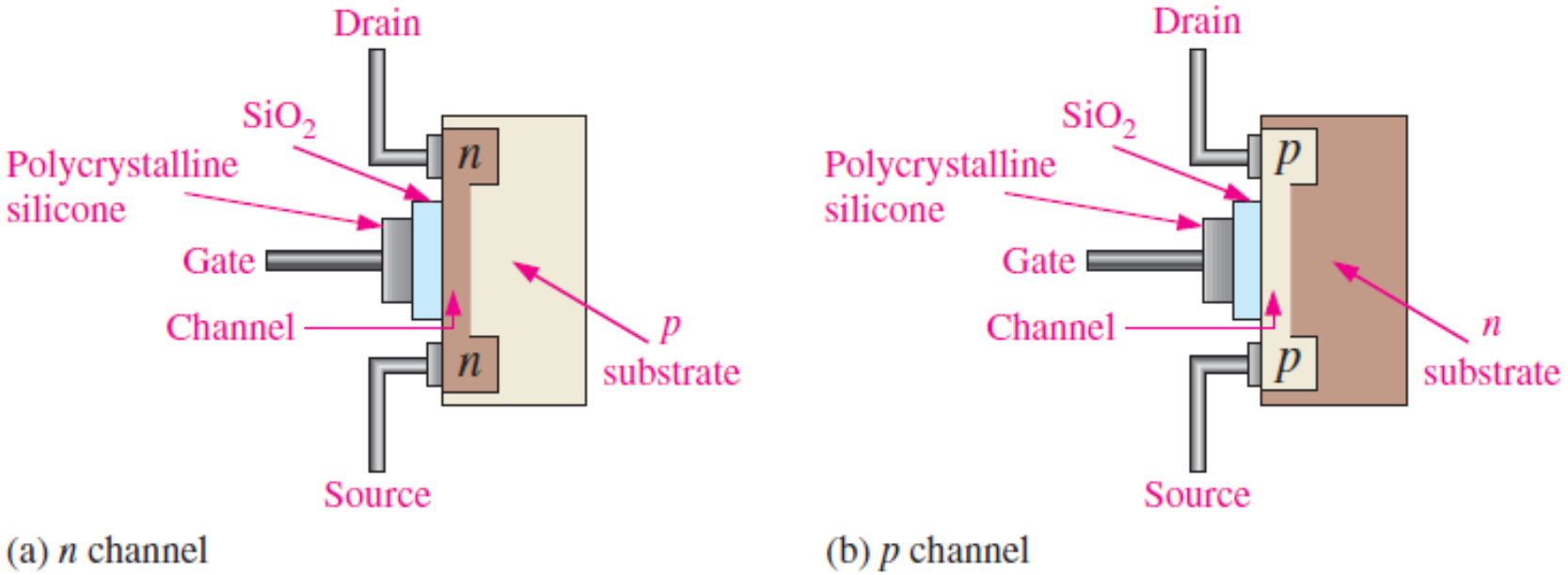
MOSFET

The MOSFET (Metal Oxide Semiconductor Field-effect Transistor) is another category of field-effect transistor. The MOSFET, different from the JFET, has no pn junction structure; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO2) layer. The two basic types of MOSFETs are **Enhancement (E)** and **Depletion (D)** of the two types, the enhancement MOSFET is more widely used. Because polycrystalline silicon is now used for the gate material instead of metal, these devices are sometimes called IGFETs (insulated-gate FETs).

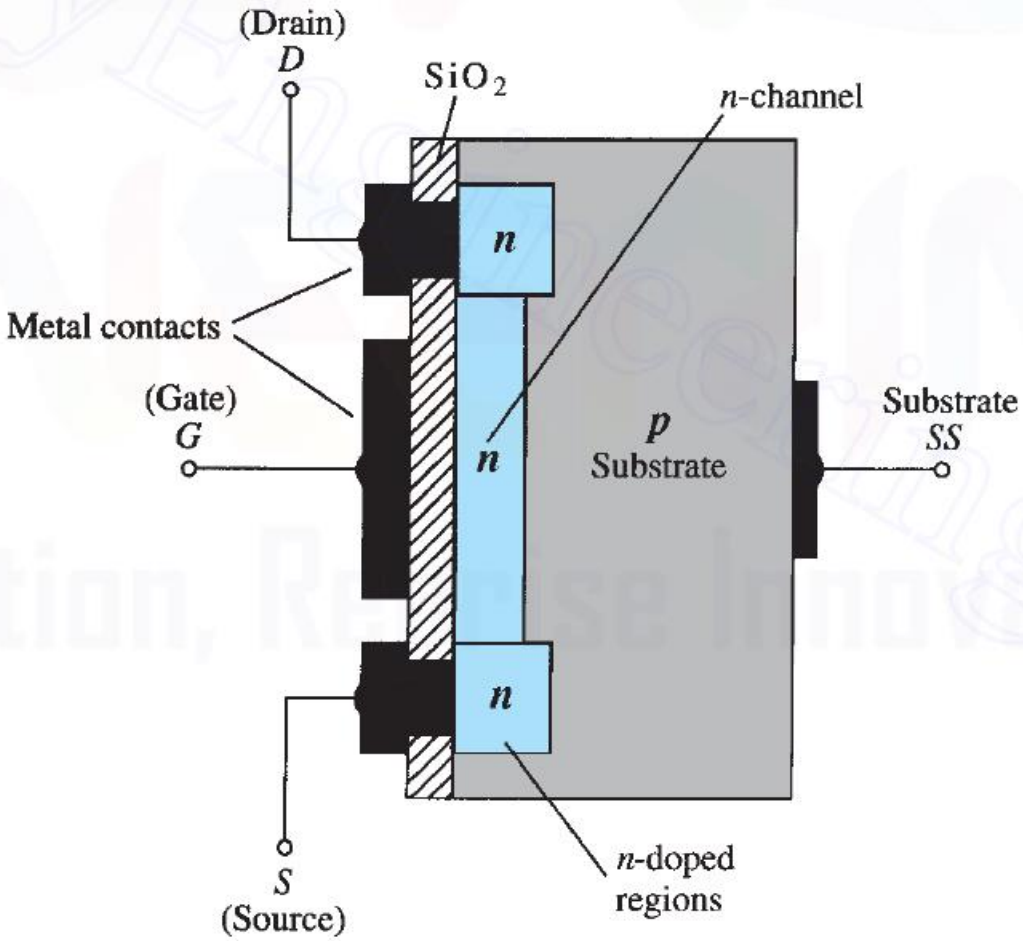


Classification of MOSFET

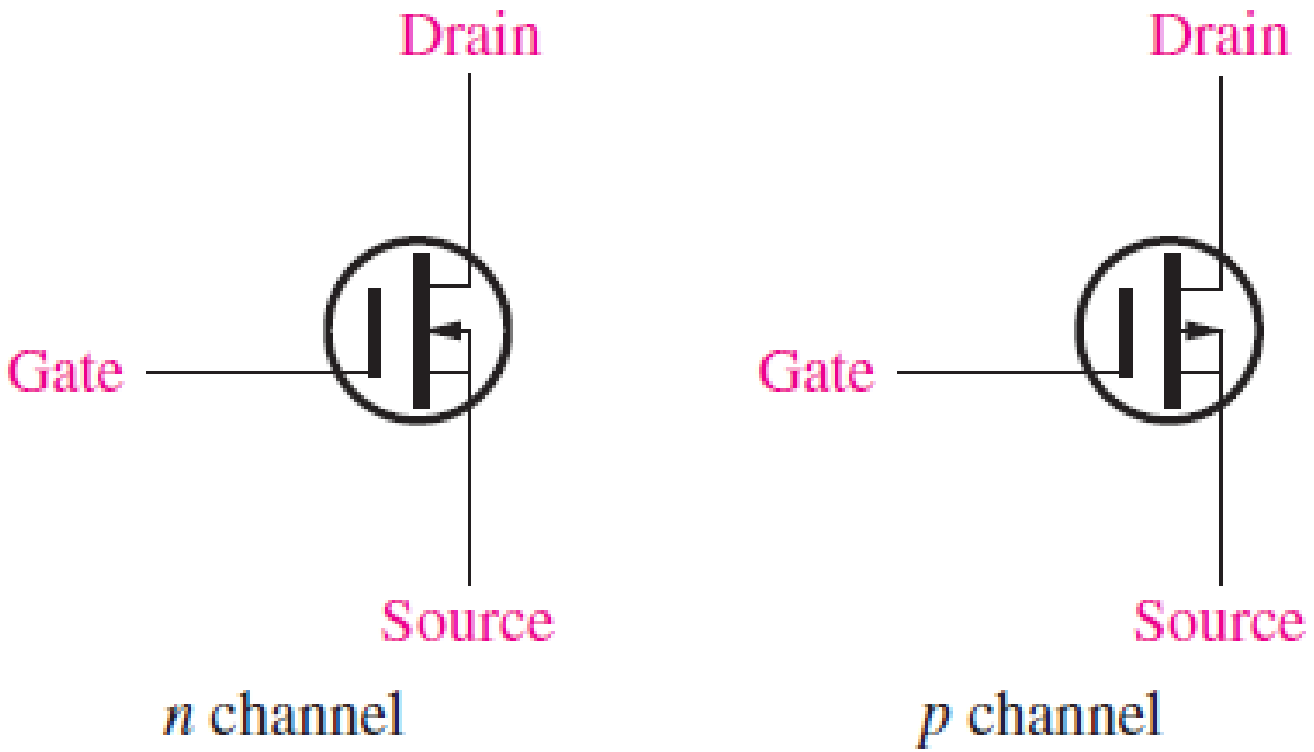
Depletion-Type MOSFET Construction



the basic structure of D-MOSFETs.


(Drain)
D
SiO2
n-channel
n
Metal contacts
(Gate)
G
n
p
Substrate
Substrate
SS
n
S
(Source)
n-doped
regions

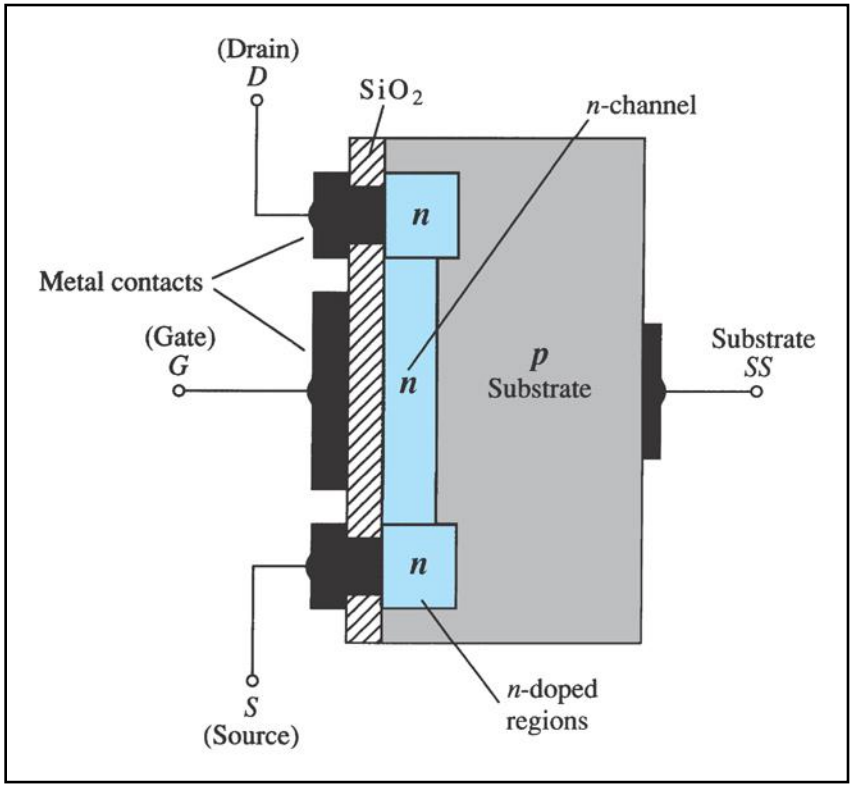
D-MOSFET schematic symbols



Depletion-Type MOSFET Construction

The **Drain (D)** and **Source (S)** connect to the to *n*-type regions. These *n*-typed regions are connected via an *n*-channel. This *n*-channel is connected to the **Gate (G)** via a thin insulating layer of silicon dioxide (SiO_2).

The *n*-type material lies on a *p*-type substrate that may have an additional terminal connection called the **Substrate (SS).**



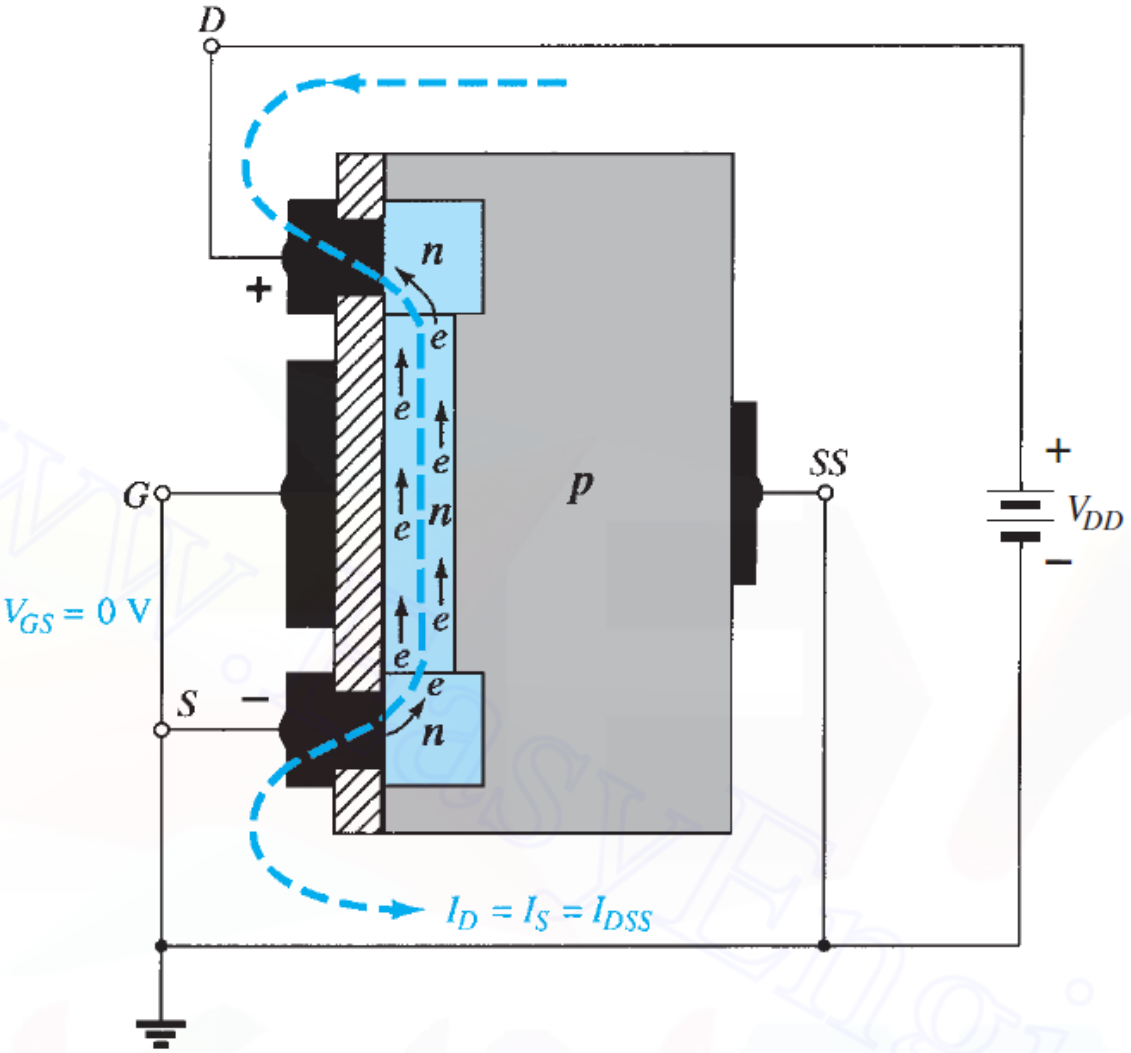
There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

In addition:

It is the insulating layer of SiO2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

Basic Operation and Characteristics

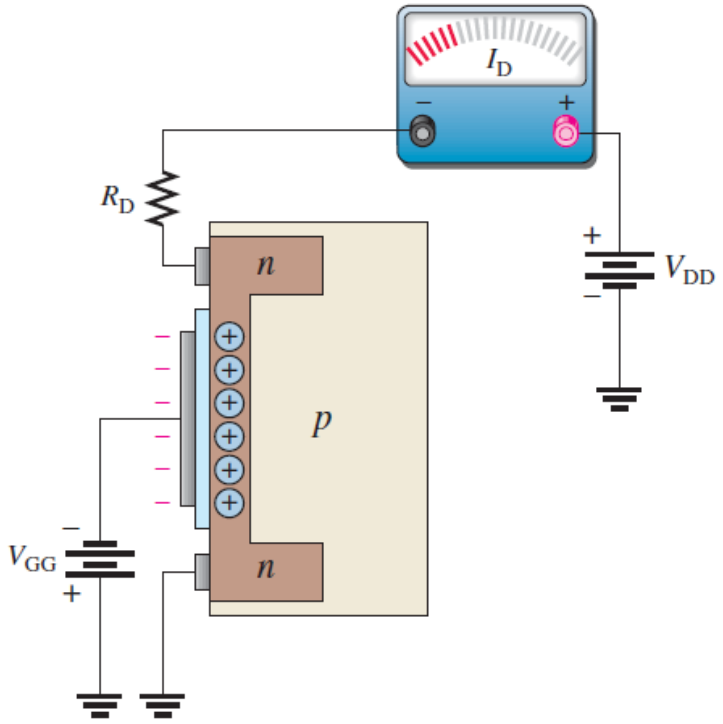
- A depletion MOSFET (D-MOSFET) can operate with a zero, positive, or negative gate-to source voltage.
- The D-MOSFET has a physical channel between the drain and source.
- For an *n*-channel D-MOSFET,
  - ✓ negative values of V_{GS} produce the depletion mode
  - ✓ positive values of V_{GS} produce the enhancement mode.



Basic Operation and Characteristics of D-MOSFET

The D-MOSFET can be operated in either of two modes—the depletion mode or the enhancement mode—and is sometimes called a depletion/enhancement MOSFET

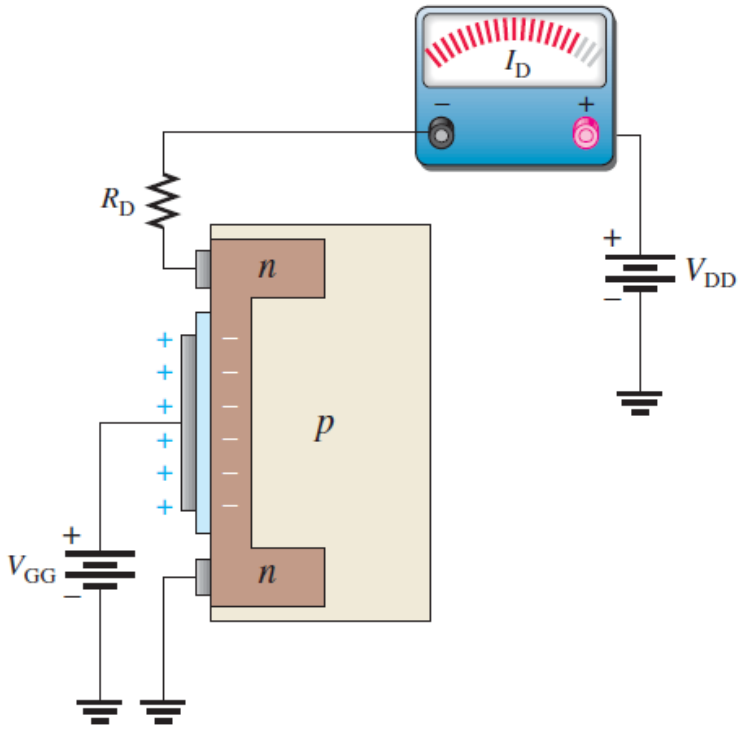
Depletion Mode The silicon dioxide insulating layer is the dielectric. With negative gate voltage, the negative charges on the gate repel conduction electrons from the channel, leaving positive ions in their place. Thereby, the n channel is depleted of some of its electrons, thus decreasing the channel conductivity. The greater the negative voltage on the gate, the greater the depletion of n-channel electrons. At a sufficiently negative gate-to source voltage, $V_{GS(off)}$, the channel is totally depleted and the drain current is zero. This depletion mode is illustrated in Figure (a). Like the n-channel JFET, the n-channel D-MOSFET conducts drain current for gate-to-source voltages between $V_{GS(off)}$, and zero. In addition, the D-MOSFET conducts for values of V_{GS} above zero.



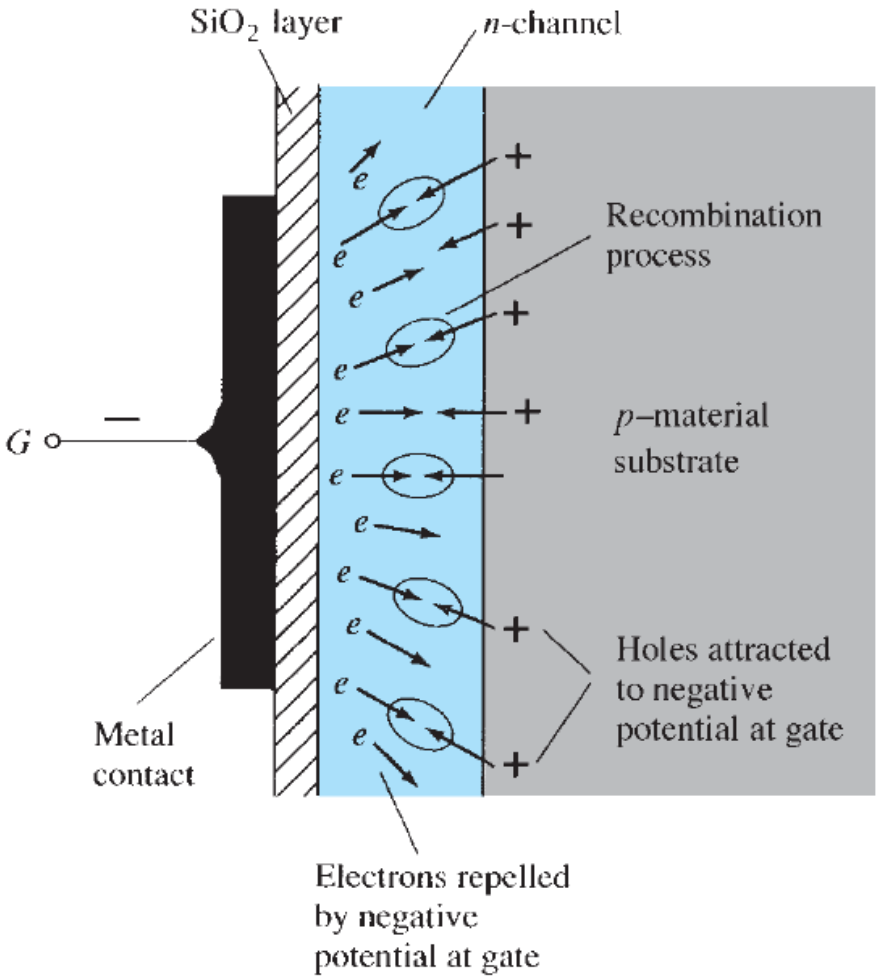
(a) Depletion mode: V_{GS} negative and less than $V_{GS(off)}$

Basic Operation and Characteristics of D-MOSFET

Enhancement Mode With a positive gate voltage, more conduction electrons are attracted into the channel, thus increasing (enhancing) the channel conductivity, as illustrated in Figure (b).



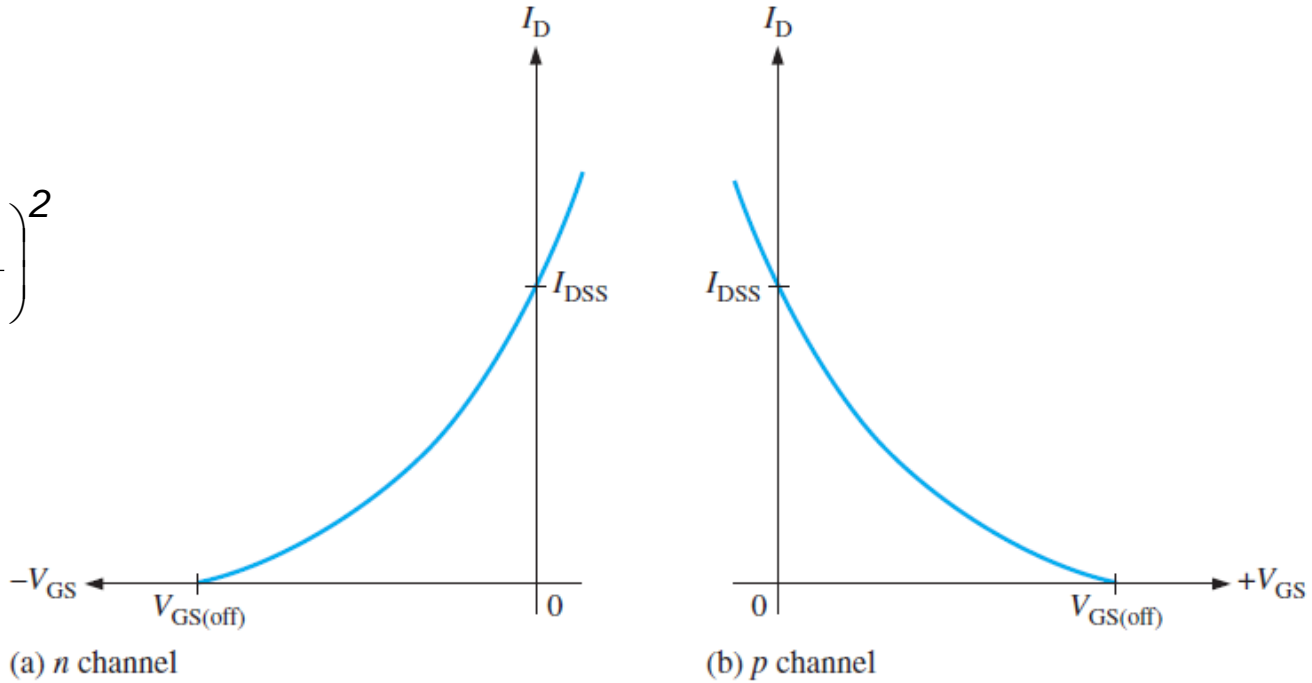
(b) Enhancement mode: V_{GS} positive


SiO_2 layer
n-channel
Recombination process
p–material substrate
G
Metal contact
Holes attracted to negative potential at gate
Electrons repelled by negative potential at gate

D-MOSFET Transfer Characteristic

As previously discussed, the D-MOSFET can operate with either positive or negative gate voltages. This is indicated on the general transfer characteristic curves in Figure below for both n-channel and p-channel MOSFETs. The point on the curves where V_{GS}=0 corresponds to I_{DSS}. The point where I_D=0 corresponds to $V_{GS(off)}$, As with the JFET,The square-law expression in Shockley's equation for the JFET curve also applies to the D-MOSFET curve.

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$



EXAMPLE : Sketch the transfer characteristics for an *n* -channel depletion-type MOSFET with I_{DSS}= 10 mA and V_P= -4 V.

EXAMPLE: Sketch the transfer characteristics for an *n*-channel depletion-type MOSFET with I_{DSS}= 10 mA and V_P= -4 V.

Solution:

$$\text{At } V_{GS} = 0\text{ V}, \quad I_D = I_{DSS} = 10\text{ mA}$$

$$V_{GS} = V_P = -4\text{ V}, \quad I_D = 0\text{ mA}$$

$$V_{GS} = \frac{V_P}{2} = \frac{-4\text{ V}}{2} = -2\text{ V}, \quad I_D = \frac{I_{DSS}}{4} = \frac{10\text{ mA}}{4} = 2.5\text{ mA}$$

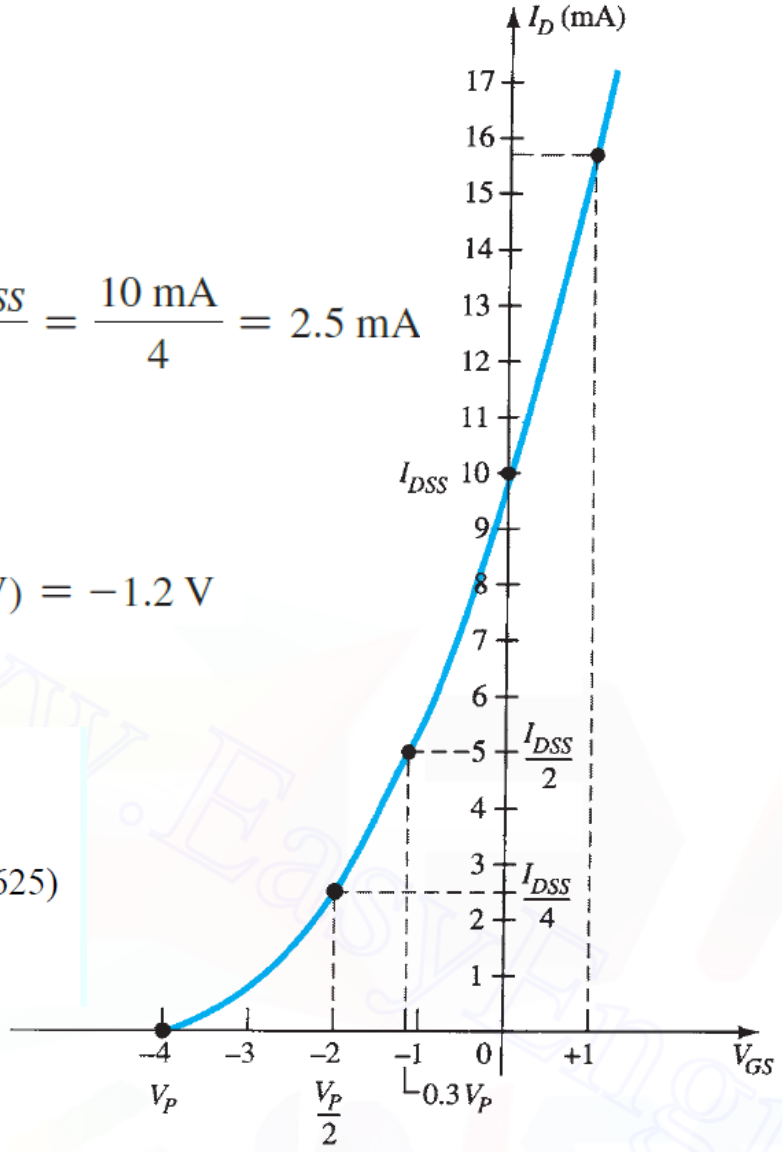
$$\text{and at } I_D = \frac{I_{DSS}}{2},$$

$$V_{GS} = 0.3V_P = 0.3(-4\text{ V}) = -1.2\text{ V}$$

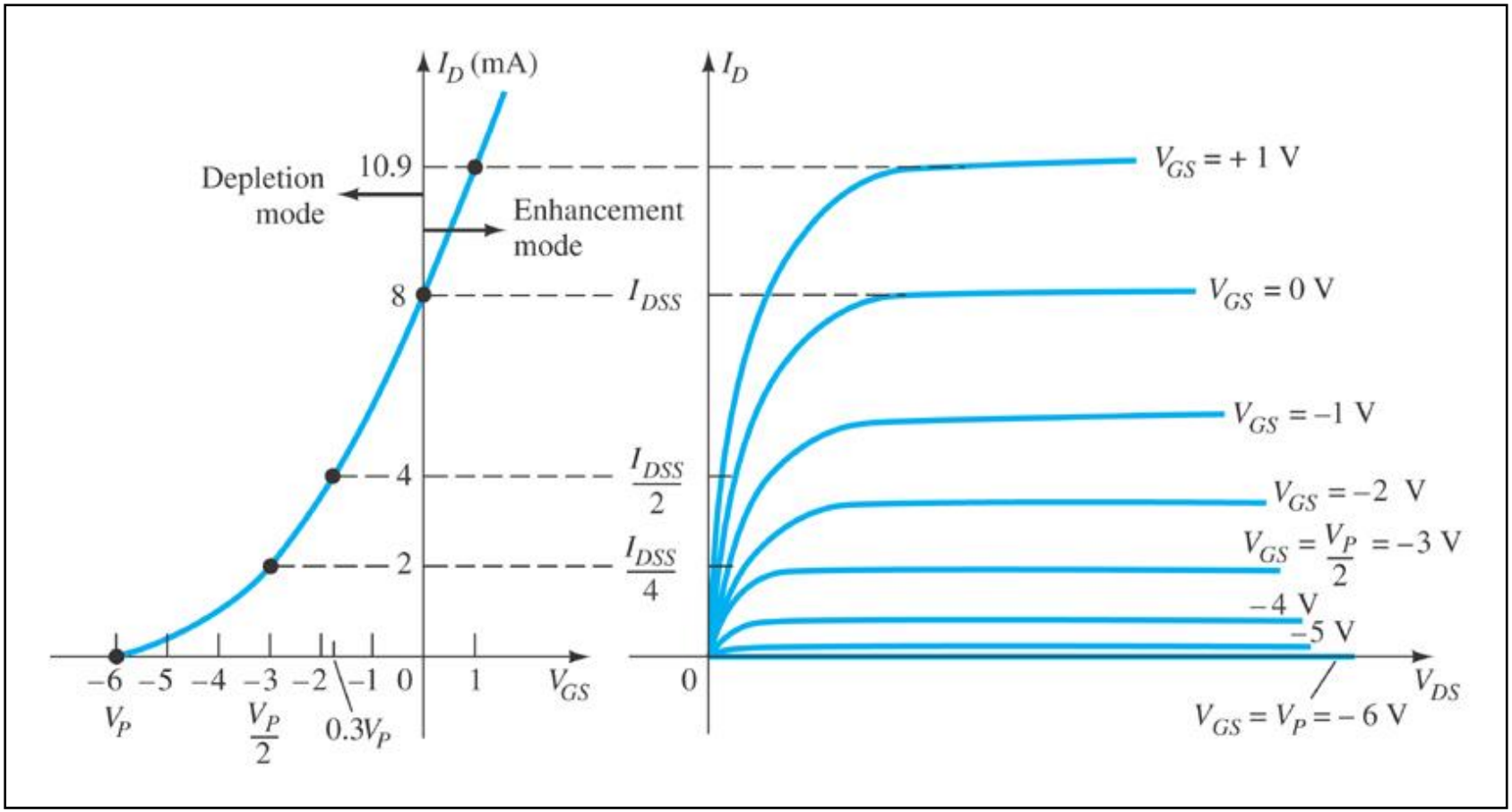
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 10\text{ mA}\left(1 - \frac{+1\text{ V}}{-4\text{ V}}\right)^2 = 10\text{ mA}(1 + 0.25)^2 = 10\text{ mA}(1.5625)$$

$$\cong 15.63\text{ mA}$$



Drain and Transfer Characteristic

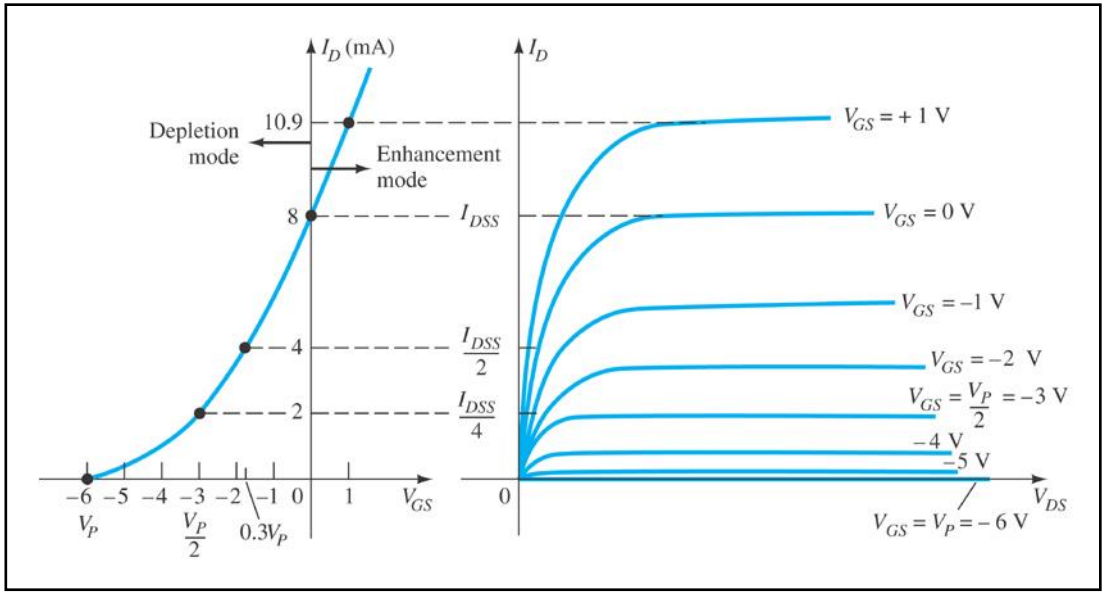


Depletion Mode Operation (D-MOSFET)

The characteristics are similar to a JFET.

When $V_{GS} = 0$ V, $I_D = I_{DSS}$

When $V_{GS} < 0$ V, $I_D < I_{DSS}$



The formula used to plot the transfer curve for a JFET applies to a D-MOSFET as well:

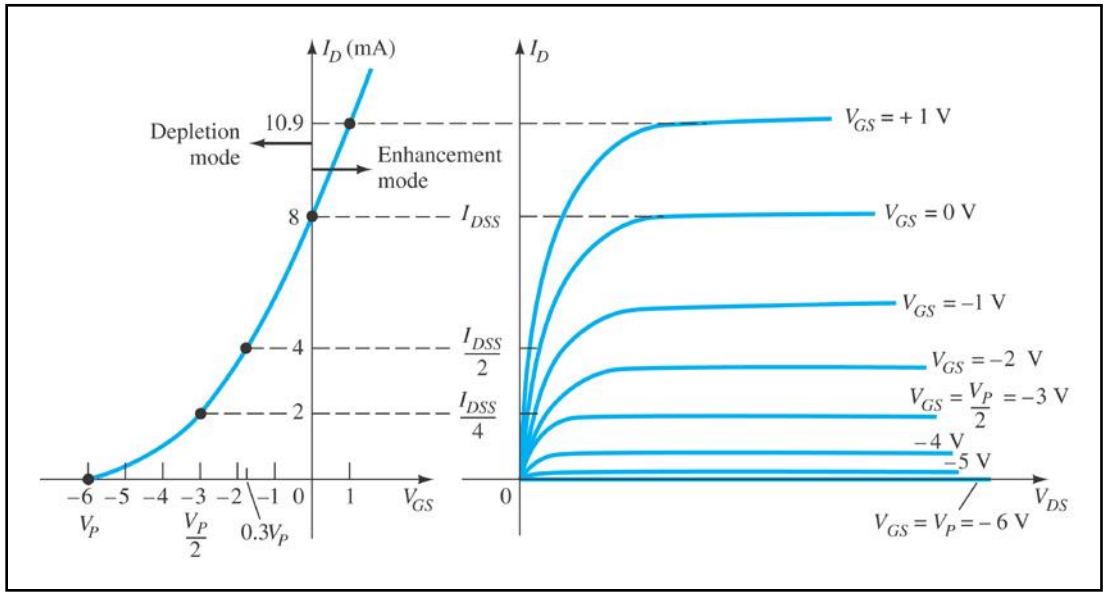
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Enhancement Mode Operation (D-MOSFET)

$V_{GS} > 0$ V, I_D increases above I_{DSS} ($I_D > I_{DSS}$)

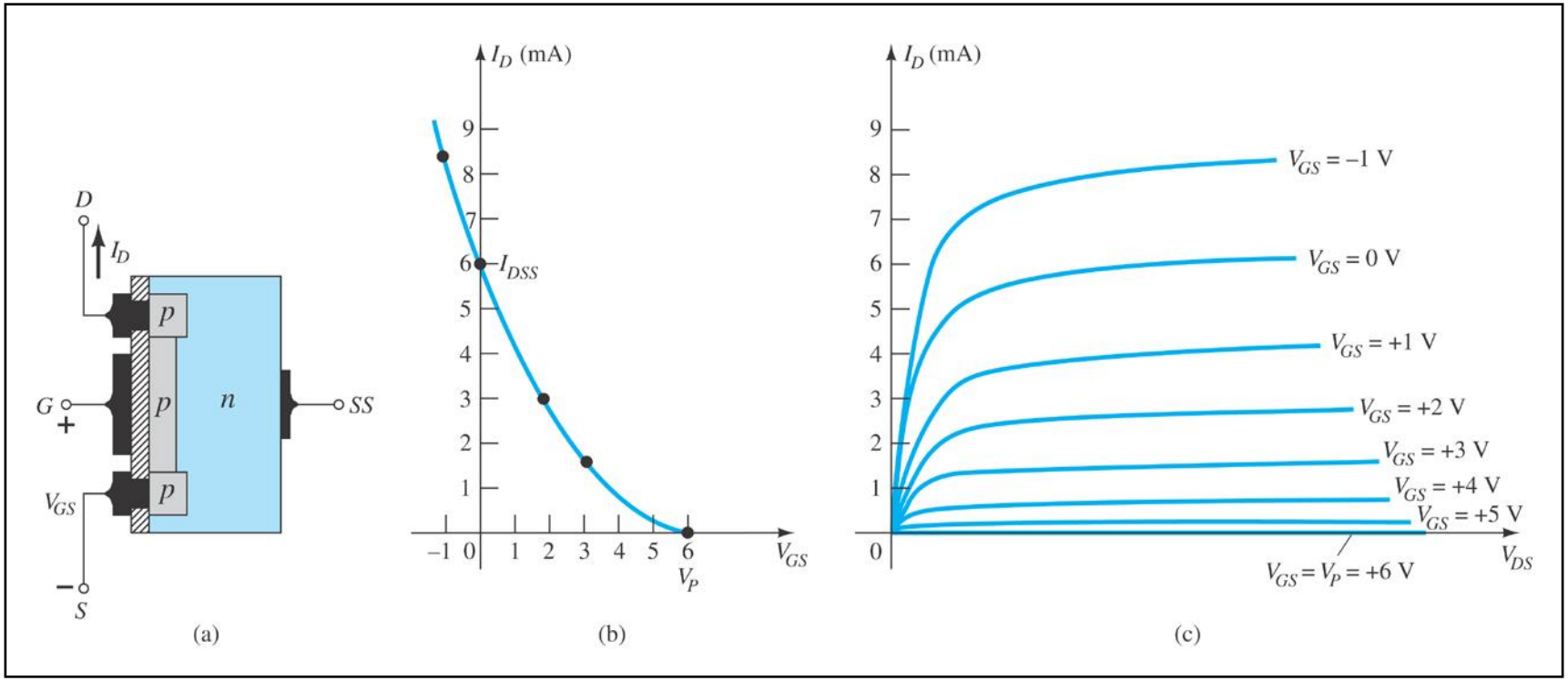
The formula used to plot the transfer curve still applies:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

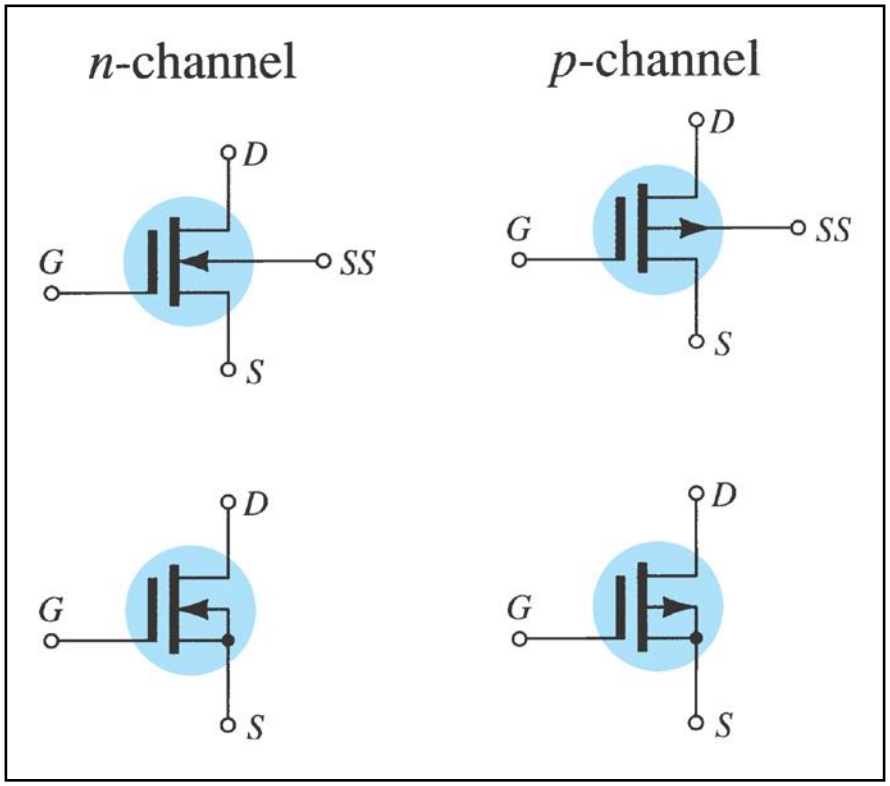


Note that V_{GS} is now positive

p-Channel D-Type MOSFET



D-Type MOSFET Symbols



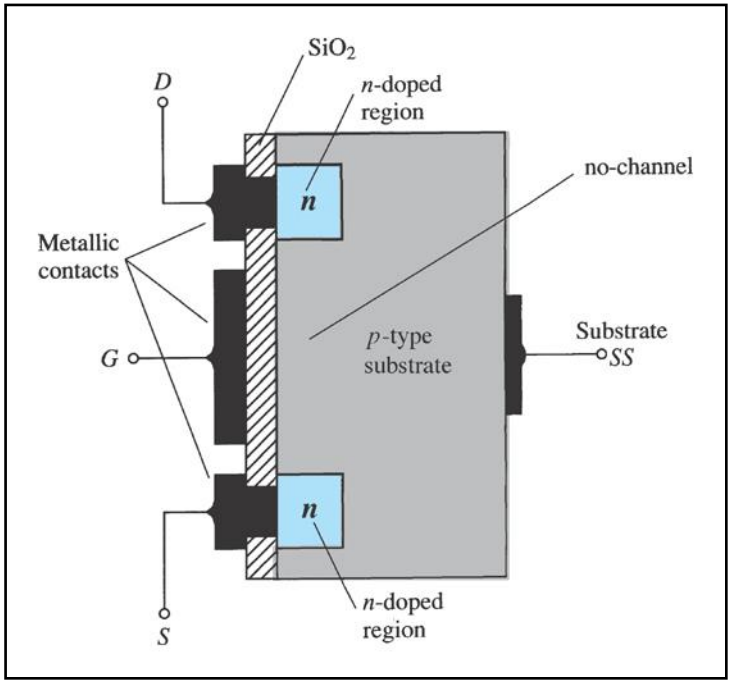
E-Type MOSFET

- The enhancement MOSFET (E-MOSFET) has no physical channel.
- Unlike JFETs and D-MOSFETs, the E-MOSFET cannot operate with V_{GS} =0 V.
- A channel is induced in an E-MOSFET by the application of a V_{GS} greater than the threshold value, $V_{GS(th)}$
- The transfer curve is not defined by Shockley's equation, and the drain current is now cut off until the gate-to-source voltage reaches a specific magnitude. In particular, current control in an n-channel device is now effected by a positive gate-to-source voltage rather than the range of negative voltages encountered for n-channel JFETs and n-channel depletion-type MOSFETs.

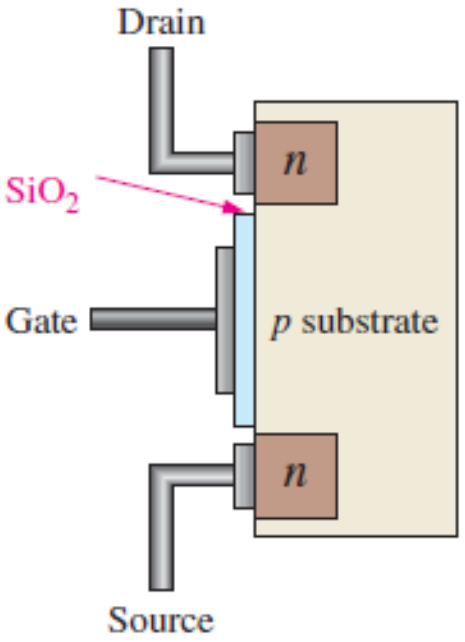
E-Type MOSFET Construction

The substrate is sometimes internally connected to the source terminal, while in other cases a fourth lead is made available for external control of its potential level. The source and drain terminals are again connected through metallic contacts to n-doped regions, but note in Fig. below the absence of a channel between the two n-doped regions.

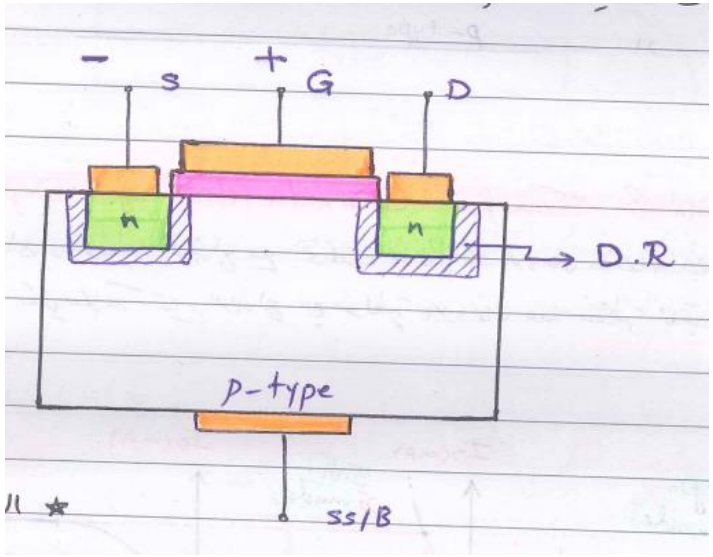
The SiO2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material. In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals

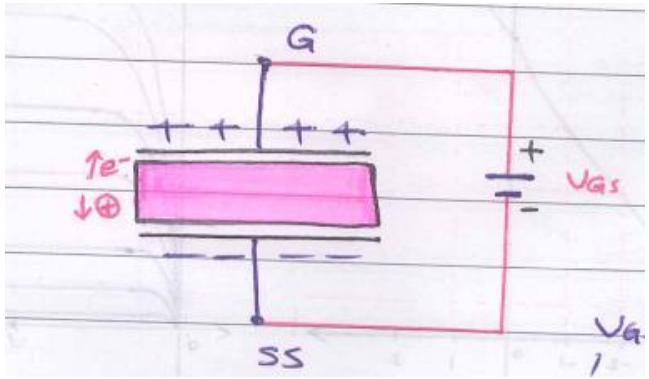


E-Type MOSFET Construction



(a) Basic construction





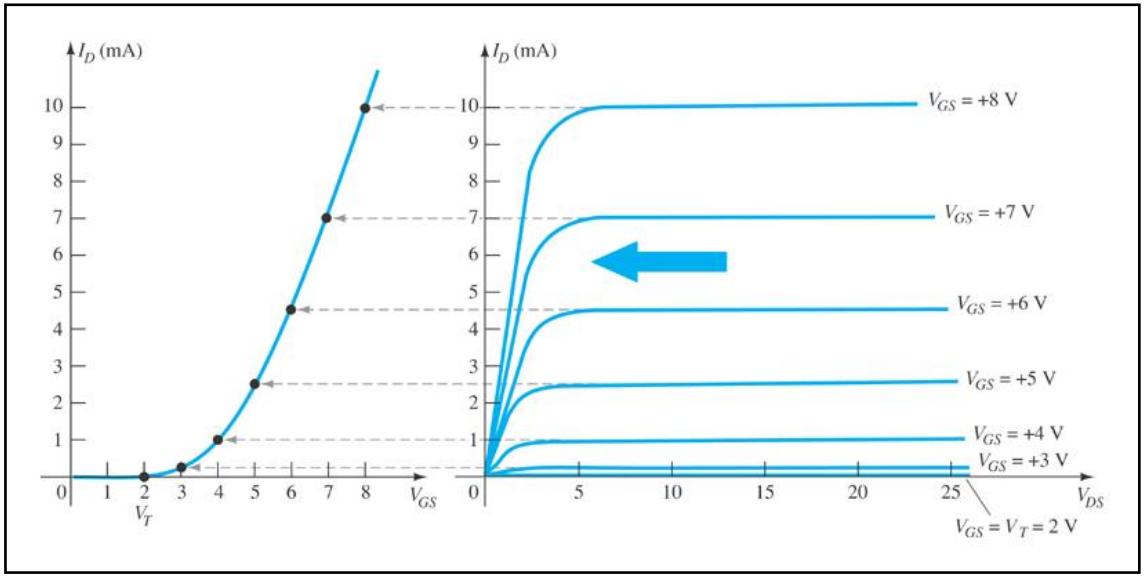
E-Type MOSFET Operation

The enhancement-type MOSFET (E-MOSFET) operates only in the enhancement mode.

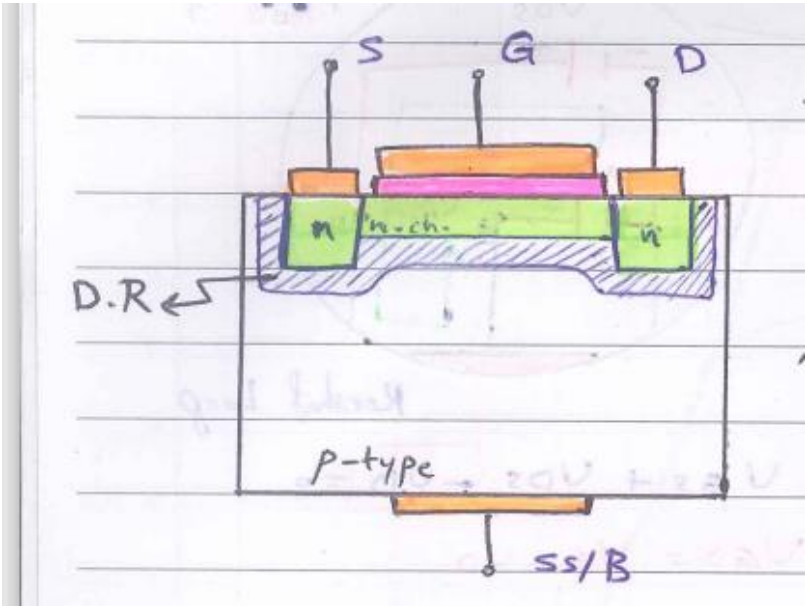
V_{GS} is always positive

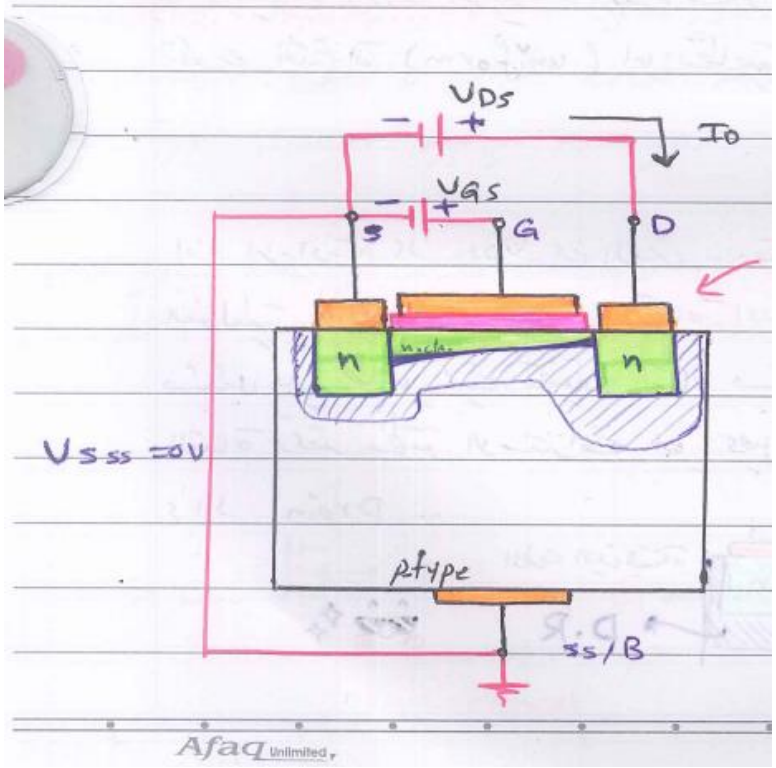
As V_{GS} increases, I_D increases

As V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS}) and the saturation level (V_{DSsat}) is reached

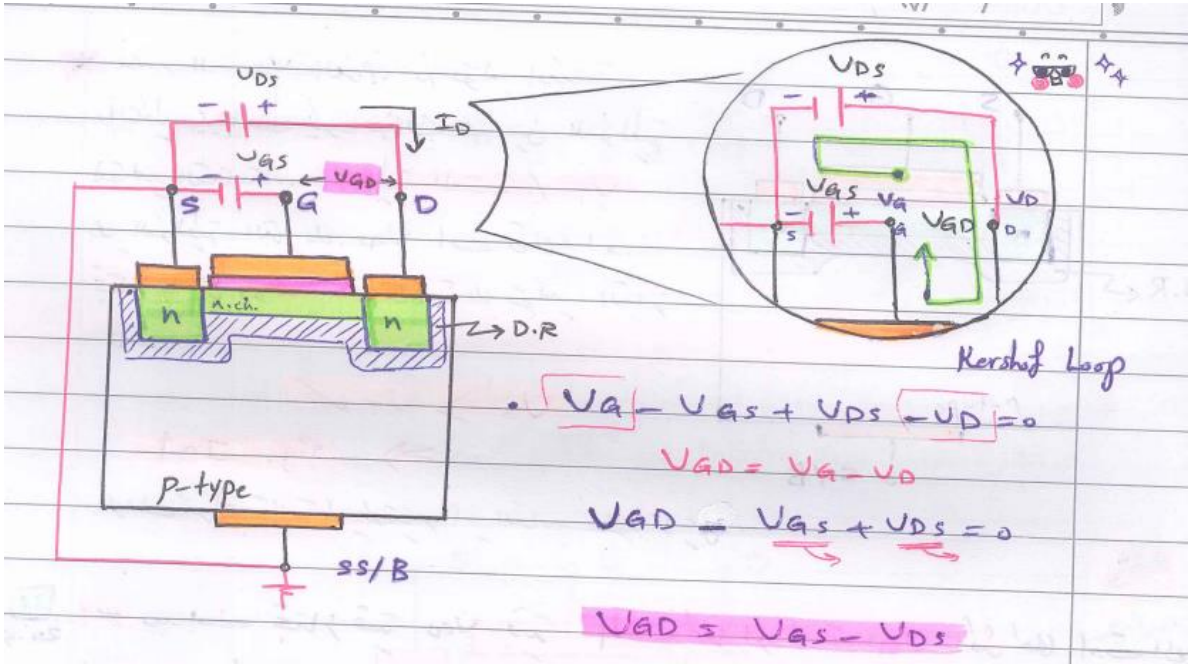


E-Type MOSFET Operation





E-Type MOSFET Operation



E-Type MOSFET Transfer Curve

To determine I_D given V_{GS}:

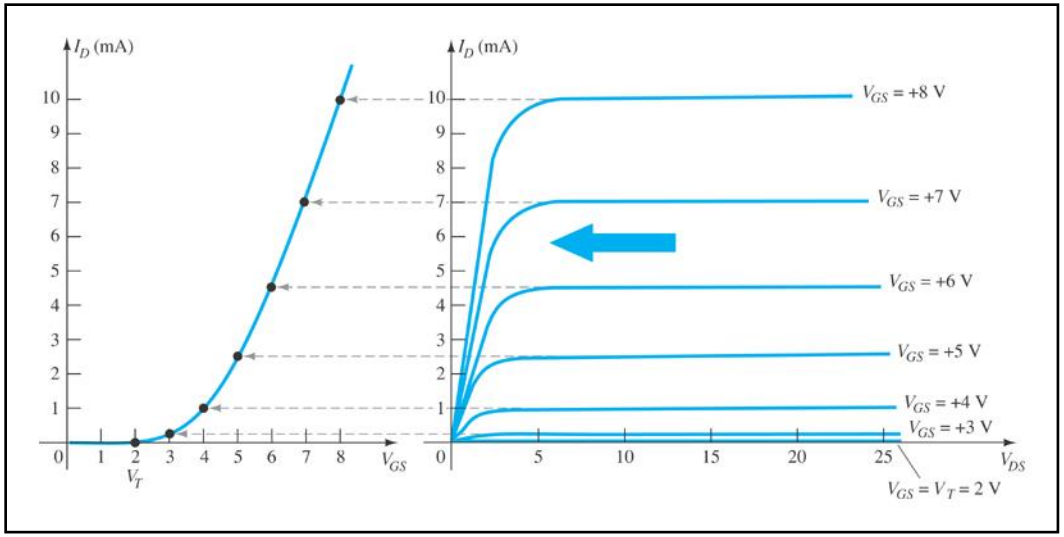
$$I_D = k(V_{GS} - V_T)^2$$

where:

V_T = the E-MOSFET threshold voltage

k, a constant, can be determined by using values at a specific point and the formula:

$$k = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$$

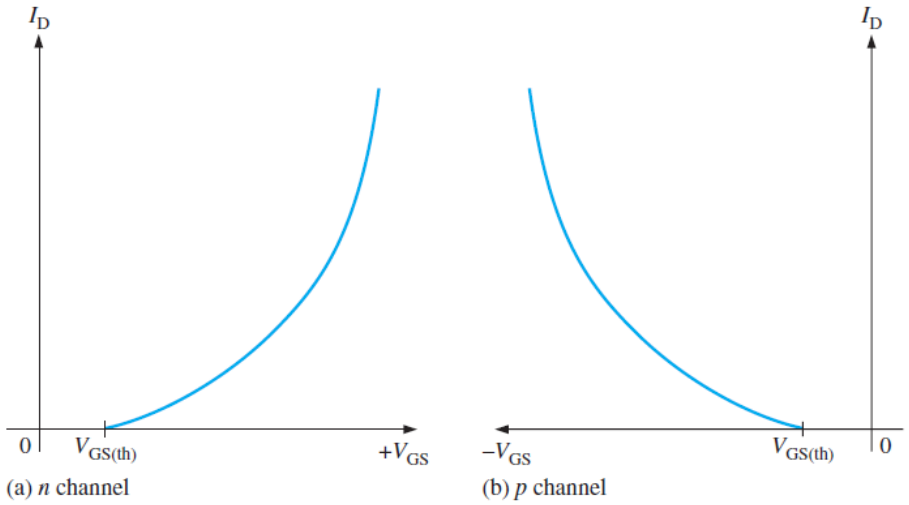


V_{DSsat} can be calculated using:

$$V_{DSsat} = V_{GS} - V_T$$

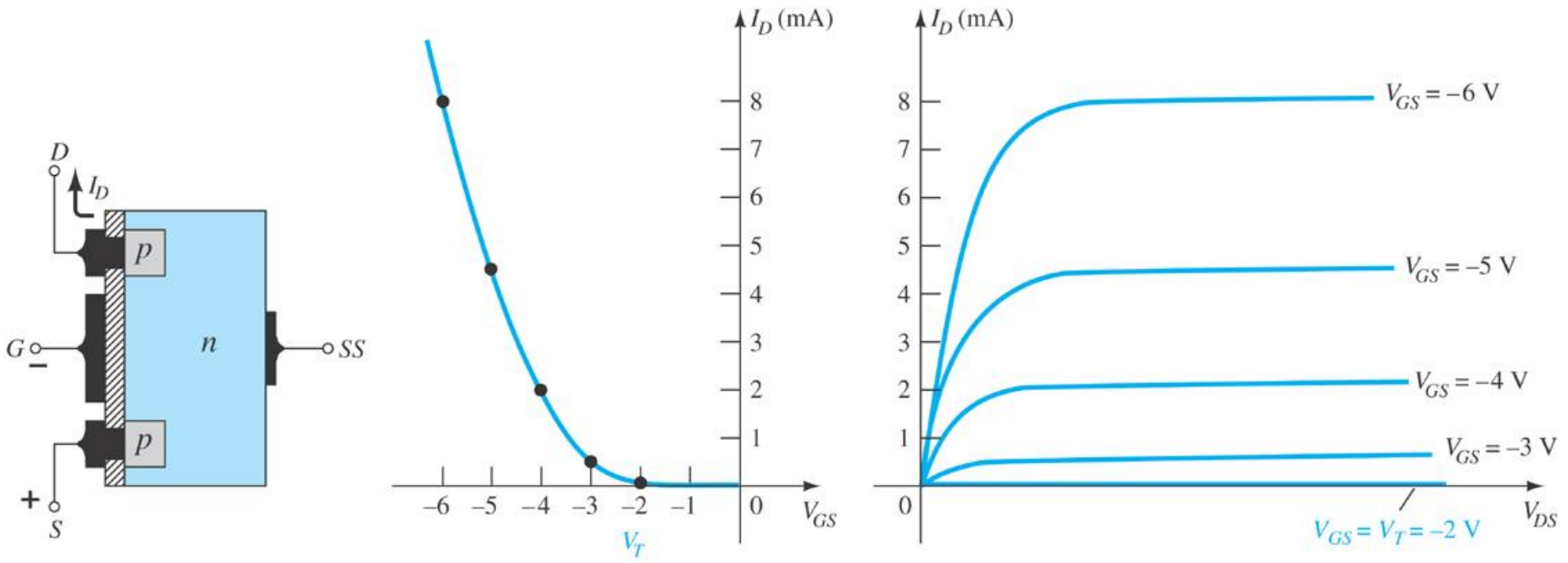
E-MOSFET Transfer Characteristic

The E-MOSFET uses only channel enhancement. Therefore, an n-channel device requires a positive gate-to-source voltage, and a p-channel device requires a negative gate-to-source voltage. The figure below shows the general transfer characteristic curves for both types of E-MOSFETs. As you can see, there is no drain current when V_{GS} =0. Therefore, the E-MOSFET does not have a significant I_{DSS} parameter, as do the JFET and the D-MOSFET.
Notice also that there is ideally no drain current until V_{GS} reaches a certain nonzero value called the threshold voltage, $V_{GS(th)}$.



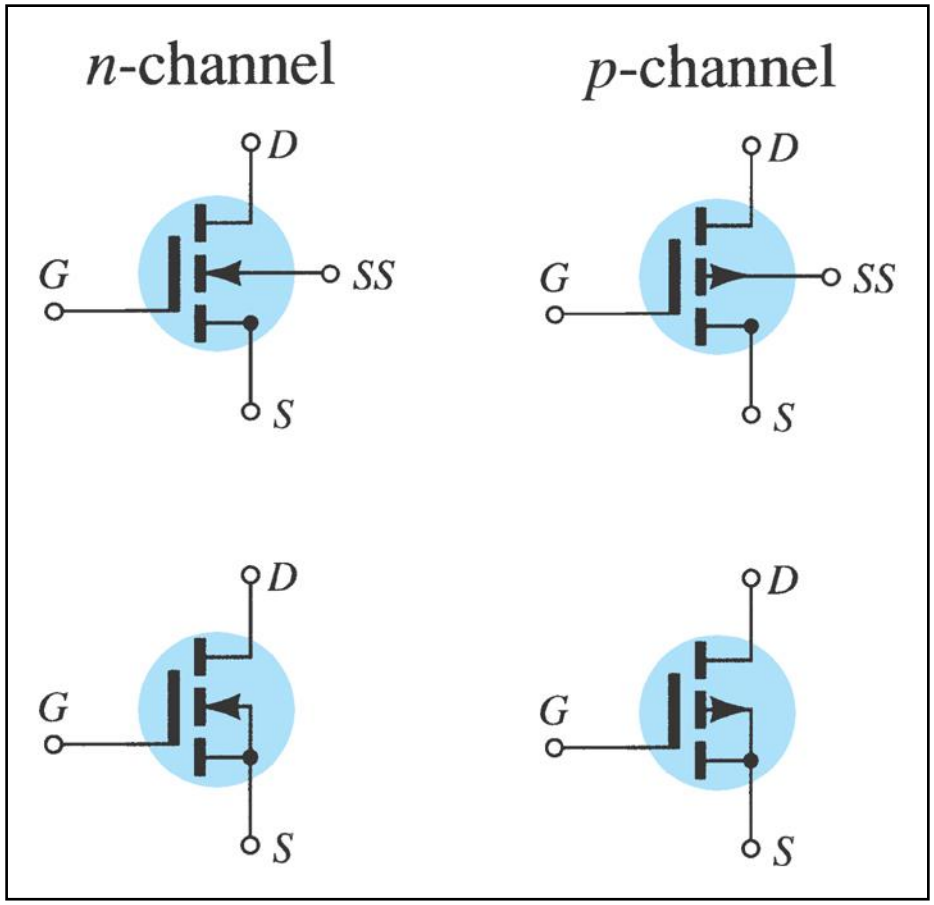
E-MOSFET general transfer characteristic curves.

p-Channel E-Type MOSFETs



The *p*-channel enhancement-type MOSFET is similar to its *n*-channel counterpart, except that the voltage polarities and current directions are reversed.

MOSFET Symbols



EXAMPLE: The datasheet for a 2N7002 E-MOSFET gives $I_{D(on)}$=500mA (minimum) at V_{GS}=10V and $V_{GS(th)}$=1V. Determine the drain current for V_{GS}= 5 V.

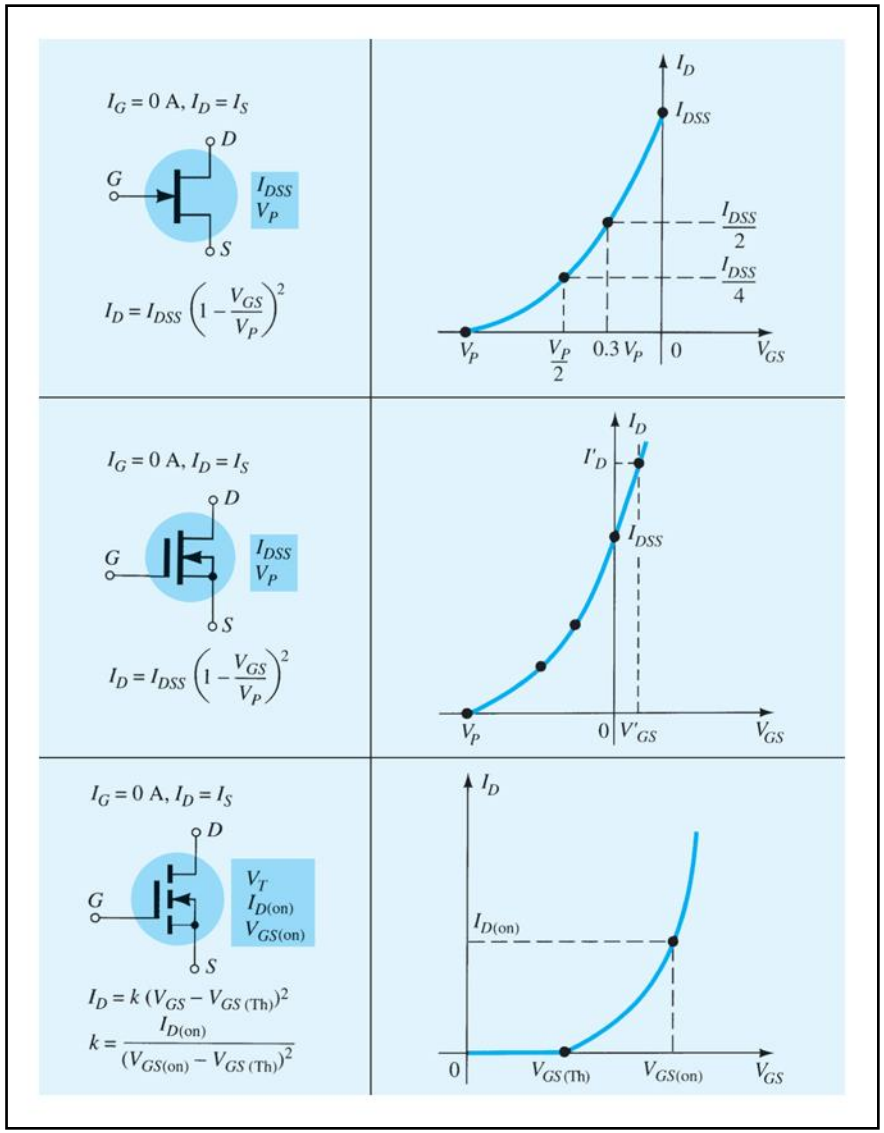
Solution:

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{500\text{ mA}}{(10\text{ V} - 1\text{ V})^2} = \frac{500\text{ mA}}{81\text{ V}^2} = 6.17\text{ mA/V}^2$$

Next, using the value of K, calculate I_D for $V_{GS} = 5$ V.

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (6.17\text{ mA/V}^2)(5\text{ V} - 1\text{ V})^2 = \mathbf{98.7\text{ mA}}$$

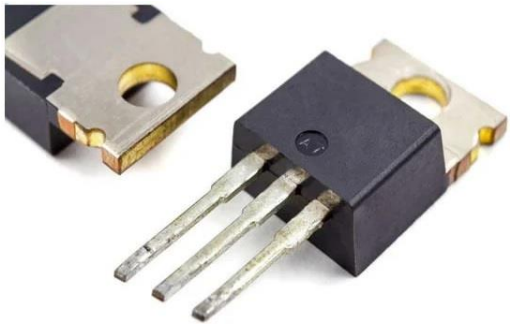
Summary Table



Ninevah University
College of Electronics Engineering
Department of Systems and Control

Electronic I I
Lecture 1

Field Effect Transistor (FET)



by
Rafal Raed Mahmood Alshaker

2nd Class

Topics of Second Semester

1 . Field-Effect Transistors

2. FET Amplifiers

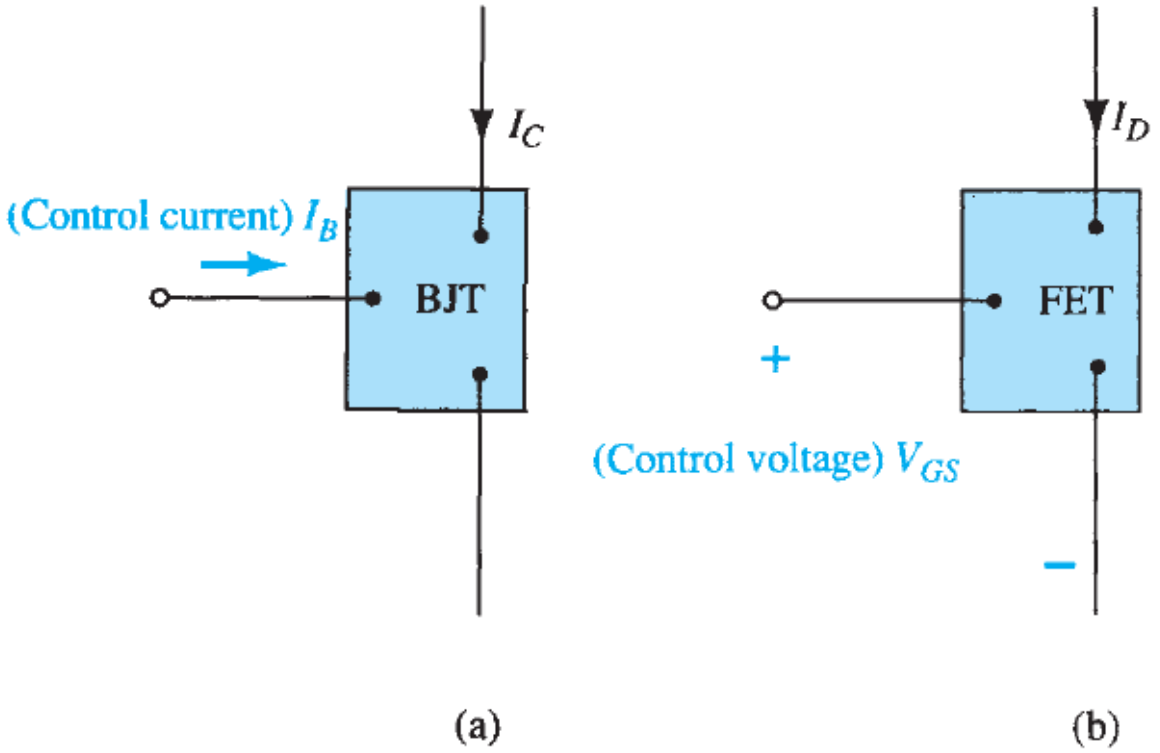
3. FET Amplifier Frequency Response

4. The Operational Amplifier

5 . Basic Op-Amp Circuits

6 . Active Filters

Transistors



FETs vs BJTs

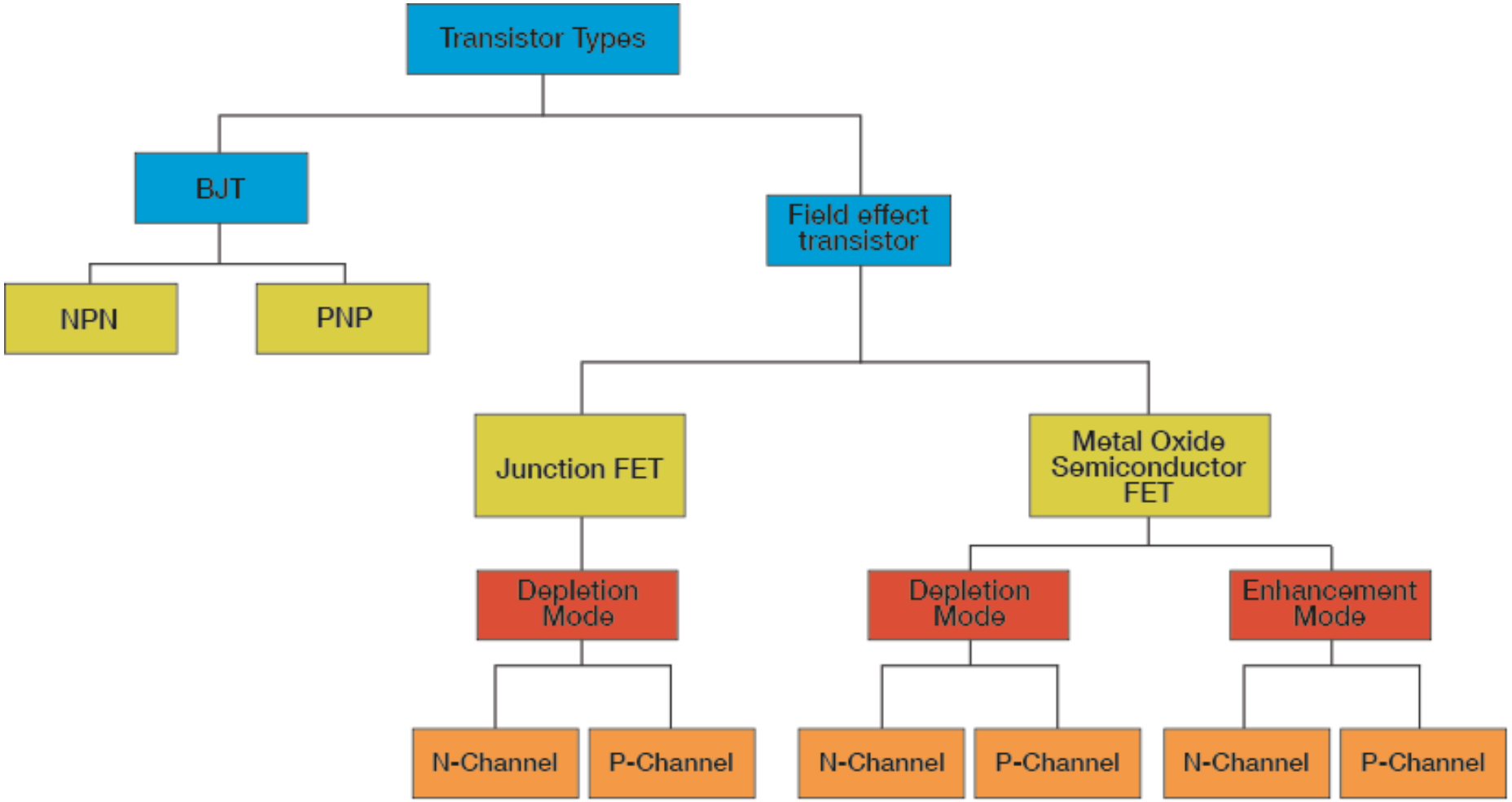
Similarities:

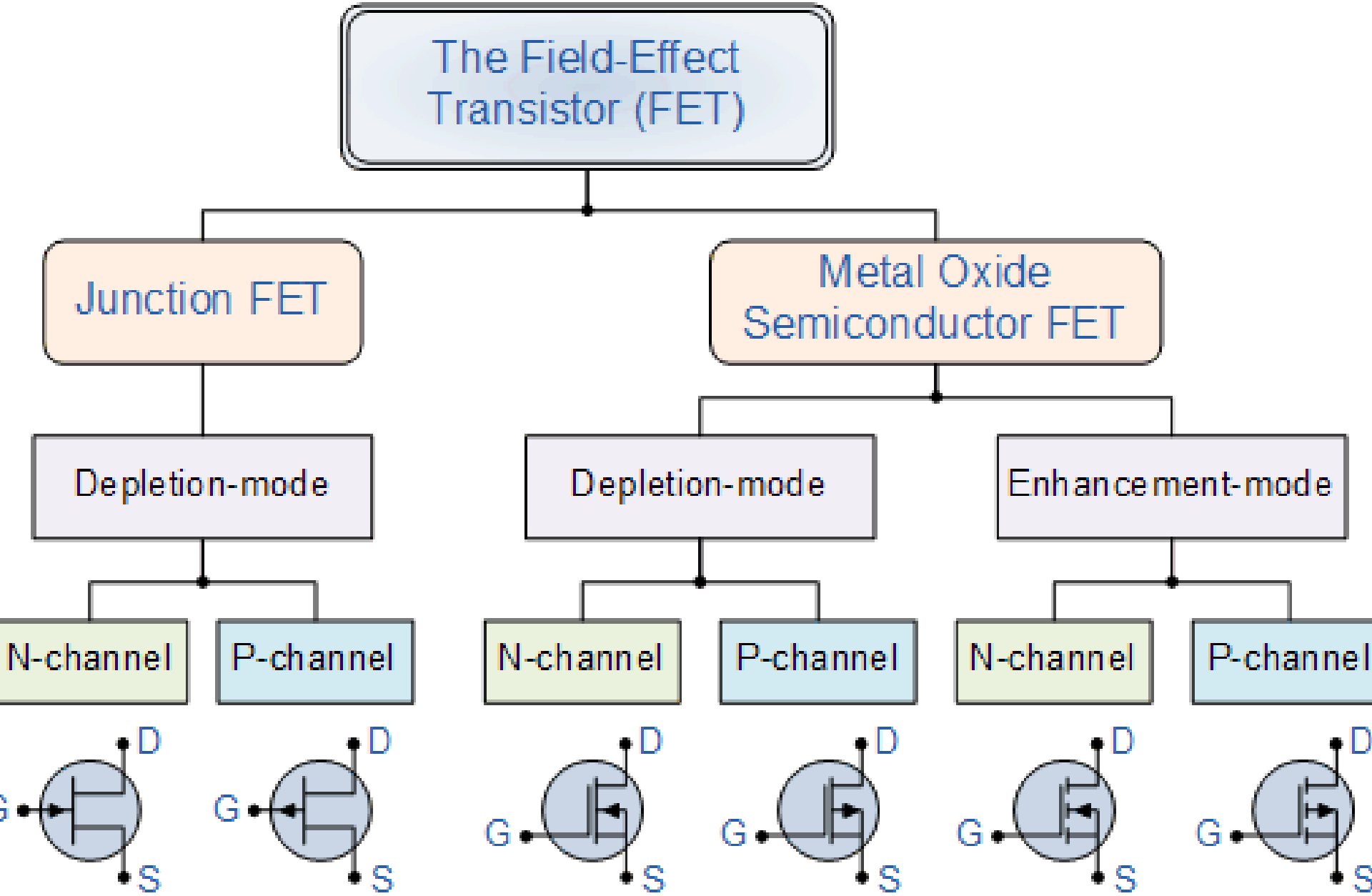
- **Amplifiers**
- **Switching devices**
- **Impedance matching circuits**

Differences:

- **FETs are voltage controlled devices. BJTs are current controlled devices.**
- **FETs have a higher input impedance. BJTs have higher gains.**
- **FETs are less sensitive to temperature variations and are more easily integrated on ICs.**

Classification of FET




The Field-Effect Transistor (FET)
Junction FET
Metal Oxide Semiconductor FET
Depletion-mode
Depletion-mode
Enhancement-mode
N-channel
P-channel
N-channel
P-channel
N-channel
P-channel
D
G
S

FET (Field Effect Transistor)

- Unipolar device i. e. operation depends on only one type of charge carrier.
- Voltage-controlled Device (gate voltage controls drain current).
- Very high input impedance ($\approx 10^9$-$10^{12}\,\Omega$).
- Low-power consumption.
- Less Noisy as Compared to BJT.
- Very small in size, occupies very small space in Ics.

Junction field-effect transistor..

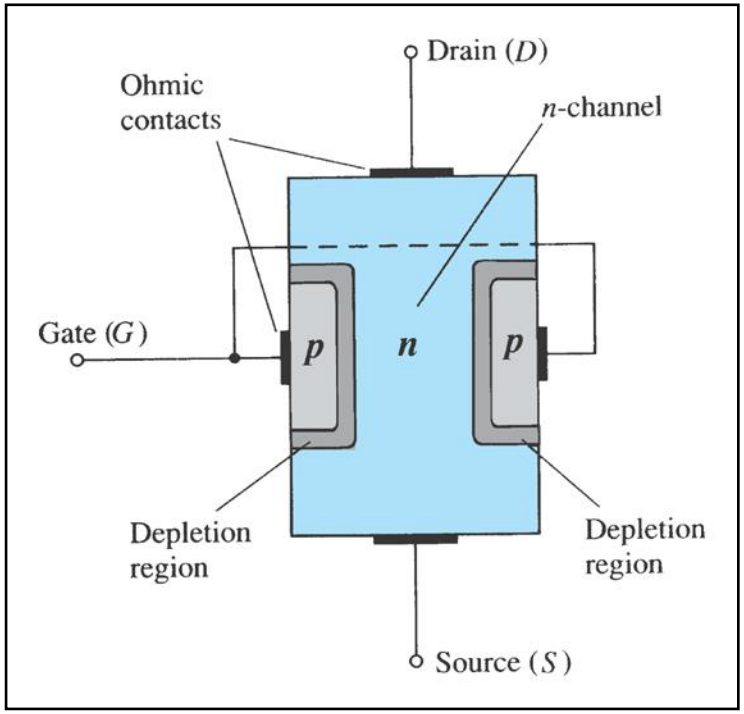
- There are 2 types of JFET
  - n-channel JFET
  - p-channel JFET
- Three Terminal
  - Drain – D
  - Gate -G
  - Source – S

JFET Construction

There are two types of JFETs:

***n*-channel**
***p*-channel**

The n-channel is the more widely used of the two.



JFETs have three terminals:

The **Drain** (D) and **Source** (S) are connected to the *n*-channel

The **Gate** (G) is connected to the *p*-type material

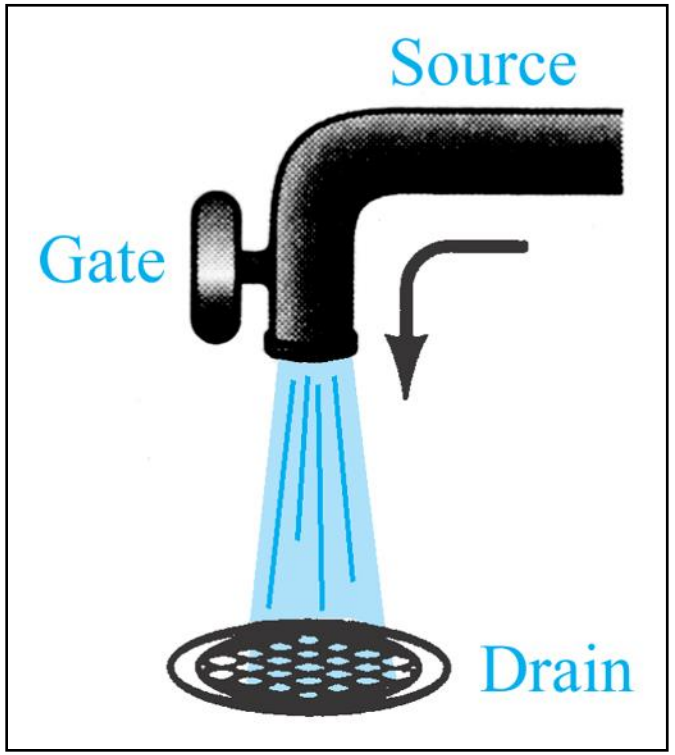
JFET Operation: The Basic Idea

JFET operation can be compared to that of a water spigot.

The **source** is the accumulation of electrons at the negative pole of the drain-source voltage.

The **drain** is the electron deficiency (or holes) at the positive pole of the applied voltage.

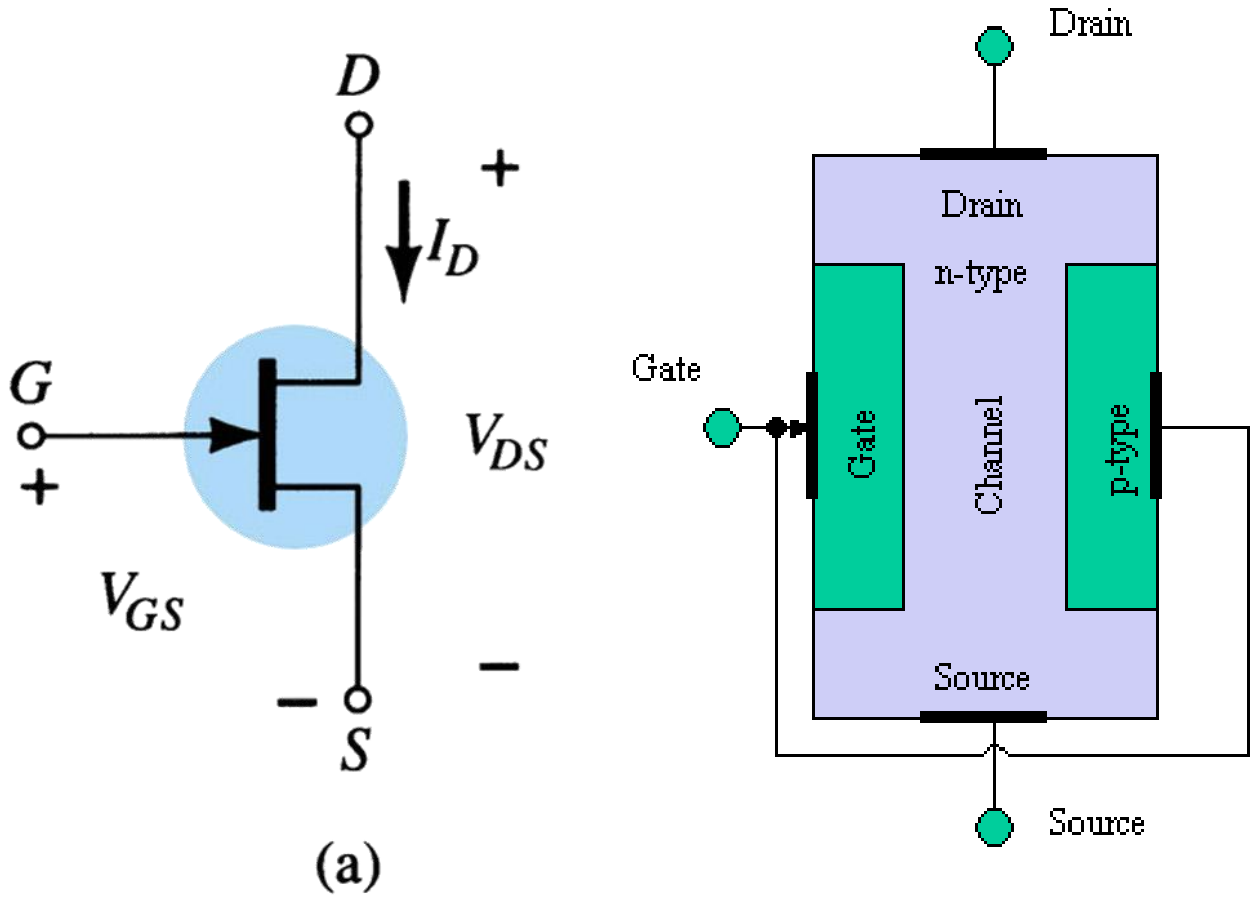
The **gate** controls the width of the n-channel and, therefore, the flow of charges from source to drain.



N–channel JFET

- N channel JFET:
  - Major structure is n-type material (channel) between embedded p-type material to form 2 p-n junction.
  - In the normal operation of an n-channel device, the Drain (D) is positive with respect to the Source (S). Current flows into the Drain (D), through the channel, and out of the Source (S)
  - Because the resistance of the channel depends on the gate-to-source voltage (V_{GS}), the drain current (I_D) is controlled by that voltage

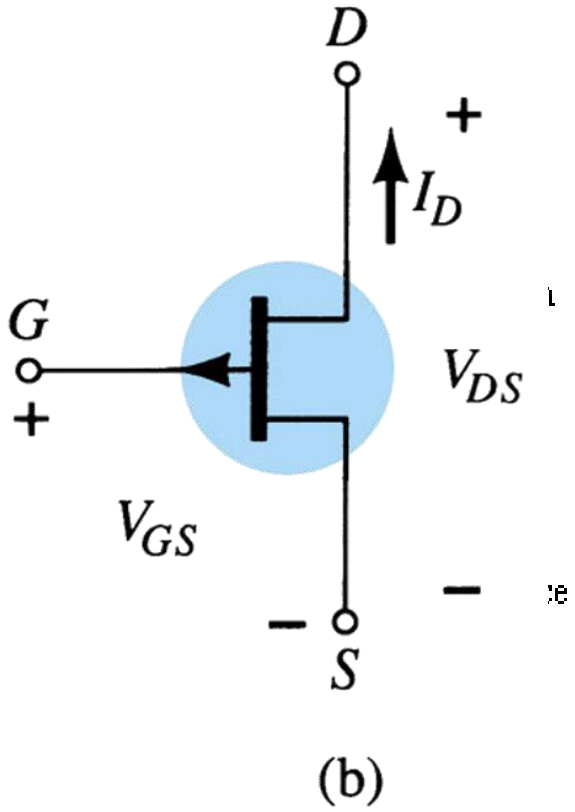
N-channel JFET..

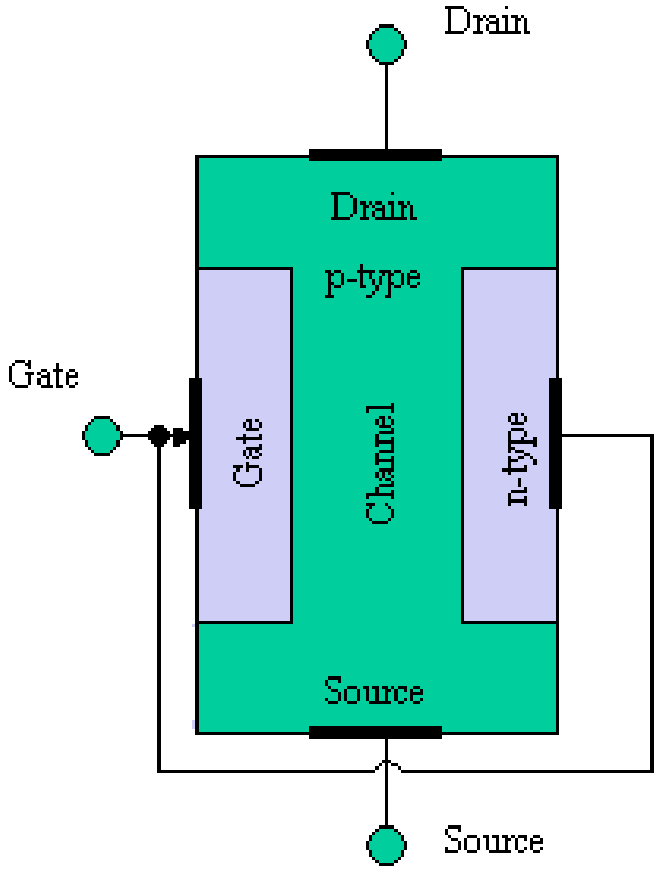


P-channel JFET

- P channel JFET:
  - Major structure is p-type material (channel) between embedded n-type material to form 2 p-n junction.
  - Current flow : from Source (S) to Drain (D)
  - Holes injected to Source (S) through p-type channel and flowed to Drain (D)

P–channel JFET..

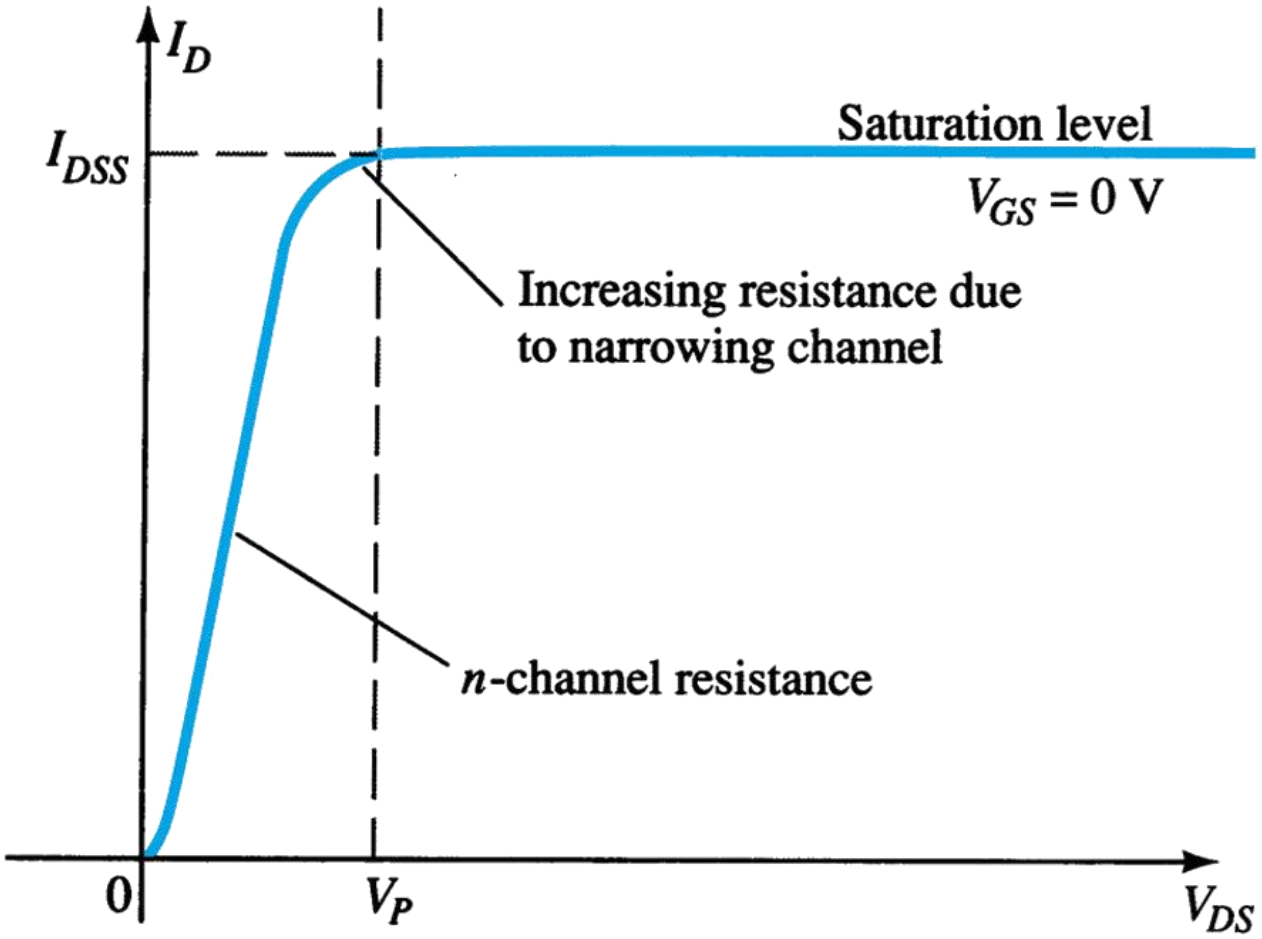




JFET Characteristic Curve

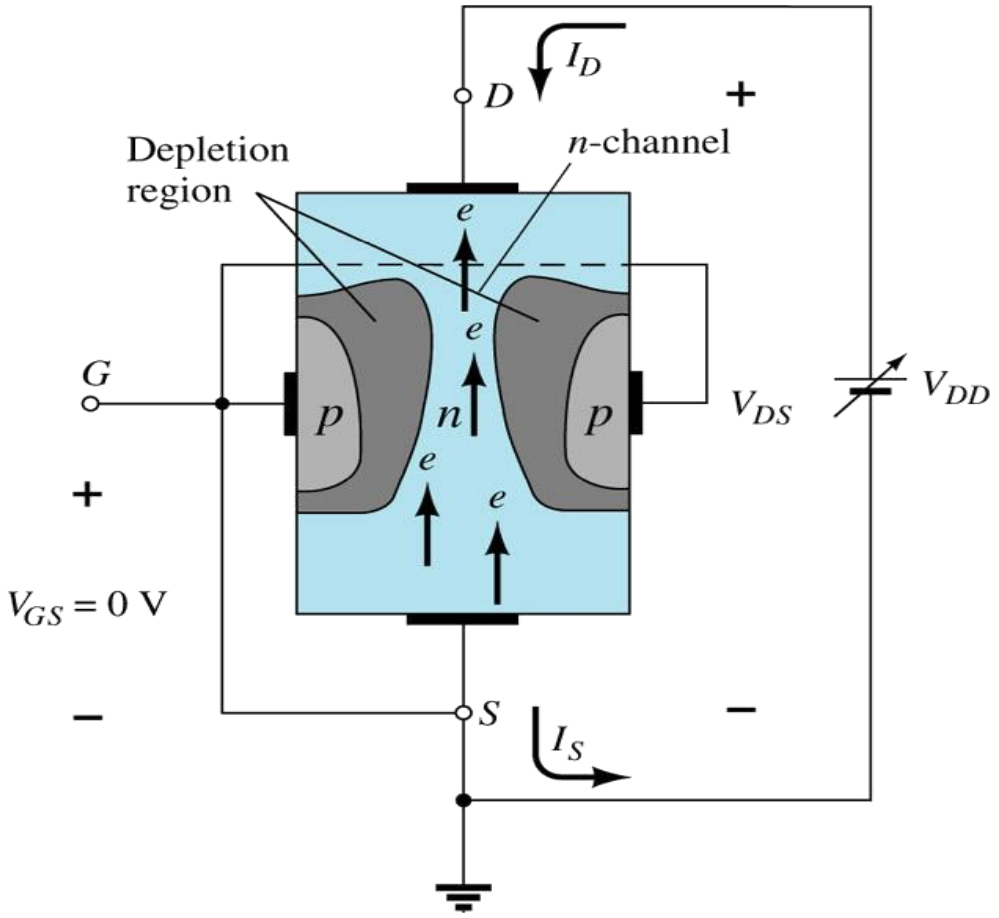
- To start, suppose $V_{GS}=0$
- Then, when V_{DS} is increased, I_D increases. Therefore, I_D is proportional to V_{DS} for small values of V_{DS}
- For larger value of V_{DS}, as V_{DS} increases, the depletion layer become wider, causing the resistance of channel increases.
- After the pinch-off voltage (V_p) is reached, the I_D becomes nearly constant (called as I_D maximum, I_{DSS}-Drain to Source current with Gate Shorted)

I_D versus V_{DS} for $V_{GS} = 0$ V.



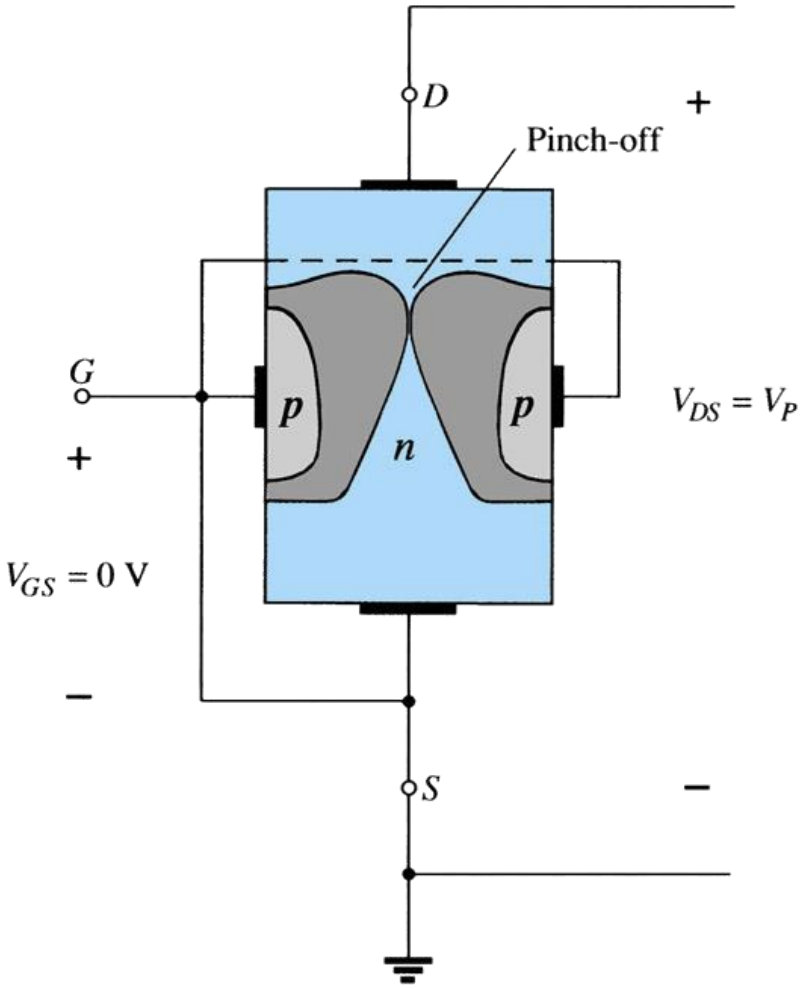
JFET Characteristic Curve

JFET for $V_{GS} = 0$ V and $0 < V_{DS} < |V_p|$

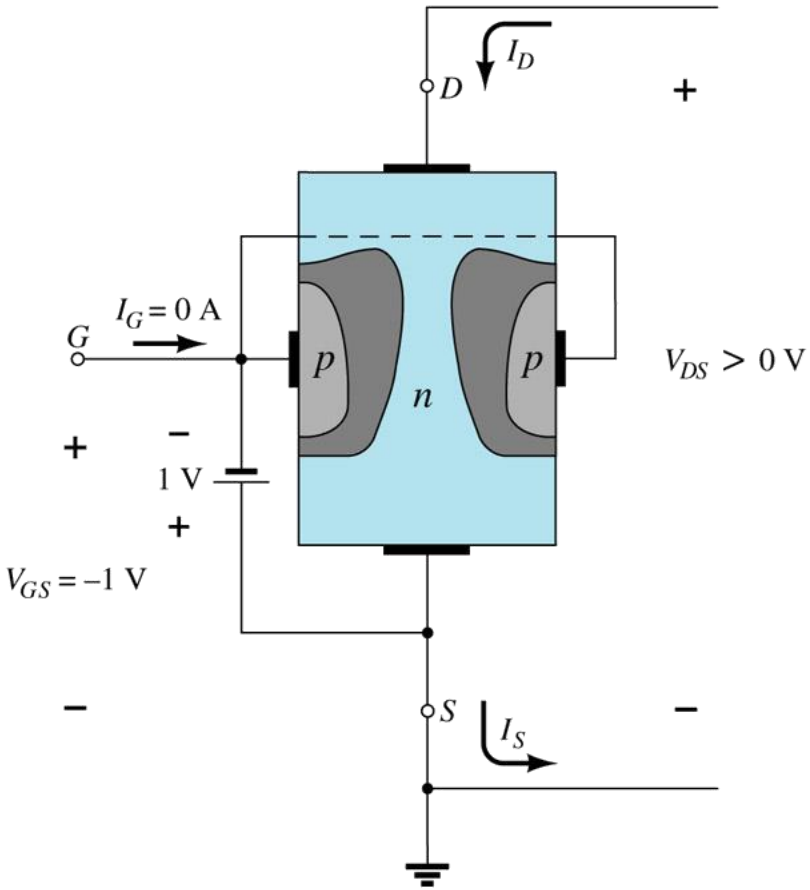


Channel becomes narrower as V_{DS} is increased

Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).



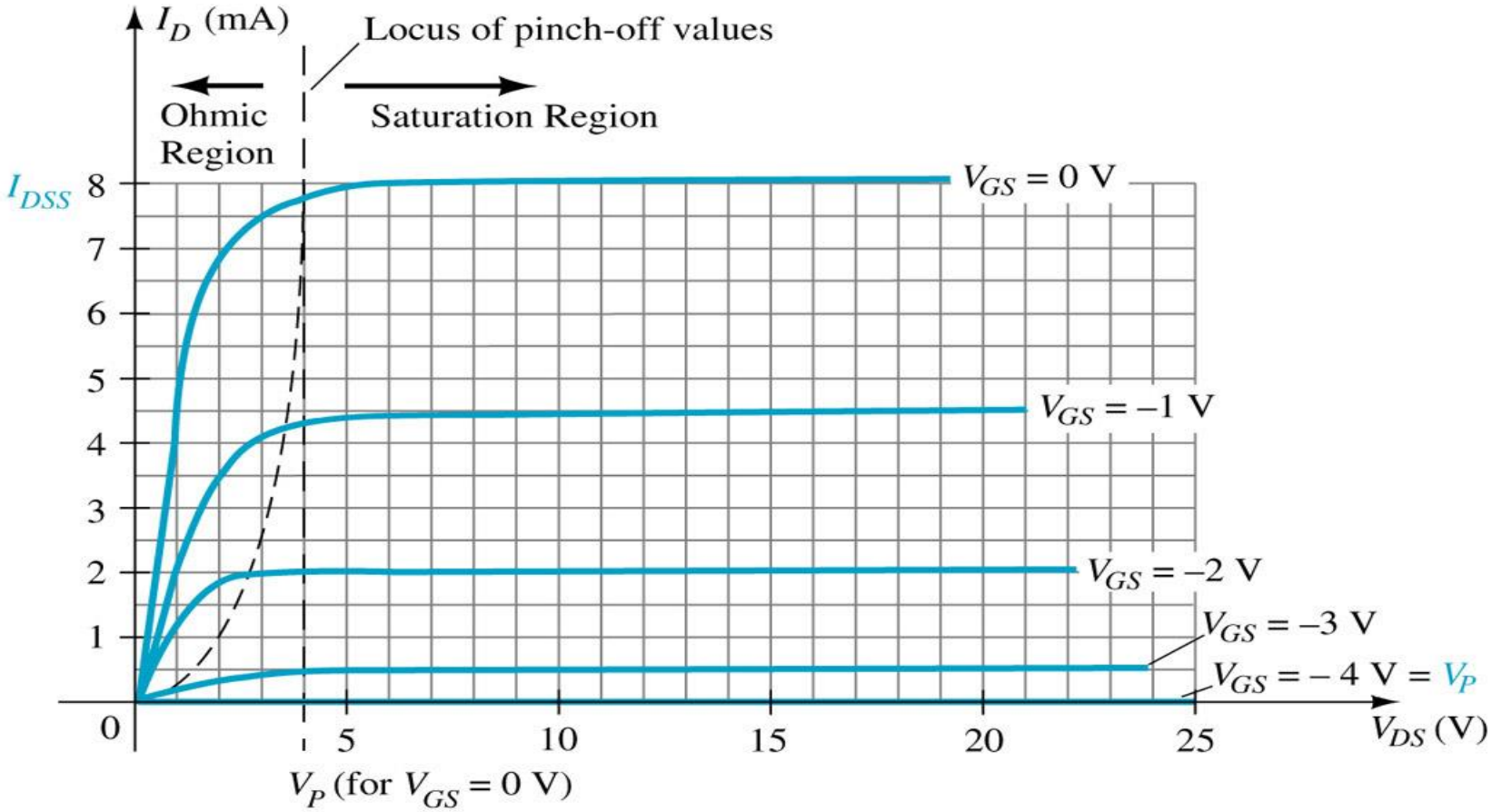
Application of a negative voltage to the gate of a JFET.



JFET Characteristic Curve..

- For negative values of V_{GS}, the gate-to-channel junction is reverse biased even with $V_{DS}=0$
- Thus, the initial channel resistance is higher (in which the initial slope of the curves is smaller for values of V_{GS} closer to the pinch-off voltage (V_P)
- The resistance value is under the control of V_{GS}
- If V_{GS} is less than pinch-off voltage, the resistance becomes an open-circuit ;therefore the device is in cutoff ($V_{GS}=V_{GS(off)}$)
- The region where I_D constant – The saturation/pinch-off region
- The region where I_D depends on V_{DS} is called the linear/triode/ohmic region

n-Channel JFET characteristics curve with $I_{DSS} = 8$ mA and $V_P = -4$ V.



JFET Characteristic Curve

JFET Operating Characteristics

There are three basic operating conditions for a JFET:

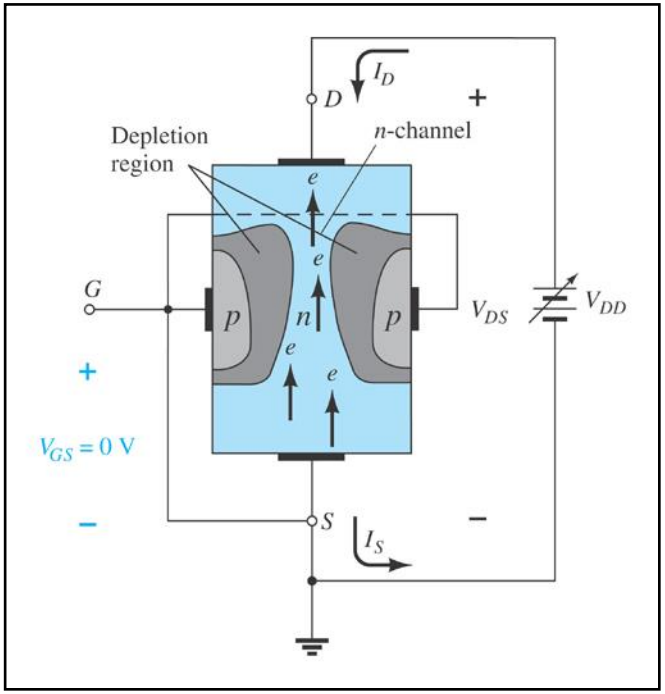
- $V_{GS} = 0$ V, V_{DS} increasing to some positive value
- $V_{GS} < 0$ V, V_{DS} at some positive value
- Voltage-controlled resistor

JFET Characteristics: V_{GS} =0V

Three things happen when V_{GS} = 0 V and V_{DS} increases from 0 V to a more positive voltage:

- The size of the depletion region between *p*- type gate and *n*-channel increases.
- Increasing the size of the depletion region decreases the width of the *n*-channel, which increases its resistance.

- Even though the *n*-channel resistance is increasing, the current from source to drain (I_D) through the *n*-channel is increasing because V_{DS} is increasing

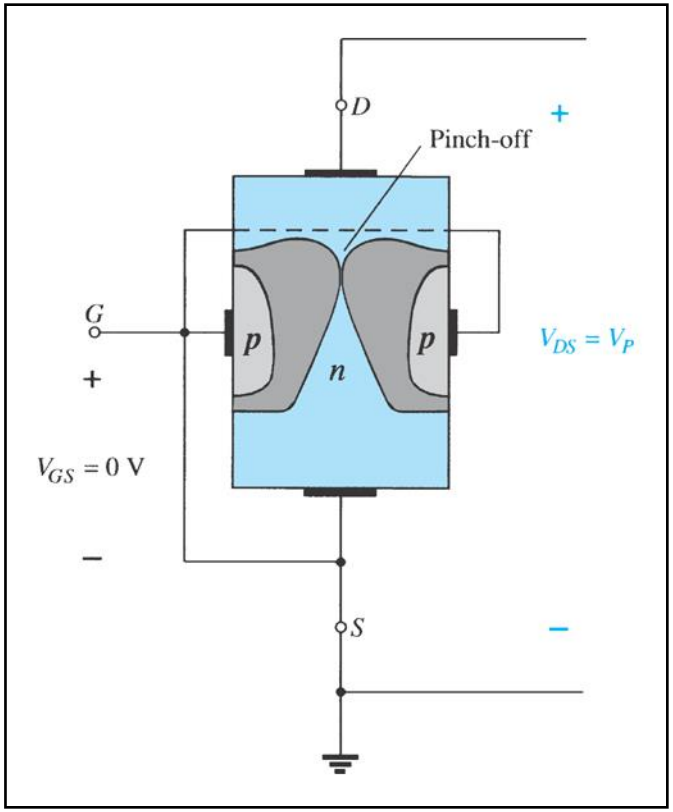


H.W لماذا يكون عرض منطقة الاستنزاف اكبر من الاعلى

JFET Characteristics: Pinch Off

• If V_{GS} = 0 V and V_{DS} continually increases to a more positive voltage, a point is reached where the depletion region gets so large that it pinches off the channel.

• This suggests that the current in channel (I_D) drops to 0 A, but it does not: As V_{DS} increases, so does I_D. However, once pinch off occurs, further increases in V_{DS} do not cause I_D to increase.

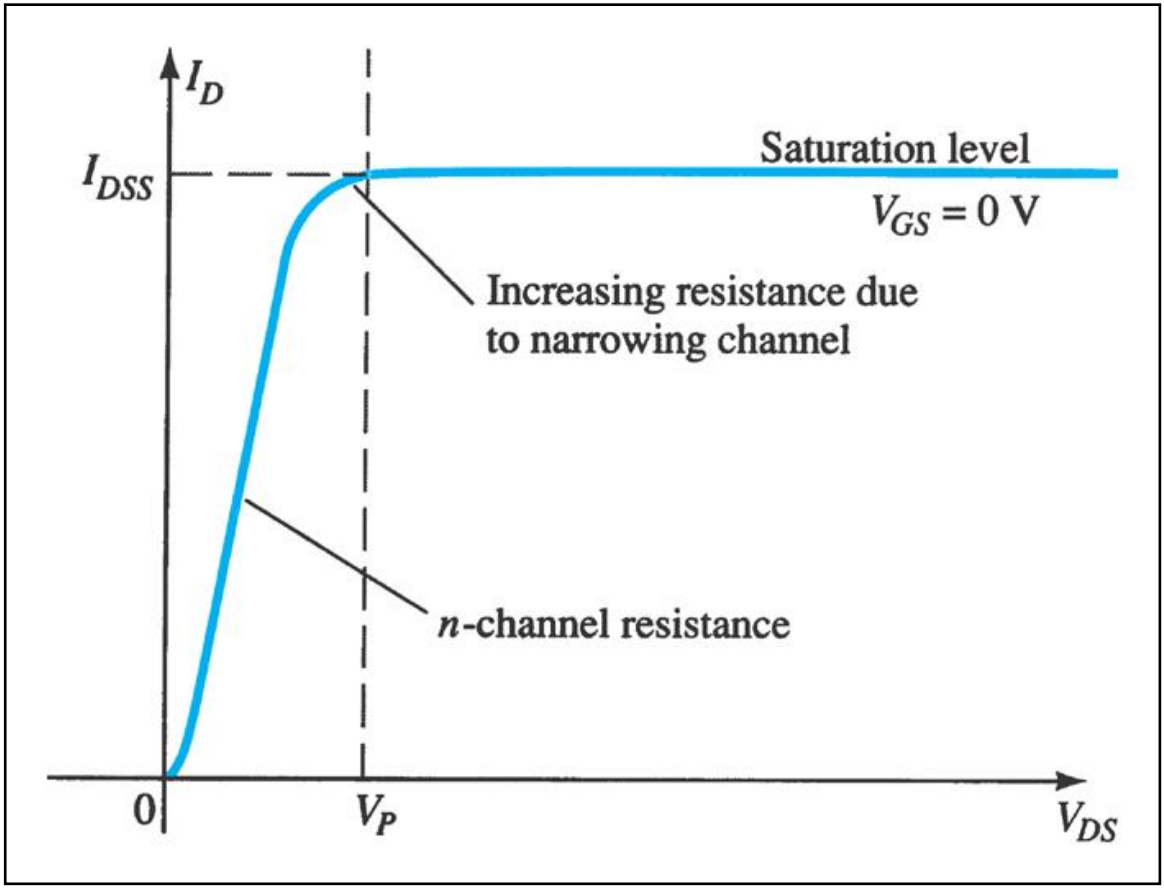


JFET Characteristics: Saturation

At the pinch-off point:

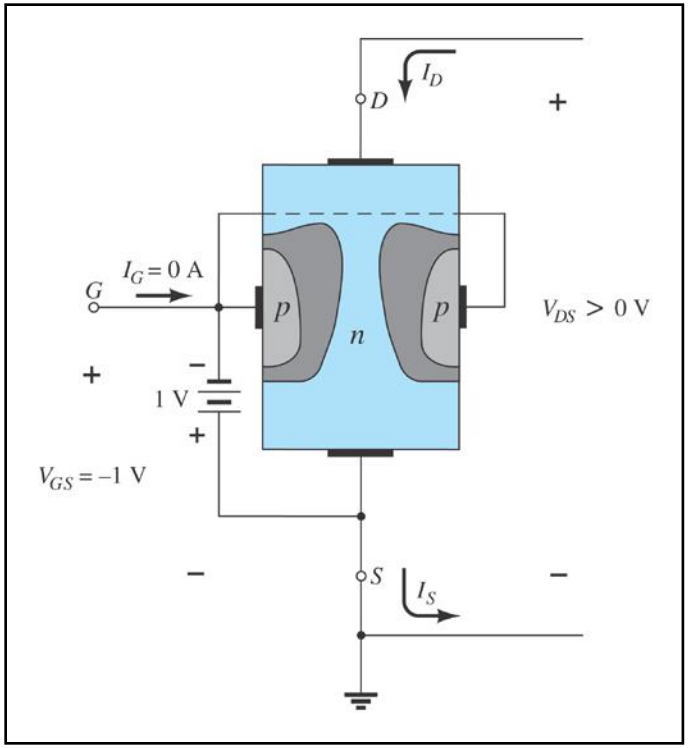
Any further increase in V_{DS} does not produce any increase in I_D. V_{DS} at pinch-off is denoted as V_p

I_D is at saturation or maximum, and is referred to as I_{DSS}.



JFET Operating Characteristics

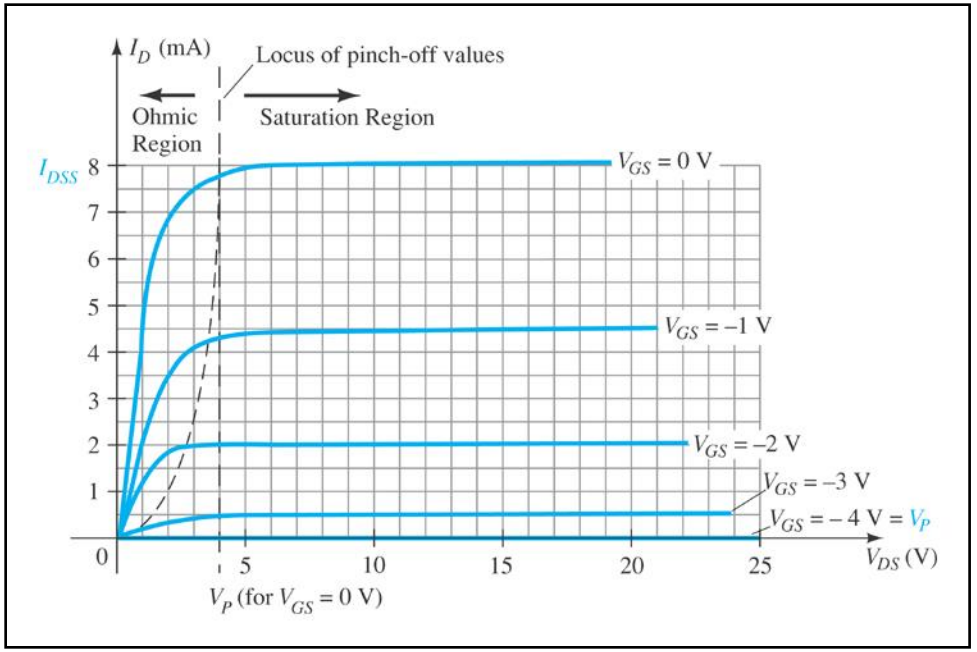
As V_{GS} becomes more negative, the depletion region increases.



JFET Operating Characteristics

As V_{GS} becomes more negative:

- The JFET experiences pinch-off at a lower voltage (V_P).
- I_D decreases ($I_D < I_{DSS}$) even when V_{DS} increases
- I_D eventually drops to 0 A. The value of V_{GS} that causes this to occur is designated $V_{GS(off)}$.



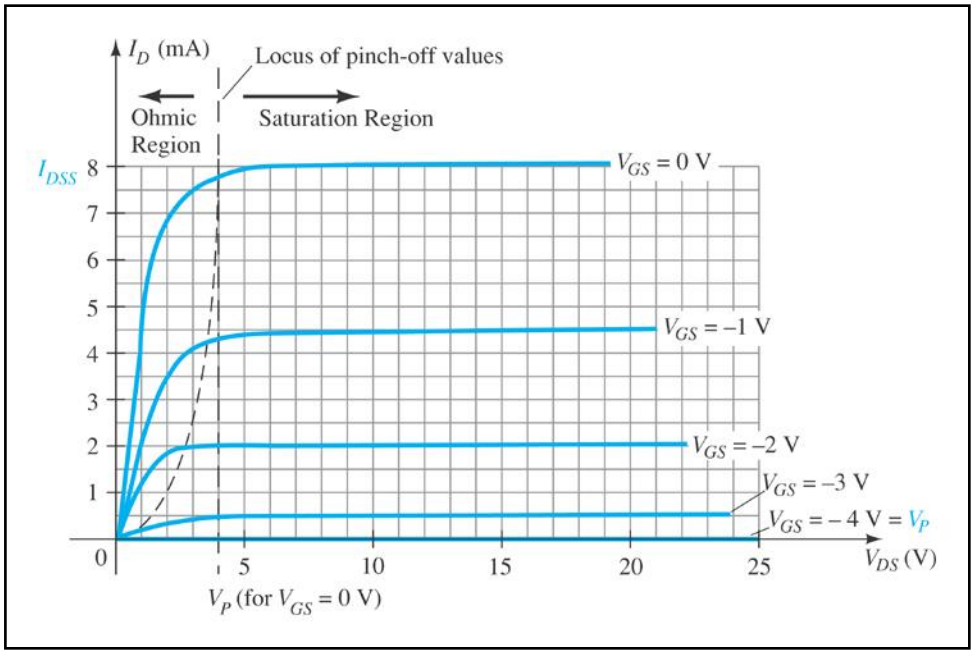
Note that at high levels of V_{DS} the JFET reaches a breakdown situation. I_D increases uncontrollably if $V_{DS} > V_{DSmax}$, and the JFET is likely destroyed.

Voltage-Controlled Resistor

The region to the left of the pinch-off point is called the **ohmic region.**

The JFET can be used as a variable resistor, where V_{GS} controls the drain-source resistance (r_d).

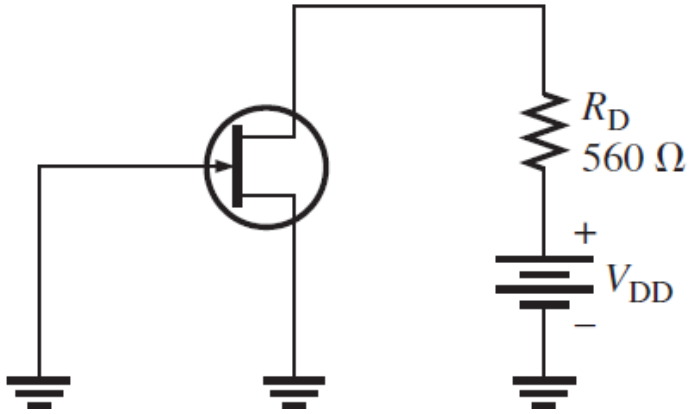
$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$



As V_{GS} becomes more negative, the resistance (r_d) increases.

EXAMPLE:

For the JFET in Figure below, Determine the *minimum* value of V_{DD} required to put the device in the constant-current region of operation when V_{GS} = 0 V. $V_{GS(off)}$ = -4 V and I_{DSS} = 12 mA



EXAMPLE:

For the JFET in Figure below, Determine the *minimum* value of V_{DD} required to put the device in the constant-current region of operation when $V_{GS} = 0$ V.

Solution:

$V_{GS(off)} = -4$ V and $I_{DSS} = 12$ mA

Since $V_{GS(off)} = -4$ V, $V_P = 4$ V. The minimum value of V_{DS} for the JFET to be in its constant-current region is

$V_{DS} = V_P = 4$ V

In the constant-current region with $V_{GS} = 0$ V,

The drop across the drain resistor is

$V_{RD} = I_D R_D = (12 \text{ mA})*560\Omega = 6.72$ V

Apply Kirchhoff's law around the drain circuit.

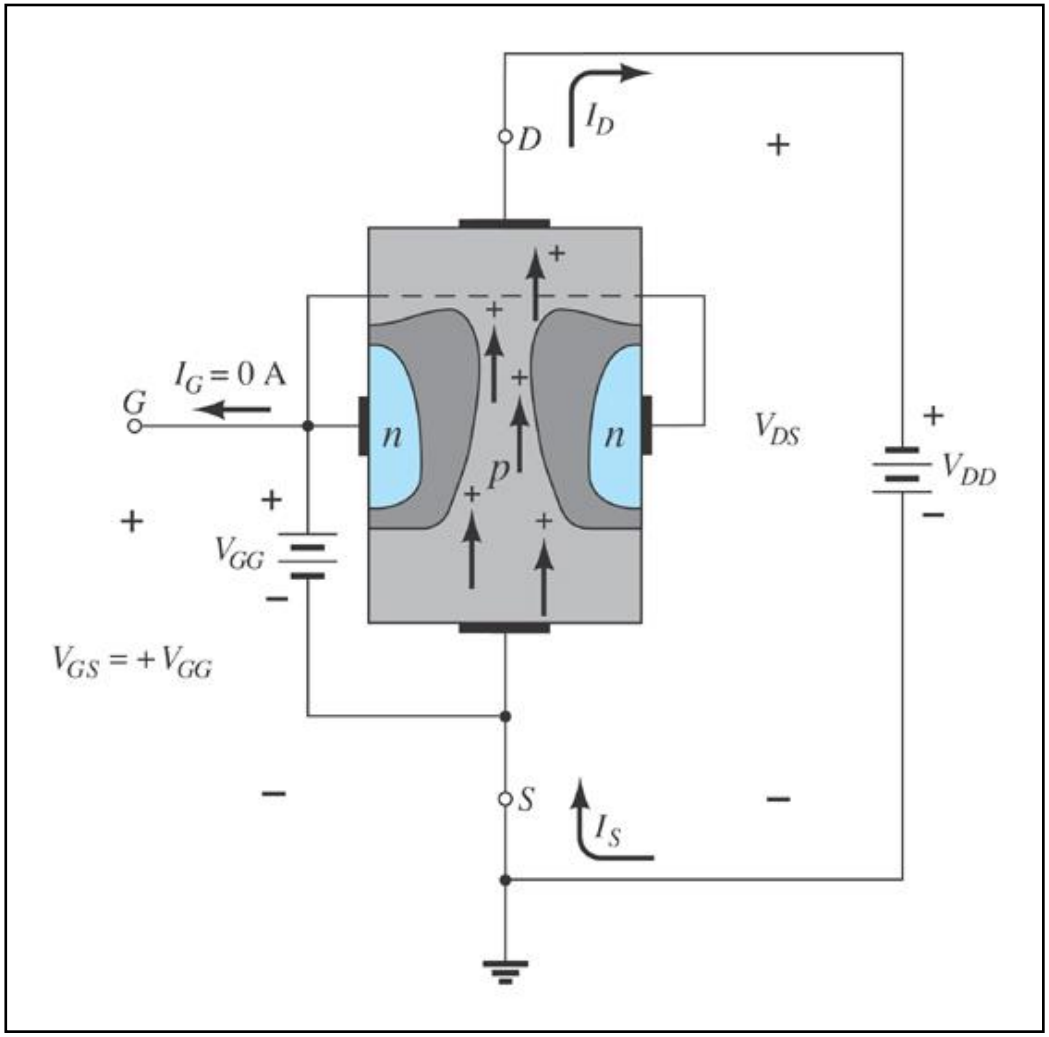
$V_{DD} = V_{DS} + V_{RD} = 4 \text{ V} + 6.72 \text{ V} = \mathbf{10.7 \text{ V}}$

This is the value of V_{DD} to make $V_{DS} = V_P$ and put the device in the constant-current region.

*Related Problem** If V_{DD} is increased to 15 V, what is the drain current?

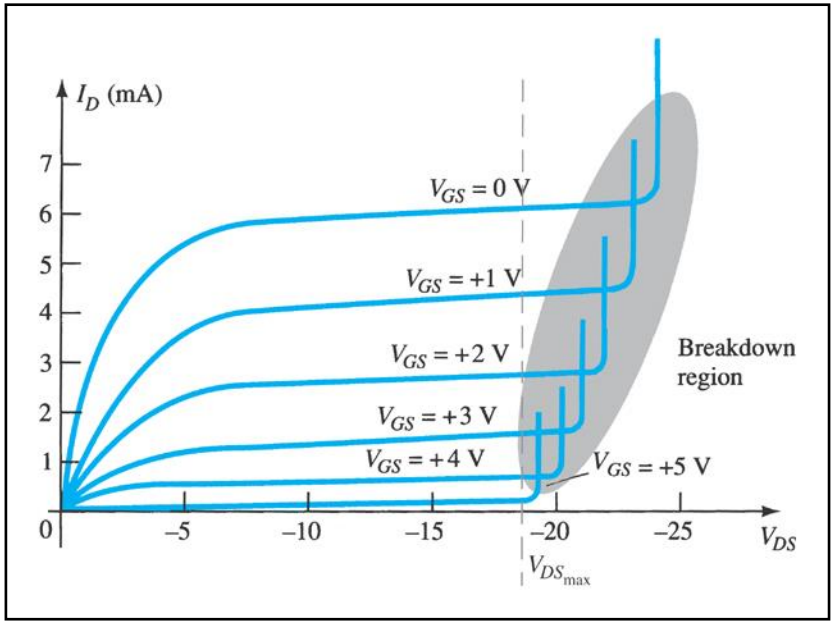
P-Channel JFETs

The *p*-channel JFET behaves the same as the *n*-channel JFET. The only differences are that the voltage polarities and current directions are reversed.



P-Channel JFET Characteristics

As V_{GS} becomes more positive:



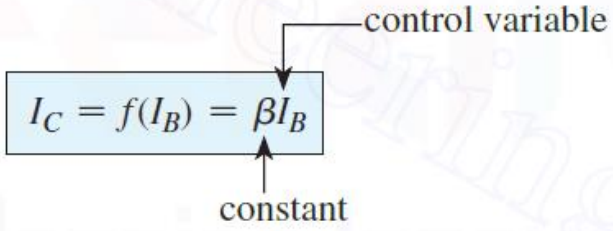
- The JFET experiences pinch-off at a lower voltage (V_P).
- The depletion region increases, and I_D decreases ($I_D < I_{DSS}$)
- I_D eventually drops to 0 A (when $V_{GS} = V_{GSoff}$)

Also note that at high levels of V_{DS} the JFET reaches a breakdown situation: I_D increases uncontrollably if $V_{DS} > V_{DSmax}$.

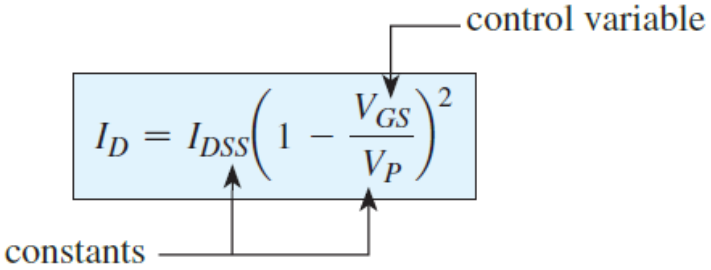
JFET Transfer Characteristics

JFET input-to-output transfer characteristics are not as straightforward as they are for a BJT.

• BJT: β indicates the relationship between I_B (input) and I_C (output).



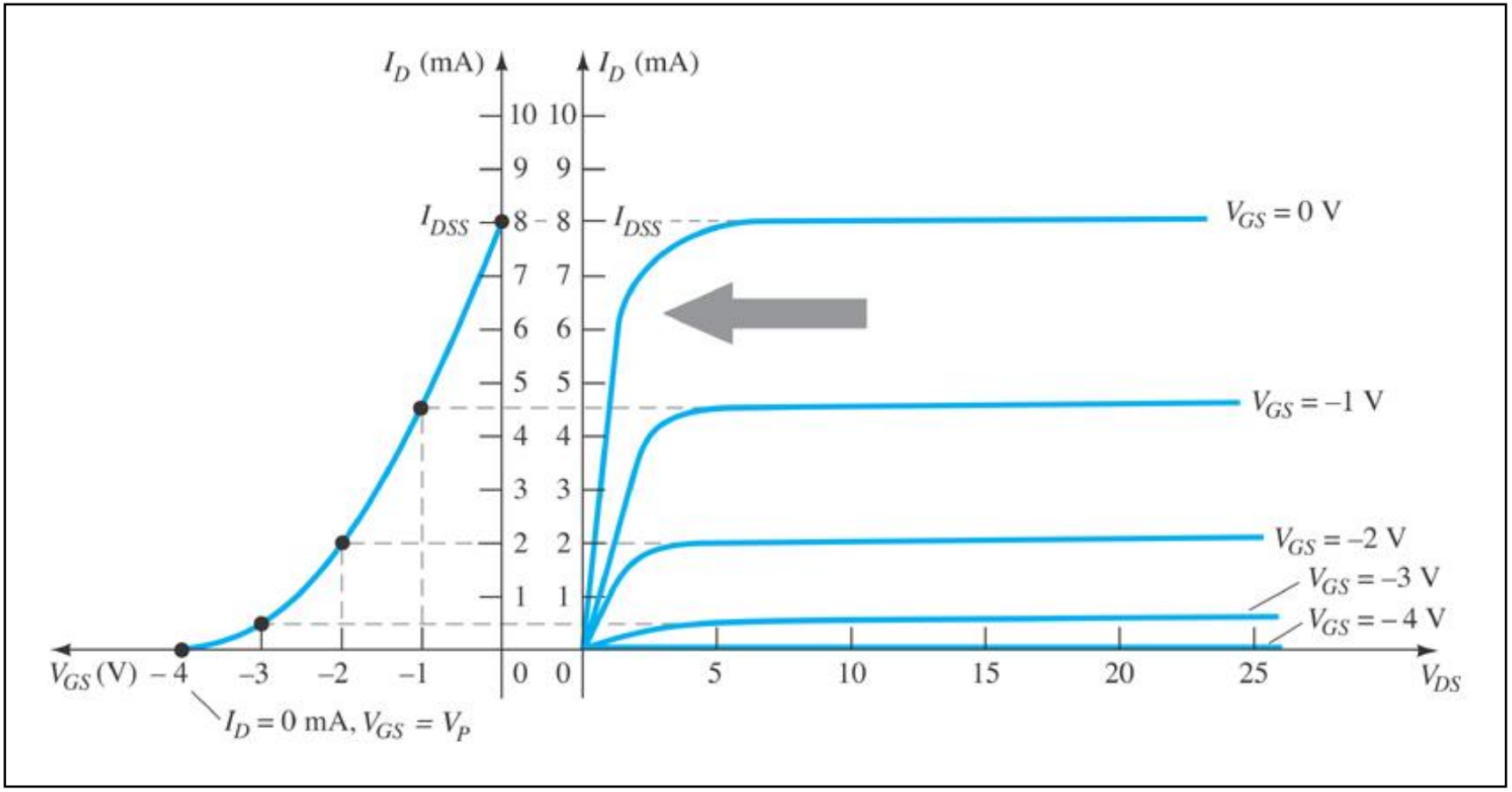
• JFET: The relationship of V_{GS} (input) and I_D (output) is a little more complicated:



•It is called as Shockley's Equation

JFET Transfer Curve

This graph shows the value of I_D for a given value of V_{GS}.



Plotting the JFET Transfer Curve

Using I_{DSS} and V_p ($V_{GS(off)}$) values found in a specification sheet, the transfer curve can be plotted according to these three steps:

1. Solving for $V_{GS} = 0$ V: $I_D = I_{DSS}$

2. Solving for $V_{GS} = V_{GS(off)}$: $I_D = 0$ A

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

3. Solving for $V_{GS} = 0$ V to $V_{GS(off)}$: $0 \text{ A} < I_D < I_{DSS}$

Example:

$I_{DSS} = 9$ mA and $V_{GS(off)} = -8$ V (maximum). Using these values, determine the drain current for $V_{GS} = 0$ V, -1 V, and -4 V.

Solution For $V_{GS} = 0$ V,

$$I_D = I_{DSS} = \mathbf{9\ mA}$$

For $V_{GS} = -1$ V, use Equation 8–1.

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (9\text{ mA})\left(1 - \frac{-1\text{ V}}{-8\text{ V}}\right)^2$$

$$= (9\text{ mA})(1 - 0.125)^2 = (9\text{ mA})(0.766) = \mathbf{6.89\ mA}$$

For $V_{GS} = -4$ V,

$$I_D \cong (9\text{ mA})\left(1 - \frac{-4\text{ V}}{-8\text{ V}}\right)^2 = (9\text{ mA})(1 - 0.5)^2 = (9\text{ mA})(0.25) = \mathbf{2.25\ mA}$$

Related Problem Determine I_D for $V_{GS} = -3$ V for the 2N5459 JFET.

Ninevah University
College of Electronics Engineering
Department of Systems and Control

Electronic I
Lecture 7 part 2

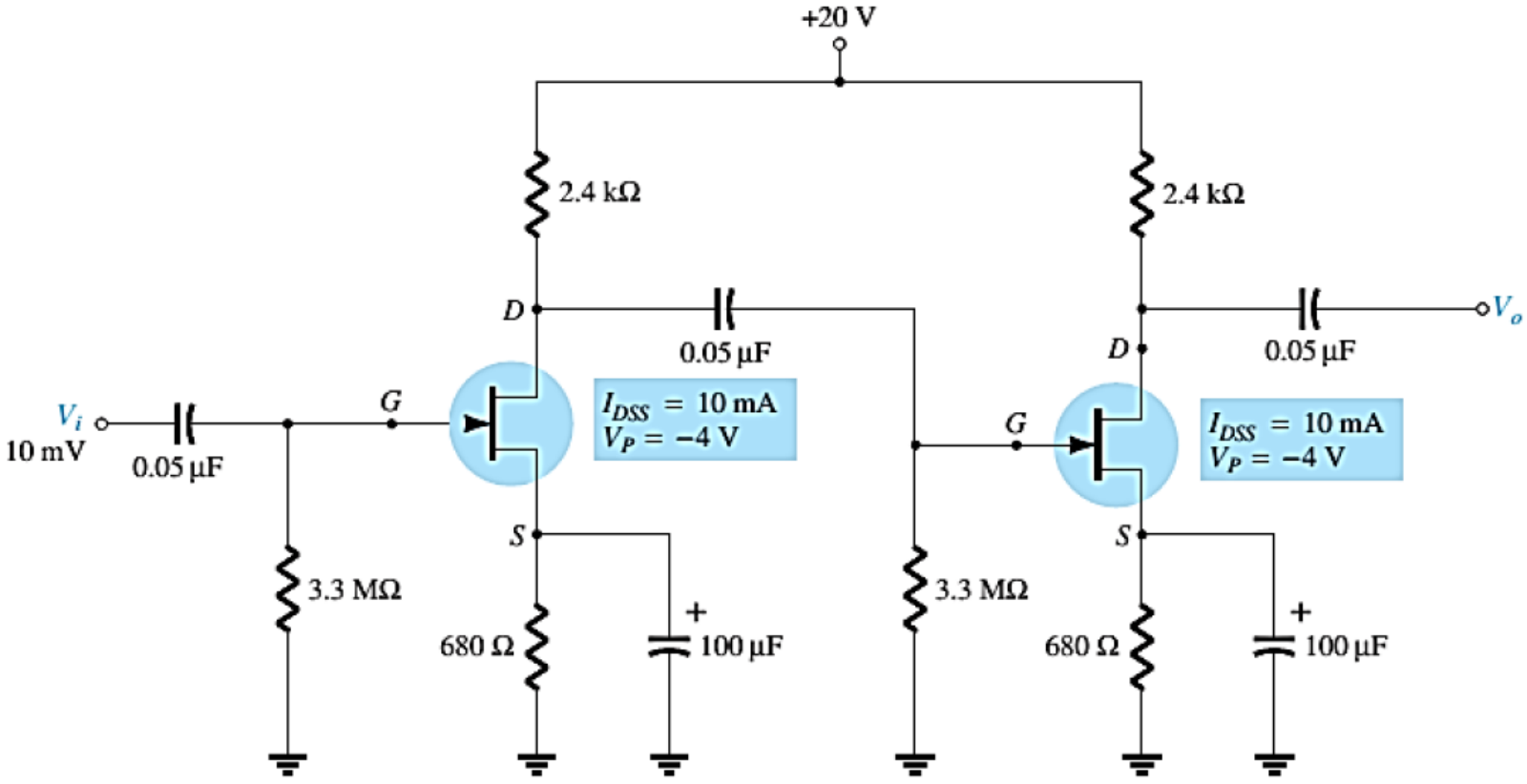
TUTORIAL FET

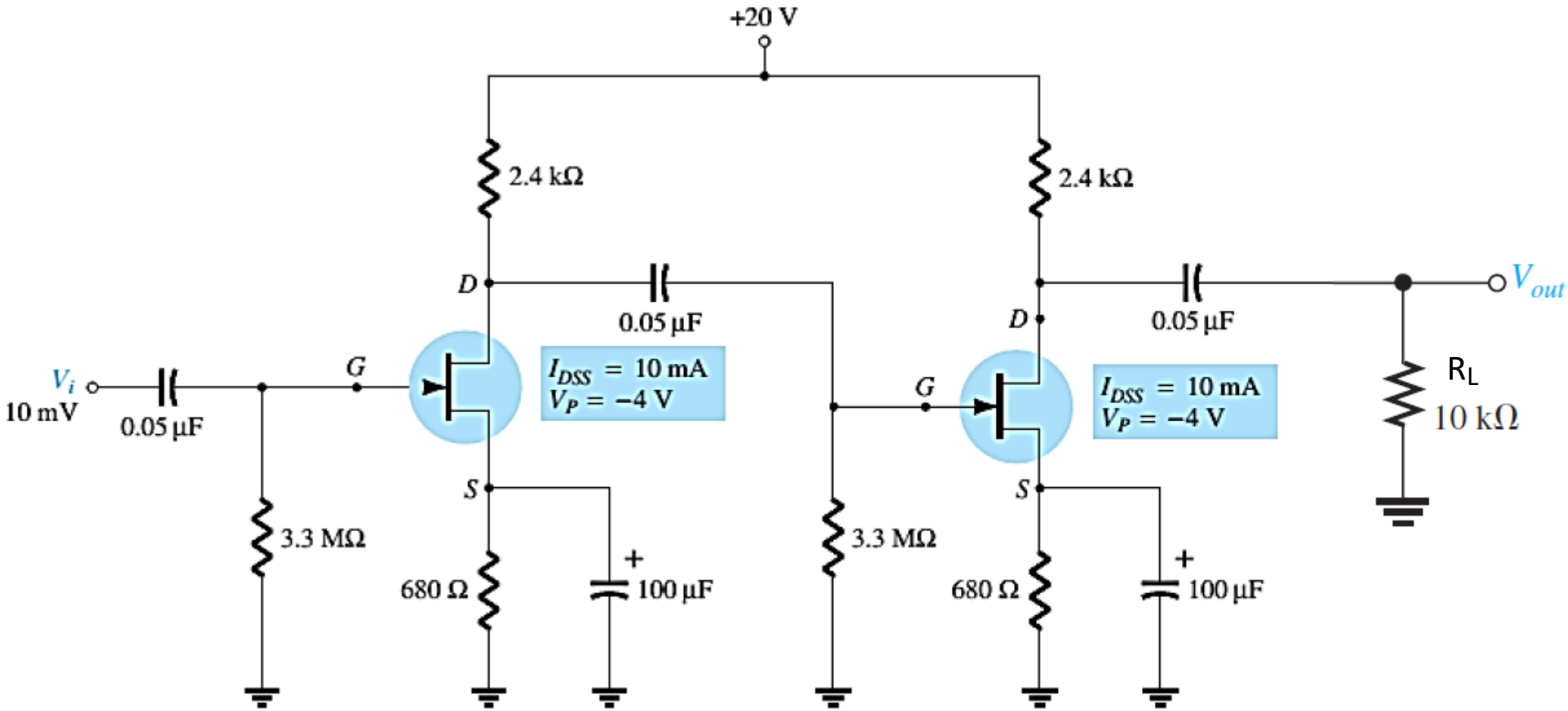
2nd Class

by
Rafal Raed Mahmood Alshaker

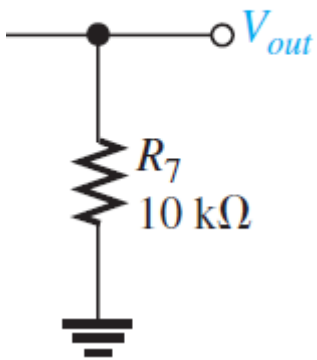
Example 1

For the circuit shown, determine Vo



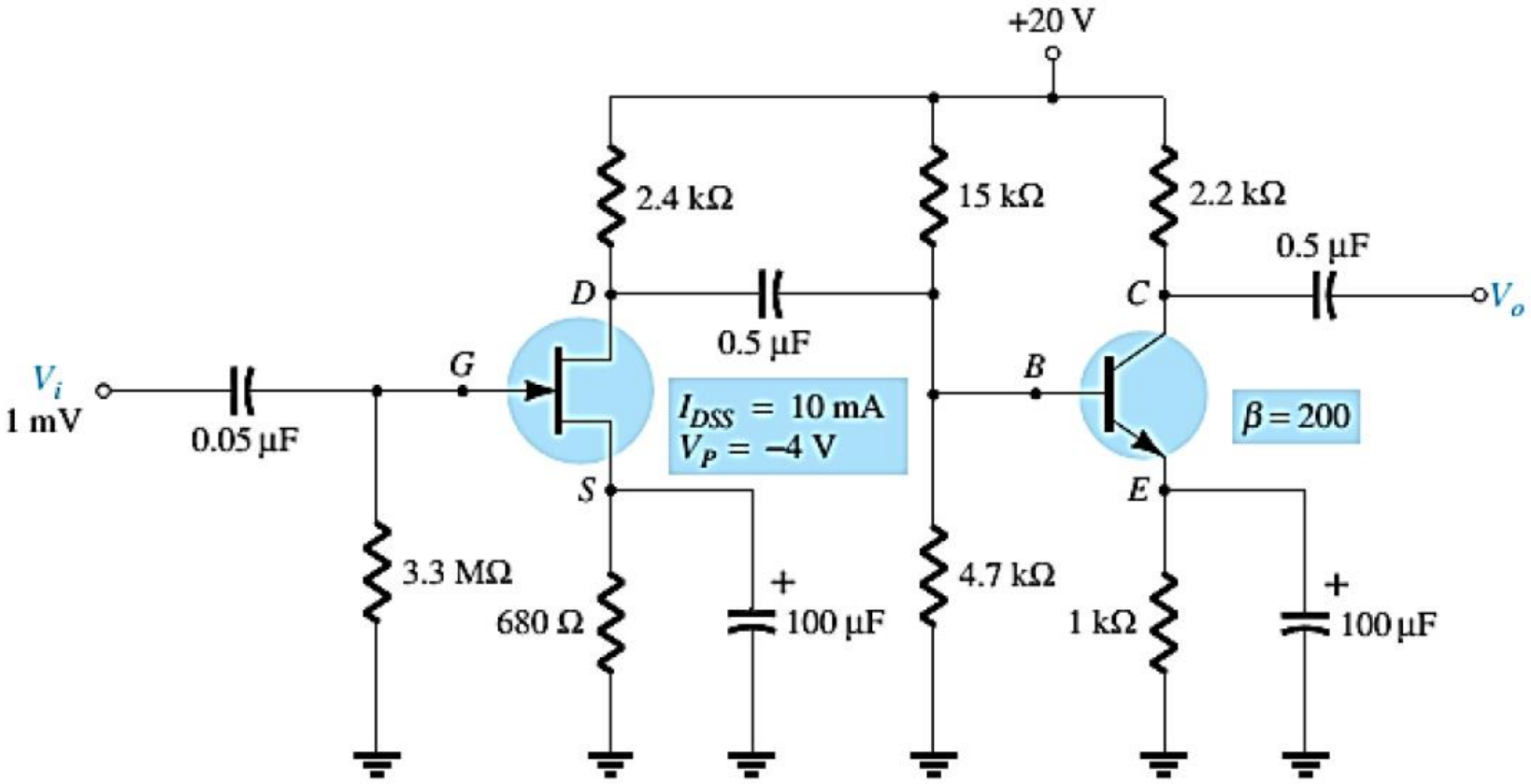

+20 V
2.4 kΩ
2.4 kΩ
D
0.05 µF
D
0.05 µF
V_{out}
V_i
10 mV
0.05 µF
G
I_{DSS} = 10 mA
V_P = −4 V
G
I_{DSS} = 10 mA
V_P = −4 V
R_L
10 kΩ
S
S
3.3 MΩ
3.3 MΩ
680 Ω
680 Ω
+
100 µF
+
100 µF

Solution:



Home Work

for the circuit shown, determine Vo



Solution:

EXAMPLE 8.16 Calculate the dc bias, voltage gain, input impedance, output impedance, and resulting output voltage for the cascade amplifier shown in Fig. 8.48.

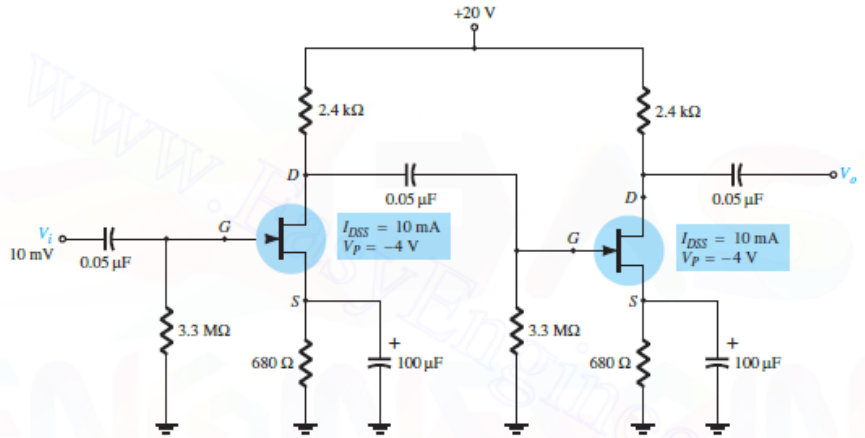


FIG. 8.48
Cascade amplifier circuit for Example 8.16.

Solution: Both amplifier stages have the same dc bias. Using dc bias techniques from Chapter 7 results in

$$V_{GS_Q} = -1.9\text{ V}, \qquad I_{D_Q} = 2.8\text{ mA} \qquad g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{|-4\text{ V}|} = \mathbf{5\text{ mS}}$$

and at the dc bias point,

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = (5\text{ mS})\left(1 - \frac{-1.9\text{ V}}{-4\text{ V}}\right) = \mathbf{2.6\text{ mS}}$$

Since the second stage is unloaded

$$A_{v_2} = -g_m R_D = -(2.6\text{ mS})(2.4\text{ k}\Omega) = \mathbf{-6.24}$$

For the first stage $2.4\text{ k}\Omega \| 3.3\text{ M}\Omega \cong 2.4\text{ k}\Omega$ resulting in the same gain.
The cascade amplifier voltage gain is

$$\text{Eq. (8.66):} \quad A_v = A_{v_1}A_{v_2} = (-6.2)(-6.2) = \mathbf{38.4}$$

Take special note of the fact that the total gain is positive.
The output voltage is then

$$V_o = A_v V_i = (38.4)(10\text{ mV}) = \mathbf{384\text{ mV}}$$

The cascade amplifier input impedance is

$$Z_i = R_G = \mathbf{3.3\text{ M}\Omega}$$

The cascade amplifier output impedance (assuming that $r_d = \infty\Omega$) is

$$Z_o = R_D = \mathbf{2.4\text{ k}\Omega}$$

Ninevah University
College of Electronics Engineering
Department of Systems and Control

Electronic I
Lecture 7

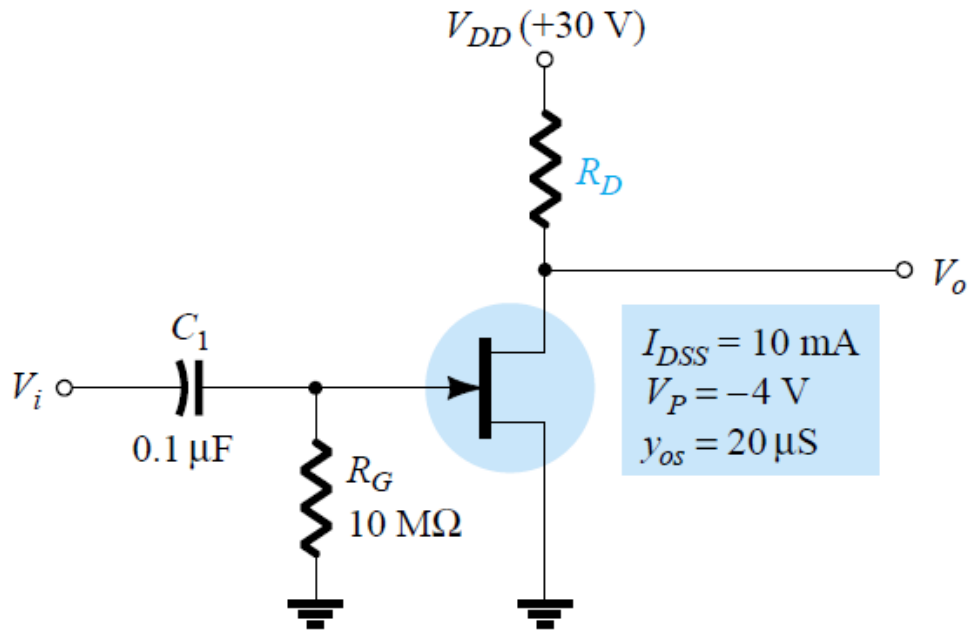
TUTORIAL FET

2nd Class

by
Rafal Raed Mahmood Alshaker

Example 1

Design the fixed-bias network of Figure below to have an ac gain of 10. That is, determine the value of RD.



Solution:

Since V_{GSQ} 0 V, the level of g_m is g_{m0}.

$$A_v = -g_m(R_D \| r_d) = -g_{m0}(R_D \| r_d)$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{4\text{ V}} = 5\text{ mS}$$

$$-10 = -5\text{ mS}(R_D \| r_d)$$

$$R_D \| r_d = \frac{10}{5\text{ mS}} = 2\text{ k}\Omega$$

$$r_d = \frac{1}{y_{os}} = \frac{1}{20 \times 10^{-6}\text{ S}} = 50\text{ k}\Omega$$

$$R_D \| r_d = R_D \| 50\text{ k}\Omega = 2\text{ k}\Omega$$

$$\frac{R_D(50\text{ k}\Omega)}{R_D + 50\text{ k}\Omega} = 2\text{ k}\Omega$$

$$50R_D = 2(R_D + 50\text{ k}\Omega) = 2R_D + 100\text{ k}\Omega$$

$$48R_D = 100\text{ k}\Omega$$

$$R_D = \frac{100\text{ k}\Omega}{48} \cong 2.08\text{ k}\Omega$$

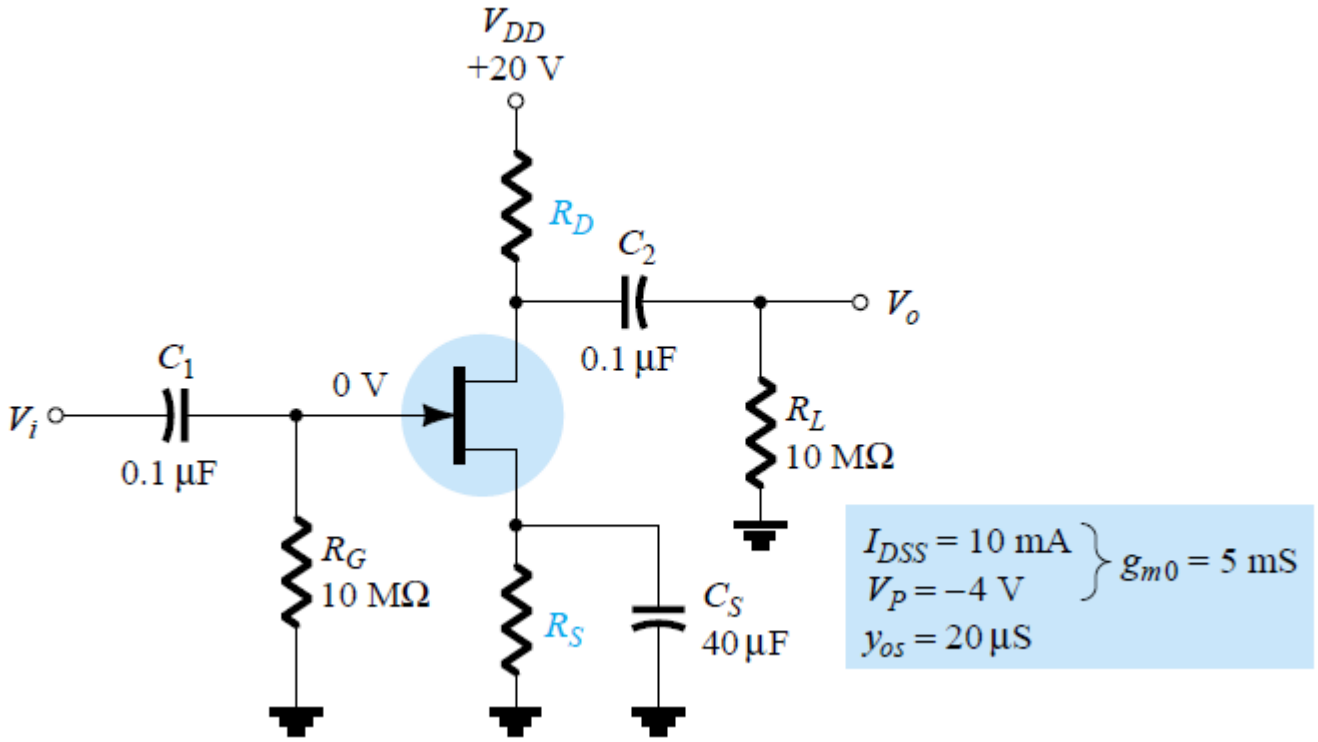
$$V_{DS_Q} = V_{DD} - I_{D_Q}R_D = 30\text{ V} - (10\text{ mA})(2\text{ k}\Omega) = \mathbf{10\text{ V}}$$

$$Z_i = R_G = \mathbf{10\text{ M}\Omega}$$

$$Z_o = R_D \| r_d = 2\text{ k}\Omega \| 50\text{ k}\Omega = \mathbf{1.92\text{ k}\Omega} \cong R_D = 2\text{ k}\Omega.$$

Example 2

Choose the values of R_D and R_S for the network of Figure below that will result in a gain of 8 using a relatively high level of *gm* for this device defined at v_{GSQ} =1/4 V_P.



Solution:

The operating point is defined by

$$V_{GS_Q} = \frac{1}{4}V_P = \frac{1}{4}(-4\text{ V}) = -1\text{ V}$$

and $$I_D = I_{DSS}\left(1 - \frac{V_{GS_Q}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{(-1\text{ V})}{(-4\text{ V})}\right)^2 = 5.625\text{ mA}$$

Determining g_m,

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right)$$

$$= 5\text{ mS}\left(1 - \frac{(-1\text{ V})}{(-4\text{ V})}\right) = 3.75\text{ mS}$$

so that $$R_D\|r_d = \frac{8}{3.75\text{ mS}} = 2.13\text{ k}\Omega$$

The magnitude of the ac voltage gain is determined by

$$|A_v| = g_m(R_D\|r_d)$$

Substituting known values will result in

$$8 = (3.75\text{ mS})(R_D\|r_d)$$

Solution:

The level of R_S is determined by the dc operating conditions as follows:

$$V_{GS_Q} = -I_D R_S$$

$$-1\text{ V} = -(5.625\text{ mA})R_S$$

and

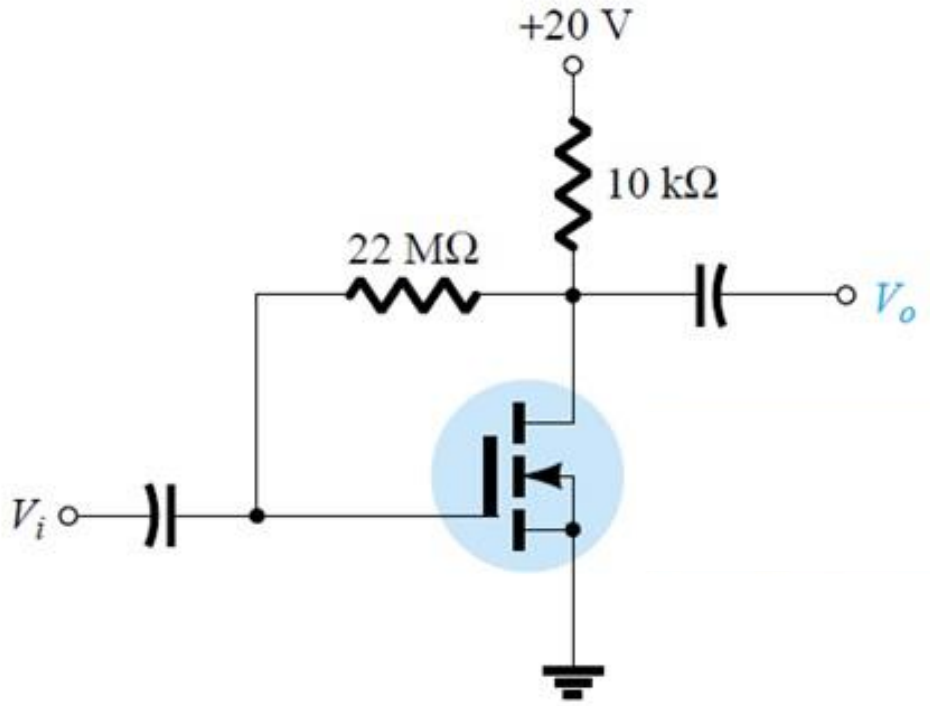
$$R_S = \frac{1\text{ V}}{5.625\text{ mA}} = 177.8\ \Omega$$

The closest standard value is 180 Ω. In this example, R_S does not appear in the ac design because of the shorting effect of C_S.

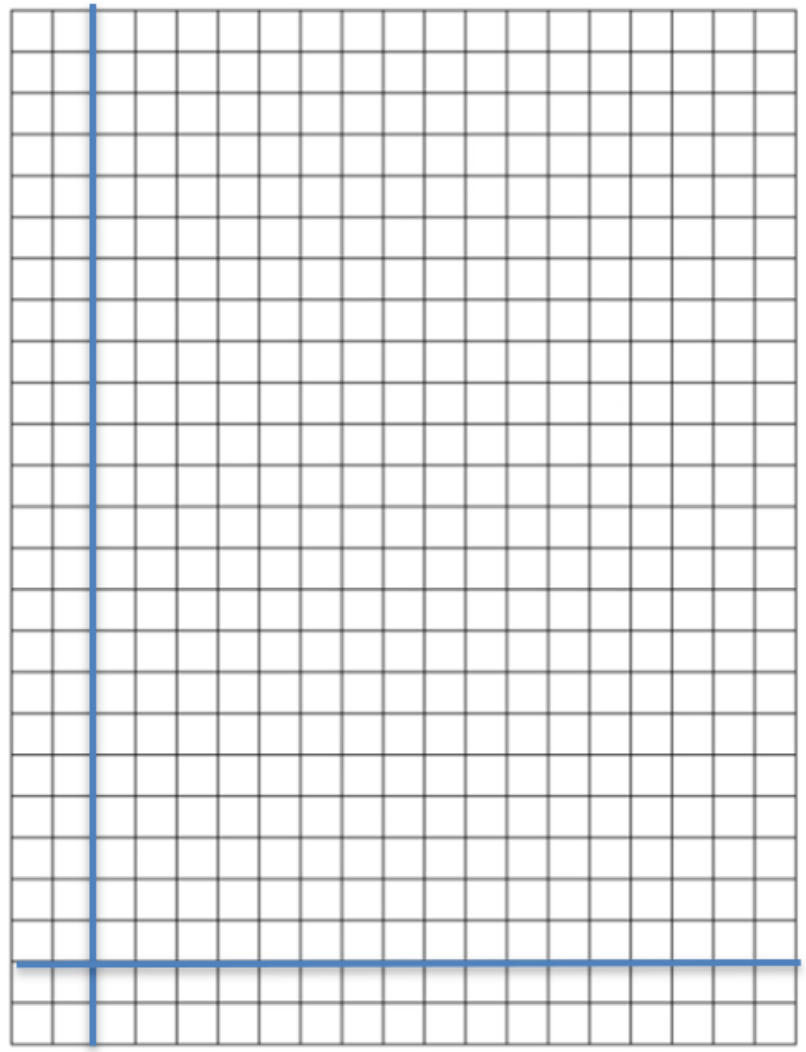
Home Work Determine R_D and R_S for the network of the previous example to establish a gain of 8 if the bypass capacitor C_S is removed.

Example 3

Determine V_o for the network of Fig. below if V_i = 4 mV, $V_{GS(Th)}$ =4 V, and $I_{D(on)}$ =4 mA, with $V_{GS(on)}$ =7 V and y_{os} =20 µS.



Solution:



Solution:

.

$$I_D = k(V_{GS} - V_T)^2$$

$$\therefore k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_T)^2} = \frac{4\ \text{mA}}{(7\ \text{V} - 4\ \text{V})^2} = 0.444 \times 10^{-3}$$

$$g_m = 2k(V_{GS_Q} - V_{GS(Th)}) = 2(0.444 \times 10^{-3})(7\ \text{V} - 4\ \text{V})$$

$$= 2.66\ \text{mS}$$

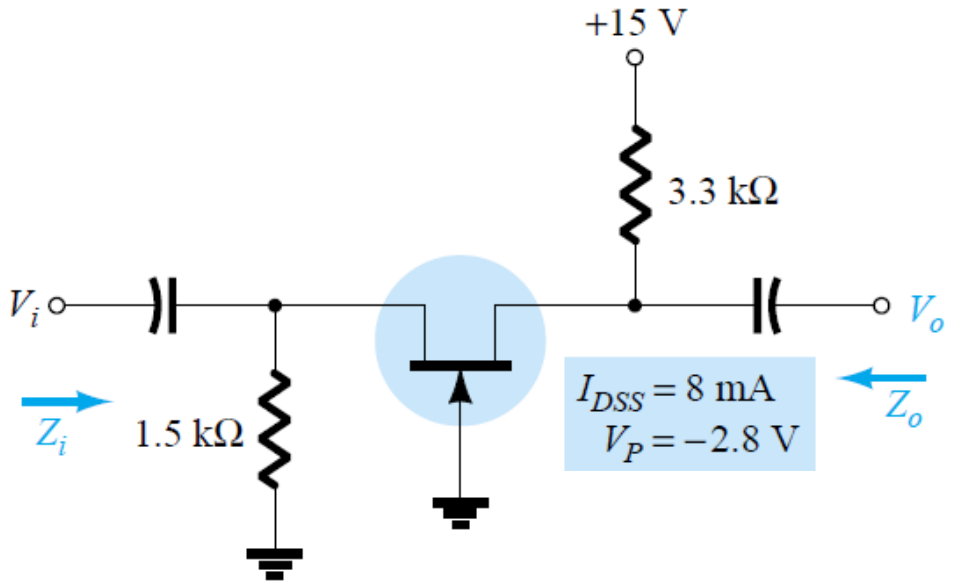
$$A_v = -g_m(R_F \parallel r_d \parallel R_D) = -(2.66\ \text{mS})(22\ \text{M}\Omega \parallel \underbrace{50\ \text{k}\Omega \parallel 10\ \text{k}\Omega}_{8.33\ \text{k}\Omega}) = -22.16$$

$$\cong 8.33\ \text{k}\Omega$$

$$V_o = A_v V_i = (-22.16)(4\ \text{mV}) = \mathbf{-88.64\ mV}$$

Example 4

Determine Z_i, Z_o, and V_o for the network of Fig. below, if $V_i = 0.1$ mV and $r_d = 50$ kΩ.



Solution:

$$V_{GS_Q} = -1.75\ \text{V}, g_m = \frac{2I_{DSS}}{V_P}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = \frac{2(8\ \text{mA})}{2.8\ \text{V}}\left(1 - \frac{-1.75\ \text{V}}{-2.8\ \text{V}}\right) = 2.14\ \text{mS}$$

$$Z_i = R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d}\right] = 1.5\ \text{k}\Omega \left\| \left[\frac{25\ \text{k}\Omega + 3.3\ \text{k}\Omega}{1 + (2.14\ \text{mS})(25\ \text{k}\Omega)}\right] = 1.5\ \text{k}\Omega \right\| \frac{28.3\ \text{k}\Omega}{54.5}$$

$$= 1.5\ \text{k}\Omega \| 0.52\ \text{k}\Omega = \mathbf{386.1\ \Omega}$$

$$Z_o = R_D \| r_d = 3.3\ \text{k}\Omega \| 25\ \text{k}\Omega = \mathbf{2.92\ \text{k}\Omega}$$

$$A_v = \frac{g_m R_D + R_D / r_d}{1 + R_D / r_d} = \frac{(2.14\ \text{mS})(3.3\ \text{k}\Omega) + 3.3\ \text{k}\Omega / 25\ \text{k}\Omega}{1 + 3.3\ \text{k}\Omega / 25\ \text{k}\Omega}$$

$$= \frac{7.062 + 0.132}{1 + 0.132} = \frac{7.194}{1.132} = 6.36$$

$$V_o = A_v V_i = (6.36)(0.1\ \text{mV}) = \mathbf{0.636\ \text{mV}}$$

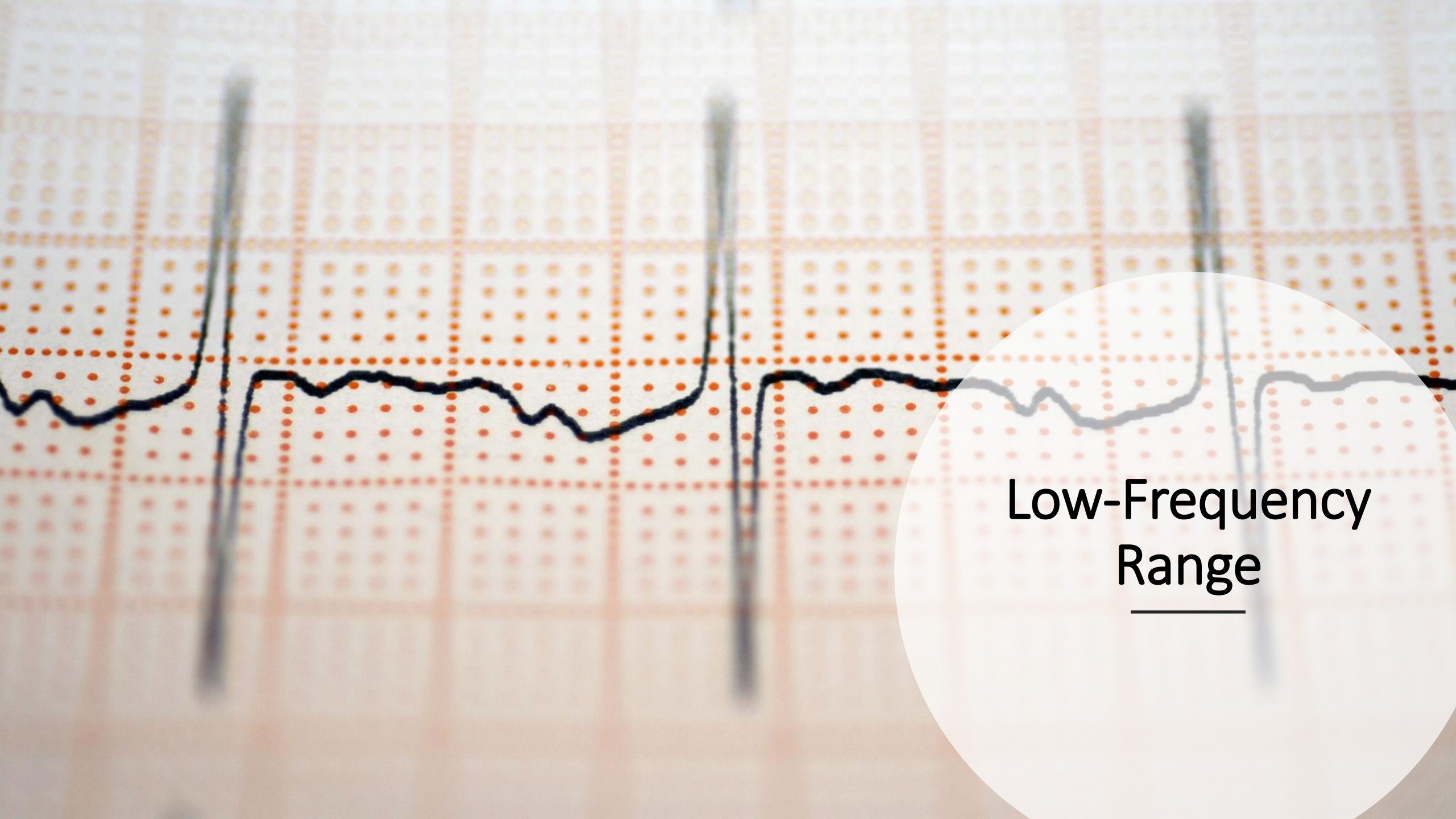
Ninevah University
College of Electronics Engineering
Department of Systems and Control

Electronic I
Lecture 8

Frequency Response of FET

2nd Class

by
Rafal Raed Mahmood Alshaker



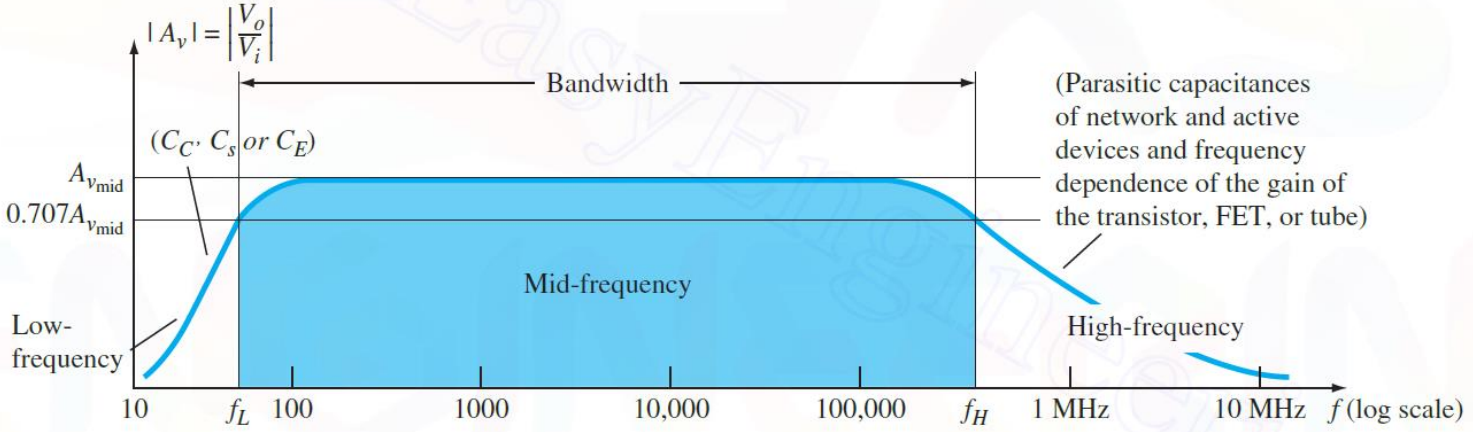
Low-Frequency Range

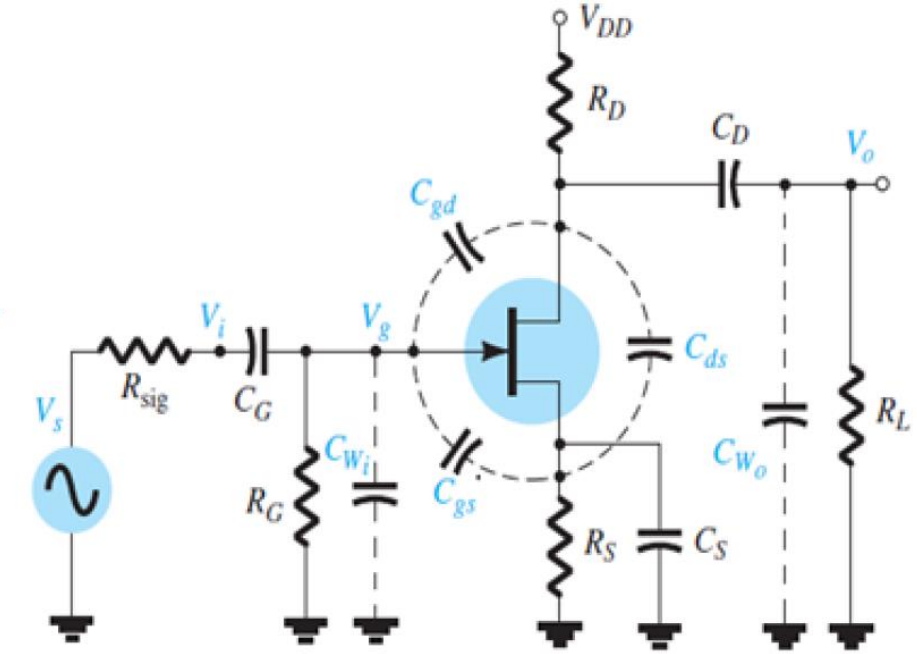
General Frequency Considerations

The **frequency response** of an amplifier refers to the frequency range in which the amplifier will operate with negligible effects from capacitors and device internal capacitance. This range of frequencies can be called the **mid-range**.

- At frequencies above and below the midrange, capacitance and any inductance will affect the gain of the amplifier.
- At low frequencies the coupling and bypass capacitors lower the gain.
- At high frequencies stray capacitances associated with the active device lower the gain.
- Also, cascading amplifiers limits the gain at high and low frequencies.

Typical Frequency Response





Typical Frequency Response

$$P_{o_{\text{mid}}} = \frac{|V_o^2|}{R_o} = \frac{|A_{v_{\text{mid}}} V_i|^2}{R_o}$$

and at the half-power frequencies,

$$P_{o_{HPF}} = \frac{|0.707\, A_{v_{\text{mid}}} V_i|^2}{R_o} = 0.5\, \frac{|A_{v_{\text{mid}}} V_i|^2}{R_o}$$

$$\boxed{P_{o_{HPF}} = 0.5\, P_{o_{\text{mid}}}}$$

The multiplier 0.707 was chosen because at this level the output power is half the midband power output, that is, at midfrequencies

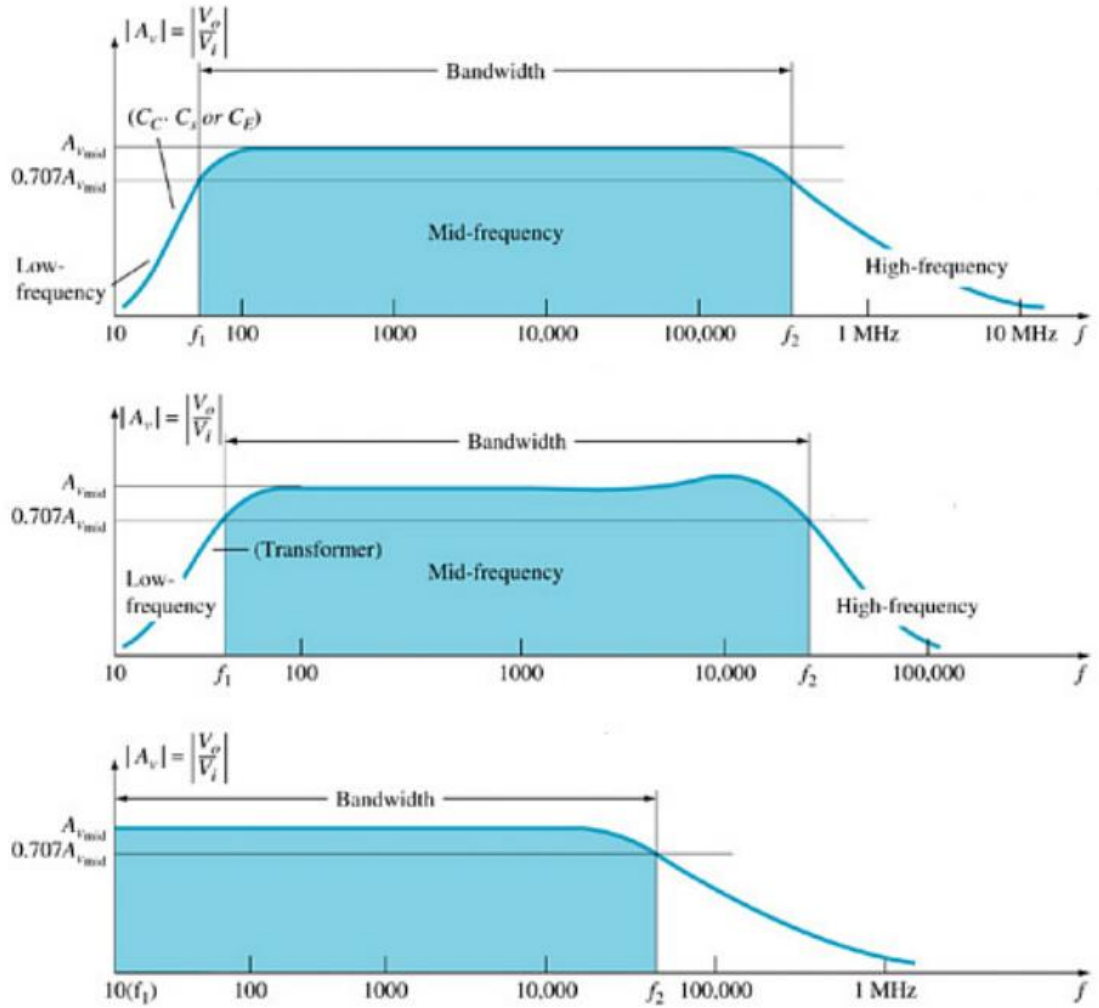
$$\boxed{\text{bandwidth (BW)} = f_H - f_L}$$

Cutoff Frequencies

The mid-range frequency range of an amplifier is called the bandwidth of the amplifier.

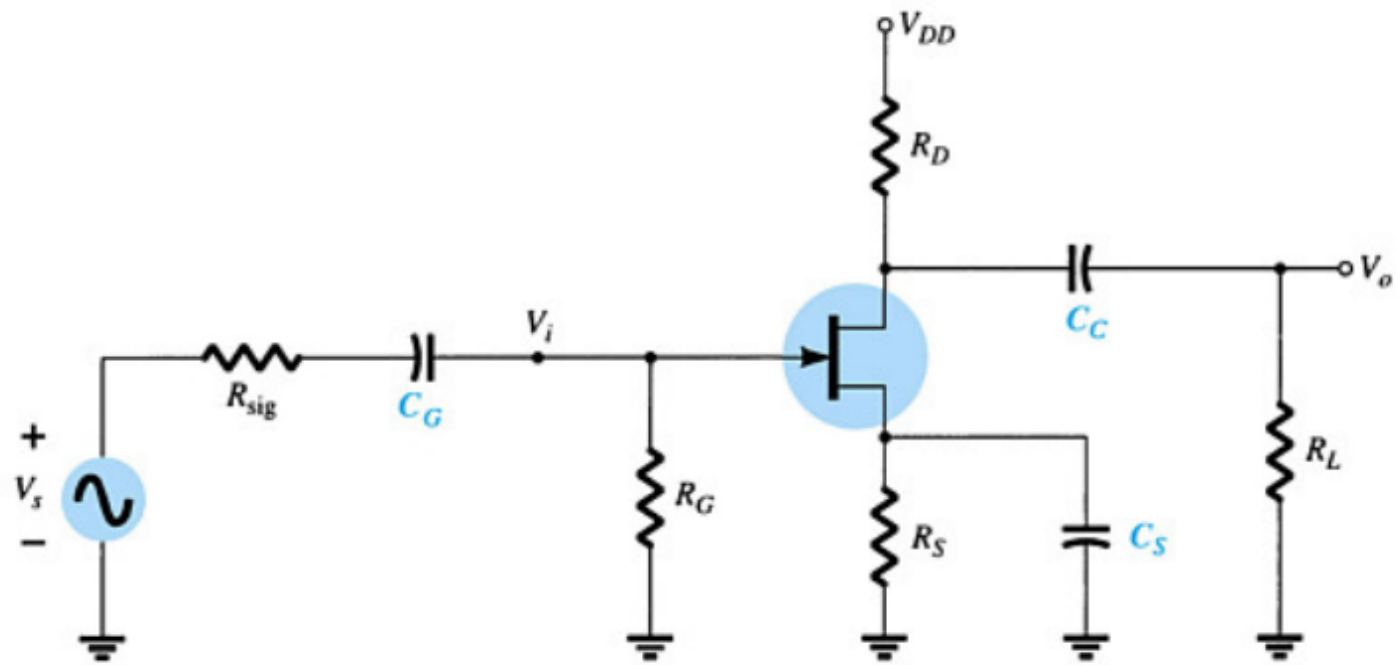
The bandwidth is defined by the lower and upper cutoff frequencies.

Cutoff – any frequency at which the gain has dropped by 3 dB.



FET Amplifier Low-Frequency Response

At low frequencies, coupling capacitor (C_G, C_C) and bypass capacitor (C_S) reactances affect the circuit impedances.



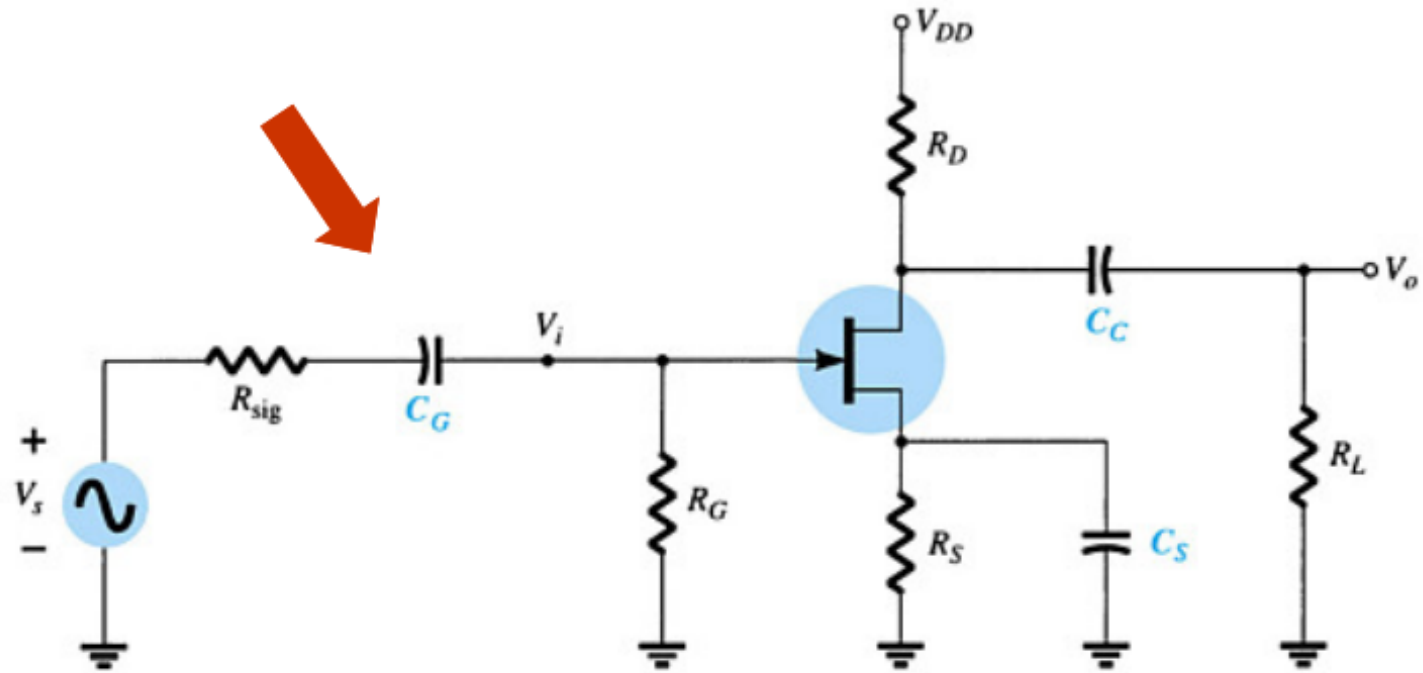
Coupling Capacitor (C_G)

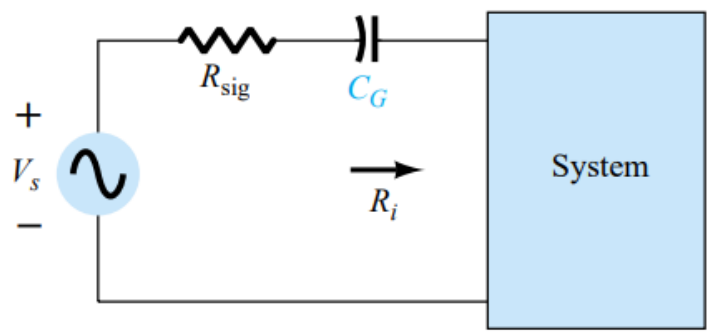
The cutoff frequency due to C_G can be calculated with

$$f_{LC} = \frac{1}{2\pi(R_{sig} + R_i)C_G}$$

where

$$R_i = R_G$$





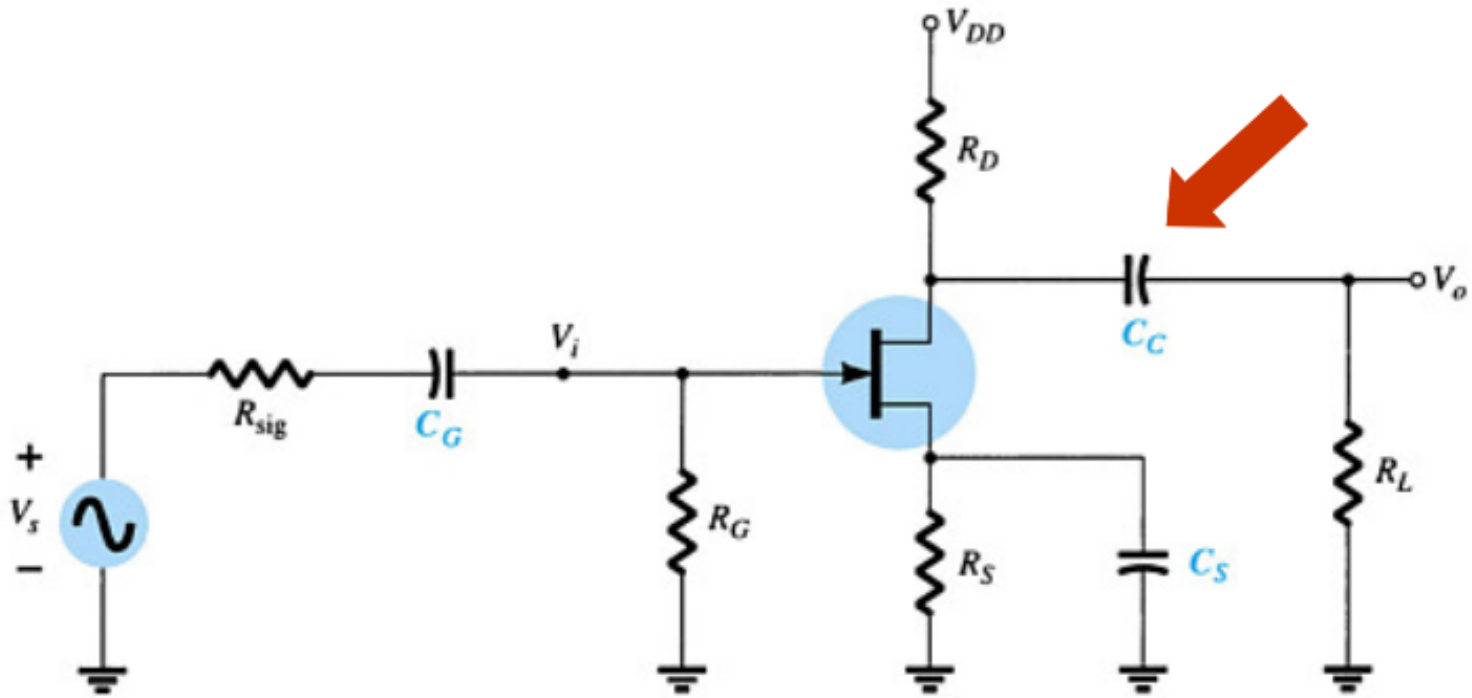
Coupling Capacitor (C_C)

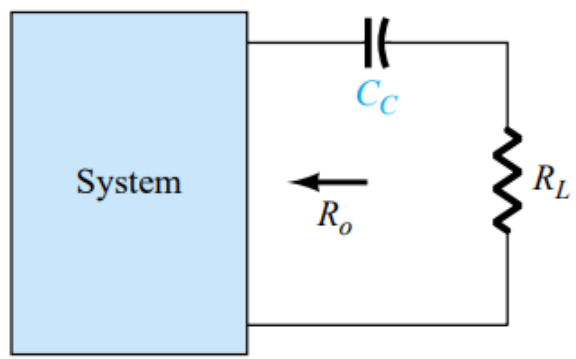
The cutoff frequency due to C_C can be calculated with

$$f_{LC} = \frac{1}{2\pi(R_o+R_L)C_C}$$

where

$$R_o = R_D \parallel r_d$$





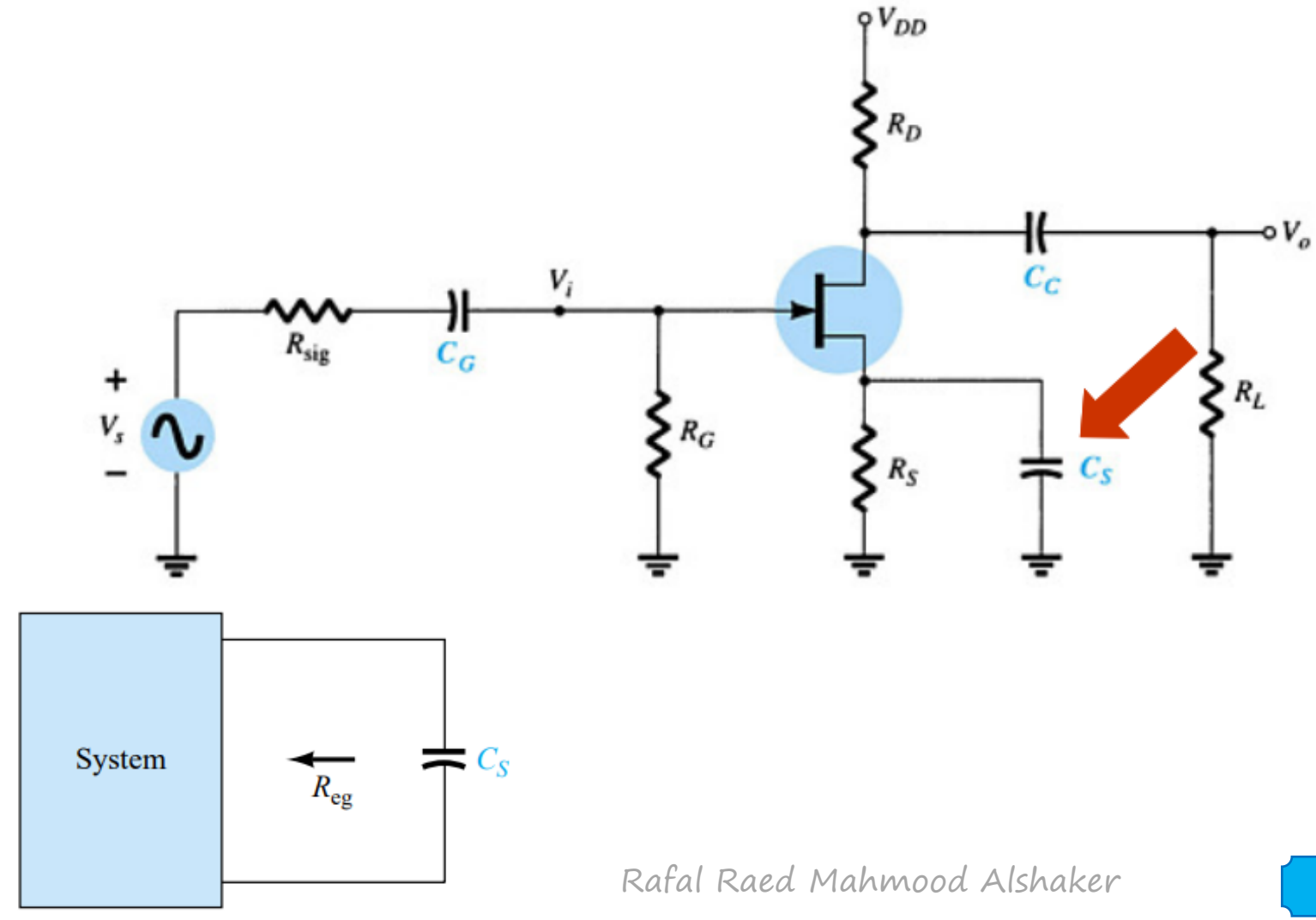
Bypass Capacitor (C_S)

The cutoff frequency due to C_S can be calculated with

$$f_{LS} = \frac{1}{2\pi R_{eq} C_S}$$

where

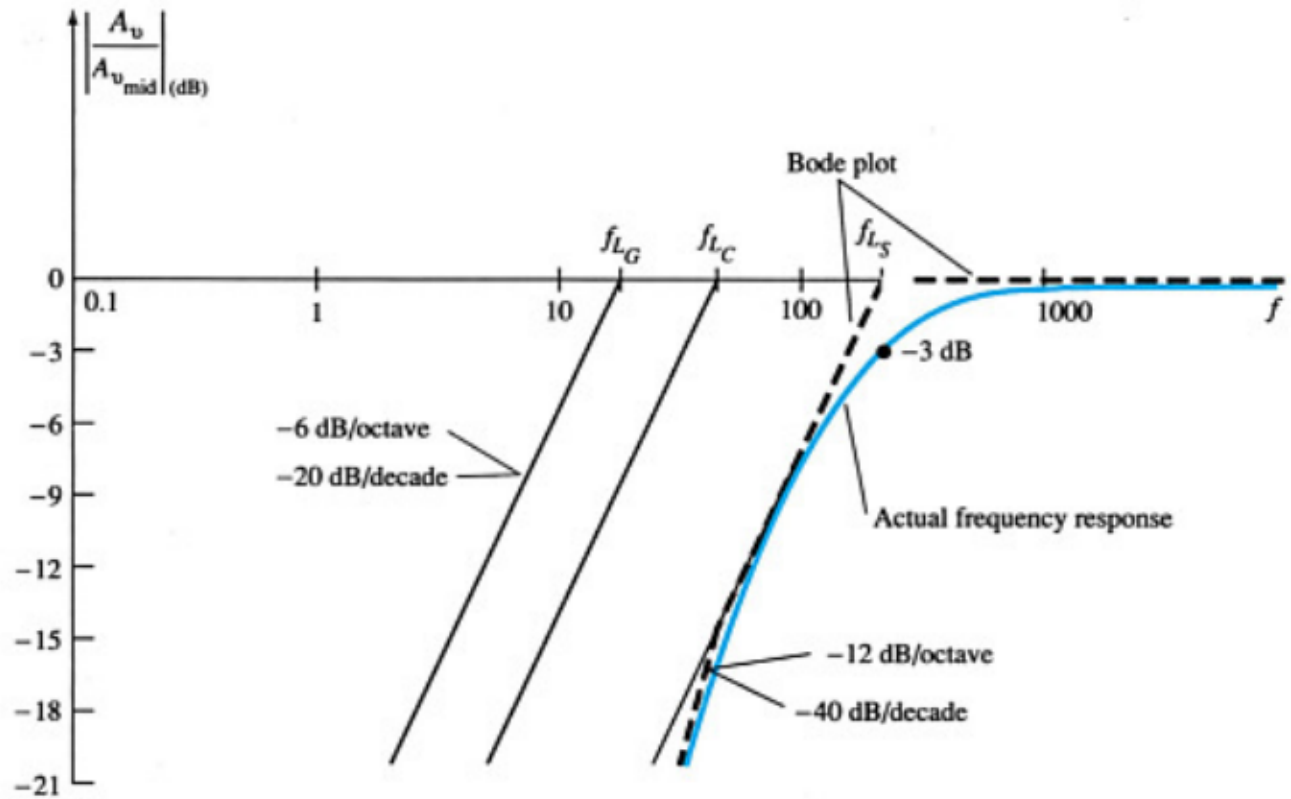
$$R_{eq} = R_S \parallel \frac{1}{g_m}\Big|_{r_d \cong \infty\Omega}$$



FET Amplifier Low-Frequency Response

The Bode plot indicates that each capacitor may have a different cutoff frequency.

The capacitor that has the *highest* lower cutoff frequency (f_L) is closest to the actual cutoff frequency of the amplifier.



FET Low Frequency Example

-For the circuit in slide 8, if the circuit parameters are given as

$C_G = 0.01\ \mu\text{F}, \quad C_C = 0.5\ \mu\text{F}, \quad C_S = 2\ \mu\text{F}$

$R_{\text{sig}} = 10\ \text{k}\Omega, \quad R_G = 1\ \text{M}\Omega, \quad R_D = 4.7\ \text{k}\Omega, \quad R_S = 1\ \text{k}\Omega, \quad R_L = 2.2\ \text{k}\Omega$

$I_{DSS} = 8\text{mA}, \quad V_P = -4\ \text{V} \quad r_d = \infty\ \Omega, \quad \text{V}_{\text{DD}} = 20\ \text{V}$

a) Find the low cutoff frequency.

$$f_{L_G} = 15.8\ Hz$$
$$f_{L_C} = 46.13\ Hz$$
$$f_{L_S} = 238.73\ Hz$$

The low cutoff frequency is max(f_{L_G}, f_{L_C}, f_{L_S})=238.73 Hz

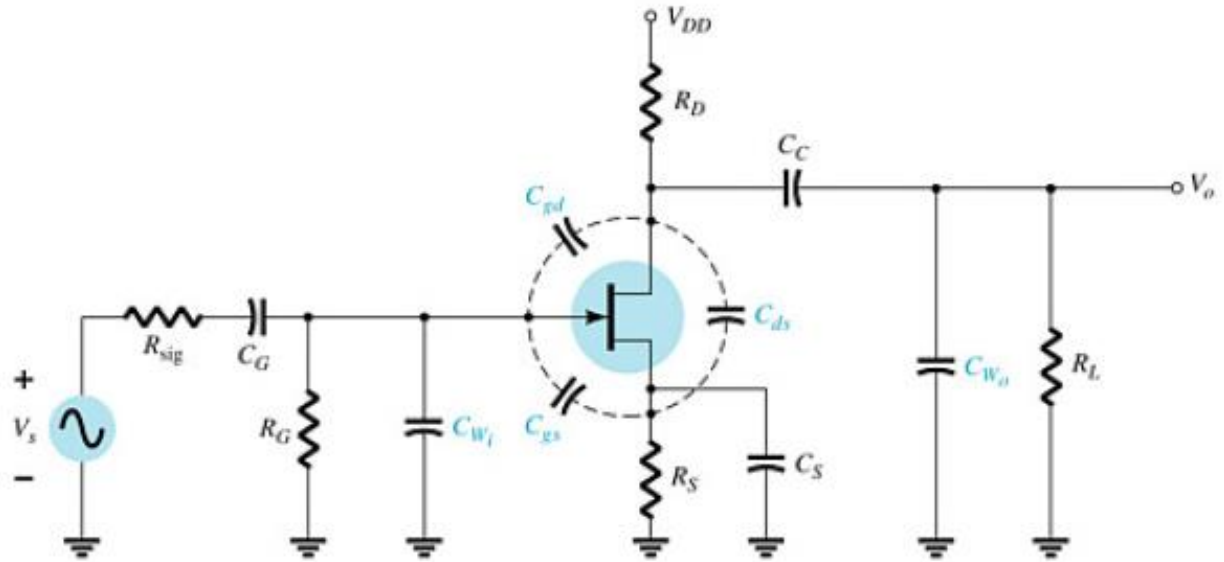
Example 1

Determine the lower cutoff frequency for the network of Fig. using the following parameters:

$C_G = 0.01\ \mu\text{F}, \quad C_C = 0.5\ \mu\text{F}, \quad C_S = 2\ \mu\text{F}$

$R_{\text{sig}} = 10\ \text{k}\Omega, \quad R_G = 1\ \text{M}\Omega, \quad R_D = 4.7\ \text{k}\Omega, \quad R_S = 1\ \text{k}\Omega, \quad R_L = 2.2\ \text{k}\Omega$

$I_{DSS} = 8\text{mA}, \quad V_P = -4\ \text{V} \quad r_d = \infty\ \Omega, \quad \text{V}_{\text{DD}} = 20\ \text{V}$



Solution:

a. DC analysis: Plotting the transfer curve of $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$ and superimposing the curve defined by $V_{GS} = -I_D R_S$ results in an intersection at $V_{GS_Q} = -2\text{ V}$ and $I_{D_Q} = 2\text{ mA}$. In addition,

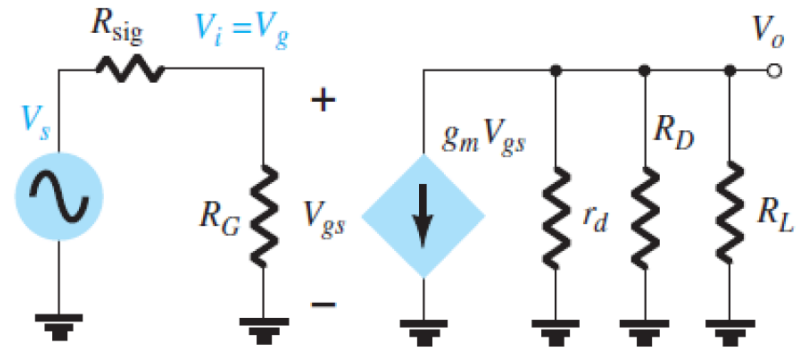
$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8\text{ mA})}{4\text{ V}} = 4\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 4\text{ mS}\left(1 - \frac{-2\text{ V}}{-4\text{ V}}\right) = 2\text{ mS}$$

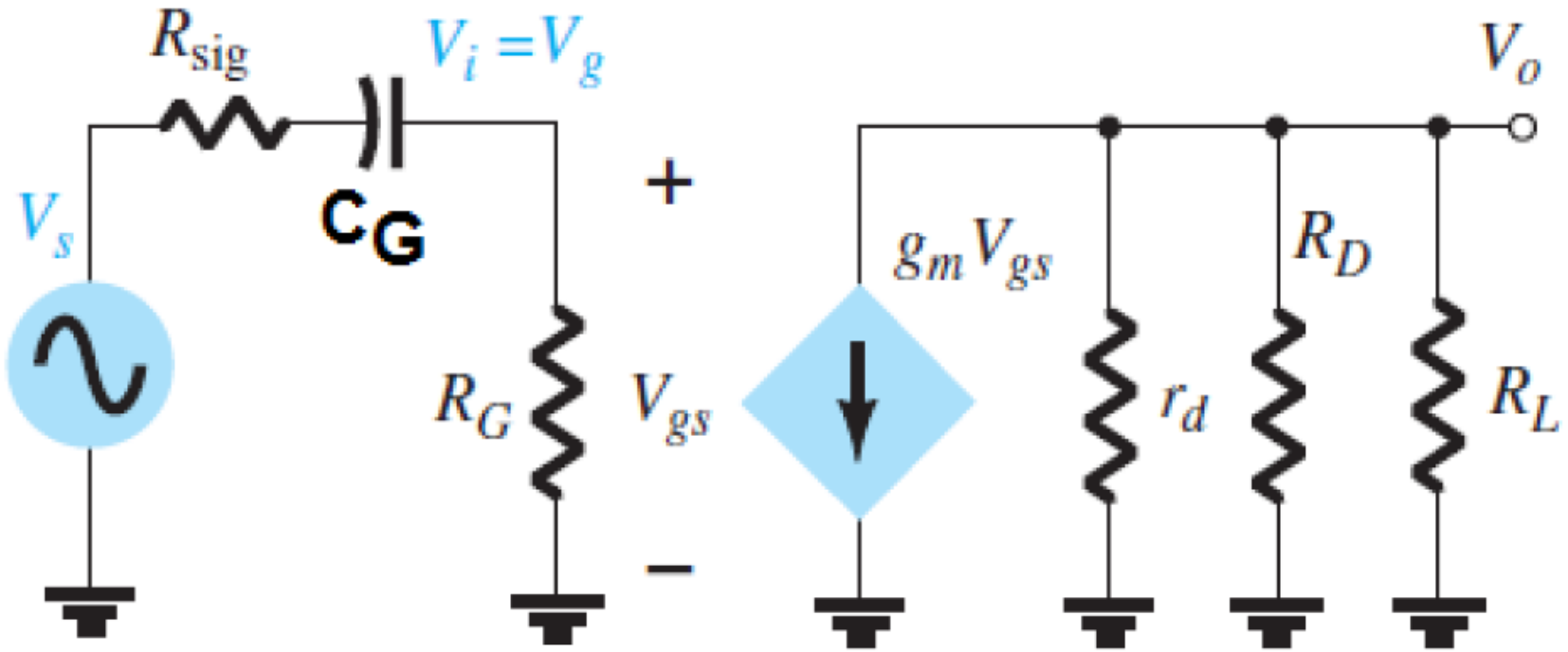
$$A_{v_{\text{mid}}} = \frac{V_o}{V_i} = -g_m(R_D \| R_L) = -(2\text{ mS})(4.7\text{ k}\Omega \| 2.2\text{ k}\Omega)$$

$$= -(2\text{ mS})(1.499\text{ k}\Omega)$$

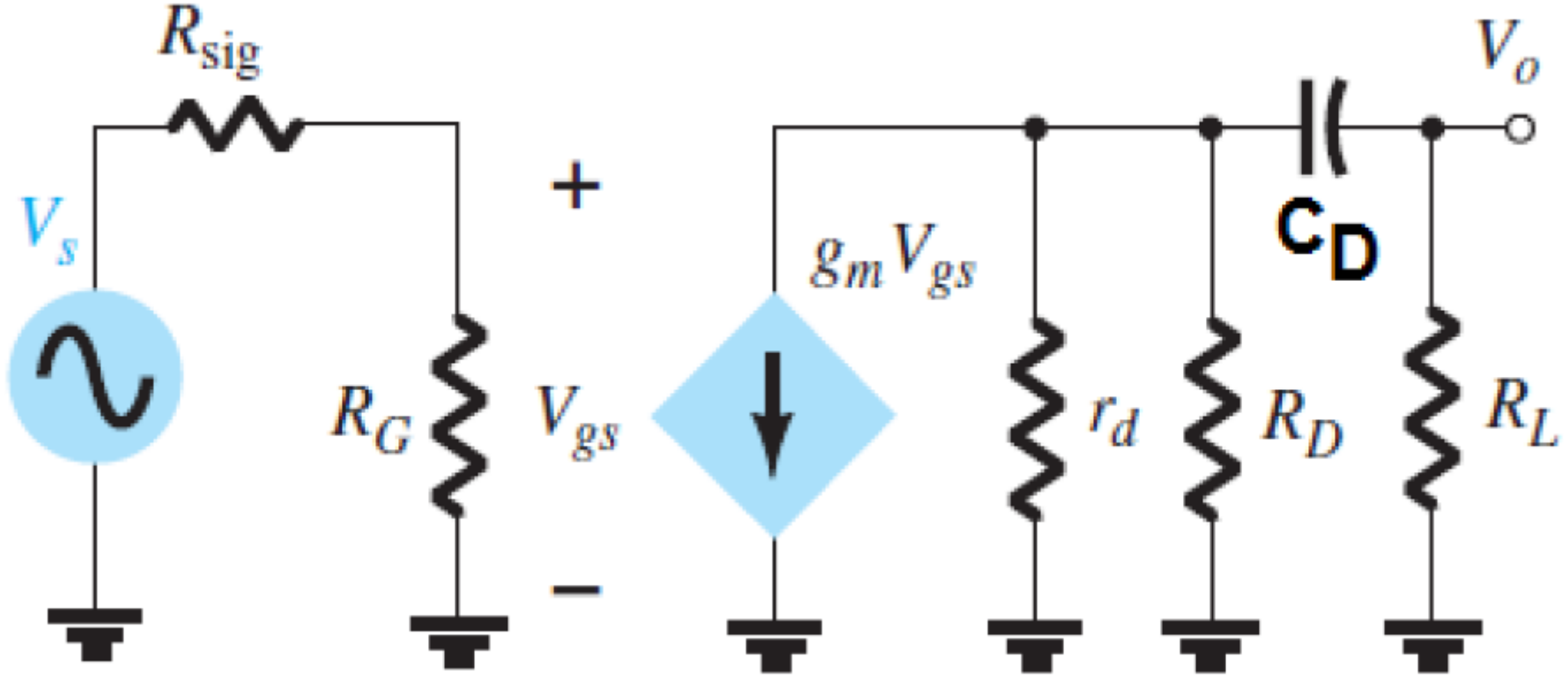
$$\cong \mathbf{-3}$$



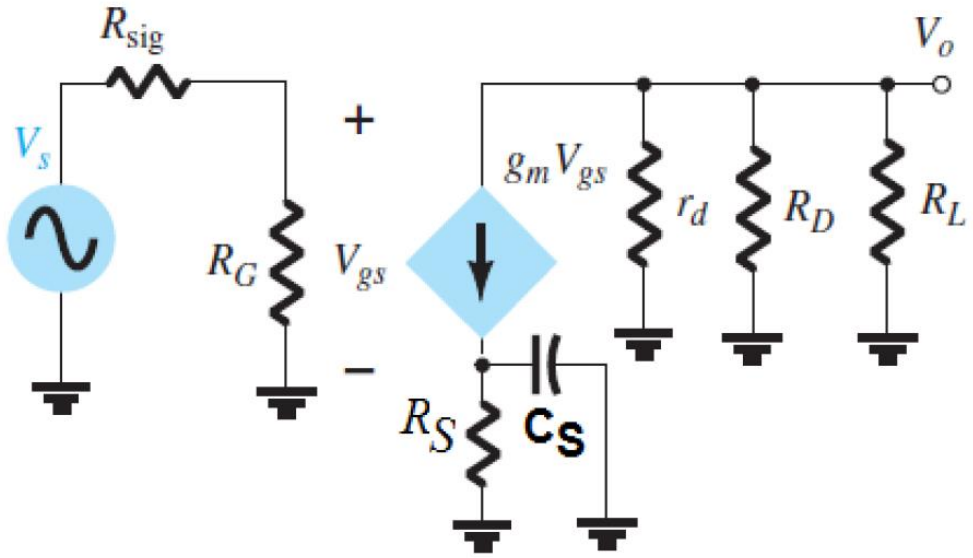
$$f_{L_G} = \frac{1}{2\pi(R_{\text{sig}} + R_i)C_G} = \frac{1}{2\pi(10\,\text{k}\Omega + 1\,\text{M}\Omega)(0.01\,\mu\text{F})} \cong \mathbf{15.8\ Hz}$$



$$f_{L_C} = \frac{1}{2\pi(R_o + R_L)C_C} = \frac{1}{2\pi(4.7\,\text{k}\Omega + 2.2\,\text{k}\Omega)(0.5\,\mu\text{F})} \cong \mathbf{46.13\ Hz}$$



C_S $R_{eq} = R_S \| \dfrac{1}{g_m} = 1\,\text{k}\Omega \| \dfrac{1}{2\,\text{mS}} = 1\,\text{k}\Omega \| 0.5\,\text{k}\Omega = 333.33\,\Omega$



$$f_{L_S} = \frac{1}{2\pi R_{eq} C_S} = \frac{1}{2\pi(333.33\ \Omega)(2\ \mu\text{F})} = \mathbf{238.73\ Hz}$$

Since f_{L_S} is the largest of the three cutoff frequencies, it defines the low cutoff frequency for the network

Solution:

a. DC analysis: Plotting the transfer curve of $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$ and superimposing the curve defined by $V_{GS} = -I_D R_S$ results in an intersection at $V_{GS_Q} = -2$ V and $I_{D_Q} = 2$ mA. In addition,

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8\text{ mA})}{4\text{ V}} = 4\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 4\text{ mS}\left(1 - \frac{-2\text{ V}}{-4\text{ V}}\right) = 2\text{ mS}$$

$$f_{L_G} = \frac{1}{2\pi(R_{\text{sig}} + R_i)C_G} = \frac{1}{2\pi(10\text{ k}\Omega + 1\text{ M}\Omega)(0.01\ \mu\text{F})} \cong \mathbf{15.8\ Hz}$$

$$f_{L_C} = \frac{1}{2\pi(R_o + R_L)C_C} = \frac{1}{2\pi(4.7\text{ k}\Omega + 2.2\text{ k}\Omega)(0.5\ \mu\text{F})} \cong \mathbf{46.13\ Hz}$$

C_S $R_{\text{eq}} = R_S \| \frac{1}{g_m} = 1\text{ k}\Omega \| \frac{1}{2\text{ mS}} = 1\text{ k}\Omega \| 0.5\text{ k}\Omega = 333.33\ \Omega$

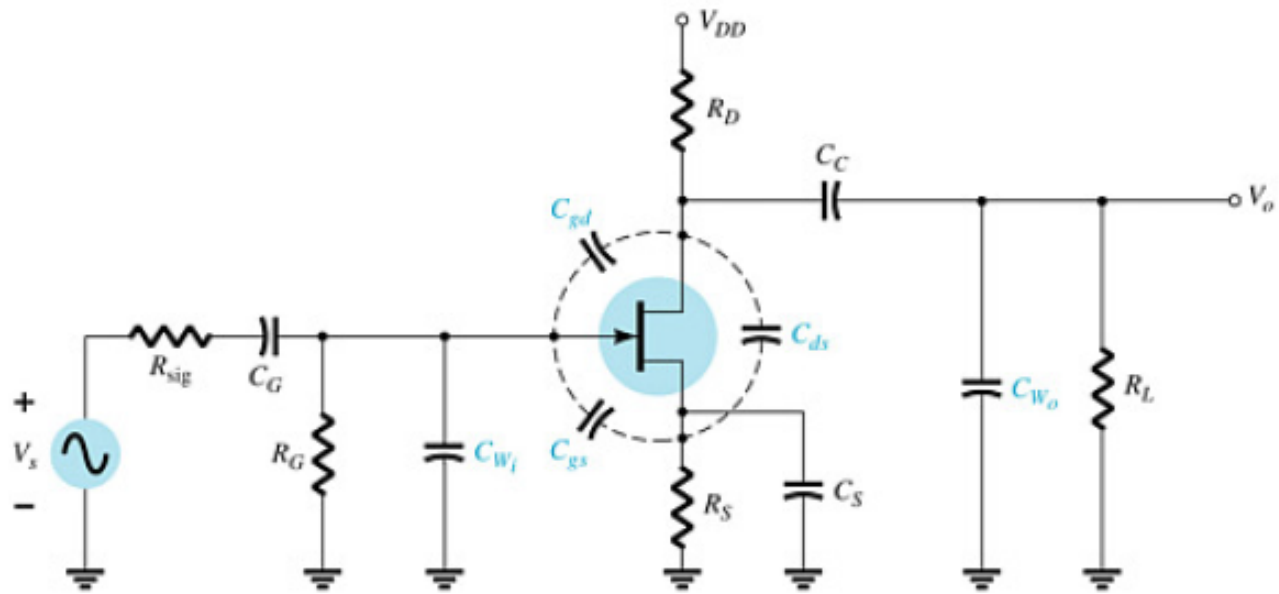
$$f_{L_S} = \frac{1}{2\pi R_{\text{eq}} C_S} = \frac{1}{2\pi(333.33\ \Omega)(2\ \mu\text{F})} = \mathbf{238.73\ Hz}$$

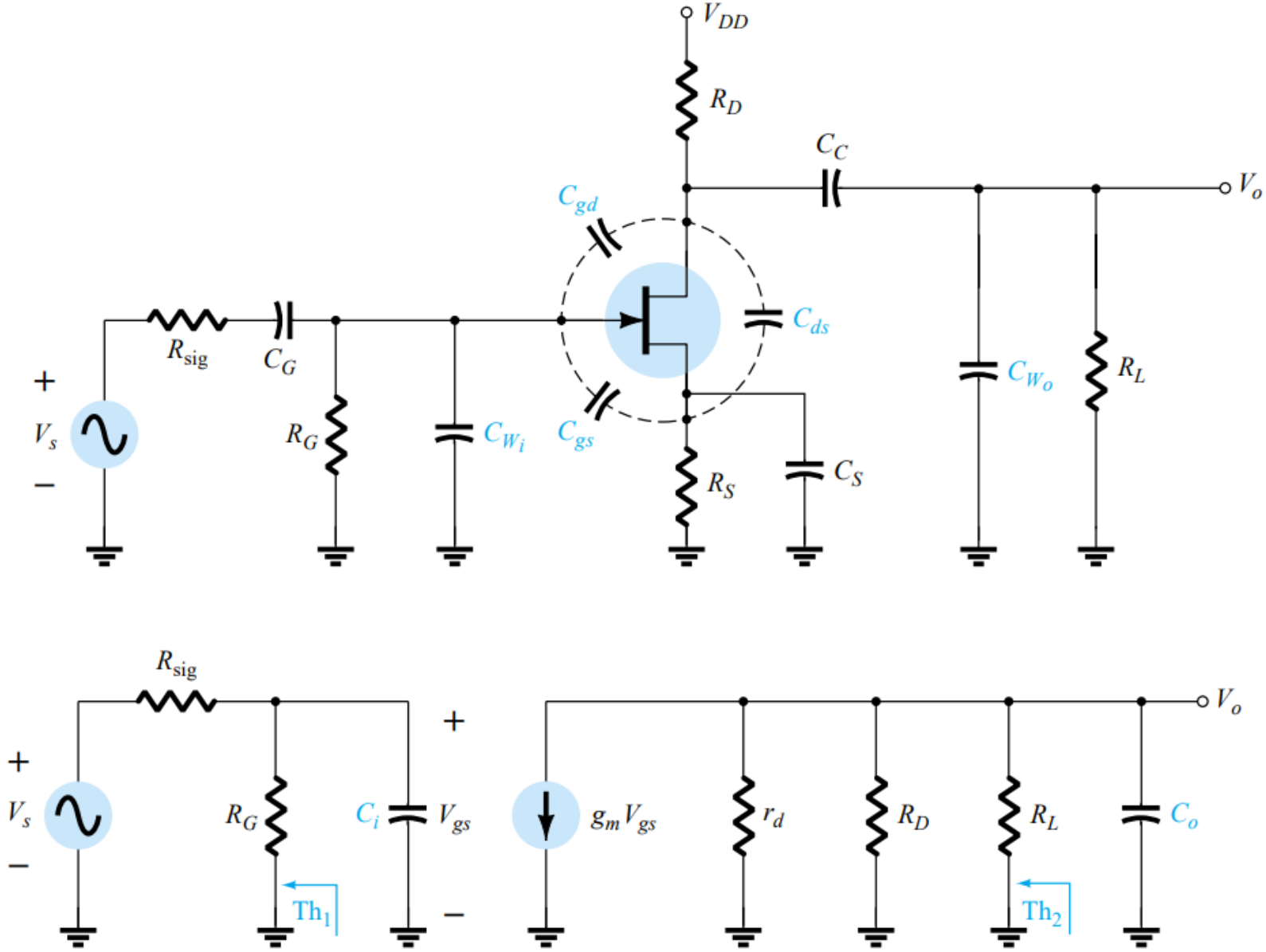
Since f_{L_S} is the largest of the three cutoff frequencies, it defines the low cutoff frequency for the network

FET Amplifier High-Frequency Response

Capacitances that affect the high-frequency response are

- **Junction capacitances**
  C_{gs}, C_{gd}, C_{ds}
- **Wiring capacitances**
  C_{wi}, C_{wo}
- **Coupling capacitors**
  C_G, C_C
- **Bypass capacitor**
  C_S




V_{DD}
R_D
C_C
V_o
C_{gd}
C_{ds}
R_{sig}
C_G
C_{W_o}
R_L
V_s
R_G
C_{W_i}
C_{gs}
R_S
C_S
R_{sig}
V_o
V_s
R_G
C_i
V_{gs}
$g_m V_{gs}$
r_d
R_D
R_L
C_o
Th_1
Th_2

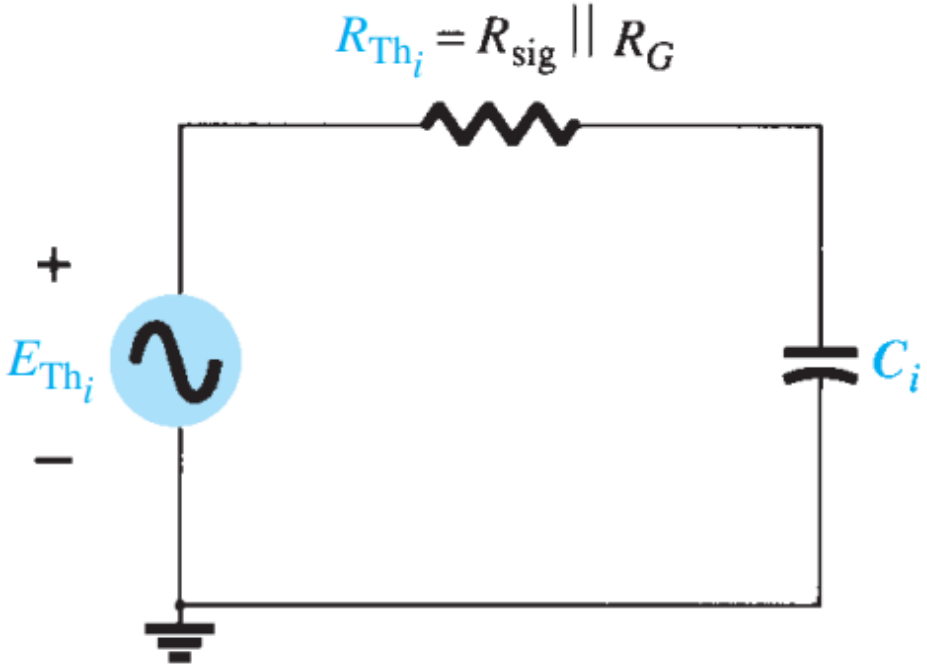
Input Network (f_{Hi}) High-Frequency Cutoff

$$f_{Hi} = \frac{1}{2\pi R_{Thi} C_i}$$

$$C_i = C_{Wi} + C_{gs} + C_{Mi}$$

$$C_{Mi} = (1 - A_v) C_{gd}$$

$$R_{Thi} = R_{sig} \parallel R_G$$



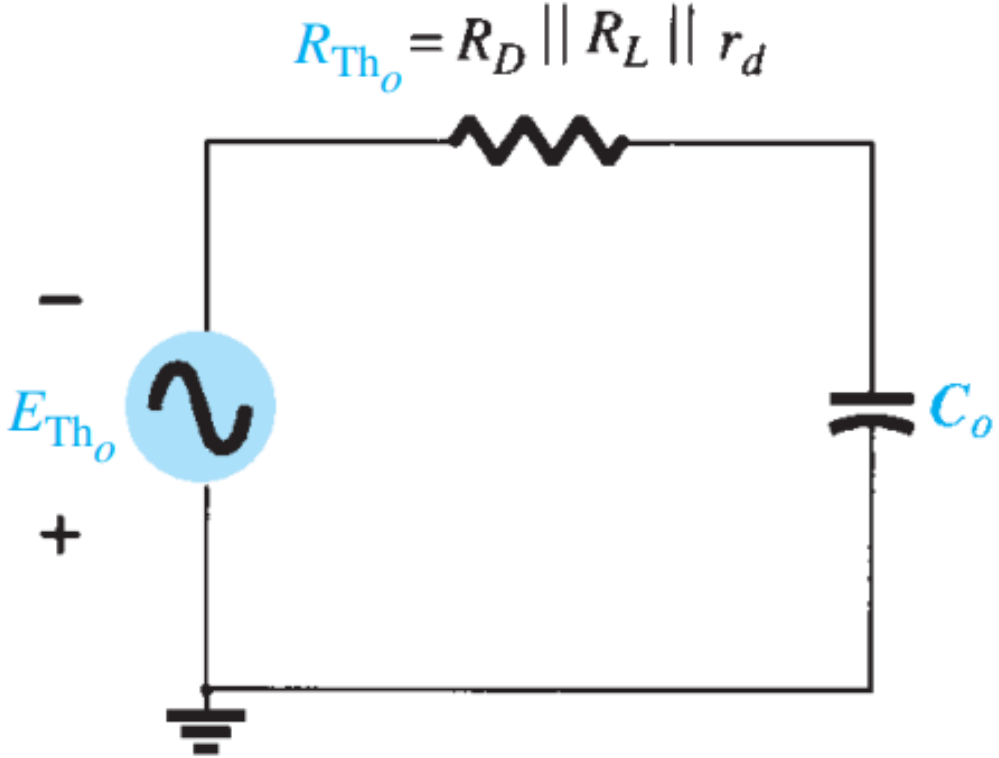
Output Network (f_{Ho}) High-Frequency Cutoff

$$f_{Ho} = \frac{1}{2\pi R_{Tho} C_o}$$

$$C_o = C_{Wo} + C_{ds} + C_{Mo}$$

$$C_{Mo} = \left(1 - \frac{1}{A_v}\right) C_{gd}$$

$$R_{Tho} = R_D \parallel R_L \parallel r_d$$



Example 2

(a) Determine the high cutoff frequencies for the network of Fig. using the same parameters

$$C_G = 0.01\ \mu\text{F}, \quad C_C = 0.5\ \mu\text{F}, \quad C_S = 2\ \mu\text{F}$$

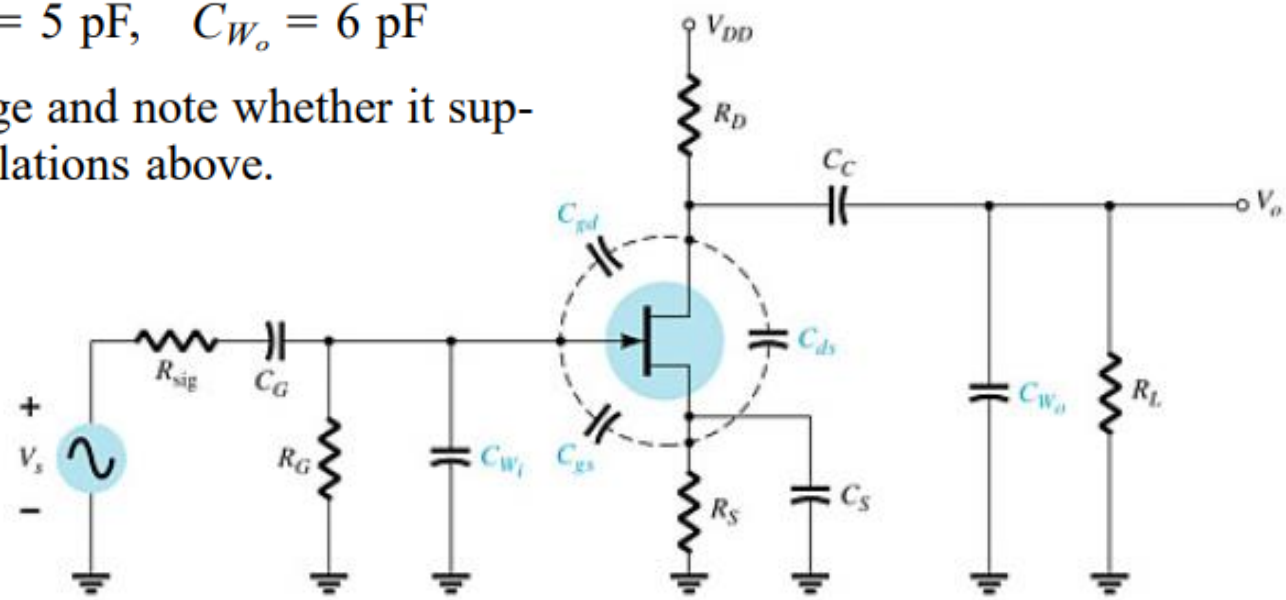
$$R_{\text{sig}} = 10\ \text{k}\Omega, \quad R_G = 1\ \text{M}\Omega, \quad R_D = 4.7\ \text{k}\Omega, \quad R_S = 1\ \text{k}\Omega, \quad R_L = 2.2\ \text{k}\Omega$$

$$I_{DSS} = 8\ \text{mA}, \quad V_P = -4\ \text{V}, \quad r_d = \infty\ \Omega, \quad V_{DD} = 20\ \text{V}$$

with the addition of

$$C_{gd} = 2\ \text{pF}, \quad C_{gs} = 4\ \text{pF}, \quad C_{ds} = 0.5\ \text{pF}, \quad C_{W_i} = 5\ \text{pF}, \quad C_{W_o} = 6\ \text{pF}$$

(b) Review a **PROBE** response for the full frequency range and note whether it supports the conclusions of Example 11.10 and the calculations above.



Solution

(a) $R_{\text{Th}_1} = R_{\text{sig}} \| R_G = 10\ \text{k}\Omega \| 1\ \text{M}\Omega = 9.9\ \text{k}\Omega$

From Example 11.10, $A_v = -3$.

$$C_i = C_{W_i} + C_{gs} + (1 - A_v)C_{gd}$$
$$= 5\ \text{pF} + 4\ \text{pF} + (1 + 3)2\ \text{pF}$$
$$= 9\ \text{pF} + 8\ \text{pF}$$
$$= 17\ \text{pF}$$

$$f_{H_i} = \frac{1}{2\pi R_{Th_1} C_i}$$
$$= \frac{1}{2\pi(9.9\ \text{k}\Omega)(17\ \text{pF})} = \mathbf{945.67\ kHz}$$

$$R_{\text{Th}_2} = R_D \| R_L$$
$$= 4.7\ \text{k}\Omega \| 2.2\ \text{k}\Omega$$
$$\cong 1.5\ \text{k}\Omega$$

$$C_o = C_{W_o} + C_{ds} + C_{M_o} = 6\ \text{pF} + 0.5\ \text{pF} + \left(1 - \frac{1}{-3}\right)2\ \text{pF} = 9.17\ \text{pF}$$

$$f_{H_o} = \frac{1}{2\pi(1.5\ \text{k}\Omega)(9.17\ \text{pF})} = \mathbf{11.57\ MHz}$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8\ \text{mA})}{4\ \text{V}} = 4\ \text{mS}$$

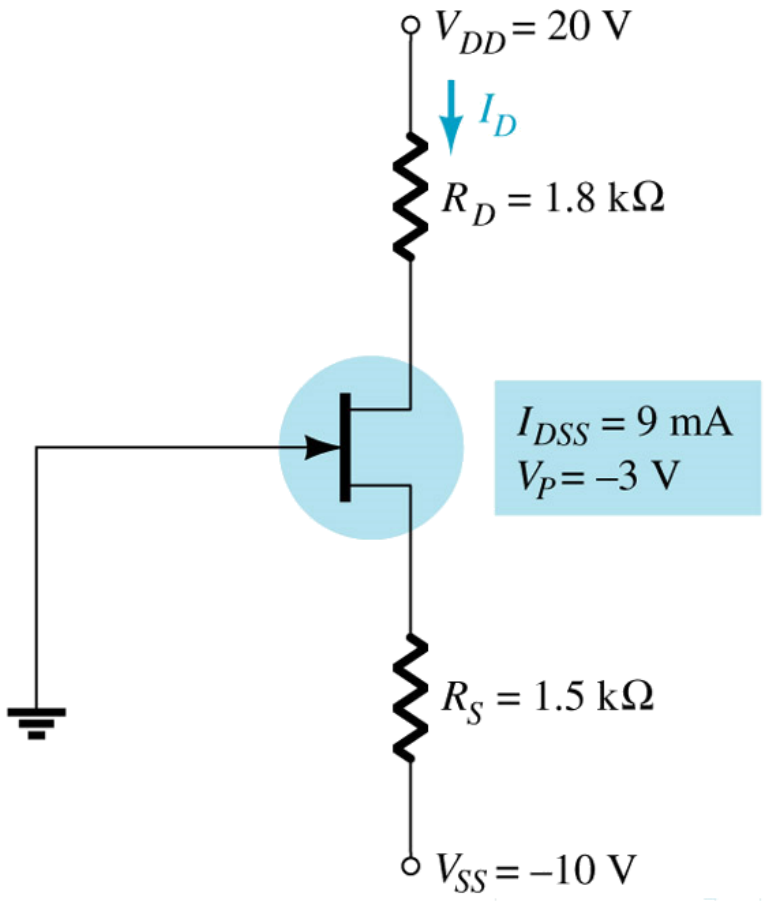
$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 4\ \text{mS}\left(1 - \frac{-2\ \text{V}}{-4\ \text{V}}\right) = 2\ \text{mS}$$

$$A_{v_{\text{mid}}} = \frac{V_o}{V_i} = -g_m(R_D \| R_L) = -(2\ \text{mS})(4.7\ \text{k}\Omega \| 2.2\ \text{k}\Omega)$$
$$= -(2\ \text{mS})(1.499\ \text{k}\Omega)$$
$$\cong \mathbf{-3}$$

Home Work:

Determine the following for the network

1. I_{DQ} and V_{GSQ}
2. V_{DS}
3. V_D
4. V_S



Drawing the self bias line

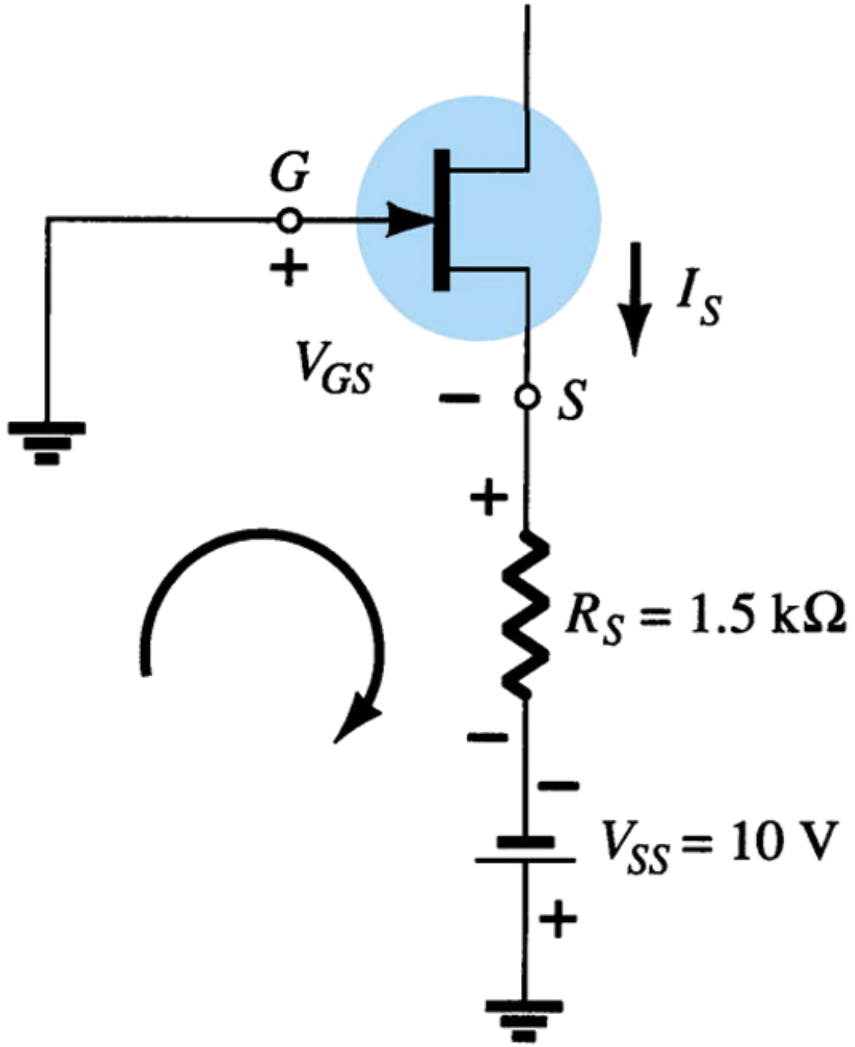
$$V_{GS} + I_D R_S - 10V = 0$$

$$V_{GS} = 10V - I_D\,(1.5k\Omega)$$

When $V_{GS} = 0V$, $I_D = \dfrac{10V}{1.5k\Omega} = 6.67mA$

When $I_D = 0mA$, $V_{GS} = 10V$

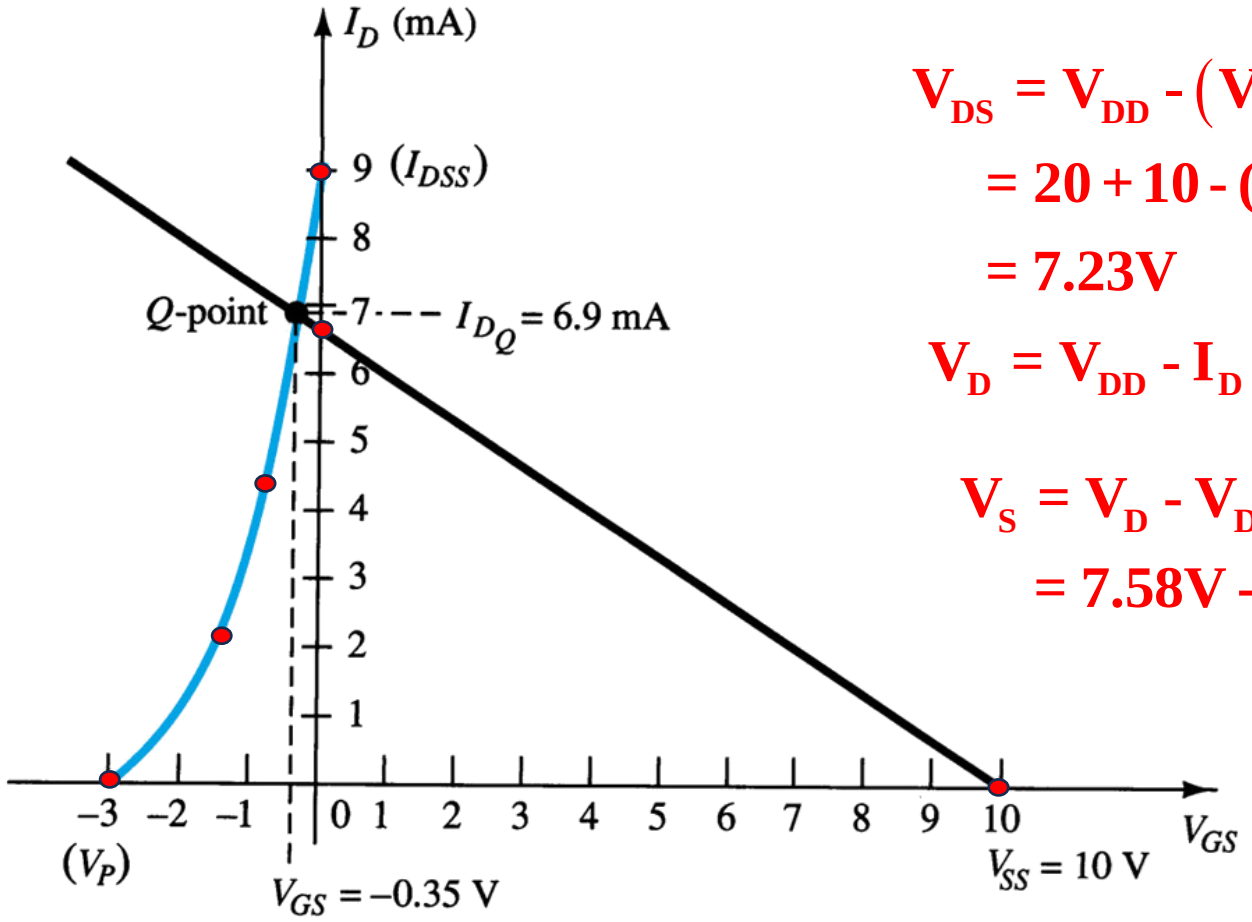
V_{GS}	I_D	V_{GS},I_D
0	I_{DSS}	(0,9)
$0.3V_P$	$I_{DSS}/2$	(-0.9,4.5)
$0.5V_P$	$I_{DSS}/4$	(-1.5,2.25)
V_P	0mA	(-3,0)



Determining the *Q*-point

$I_{DQ}=6.9mA$

$V_{GSQ}=-0.35V$



$$V_{DS} = V_{DD} - (V_{SS}) - I_D(R_S + R_D)$$

$$= 20 + 10 - (6.9mA)(1.8k\Omega + 1.5k\Omega)$$

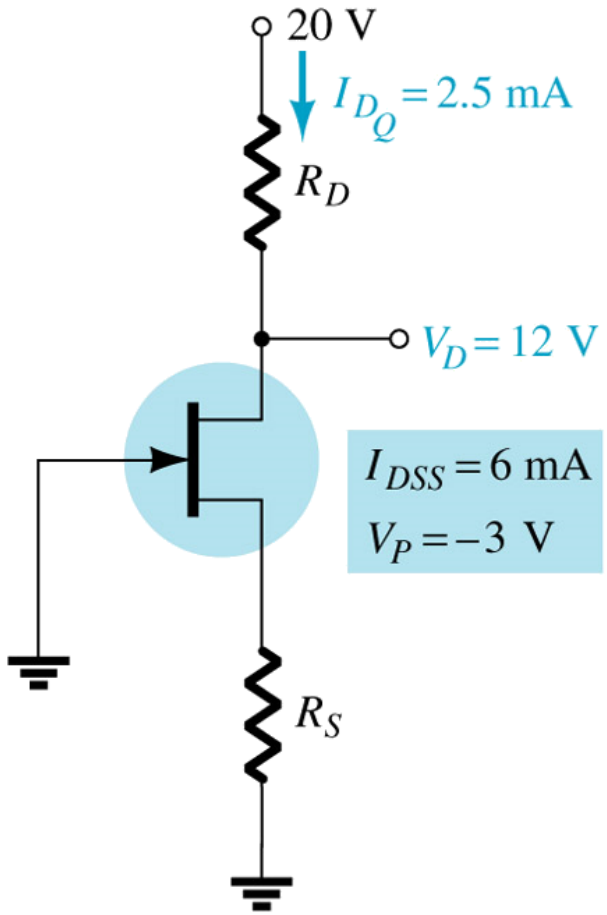
$$= 7.23V$$

$$V_D = V_{DD} - I_D(R_D) = 7.58V$$

$$V_S = V_D - V_{DS}$$

$$= 7.58V - 7.23V = 0.35V$$

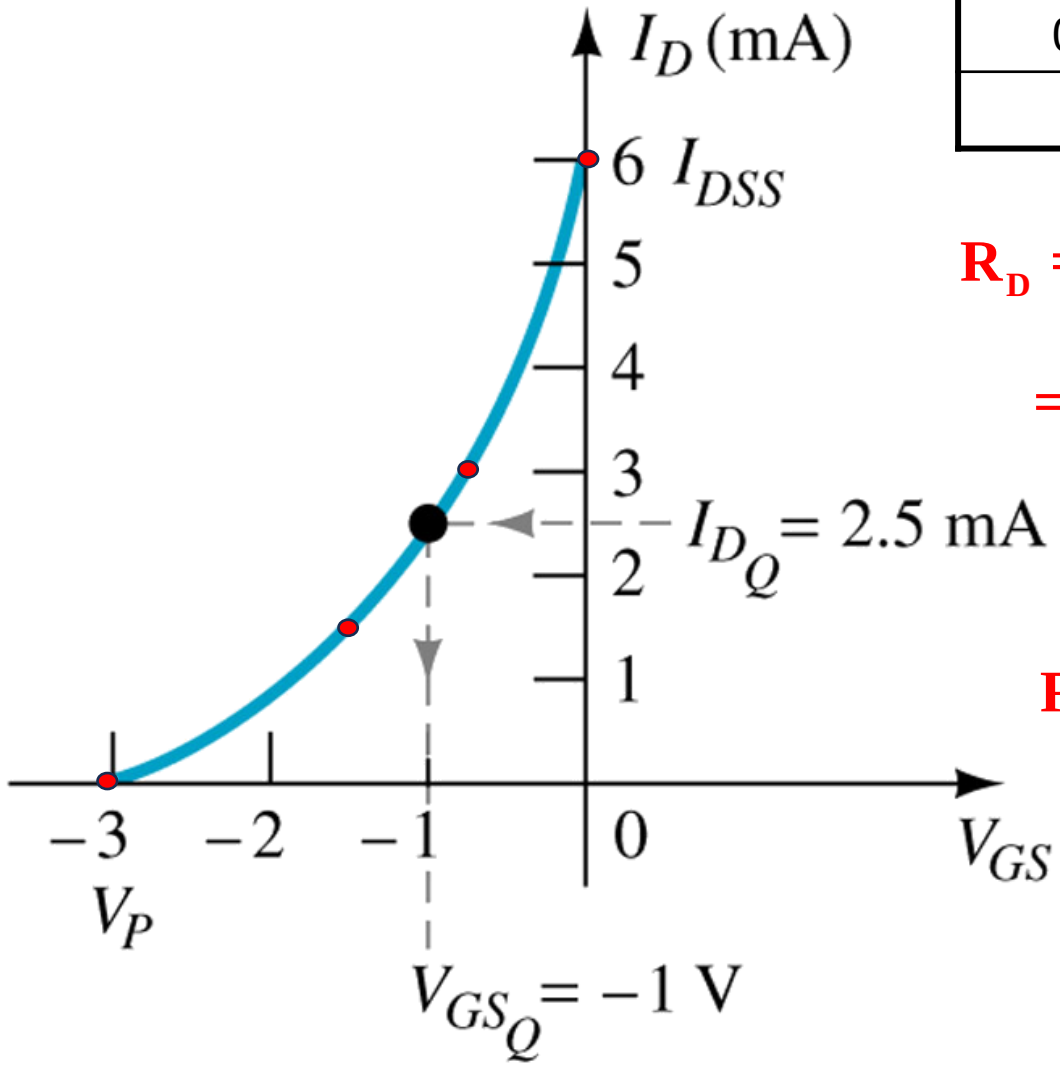
Exercise 4



Determine the required values of R_D and R_S

Determining V_{GS_Q} for the network

V_{GS}	I_D	V_{GS},I_D
0	I_{DSS}	(0,6)
$0.3V_P$	$I_{DSS}/2$	(-0.9,3)
$0.5V_P$	$I_{DSS}/4$	(-1.5,1.5)
V_P	0mA	(-3,0)



$$R_D = \frac{V_{RD}}{I_{DQ}} = \frac{V_{DD} - V_{DQ}}{I_{DQ}} = \frac{20V - 12V}{2.5mA}$$

$$= 3.2k\Omega$$

$$R_S = \frac{-(V_{GSQ})}{I_{DQ}} = \frac{-(-1)}{2.5mA} = 0.4k\Omega$$

Home Work

- Determine I_{DQ}, V_{GSQ}, V_{DS}, V_D and V_S