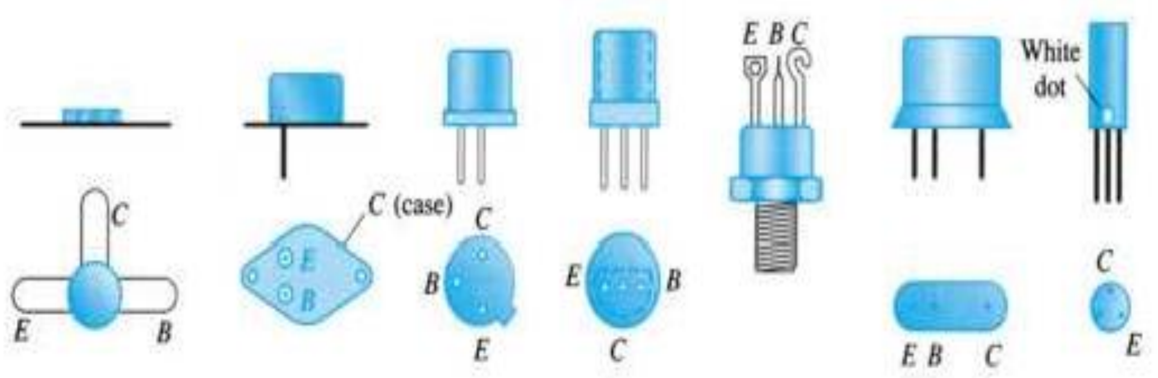
Ninevah University
College of Electronics Engineering
Department of Systems and Control

Electronic I
Lecture 1

The Bipolar Junction Transistor (BJT)



2nd Class

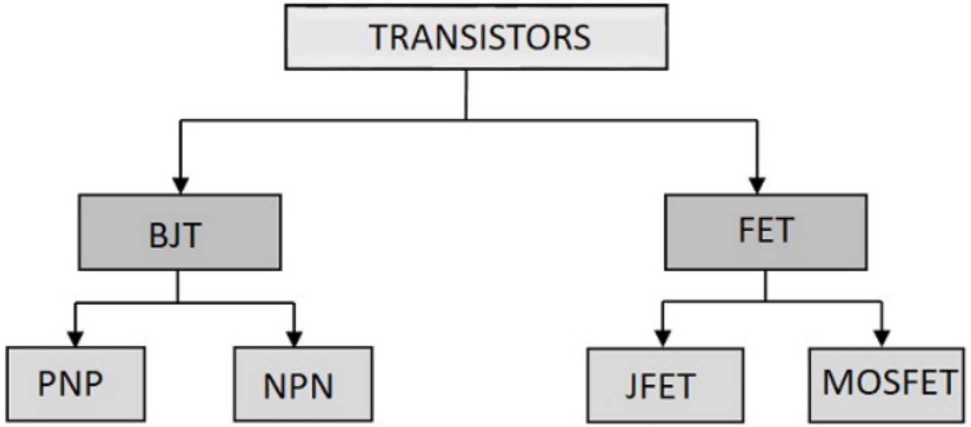
by
Rafal Raed Mahmood Alshaker

Outline of Presentation

1	• Basic Transistor Operation
2	• Transistor Currents
3	• Characteristics Curves
4	• DC Load Line

Introduction

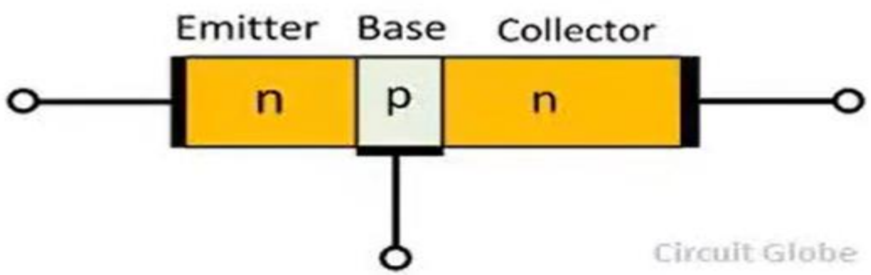
- John Bardeen, William Shockley and Walter Brattain at Bell Labs, 1948
- **Transistor** is a combination of **transfer** and **resistance**. This is because it transfers the resistance from one end of the device to the other end

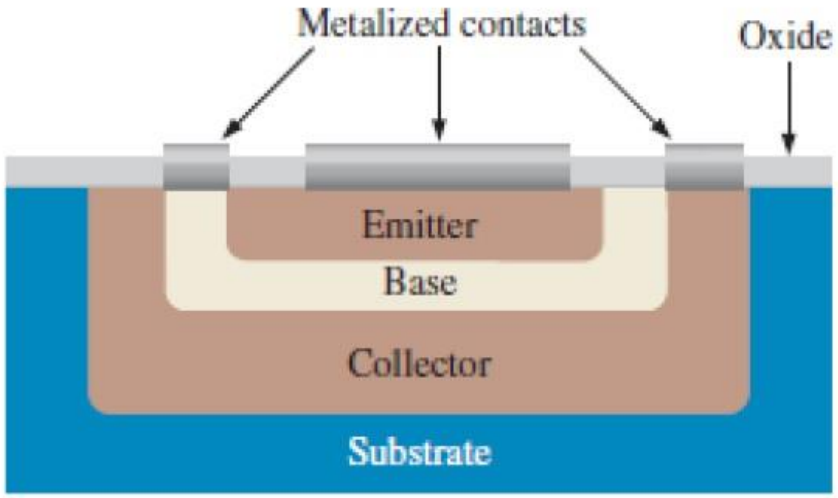


Transistor Structure

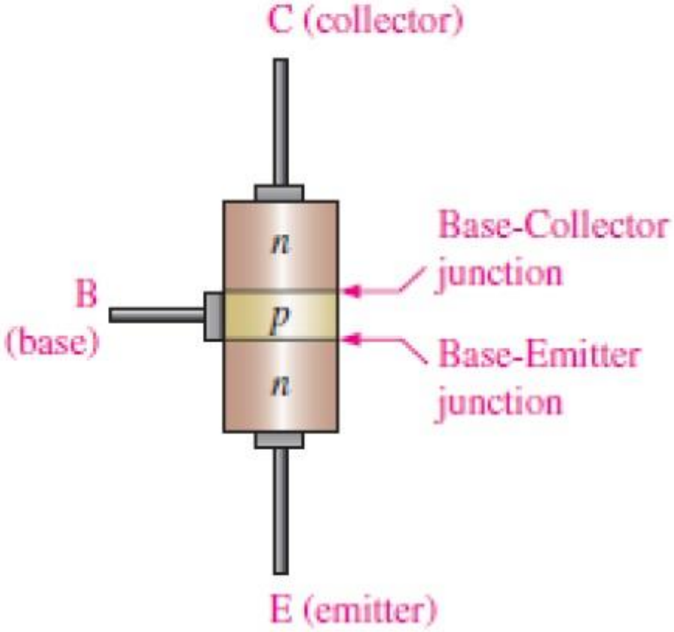
The term bipolar refers to the use of both holes and electrons as current carriers in the Transistor Structure.

base region is **lightly doped** and **very thin**
emitter region **heavily doped**
collector regions **moderate**e doped

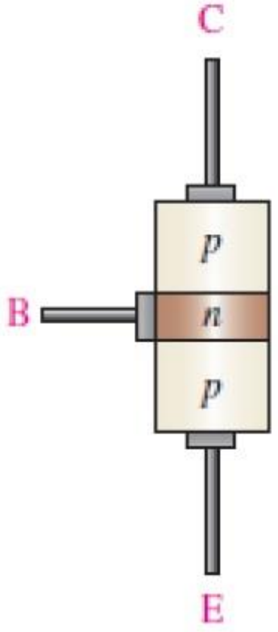




(a) Basic epitaxial planar structure

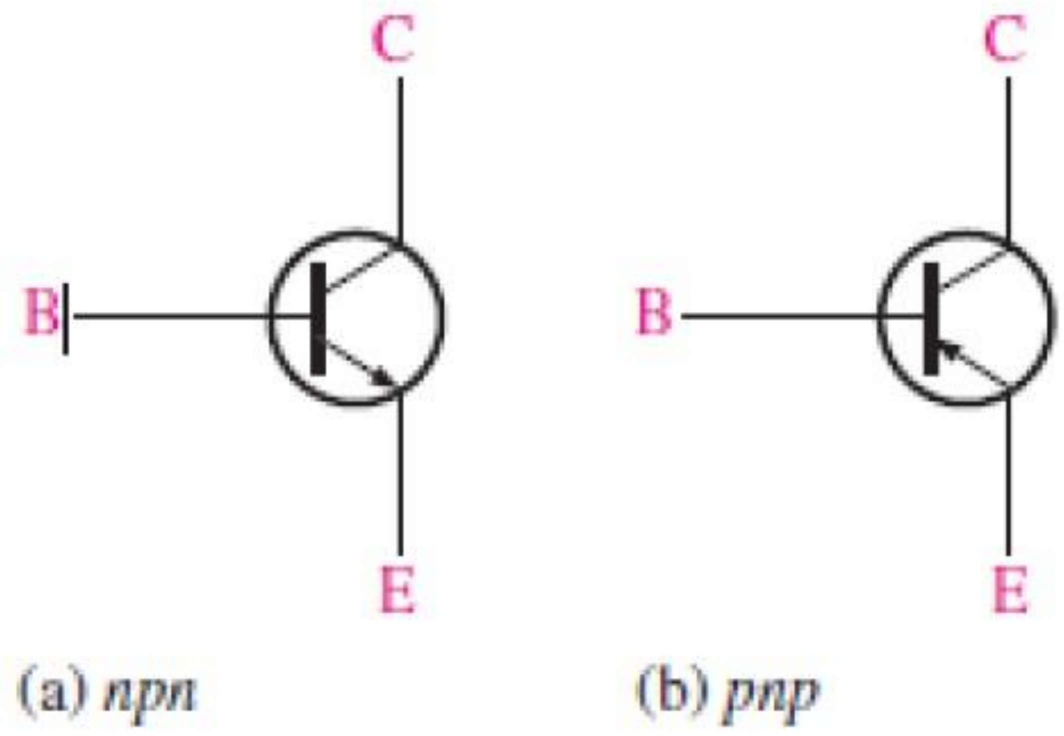


(b) *npn*



(c) *pnp*

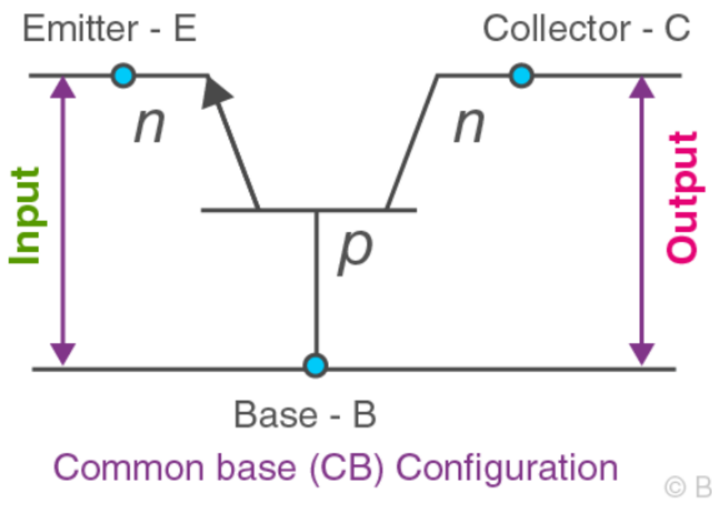
Standard BJT (bipolar junction transistor) symbols



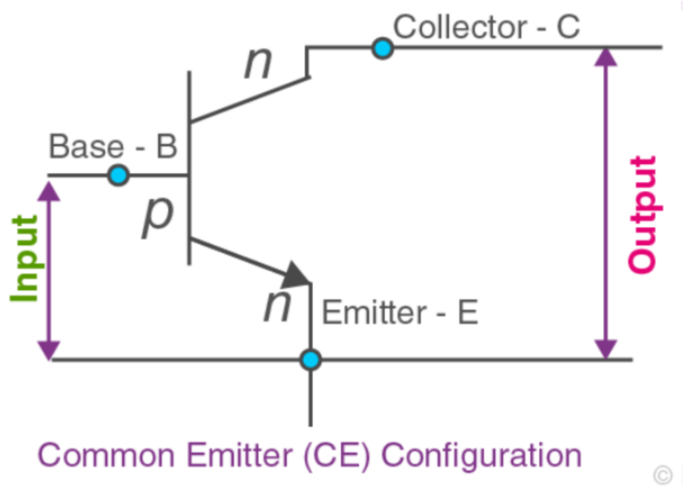
Transistor Configuration

A transistor is a three-terminal device, but we require four terminals (two for input and two for output) for connecting it in a circuit.

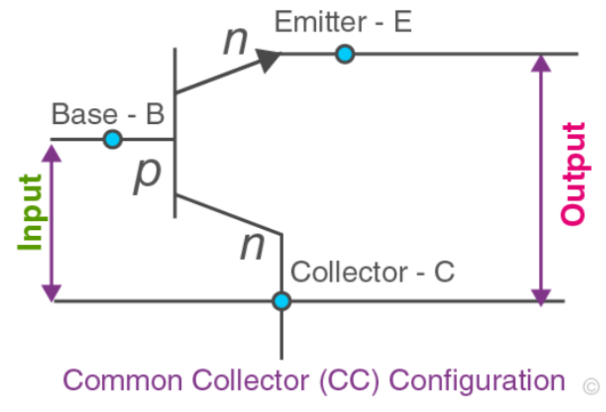
Common Base Configuration



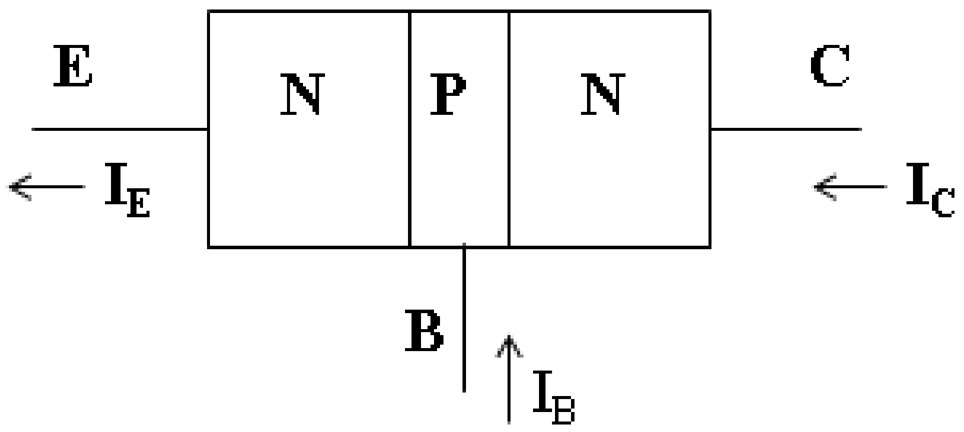
Common Emitter Configuration(CE)



Common collector configuration(CC)

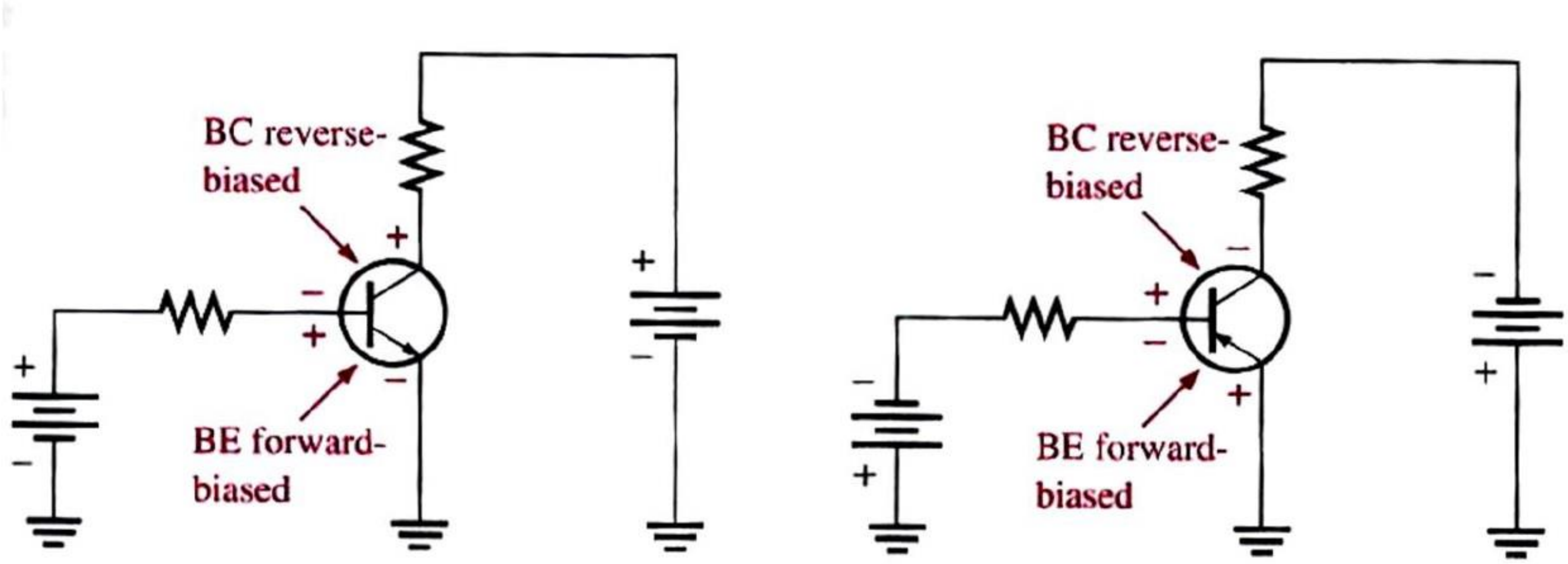


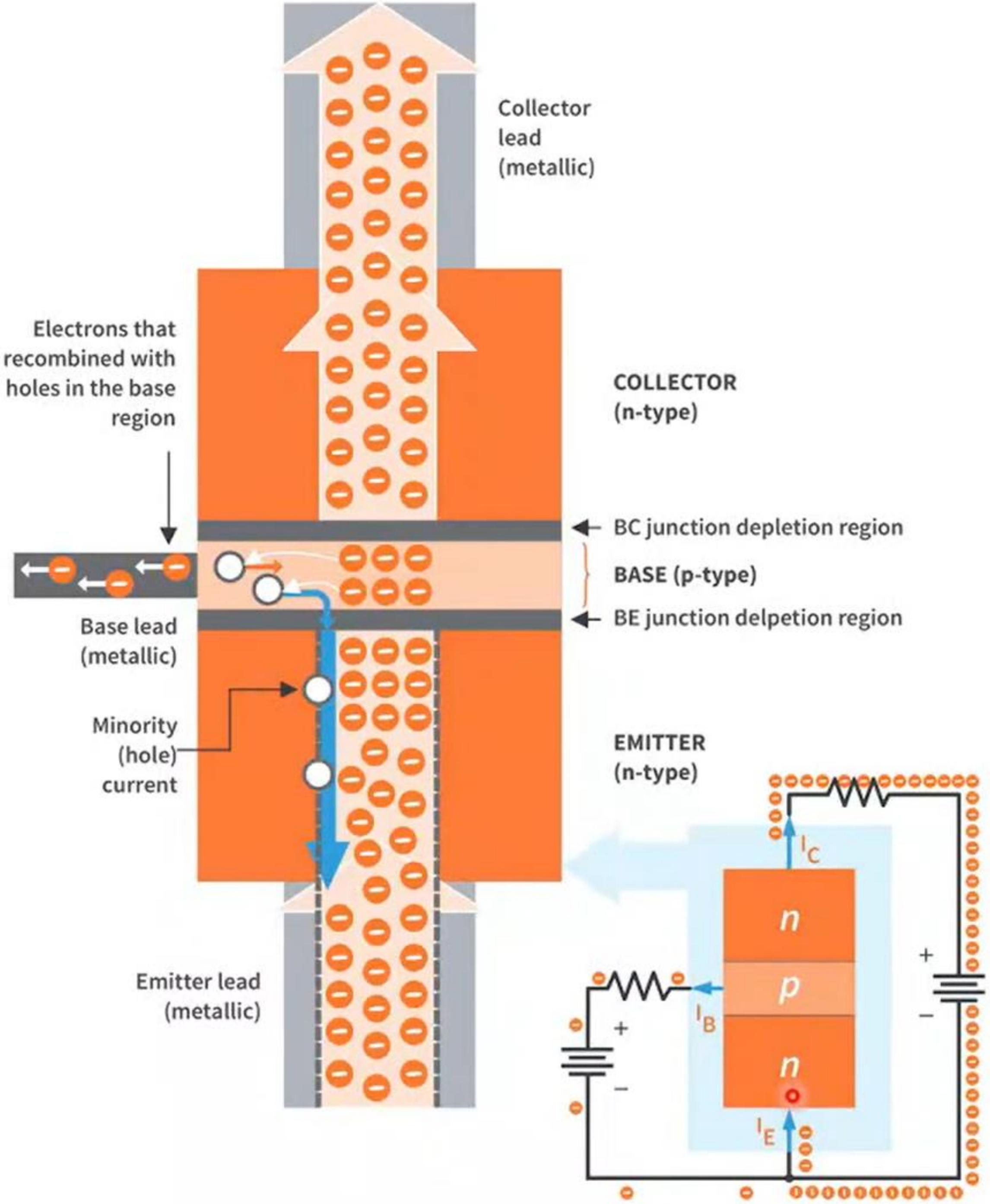
Modes of BJT Operation

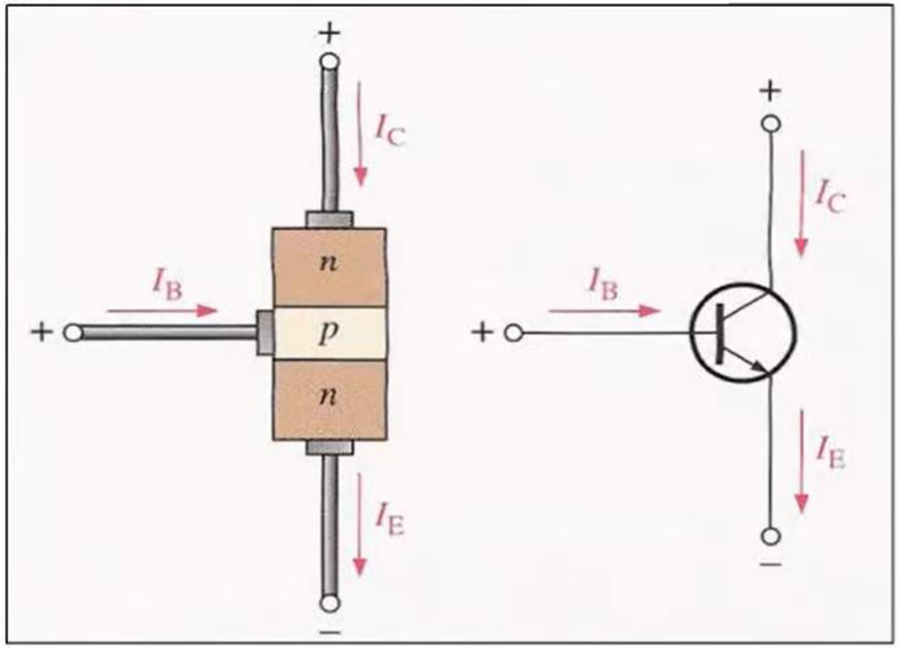


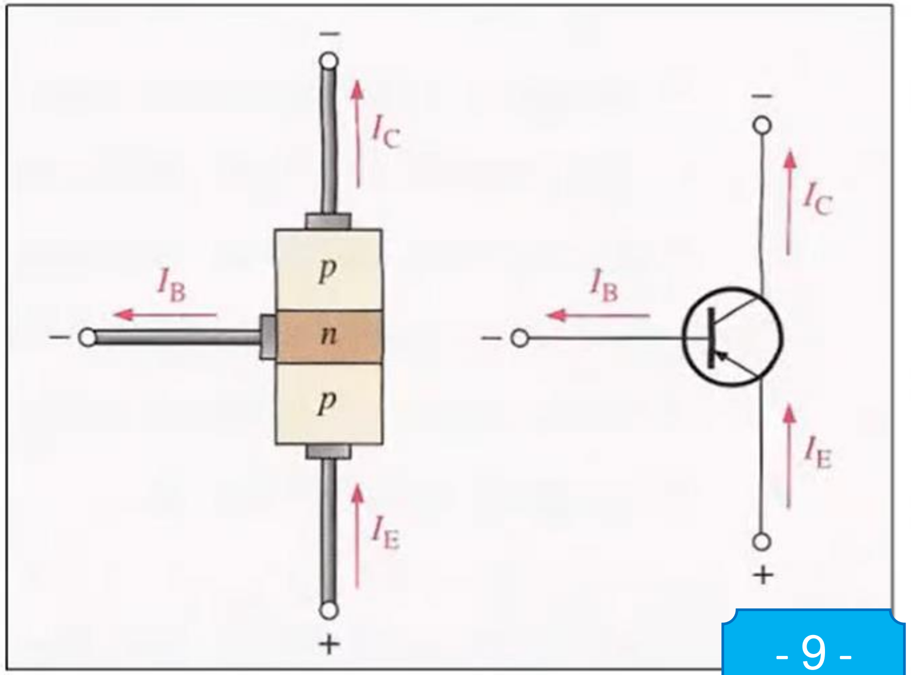
CB Junction	BE Junction	Mode of Operation
Reverse	Reverse	Cut-off
Forward	Reverse	Inverted
Reverse	Forward	Active
Forward	Forward	Saturation

Basic Transistor Operation

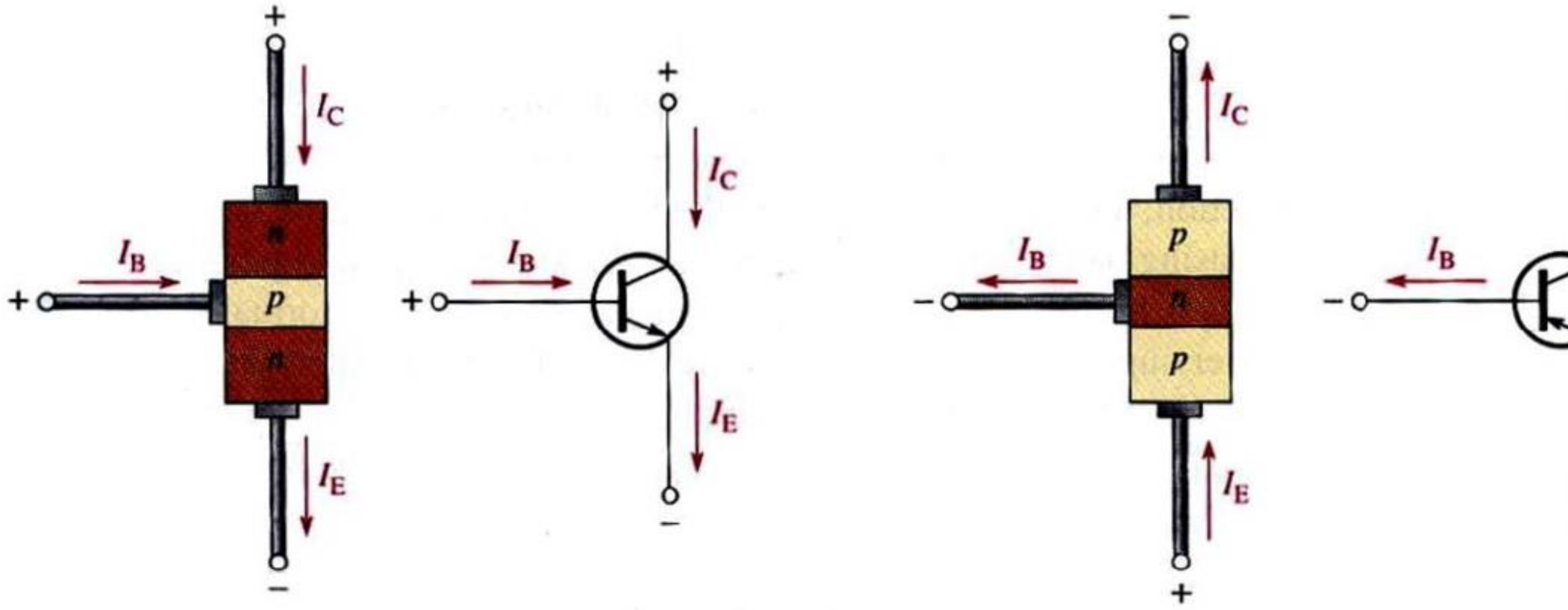



Collector lead (metallic)
Electrons that recombined with holes in the base region
COLLECTOR (n-type)
BC junction depletion region
BASE (p-type)
BE junction delpetion region
Base lead (metallic)
Minority (hole) current
EMITTER (n-type)
Emitter lead (metallic)
n
p
n
I_C
I_B
I_E
+
−
+
−


+
I_C
I_B
n
p
n
I_E
−
+
I_C
I_B
+
I_E
−


−
I_C
I_B
p
n
p
I_E
+
−
I_C
I_B
−
I_E
+

Transistor Currents



(a) *npn* (b) *pnp*

The emitter current (I_E) is the sum of the collector current (I_C) and the base current (I_B):

$$I_E = I_C + I_B \quad \dots\dots\dots\dots\dots\dots (1)$$

Usually, we assume $I_E \cong I_C$, because I_B is very small compared to I_E and I_C.

The dc current gain of a transistor is given:

$$\beta_{DC} = \frac{I_C}{I_B} \quad \dots\dots\dots\dots\dots\dots (2)$$

Typically, values of β_{DC} range from **20** to **200** or higher.

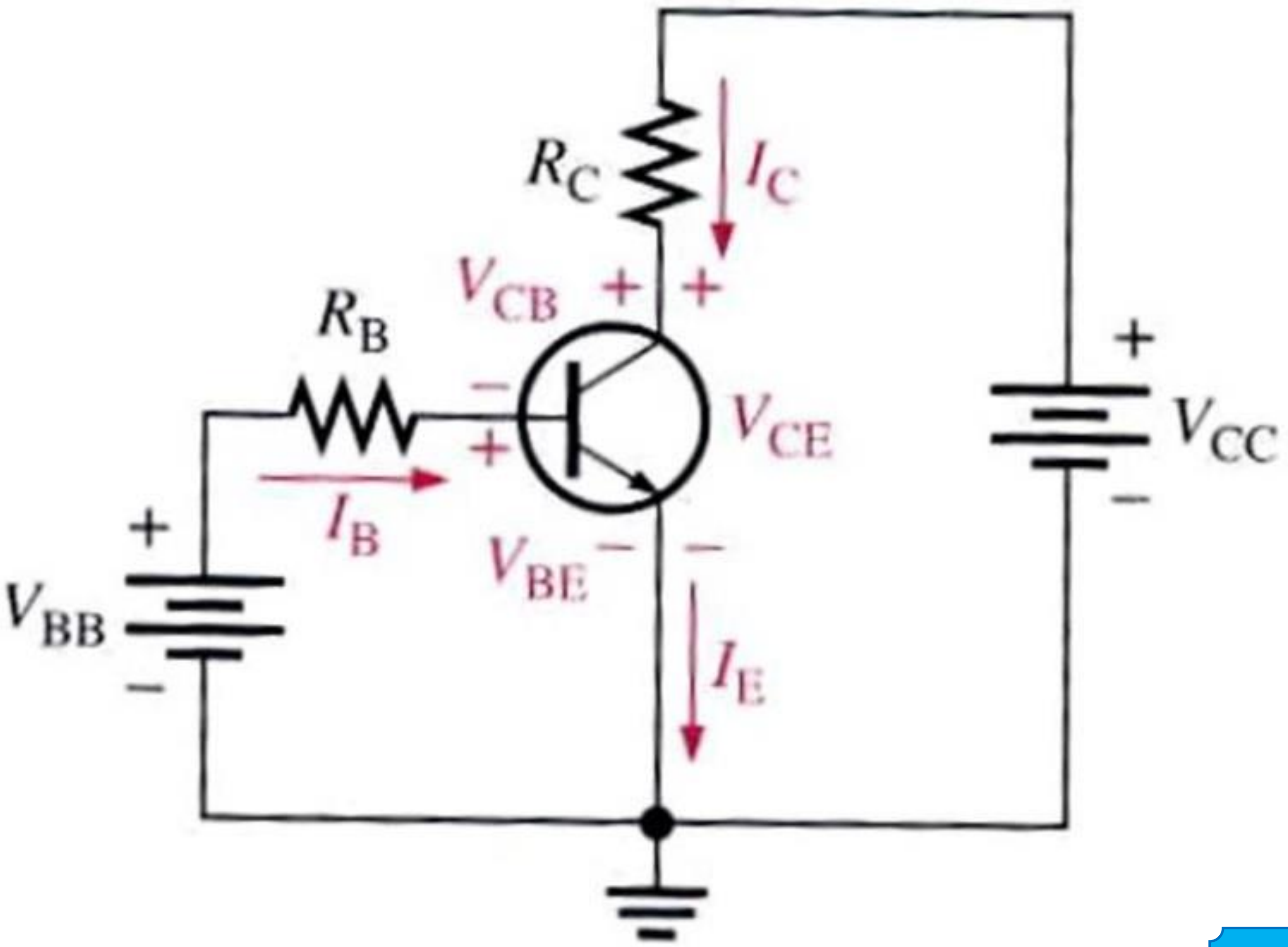
(α_{DC}) is less used parameter than (β_{DC}) in transistor circuit:

$$\alpha_{DC} = \frac{I_C}{I_E} \quad \dots\dots\dots\dots\dots\dots\dots (3)$$

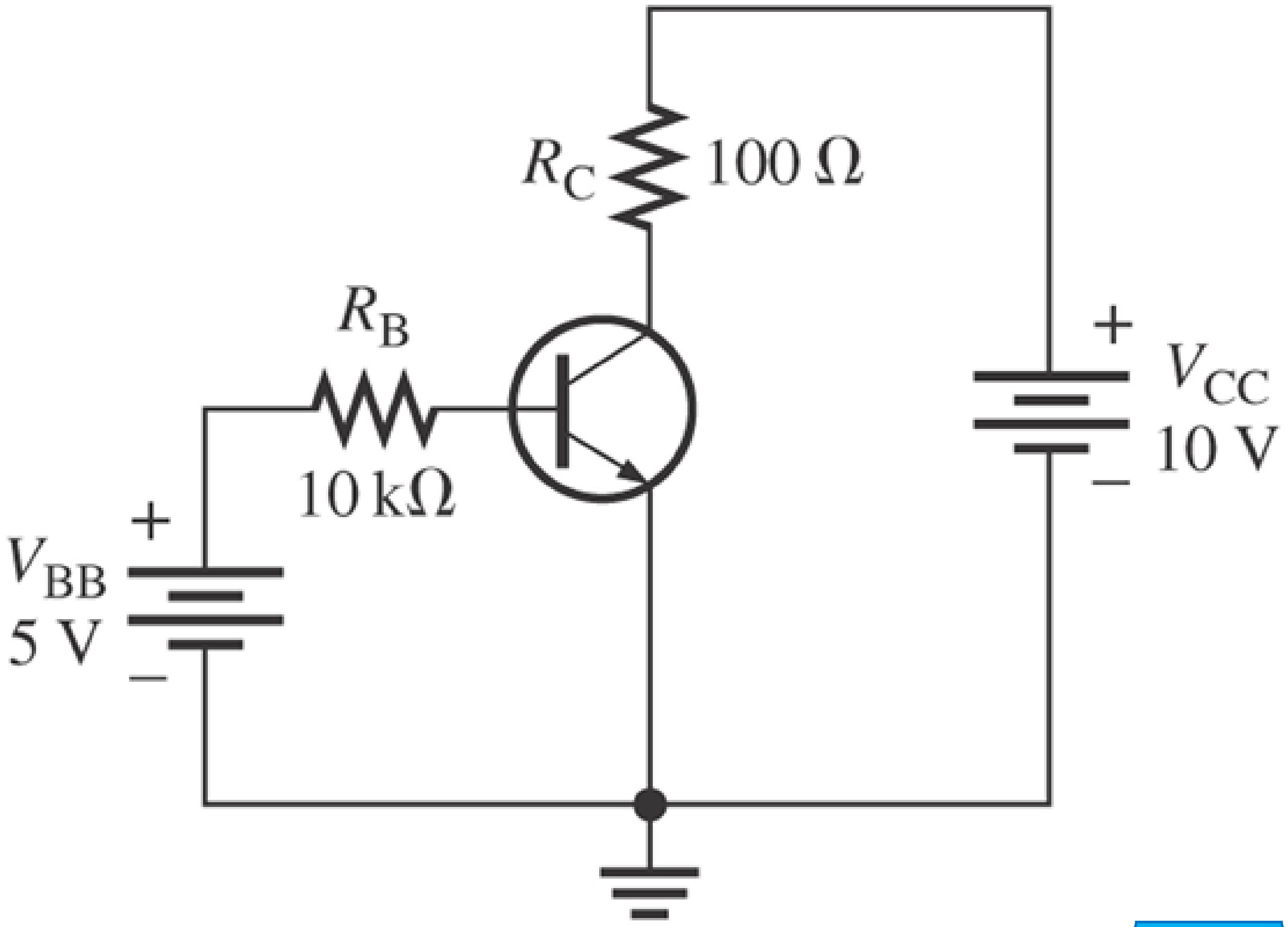
Typically, values of α_{DC} range from **0.95** to **0.99** or greater, but α_{DC} is always less than **1**.

Example 1: Determine the dc current gain β_{DC} and the emitter current I_E for a transistor where I_B = 50 μA and I_C = 3.65 mA.

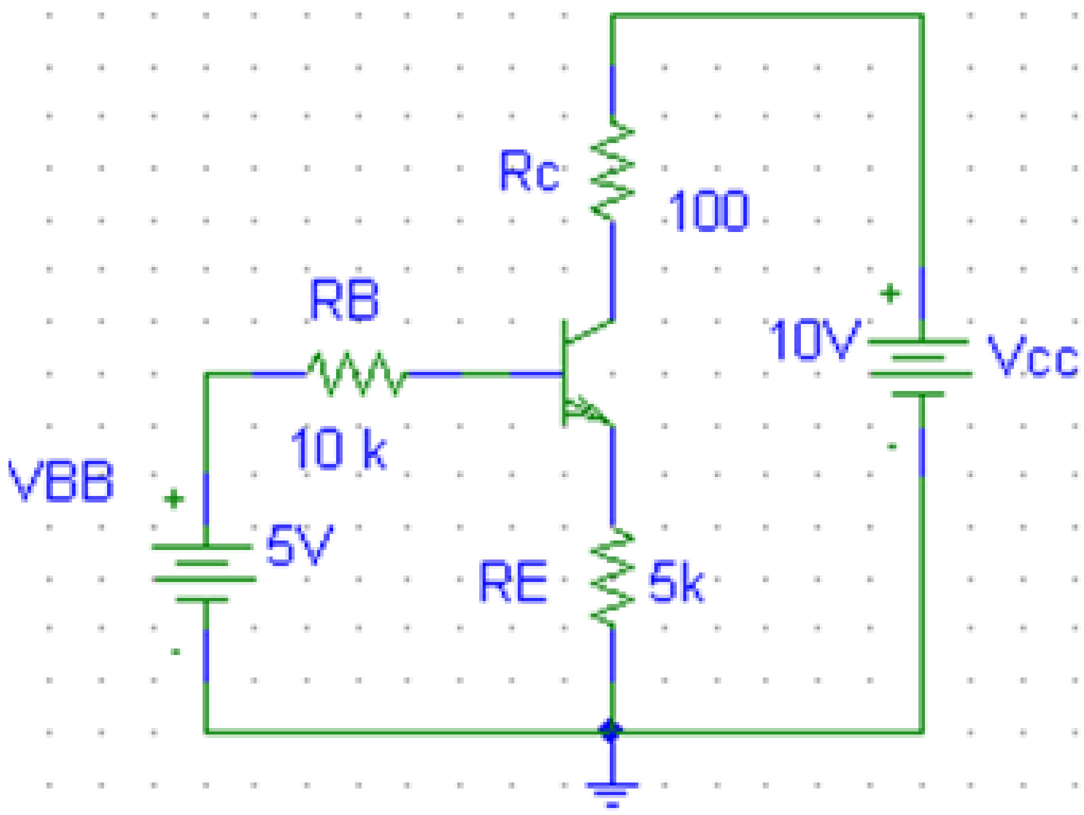
Current and Voltage Analysis



Example 2: Determine I_B, I_C, I_E, V_{BE}, V_{CE}, and V_{CB} in the circuit. Assume $\beta_{DC} = 150$.



Home Work: Determine I_B, I_C, I_E, V_{BE}, V_{CE}, and V_{CB} in the circuit. Assume β_{DC} = 150.



SUMMARY

The BJT (bipolar junction transistor) is constructed with three regions: base, collector, and emitter.

- The BJT has two *pn* junctions, the base-emitter junction and the base-collector junction.
- Current in a BJT consists of both free electrons and holes, thus the term *bipolar*.
- The base region is very thin and lightly doped compared to the collector and emitter regions.
- The two types of bipolar junction transistor are the *npn* and the *pnp*.

Section

- To operate as an amplifier, the base-emitter junction must be forward-biased and the base-collector junction must be reverse-biased. This is called *forward-reverse bias*.
- The three currents in the transistor are the base current (I_B), emitter current (I_E), and collector current (I_C).
- I_B is very small compared to I_C and I_E.

Section

- The dc current gain of a transistor is the ratio of I_C to I_B and is designated β_{DC}. Values typically range from less than 20 to several hundred.
- β_{DC} is usually referred to as h_{FE} on transistor datasheets.
- The ratio of I_C to I_E is called α_{DC}. Values typically range from 0.95 to 0.99.
- There is a variation in β_{DC} over temperature and also from one transistor to another of the same type.

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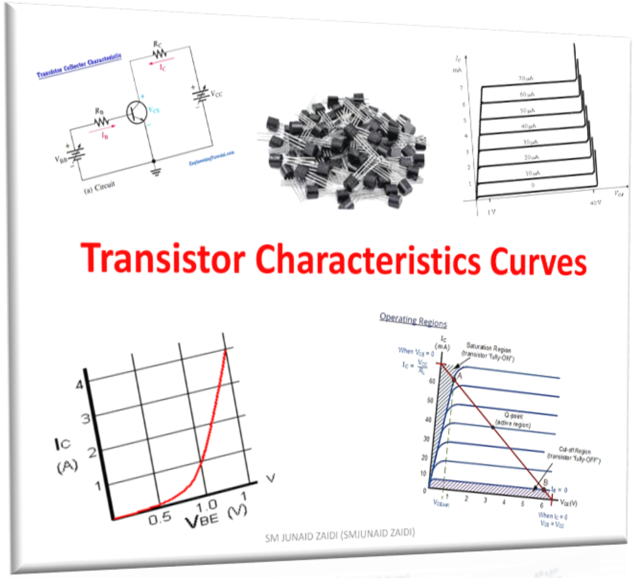
Electronic I
Lecture 2

Transistor Characteristics and parameters



2nd Class

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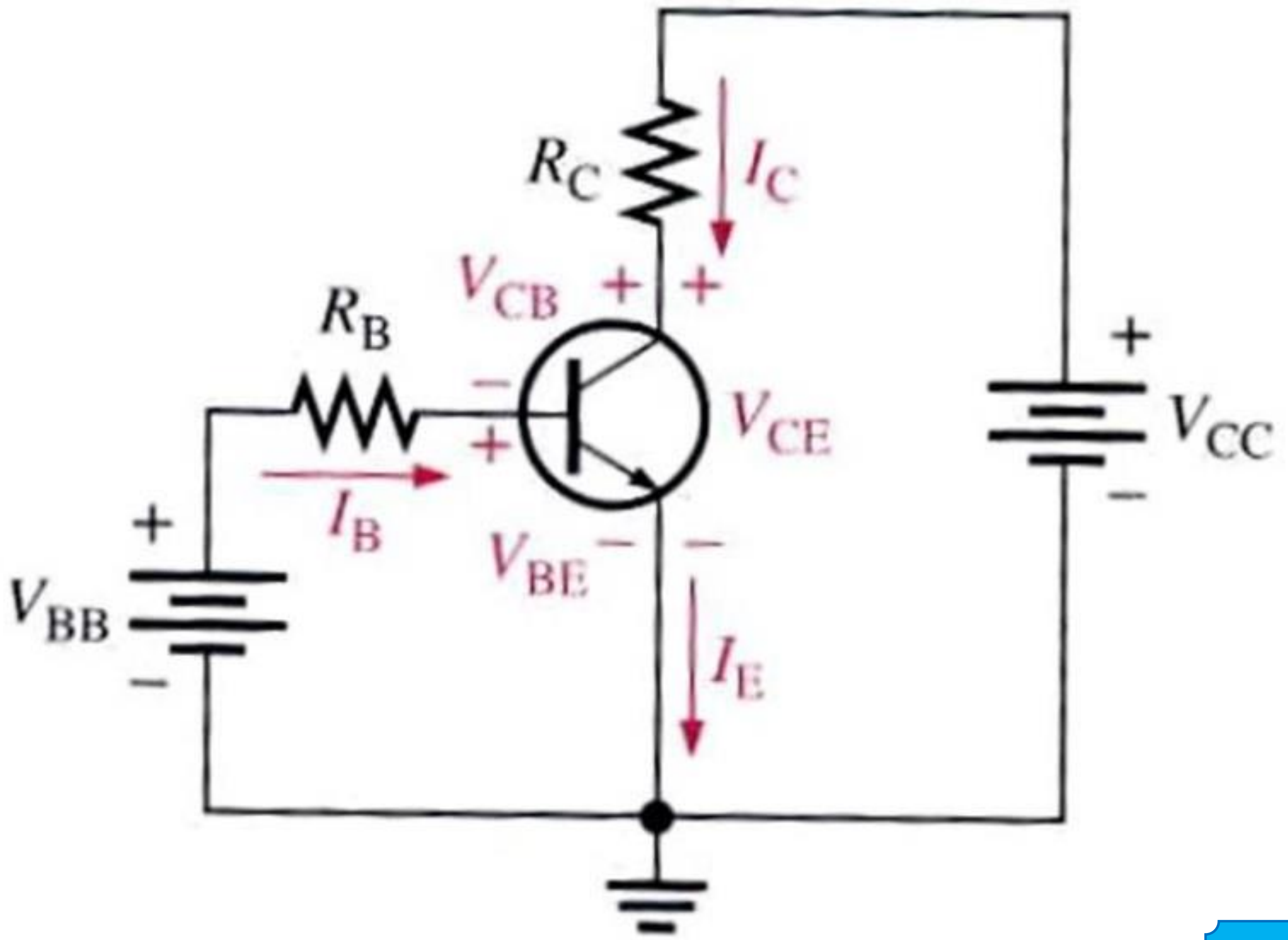
Outline of Presentation

1. Transistor Currents
2. Characteristics Curves
3. DC Load Line

Current and Voltage Analysis



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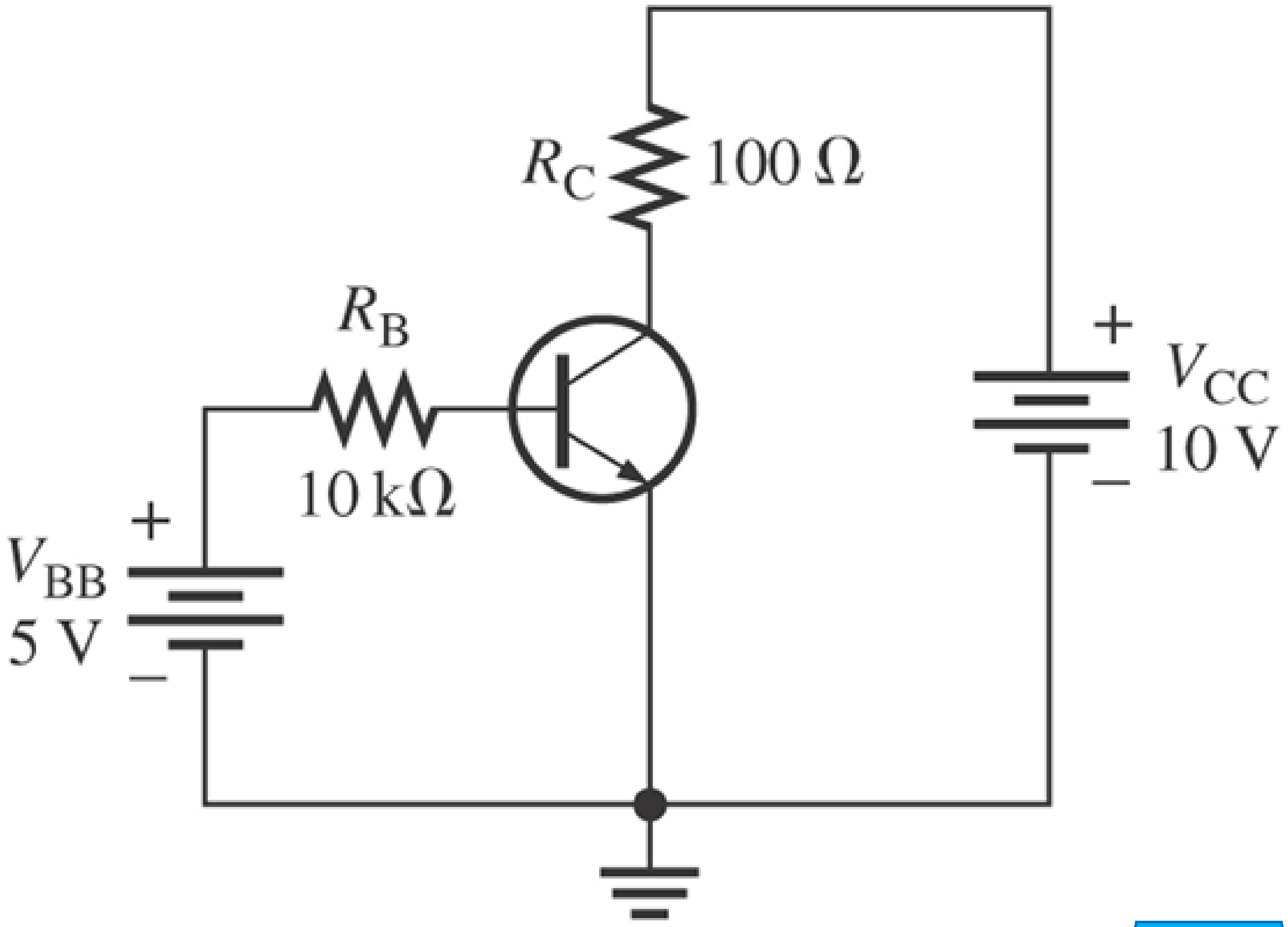
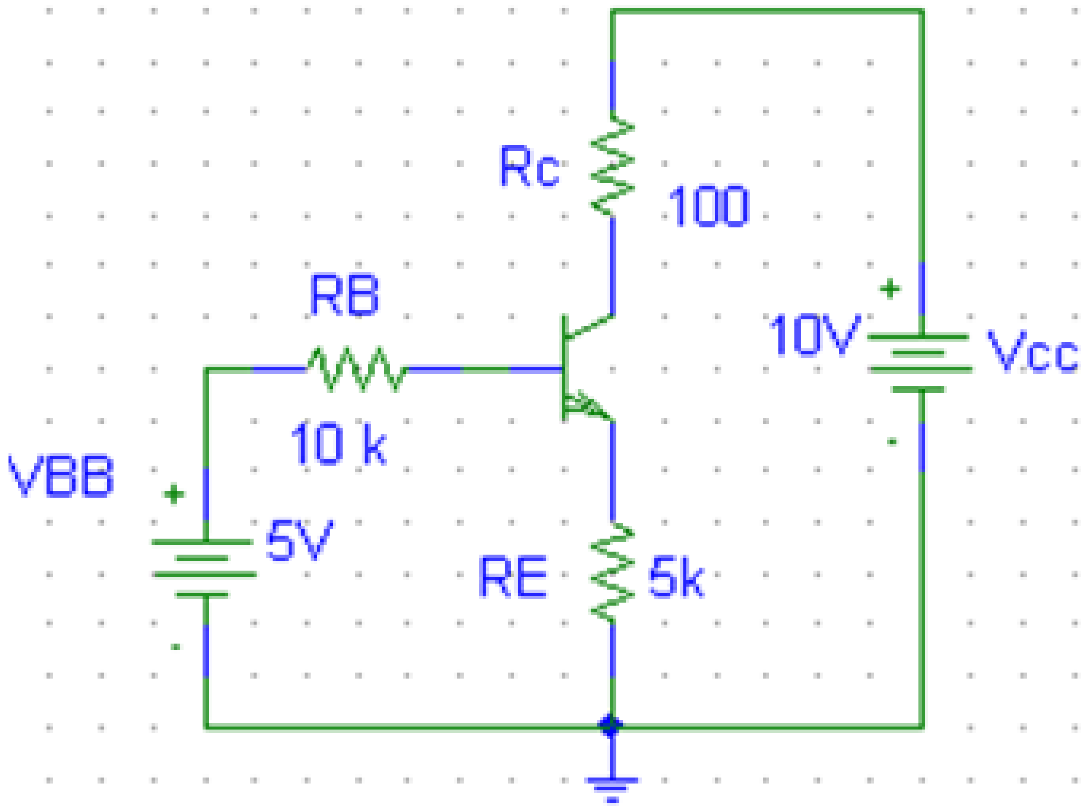
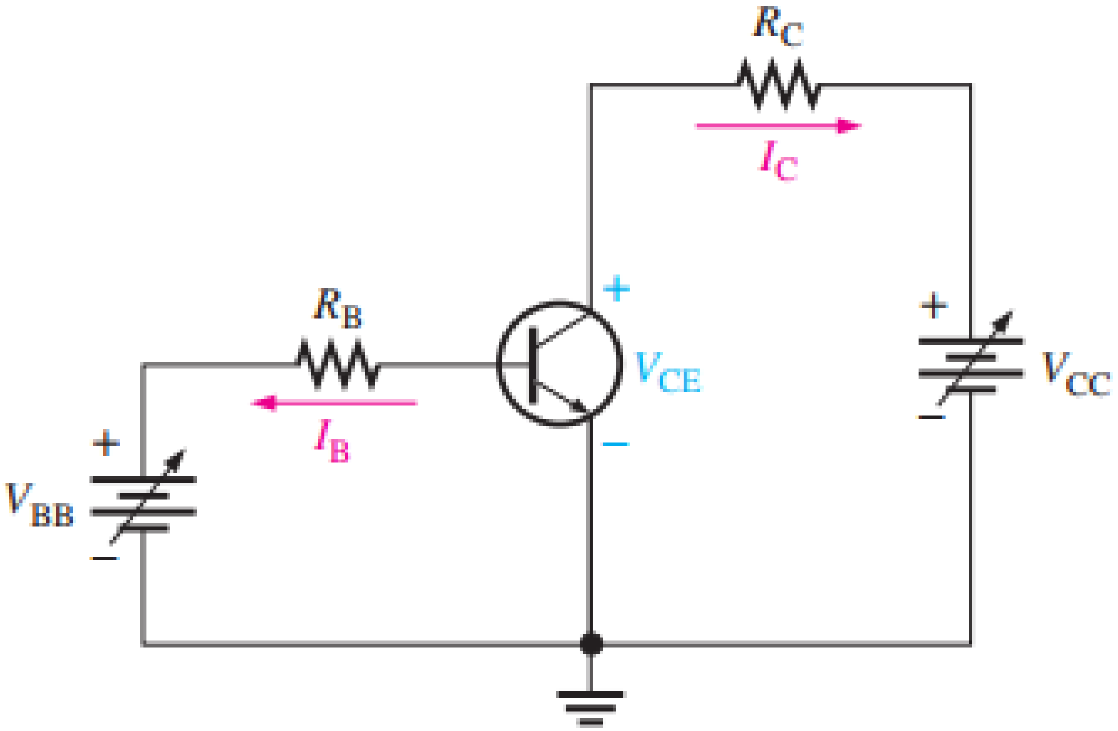
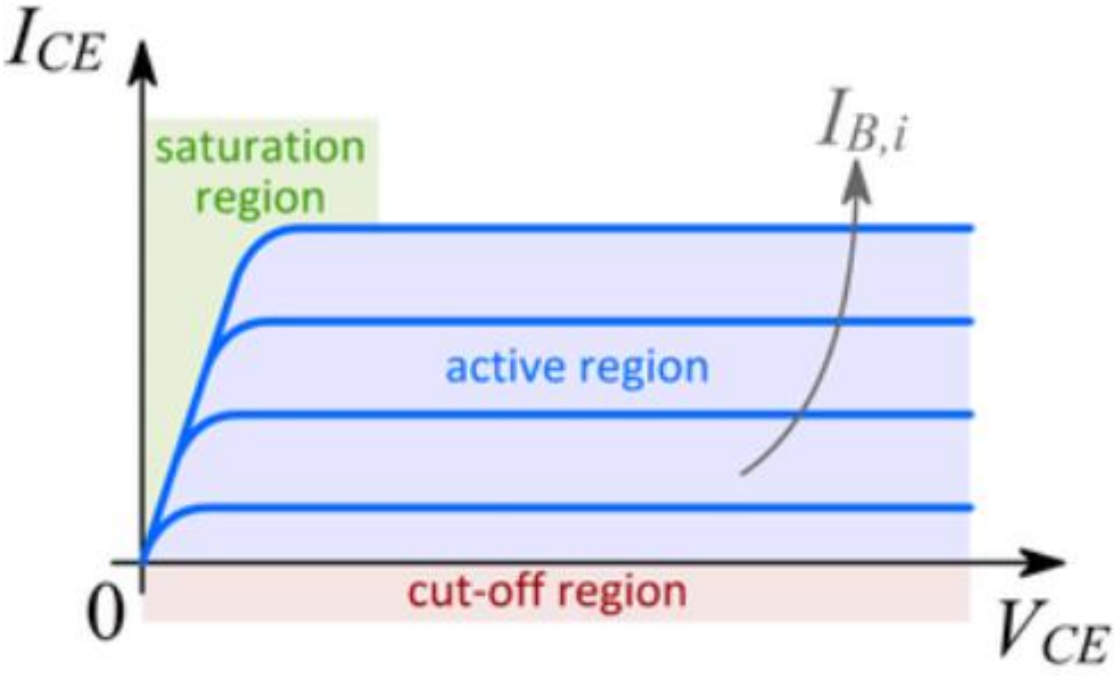


Home Work: Determine I_B, I_C, I_E, V_{BE}, V_{CE}, and V_{CB} in the circuit. Assume β_{DC} = 150.

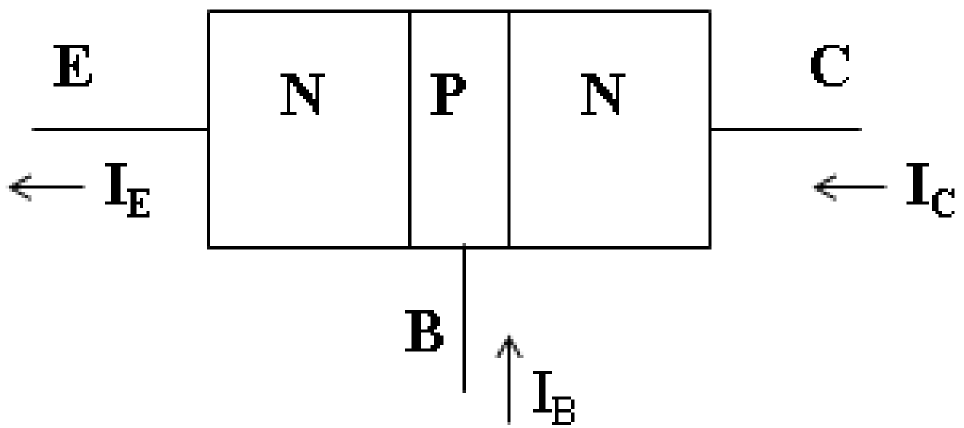


CHARACTERISTICS CURVES





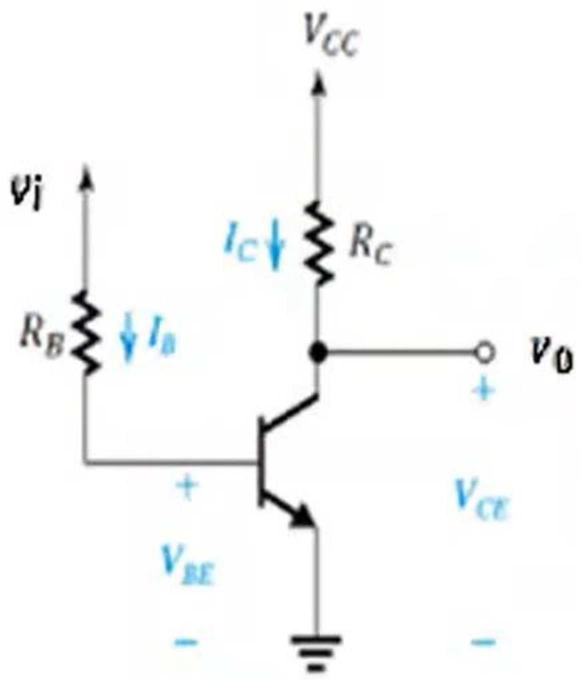
Modes of BJT Operation

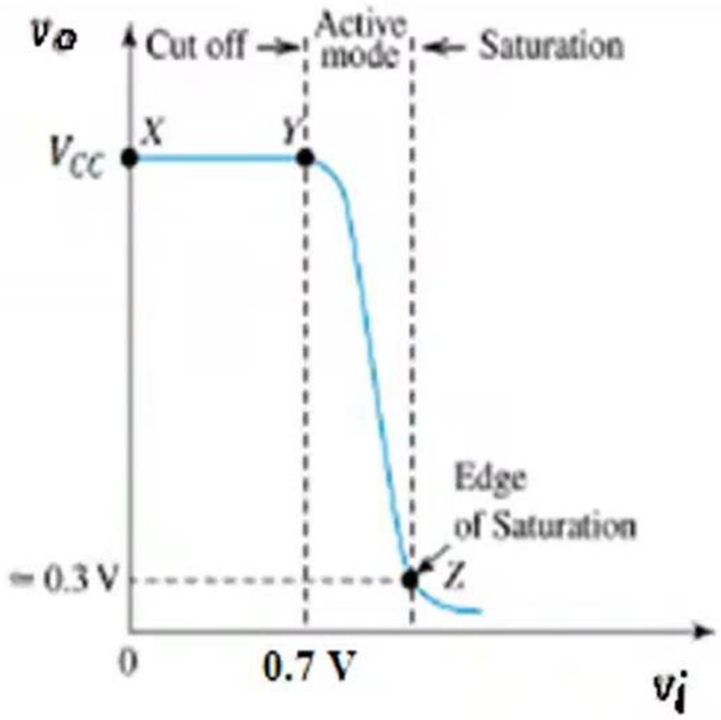


CB Junction	BE Junction	Mode of Operation
Reverse	Reverse	Cut-off
Forward	Reverse	Inverted
Reverse	Forward	Active
Forward	Forward	Saturation

Modes of Transistor Operation

Transistor operates in three regions:





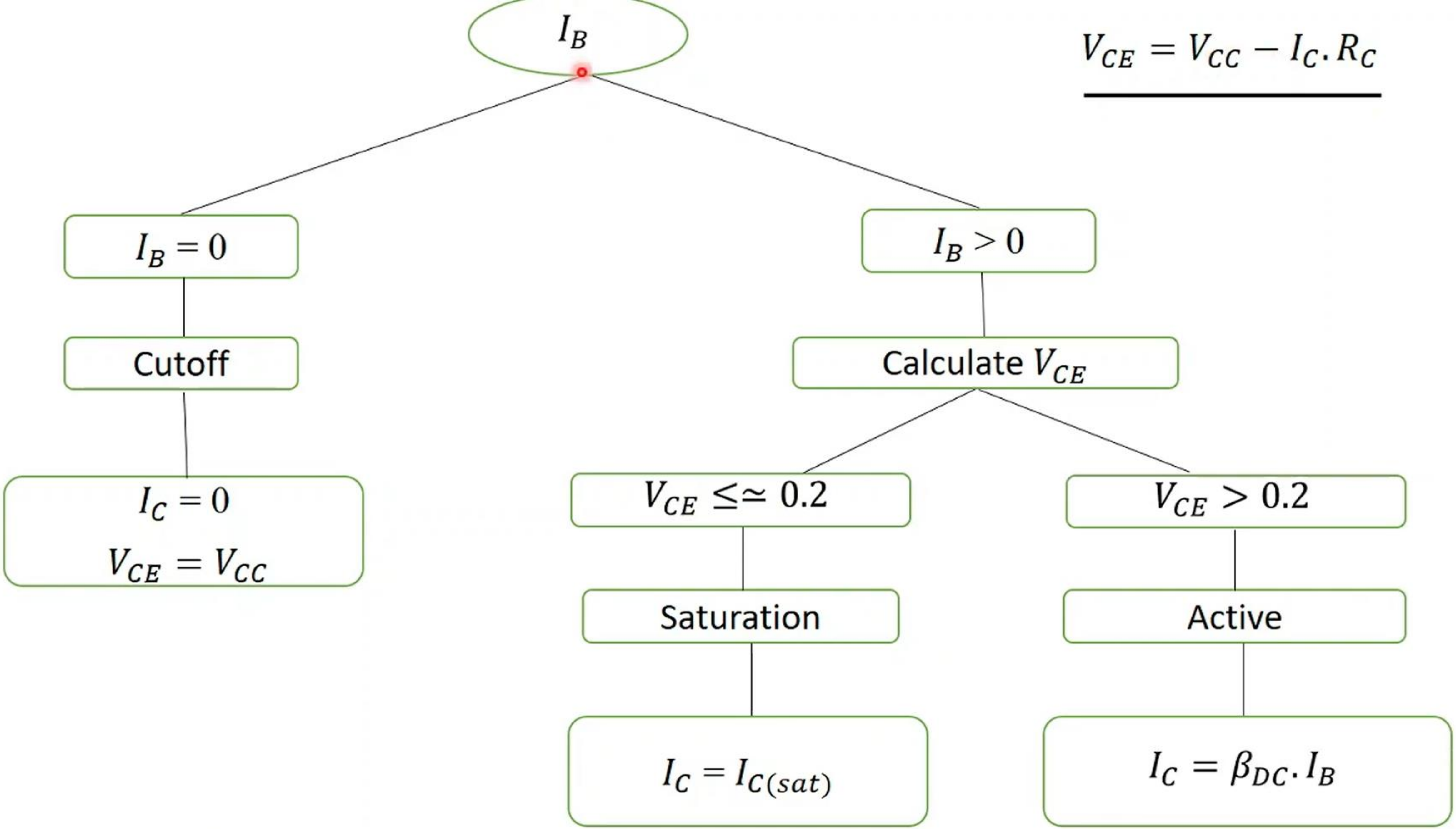
1. **Cutoff** : $I_B = 0$, $(V_{BE} < 0.7)$, $I_C = 0$, $V_{CE} = V_{CC}$

2. **Active** : I_B = average value , $I_C = \beta_{DC}.I_B$, $V_{CE} = V_{CC} - I_C.R_C$

3. **Saturation** : I_B = high value , $I_C = I_{C(sat)} = \frac{V_{CC}-V_{CE(sat)}}{R_C}$, $V_{CE(sat)} \simeq 0.2$ (for most types of transistor).

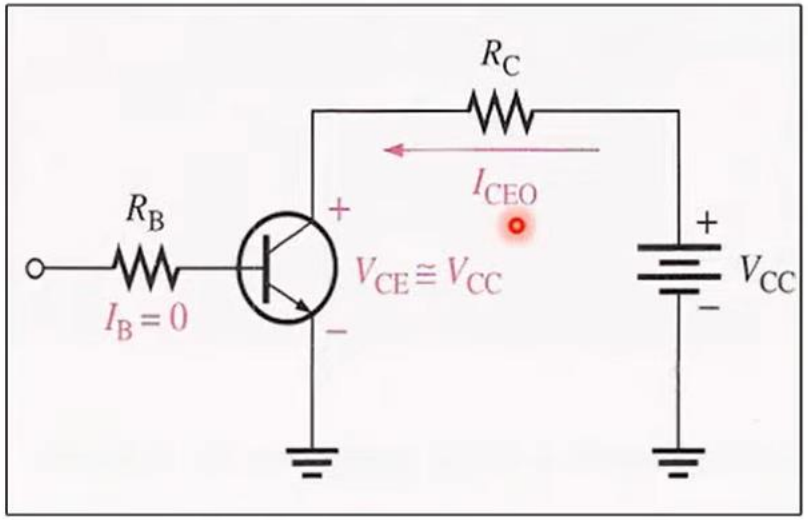
$$I_{B(\min)} = \frac{I_{C(sat)}}{\beta_{DC}}$$

$$V_{CE} = V_{CC} - I_C . R_C$$

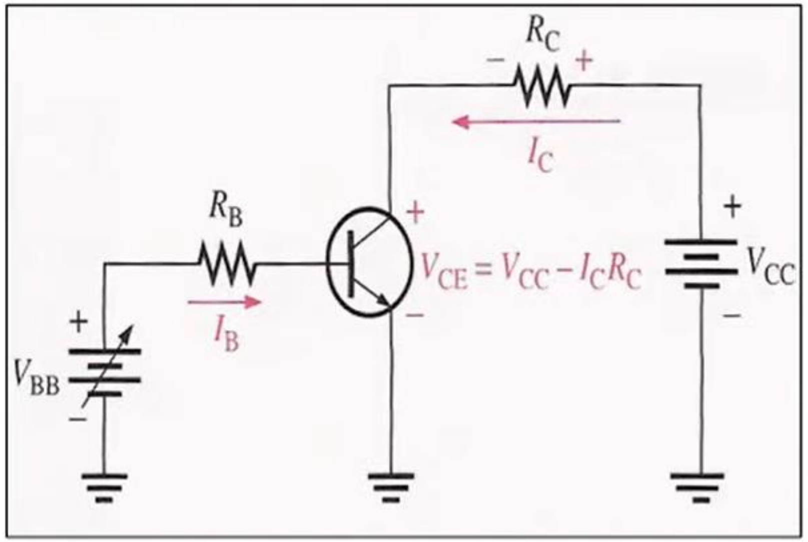


I_B
$I_B = 0$
Cutoff
$I_C = 0$
$V_{CE} = V_{CC}$
$I_B > 0$
Calculate V_{CE}
$V_{CE} \leq\simeq 0.2$
$V_{CE} > 0.2$
Saturation
Active
$I_C = I_{C(sat)}$
$I_C = \beta_{DC} . I_B$

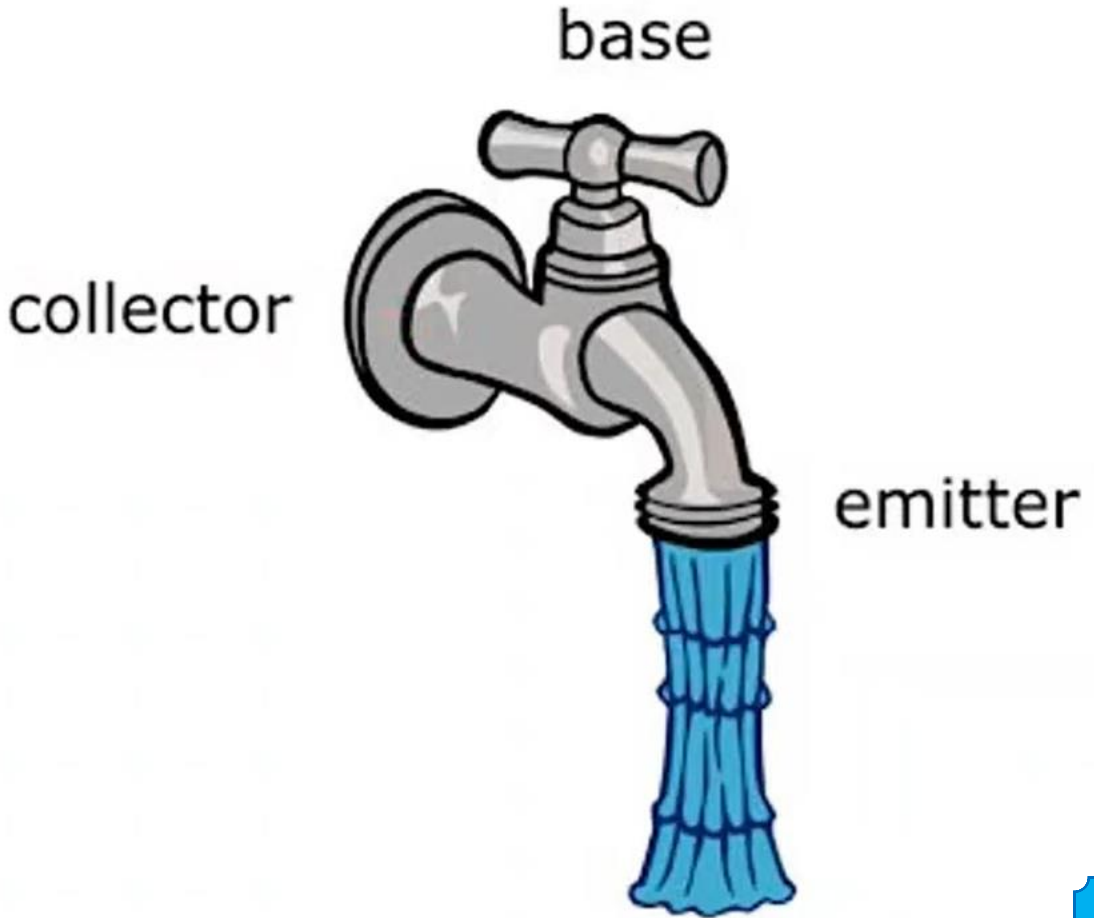
Cutoff



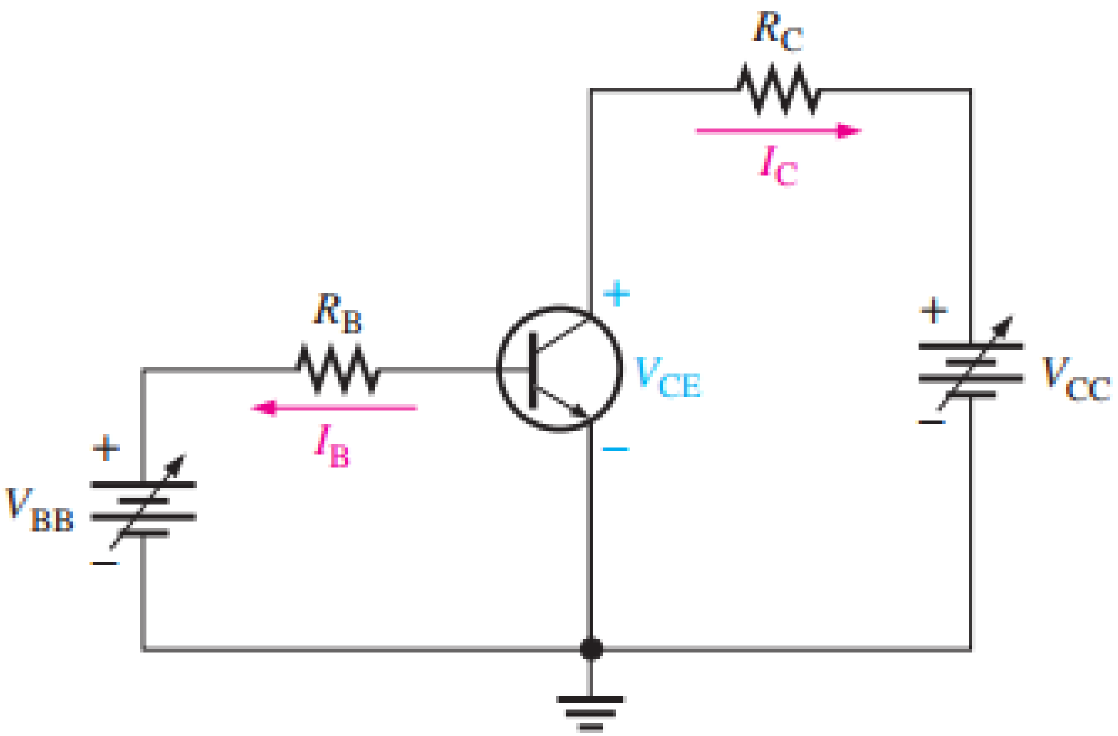
Saturation

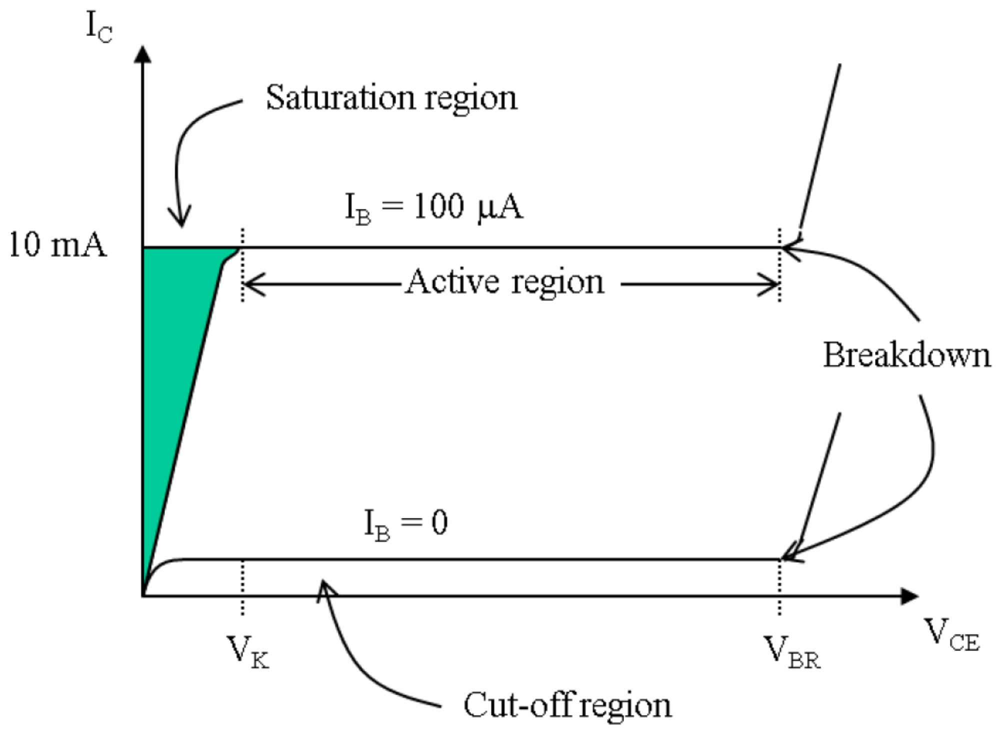


$$I_C = \beta_{DC}\, I_B$$

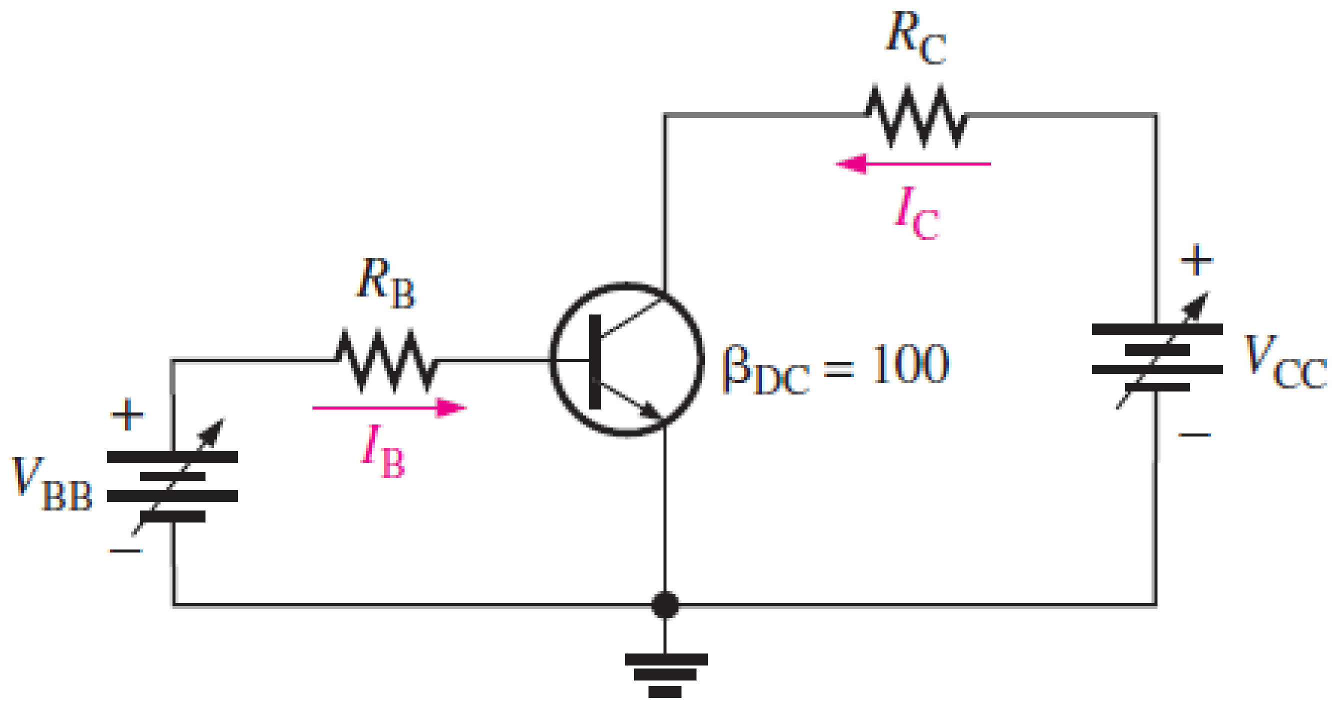


CHARACTERISTICS CURVES



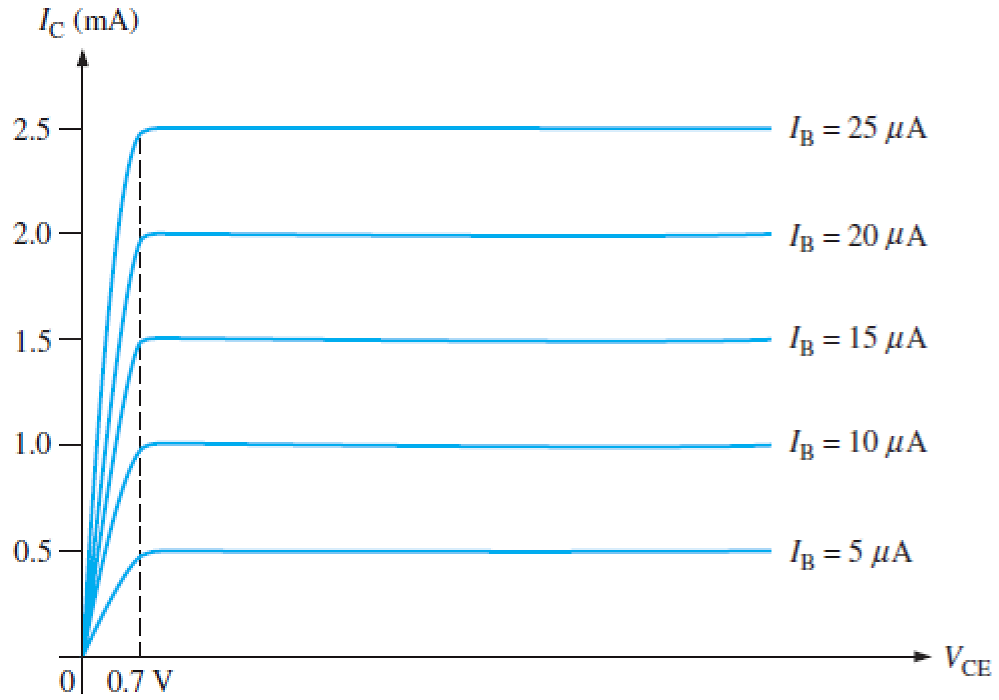


Example : Sketch an ideal family of collector curves for the circuit in Figure below , for I_B = 5 μA to 25 μA in 5 μA increments. Assume β_{DC} = 100 and that V_{CE} does not exceed breakdown

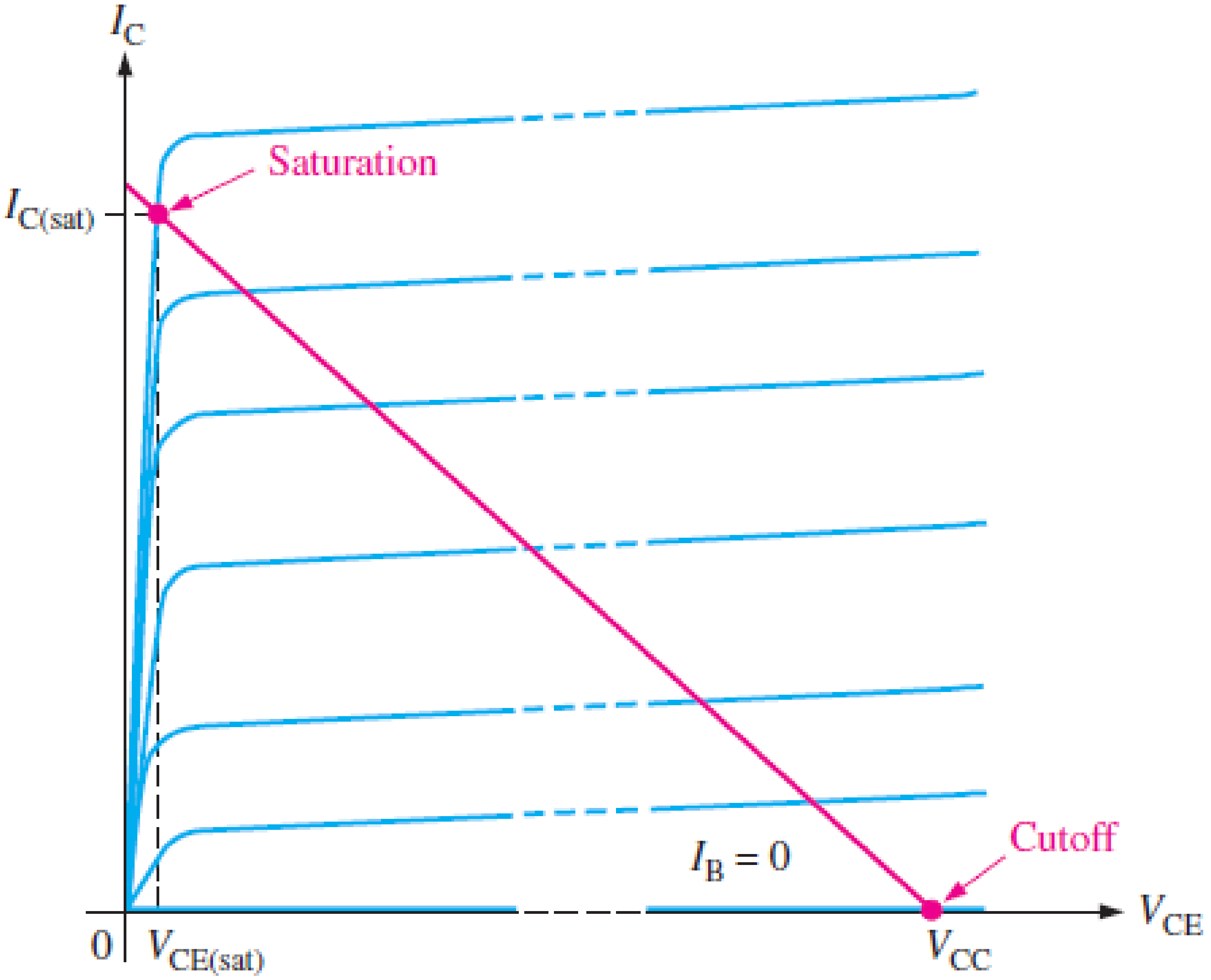


Solution:

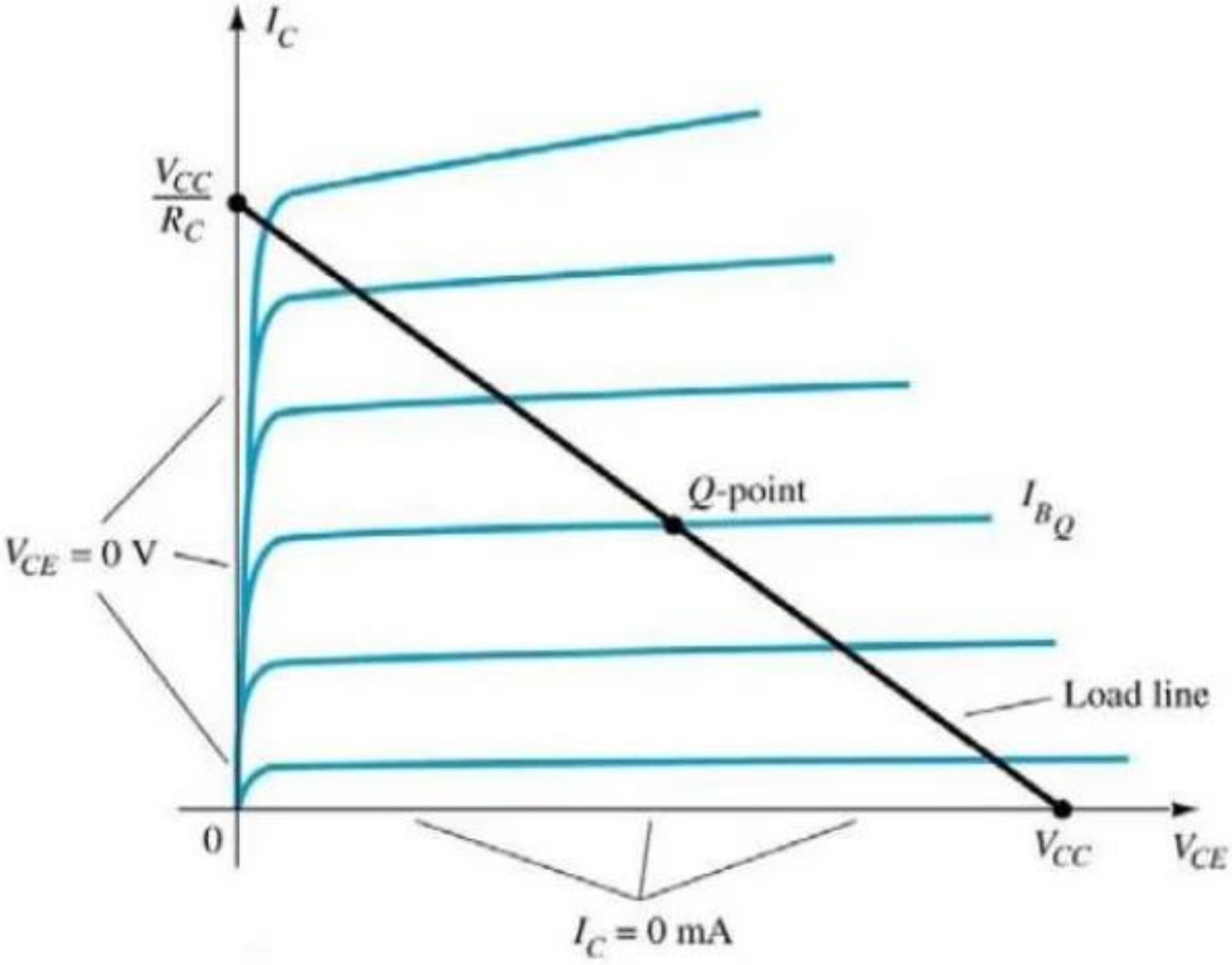
I_B	I_C
$5\,\mu A$	$0.5\,mA$
$10\,\mu A$	$1.0\,mA$
$15\,\mu A$	$1.5\,mA$
$20\,\mu A$	$2.0\,mA$
$25\,\mu A$	$2.5\,mA$



DC Load Line



Load Line Analysis



DC Load Line Analysis and Operation Point

An output equation that relates the variables I_C and V_{CE} in the following manner:

$$V_{CE} = V_{CC} - I_C R_C \dots\dots\dots\dots (1)$$

The load line is determined by two points:

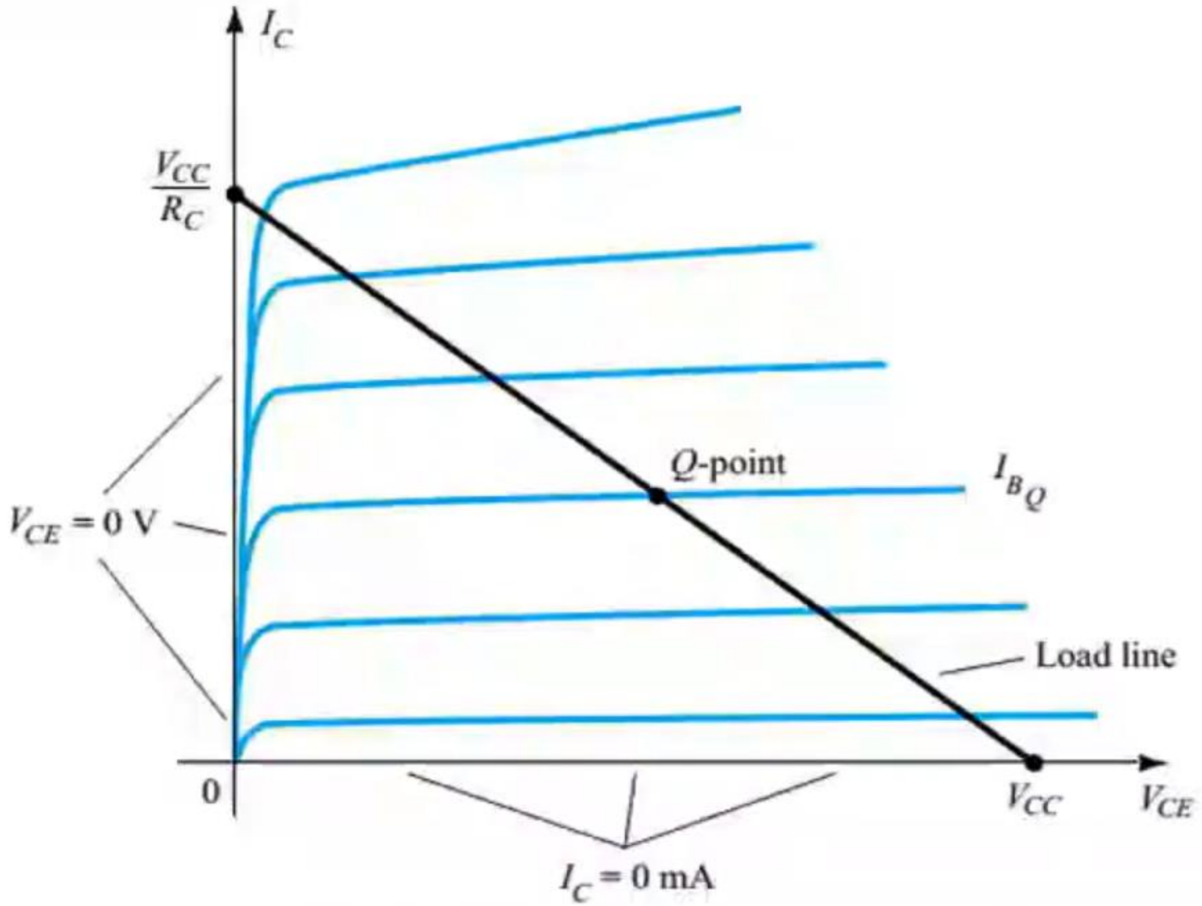
1) By substituting $I_C = 0$ mA into Eq. (1), we find that

$$V_{CE} = V_{CC} \quad \dots\dots\dots\dots (2)$$

2) By substituting $V_{CE} = 0$ mA into Eq. (1), we find that

$$0 = V_{CC} - I_C R_C$$

$$I_C = \frac{V_{CC}}{R_C} \quad \dots\dots\dots (3)$$



By joining the two points defined by Eqs. (2) and (3), the straight line can be drawn, which is called the **load line.**

The point at which the load line intersects a characteristic curve represents **the operating point** for that particular value of $I_{B\,Q}$. It is also called the *quiescent point* (abbreviated ***Q*-point**).

Load Line Analysis

The end points of the line are : I_{Csat} and V_{CE}cutoff

For load line analysis, use $V_{CE} = 0$ for I_{CSAT}, and $I_C = 0$ for $V_{CEcutoff}$

I_{Csat}:

$$I_{Csat} = \frac{V_{CC}}{R_C} \bigg|_{V_{CE} = 0V}$$

$V_{CEcutoff}$:

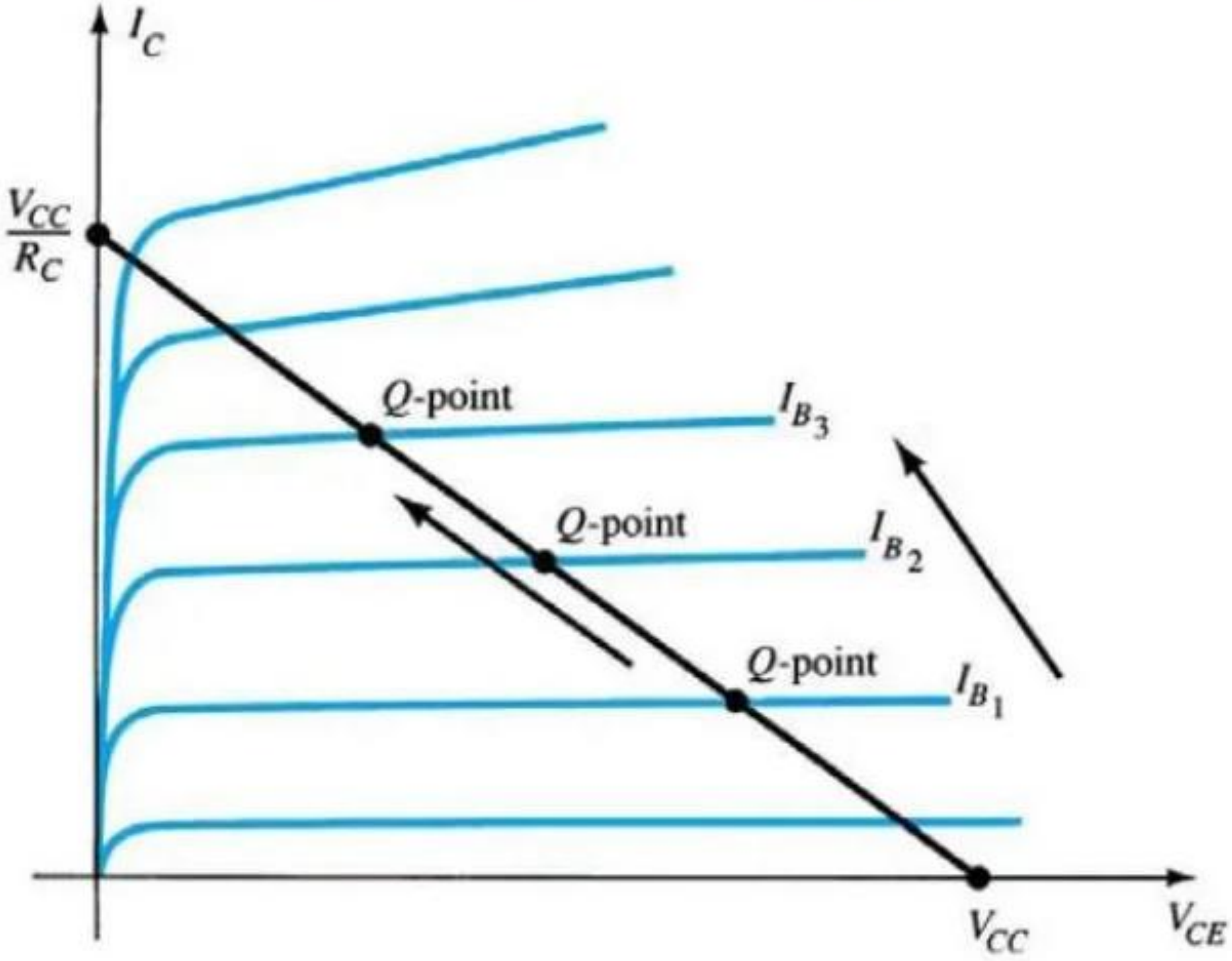
$$V_{CE} = V_{CC} \bigg|_{I_C = 0mA}$$

Where I_B intersects with the load line we have the Q point

Q-point is the particular operating point:

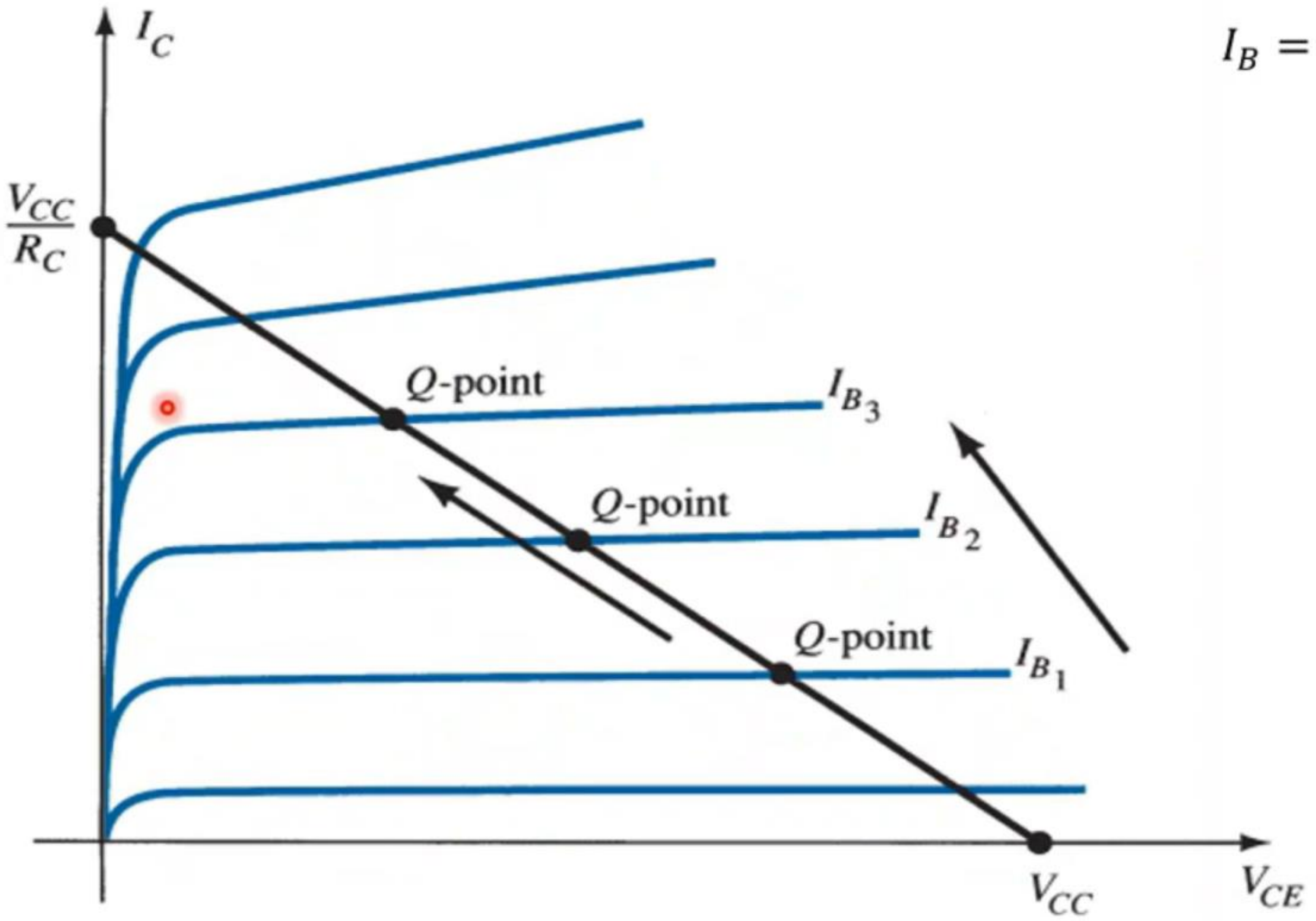
- Value of R_B
- Sets the value of I_B
- Where I_B and Load Line intersect
- Sets the values of V_{CE} and I_C.

Circuit values effect Q-point

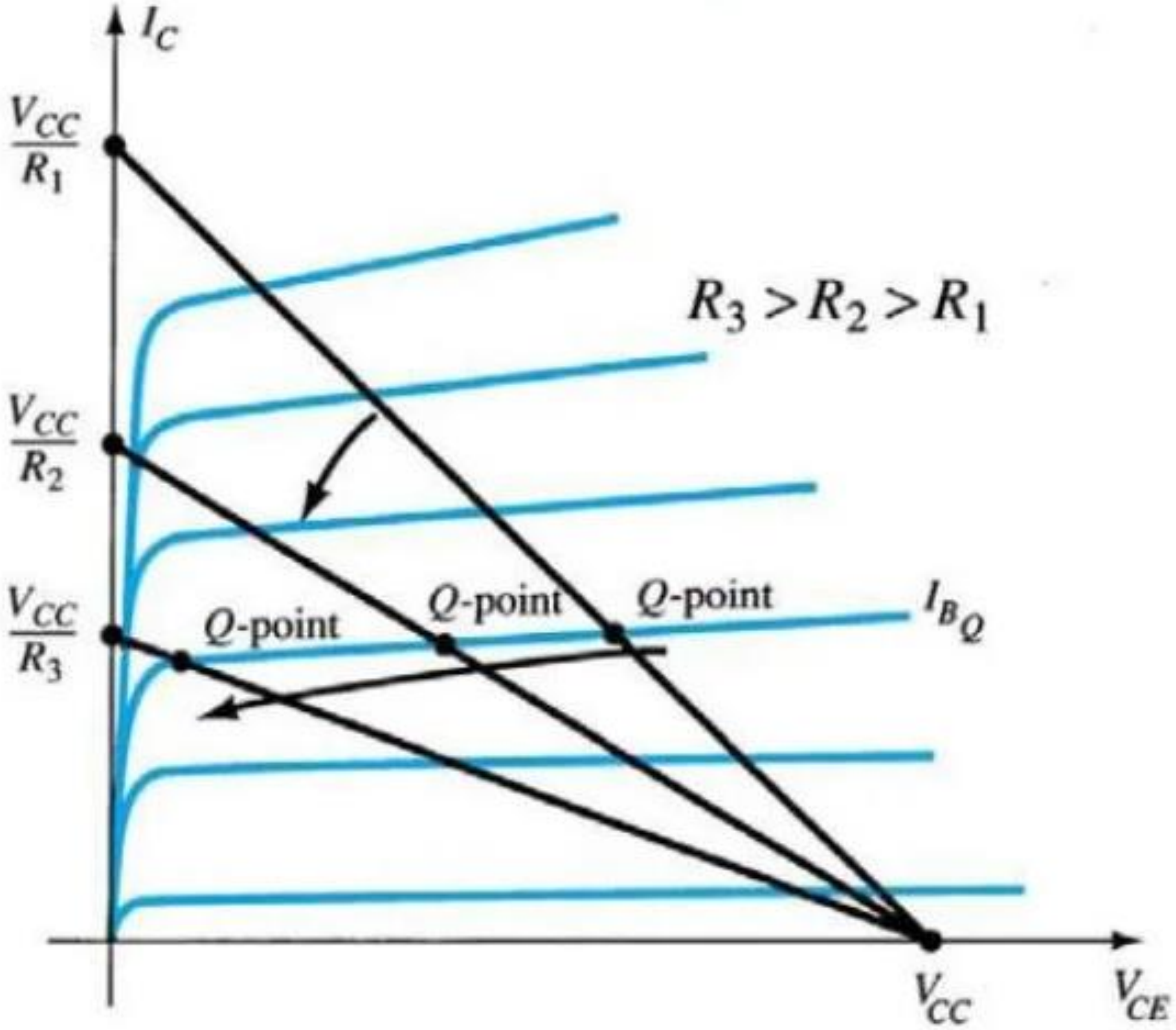


If the level of I_B is changed by varying the value of R_B or V_{BB}, the Q-point moves up or down the load line as shown in Figure for increasing values of I_B.

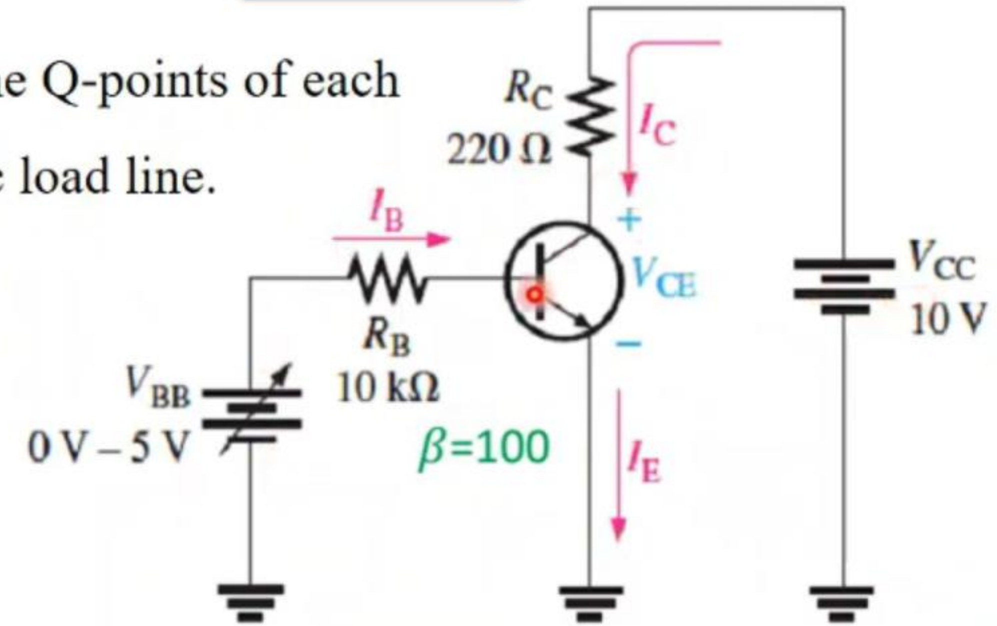
$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$



Circuit values effect Q-point (continued)



Example 1: For the transistor circuit shown in Figure. Determine the Q-points of each value of $I_B = 200\ \mu A$, $I_B = 300\ \mu A$ and $I_B = 400\ \mu A$. Also draw the dc load line.



Solution:

1) $I_B = 200\ \mu A$, Q_1 point is

$$I_C = \beta . I_B = (100)(200\mu A) = 20\ \text{mA}$$

$$V_{CE} = V_{CC} - I_C . R_C = 10V - (20\ mA)(220\Omega) = 5.6V$$

2) $I_B = 300\ \mu A$, Q_2 point is

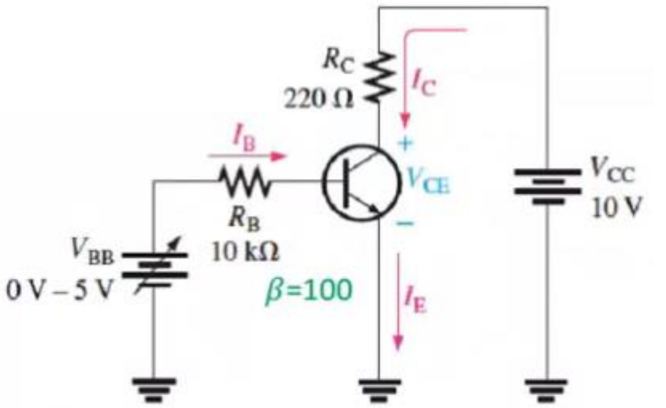
$$I_C = \beta . I_B = (100)(300\mu A) = 30\ \text{mA}$$

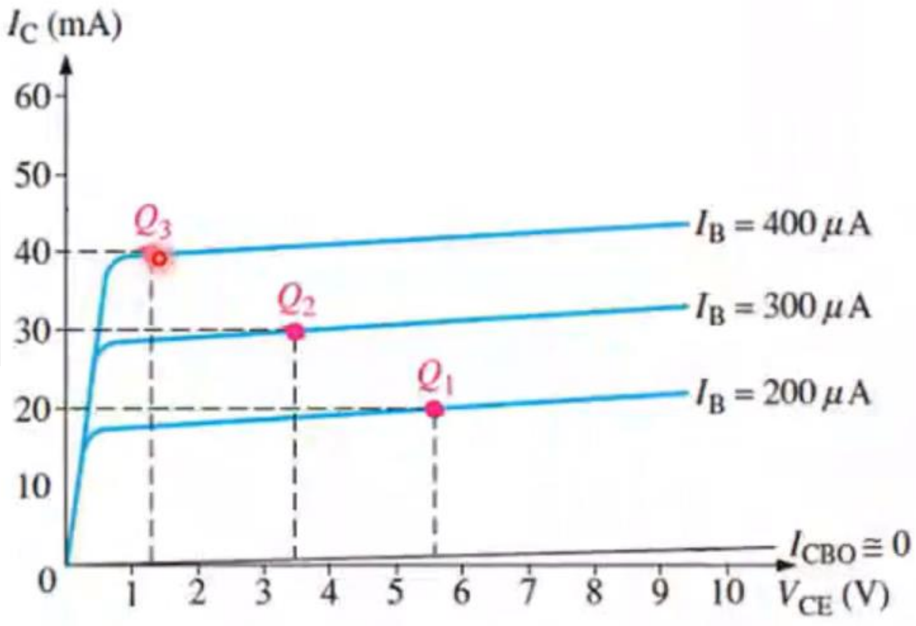
$$V_{CE} = V_{CC} - I_C . R_C = 10V - (30\ mA)(220\Omega) = 3.4V$$

3) $I_B = 400\ \mu A$, Q_3 point is

$$I_C = \beta . I_B = (100)(400\mu A) = 40\ \text{mA}$$

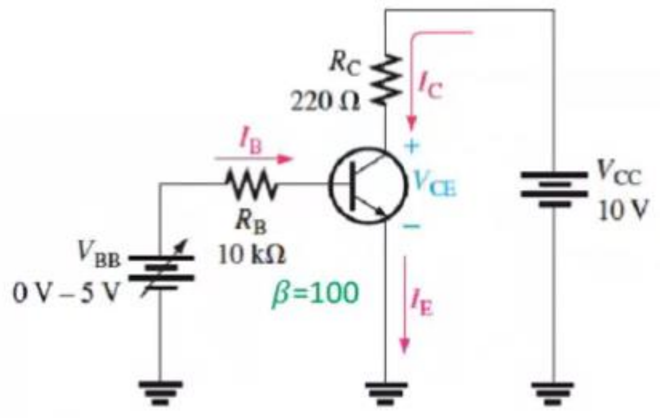
$$V_{CE} = V_{CC} - I_C . R_C = 10V - (40\ mA)(220\Omega) = 1.2V$$





D.C. load line: In order to draw the dc load line, we need two end points.

$$V_{CE} = V_{CC} - I_C R_C$$

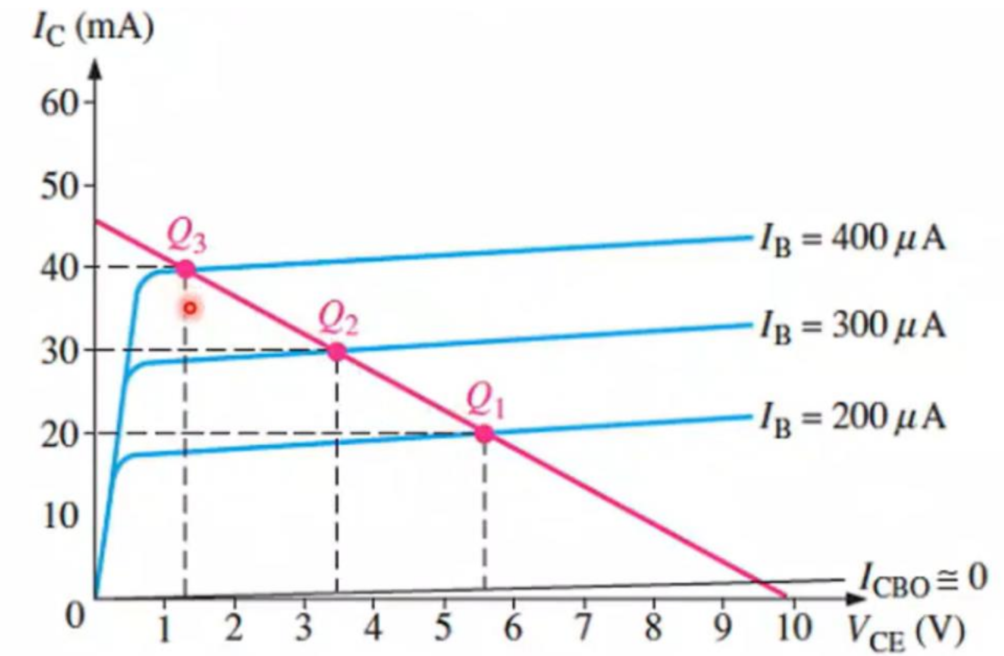


First, $I_C = 0$,

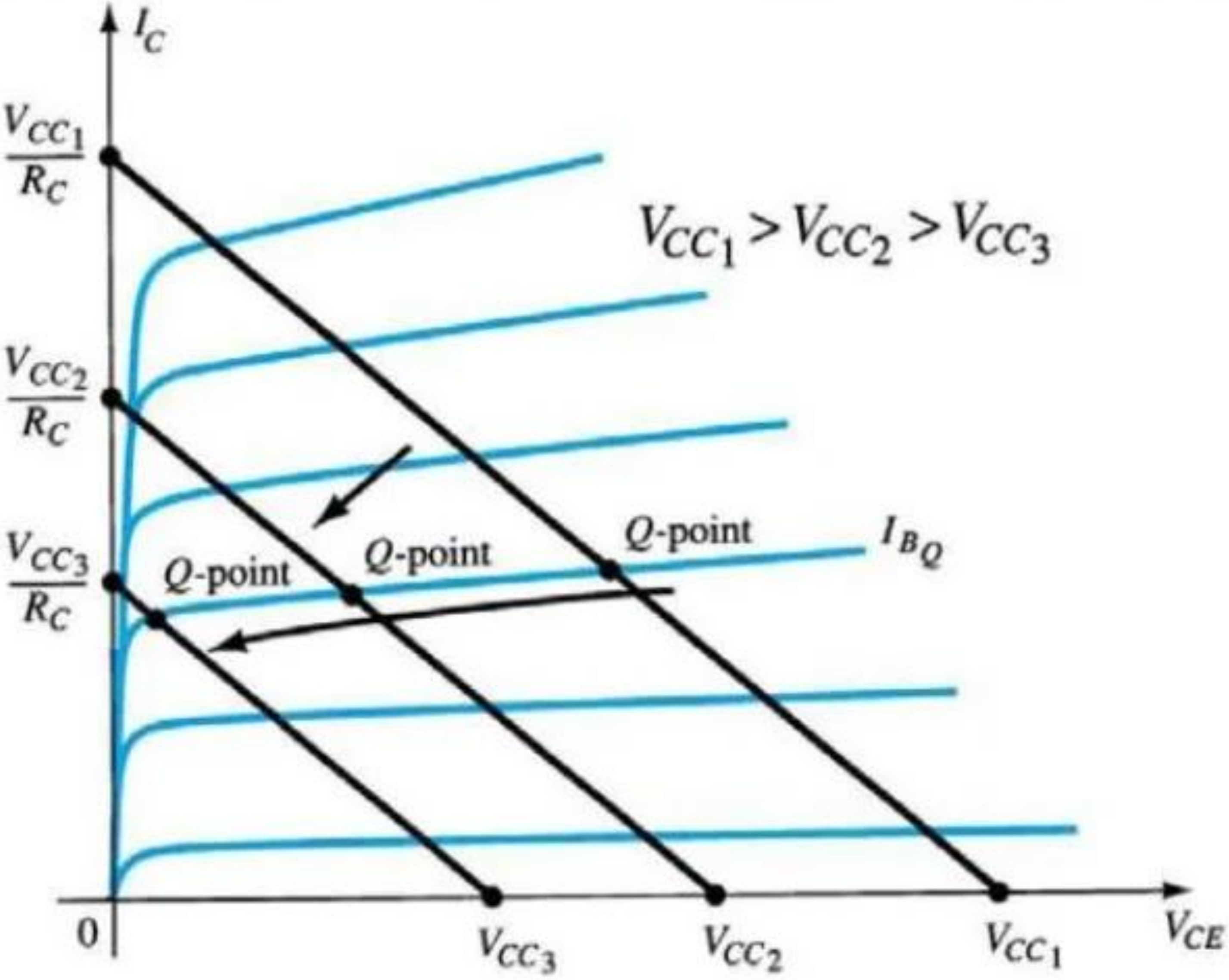
$$V_{CE} = V_{CC} = 10\text{V}.$$

Second, $V_{CE} = 0$,

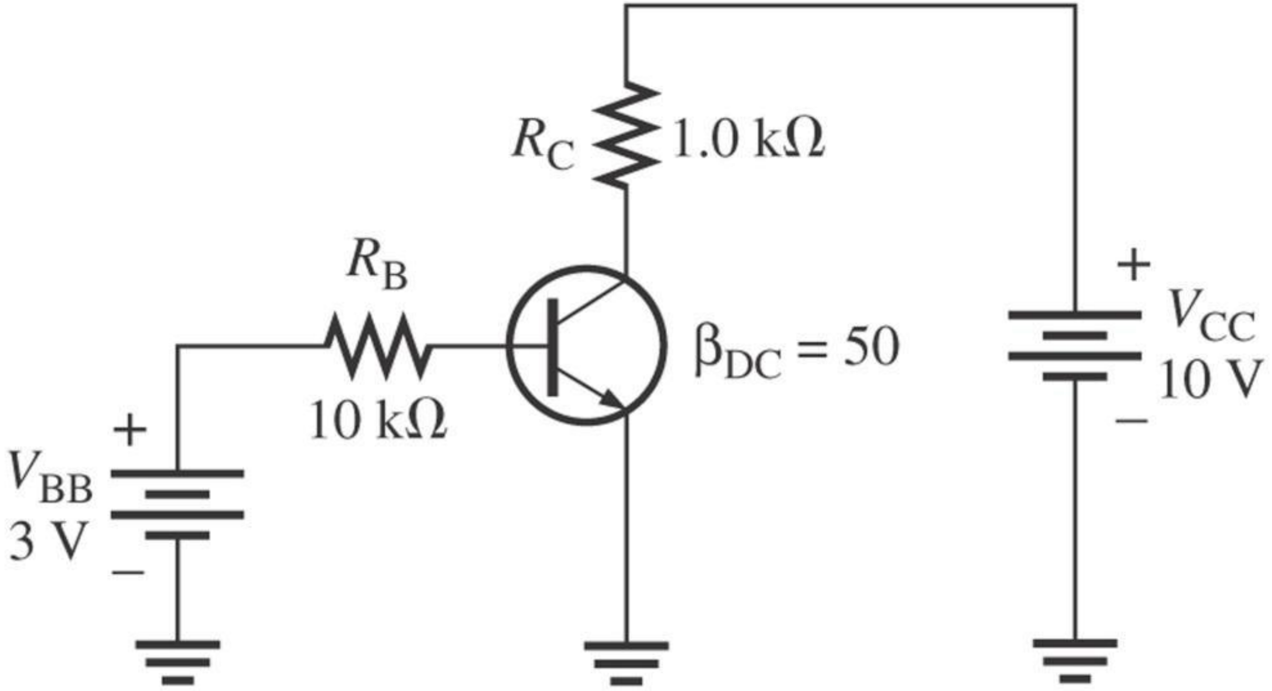
$$I_C = \frac{V_{CC}}{R_C} = \frac{10}{220} = 45.5\ mA$$



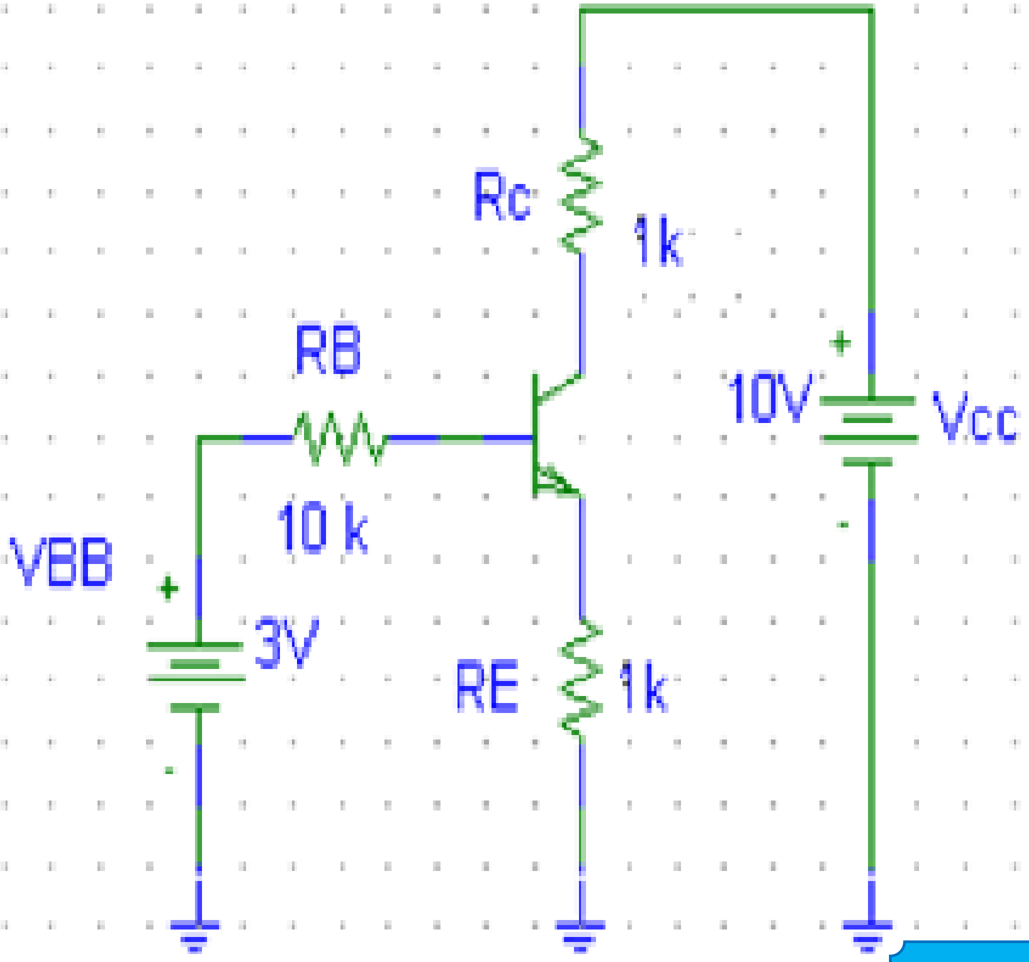
Circuit values effect Q-point (continued)



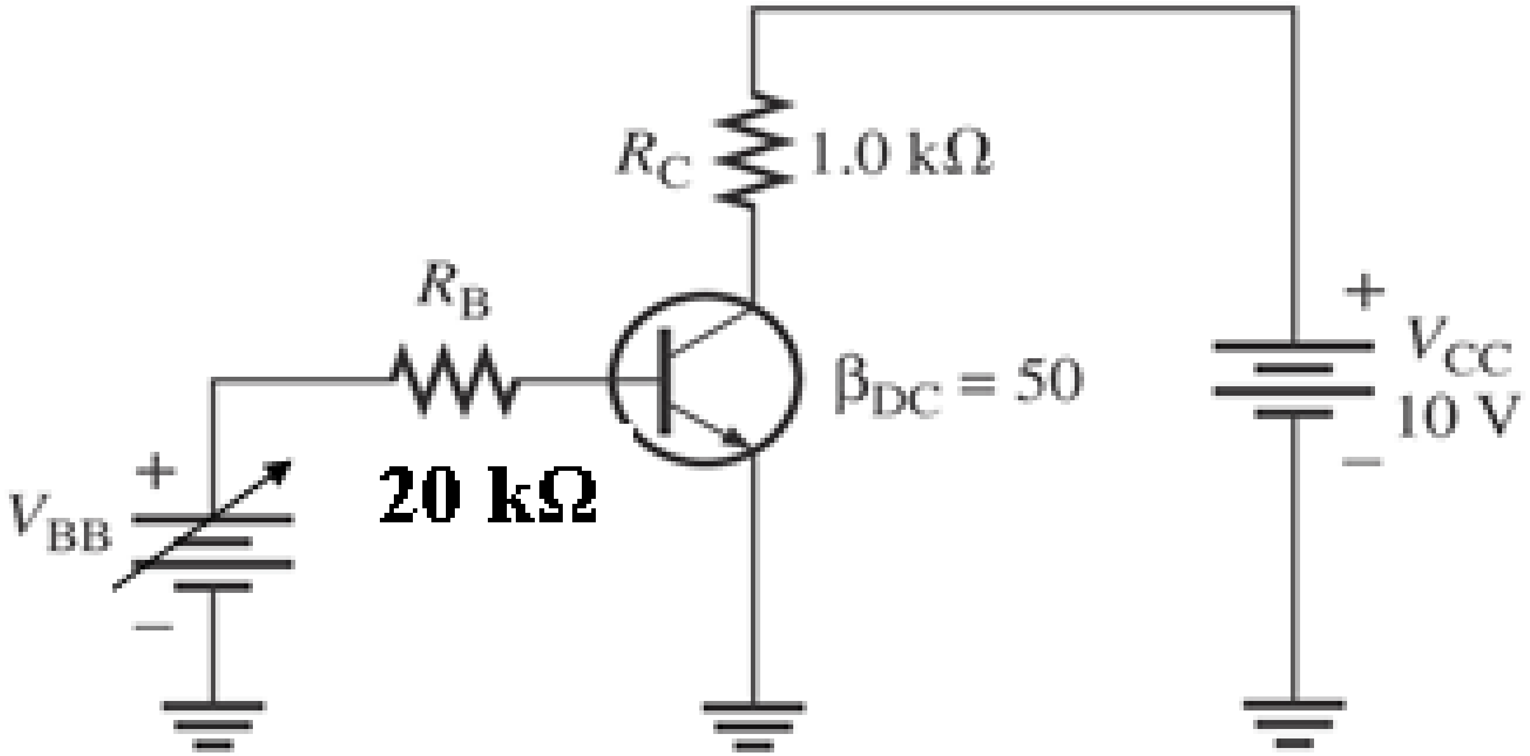
Example : Determine whether or not the transistor in Figure below is in saturation. Assume $V_{CE(sat)} = 0.2$ V.



Example 7: Determine whether or not the transistor in Figure 21 is in saturation. Assume $V_{CE(sat)} = 0.2$ V. $\beta_{DC}=50$.



Home work: Find Q-point when V_{BB} = 1V, 2 V and 3 V. And then construct DC load line for this transistor. Assume $V_{CE(sat)}$ = 0 V.



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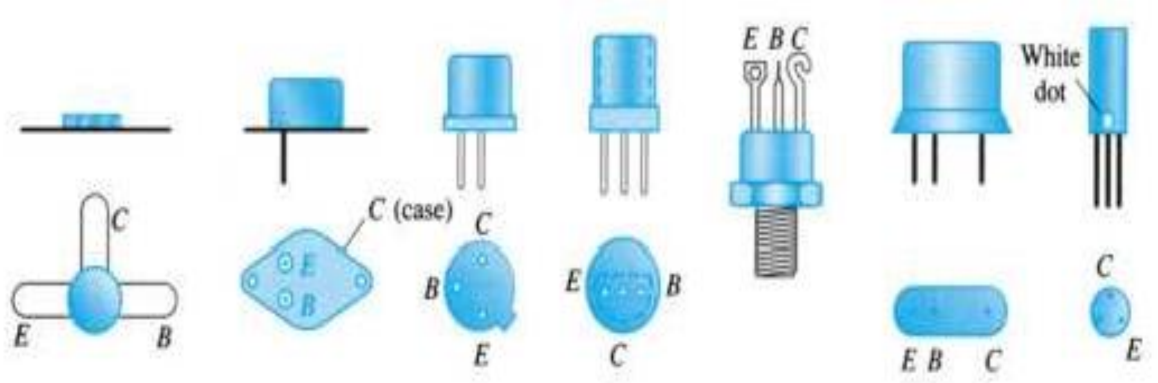
Electronic I
Lecture 3

BJT Biasing Circuits



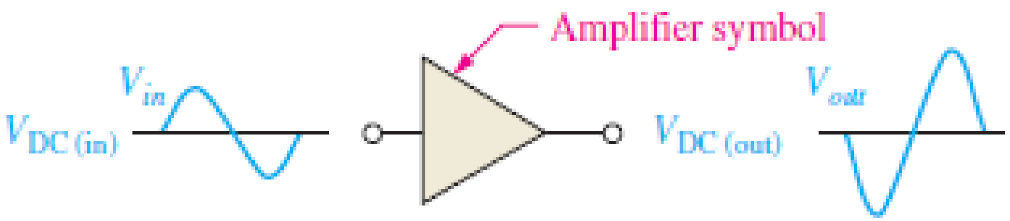
2nd Class

by
Rafal Raed Mahmood Alshaker

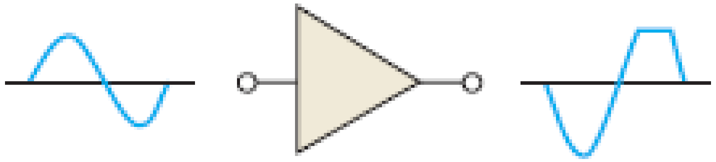
Outline of Presentation

1	• **The DC Operation Point**
2	• **Linear Operation:**
3	• **Waveform Distortion:**
4 Transistor Biasing	• Base Bias • Emitter Bias • Voltage Divider Bias

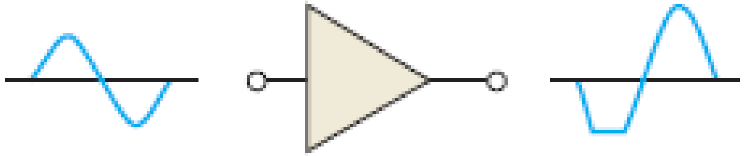
The DC Operation Point



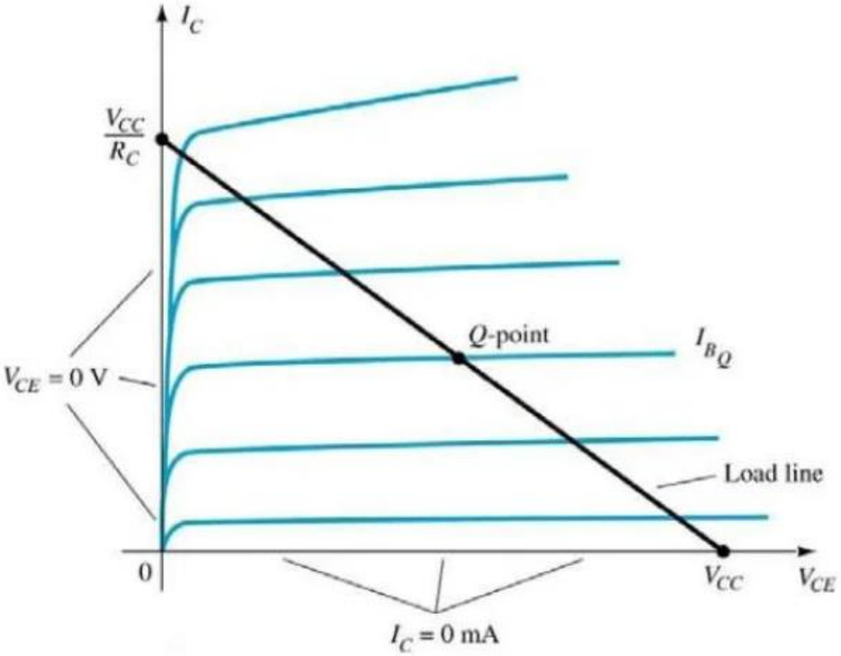
(a) Linear operation: larger output has same shape as input except that it is inverted



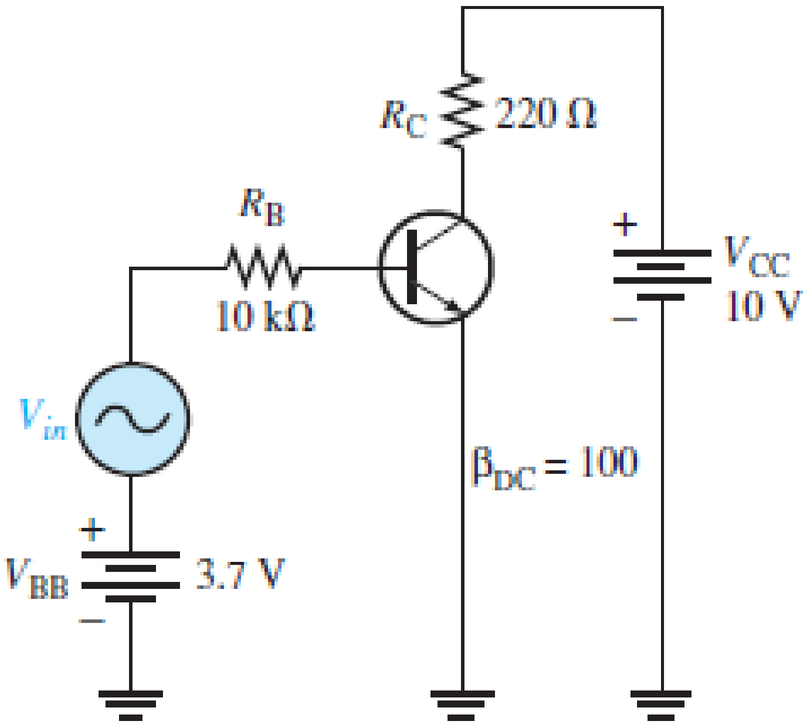
(b) Nonlinear operation: output voltage limited (clipped) by cutoff



(c) Nonlinear operation: output voltage limited (clipped) by saturation



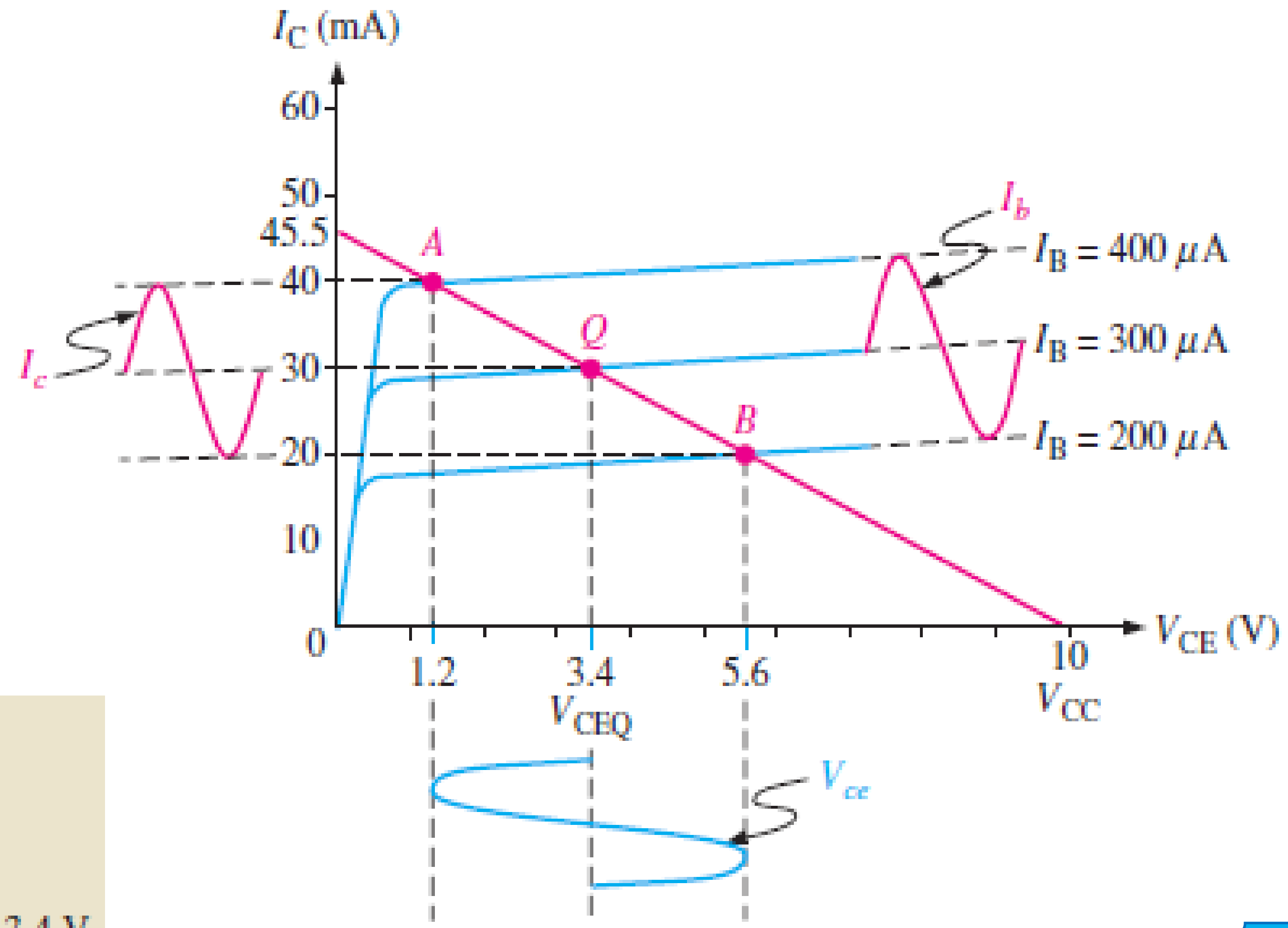
Linear Operation:



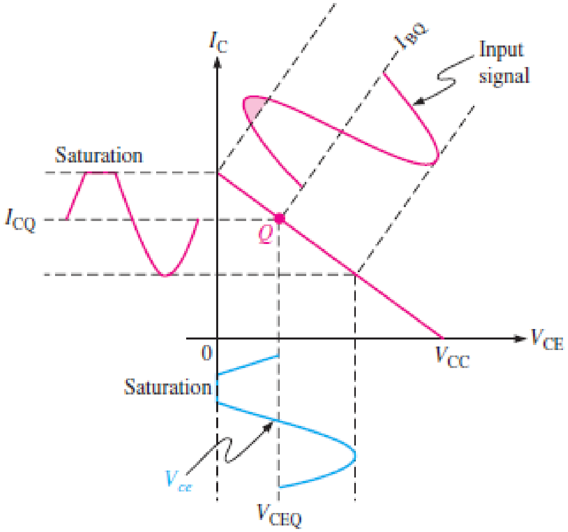
$$I_{BQ} = \frac{V_{BB} - 0.7\text{ V}}{R_B} = \frac{3.7\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega} = 300\ \mu\text{A}$$

$$I_{CQ} = \beta_{DC} I_{BQ} = (100)(300\ \mu\text{A}) = 30\text{ mA}$$

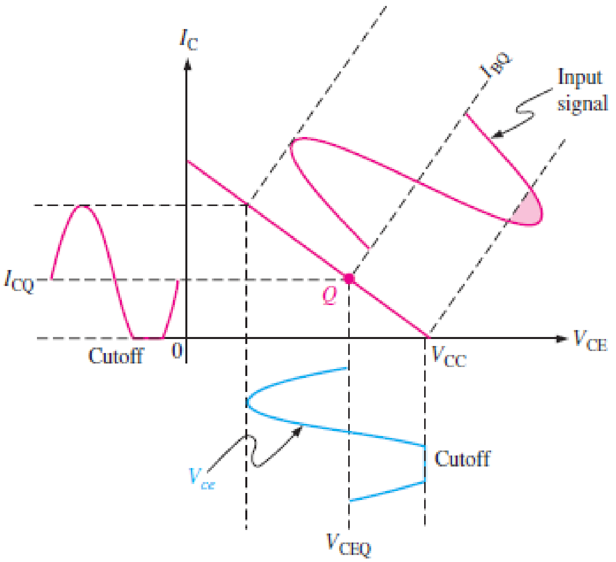
$$V_{CEQ} = V_{CC} - I_{CQ}R_C = 10\text{ V} - (30\text{ mA})(220\ \Omega) = 3.4\text{ V}$$



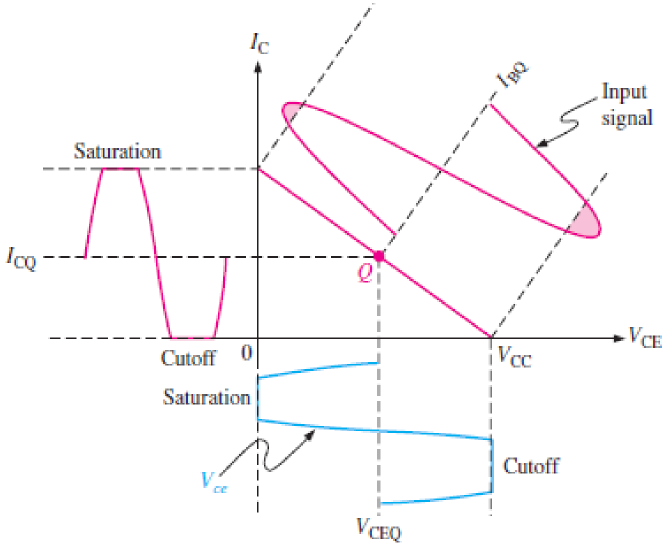
Waveform Distortion:



(a) Transistor is driven into saturation because the Q-point is too close to saturation for the given input signal.

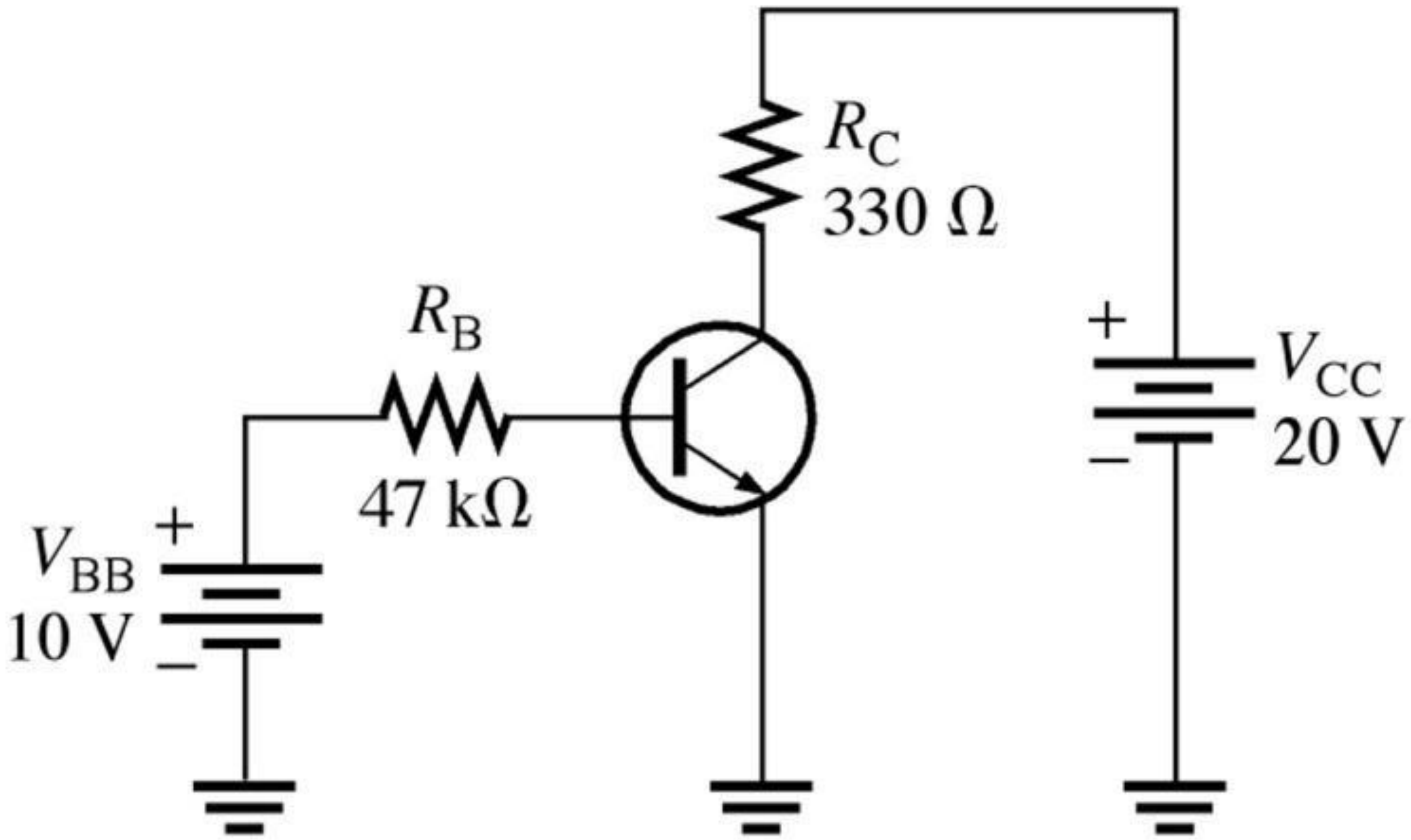


(b) Transistor is driven into cutoff because the Q-point is too close to cutoff for the given input signal.



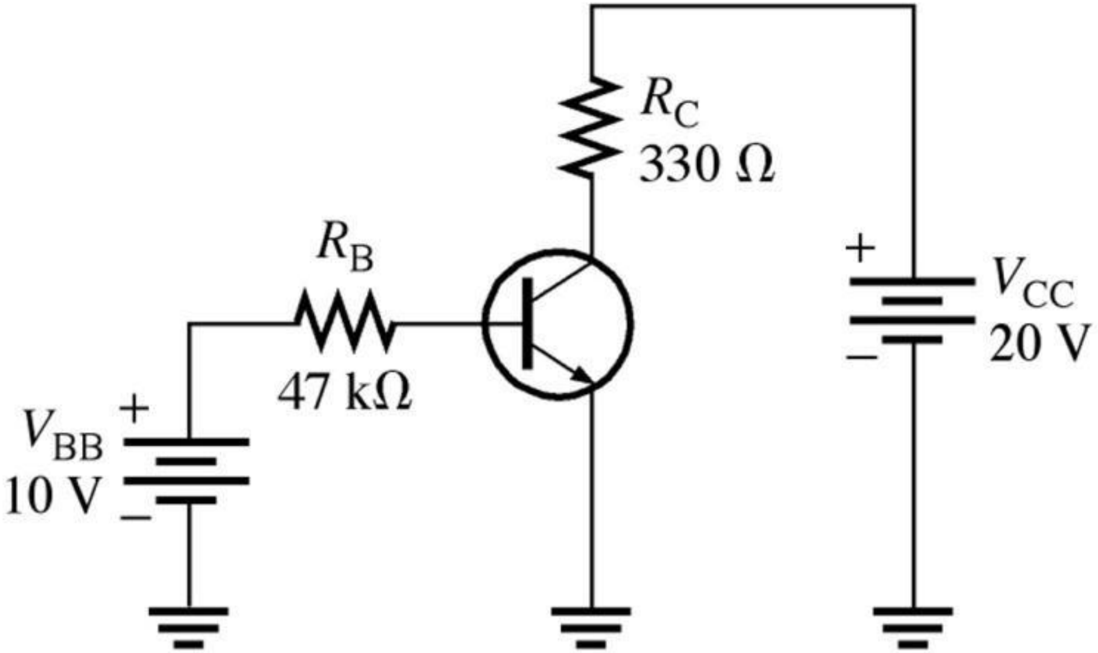
(c) Transistor is driven into both saturation and cutoff because the input signal is too large.

Example 1: Determine the Q-point and find the maximum peak value of the base current for linear operation. Assume $\beta_{DC} = 200$.



Example 1: Determine the Q-point and find the maximum peak value of the base current for linear operation. Assume $\beta_{DC} = 200$.

Solution:



The Q-point is defined by I_C and V_{CE}

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{10V - 0.7V}{47K\Omega} = 198\mu A = I_{BQ}$$

$$I_C = \beta_{DC} I_B = (200)(198\mu A) = 39.6mA = I_{CQ}$$

$$V_{CE} = V_{CC} - I_C R_C = 20V - 13.07$$

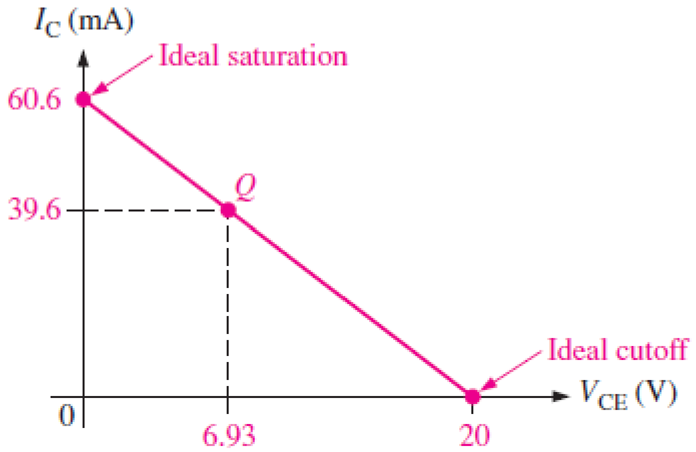
$$= 6.93V = V_{CEQ}$$

$$*I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{20V}{330\Omega}$$

$$*I_{C(\text{cut off})} = 0$$

$$I_{C(sat)} - I_{CQ} = 60.6 - 39.6 = 21mA$$

$$I_{CQ} - I_{C(\text{cut off})} = 39.6 - 0 = 39.6mA$$

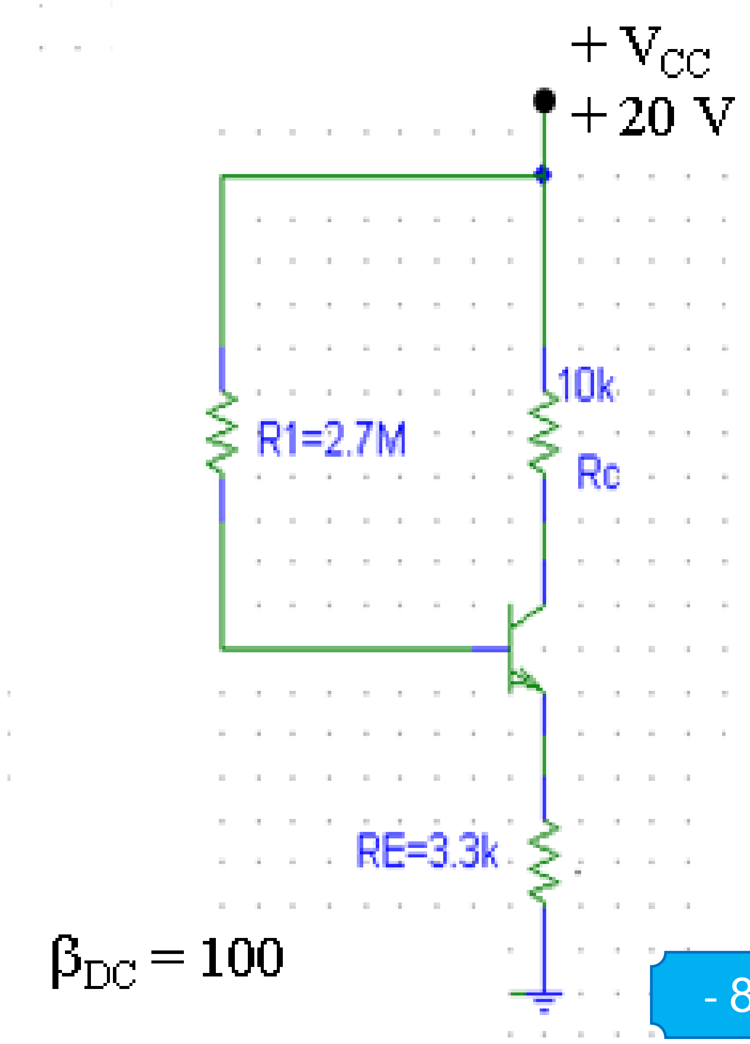


$\therefore$ Q-point is in closer to saturation than the cutoff

$\therefore$ $21mA$ is the maximum peak variation ($I_{C(max)}$) of the collector curent

$$\therefore I_{b(peak)} = \frac{I_{C(peak)}}{\beta_{DC}} = \frac{21mA}{200} = 105\mu A \_\_\_\_\#$$

H.W: Determine the Q-point values of I_C and V_{CE} for the circuit in the Figure below
Find $I_{C(sat)}$ and $V_{CE(cut\ off)}$, and then construct the load line and plot the Q-point.
** Assume $I_C = I_E$ to find $I_{C(sat)}$ and $V_{CE(cut\ off)}$



Transistor Biasing is the process of setting a transistors DC operating voltage or current conditions to the correct level so that AC input signal can be amplified correctly by the transistor.

DC Biasing

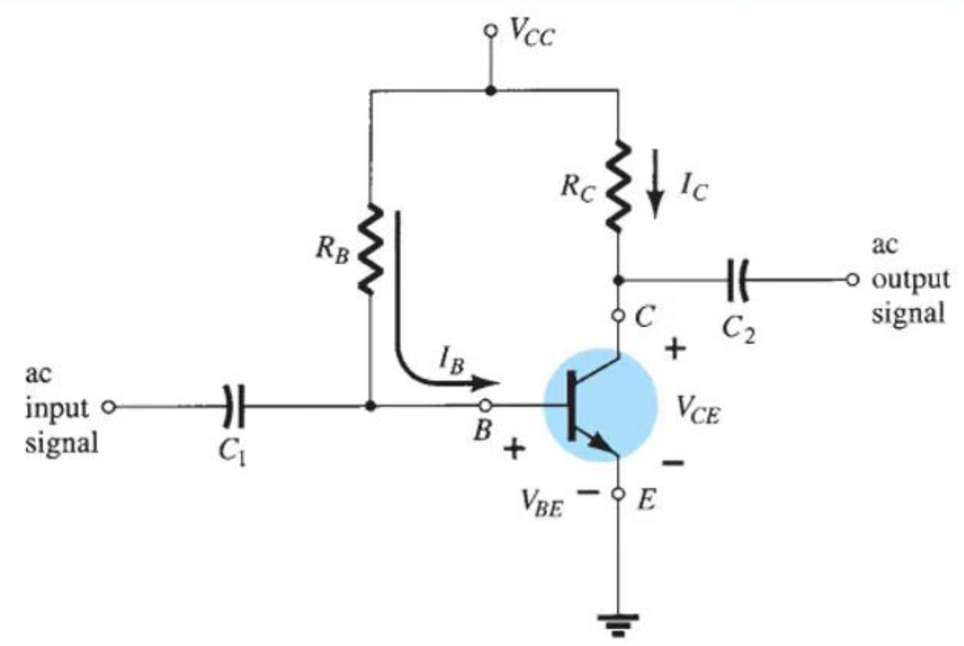
- Be able to determine the dc levels for the variety of important BJT configurations.

- Understand how to measure the important voltage levels of a BJT transistor configuration and use them to determine whether the network is operating properly.

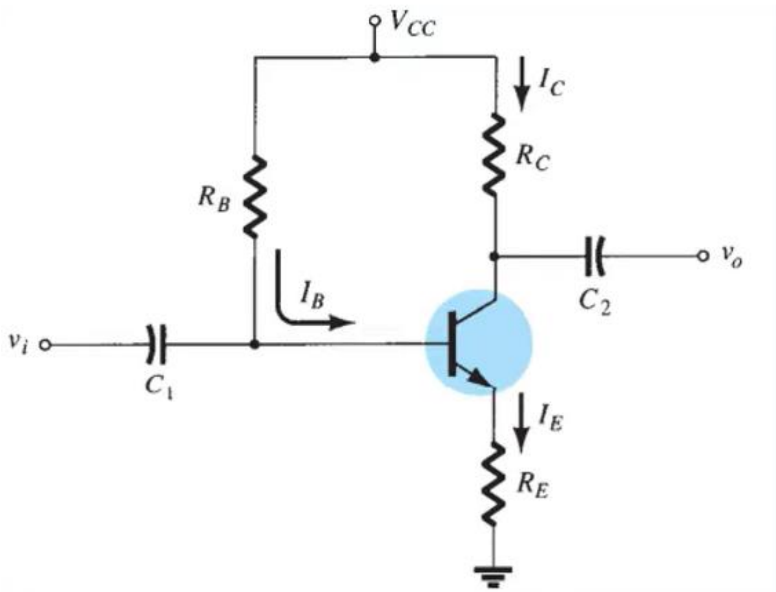
- Become aware of the saturation and cutoff conditions of a BJT network and the expected voltage and current levels established by each condition.

- Be able to perform a load-line analysis of the most common BJT configurations.
- Become familiar with the design process for BJT amplifiers.

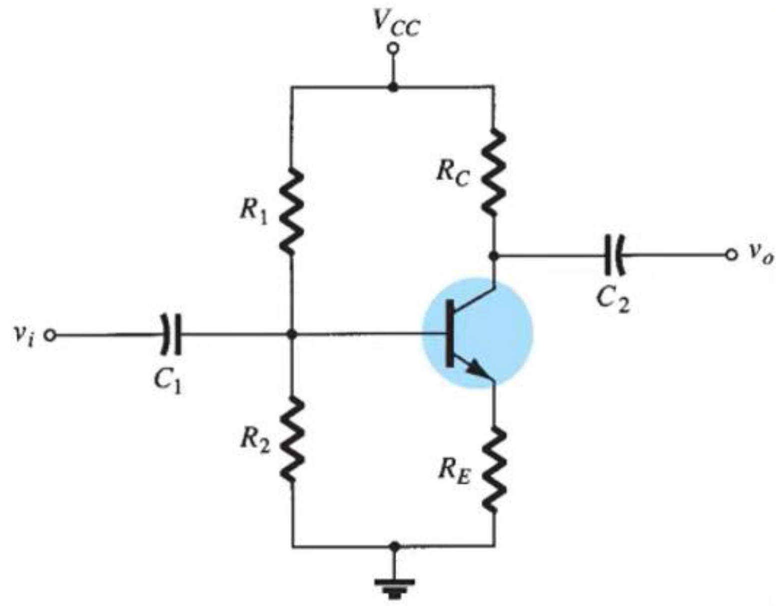
DC Biasing Types



Fixed-Bias
Configuration



Emitter-Bias
Configuration



Voltage-Divider Bias
Configuration

Remember

Important basic relationships for a transistor

(1) $$V_{BE} \cong 0.7\ \text{V}$$

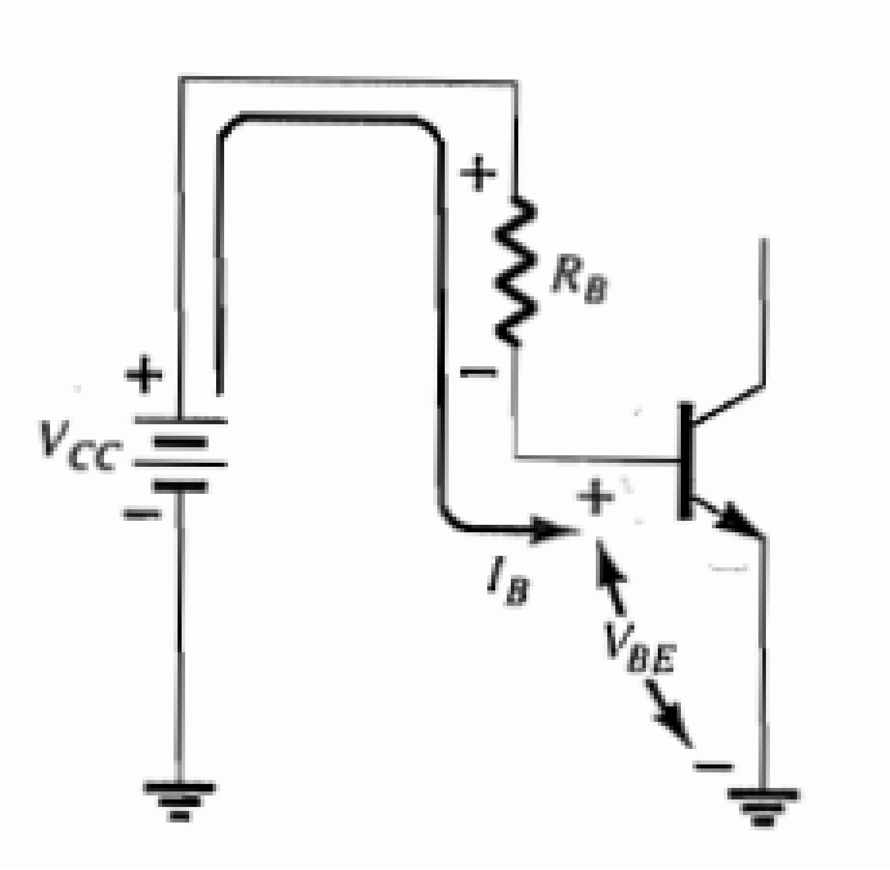
$$I_E = I_C + I_B$$

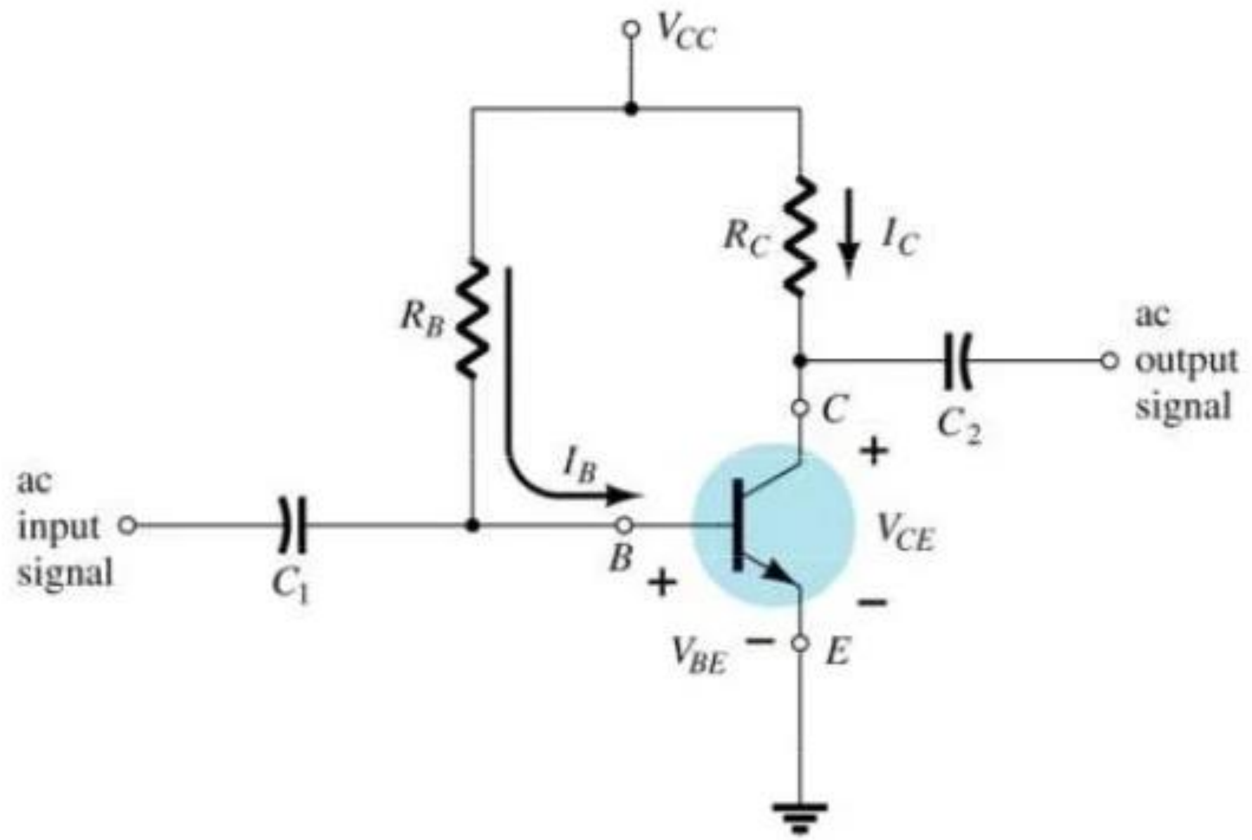
(2) $$I_C = \beta I_B$$

$$I_E = \beta I_B + I_B$$

(3) $$I_E = (\beta + 1)I_B \cong I_C$$

Fixed Bias



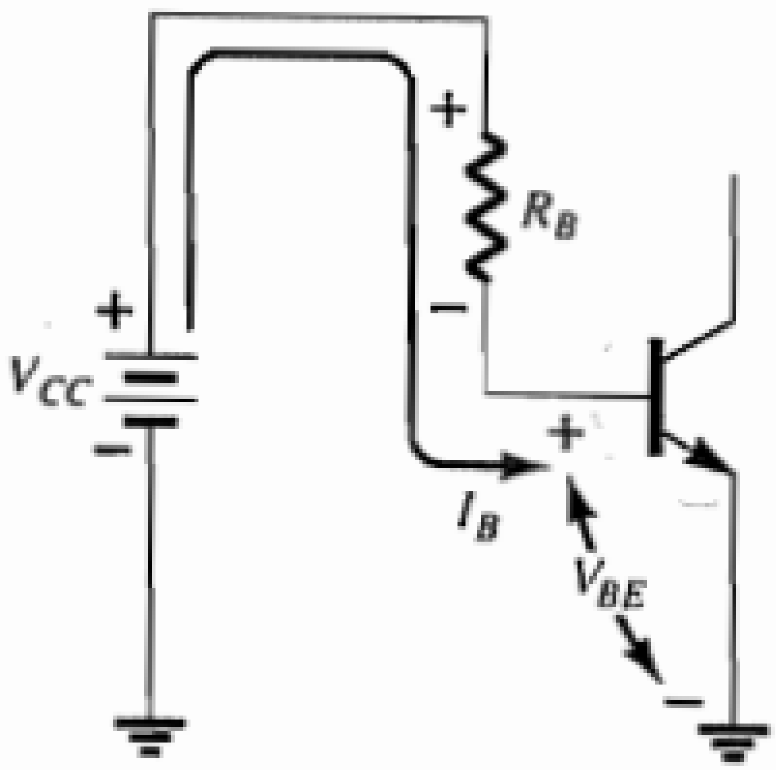


For the DC analysis the network can be isolated from the indicated AC levels by replacing the capacitor with an open circuit equivalent

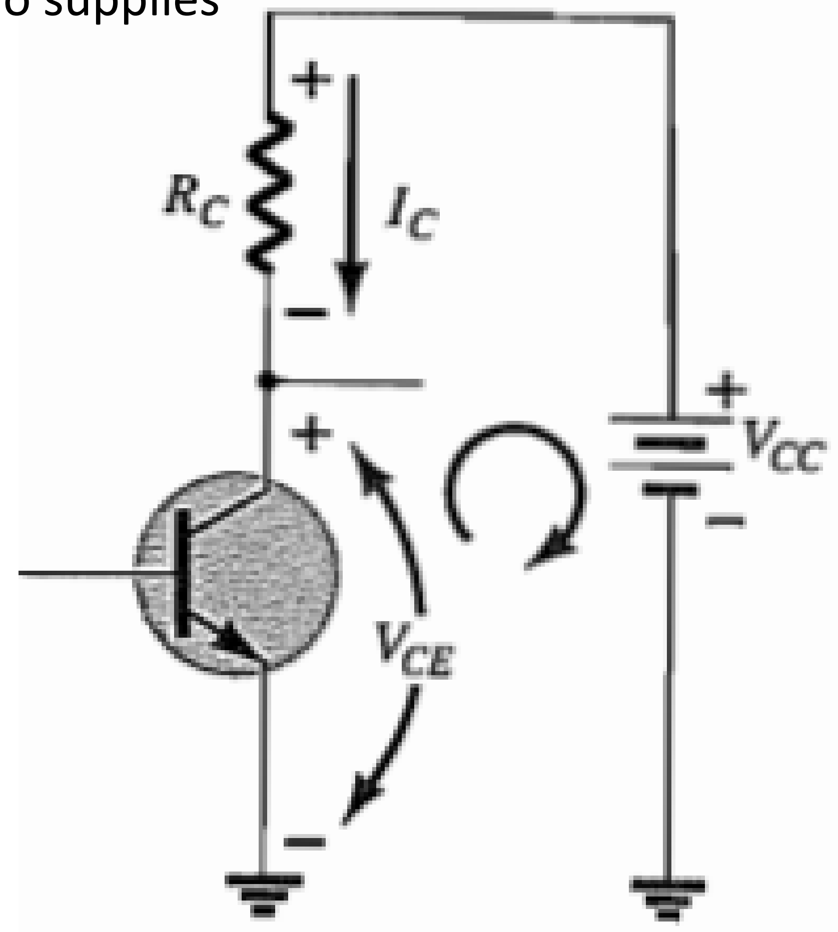
KVL Base emitter loop

Fixed Bias

The DC supply VCC can be separated into two supplies



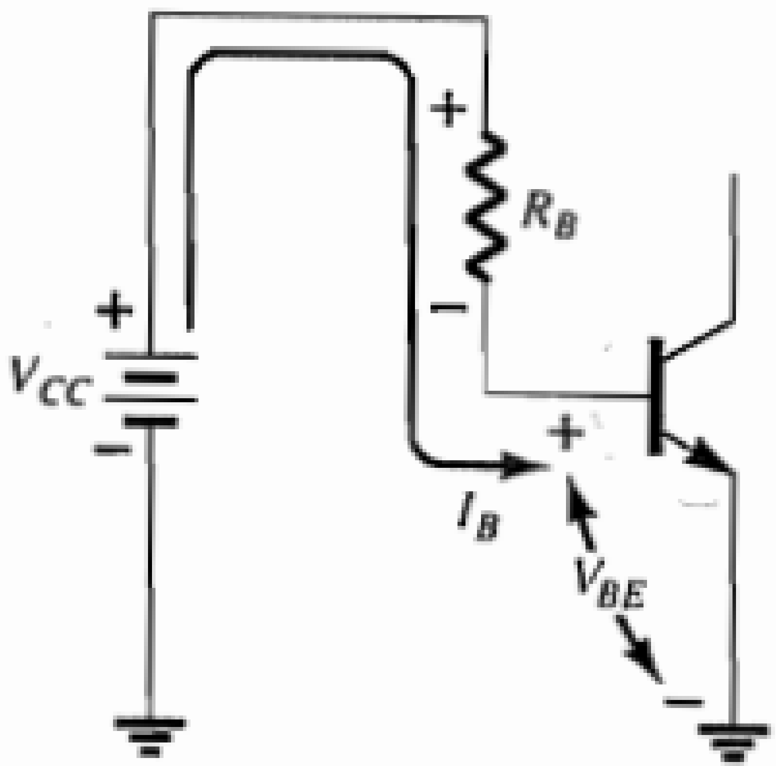
KVL Base emitter loop



KVL collector emitter loop

Fixed Bias

Forward Bias of Base–Emitter



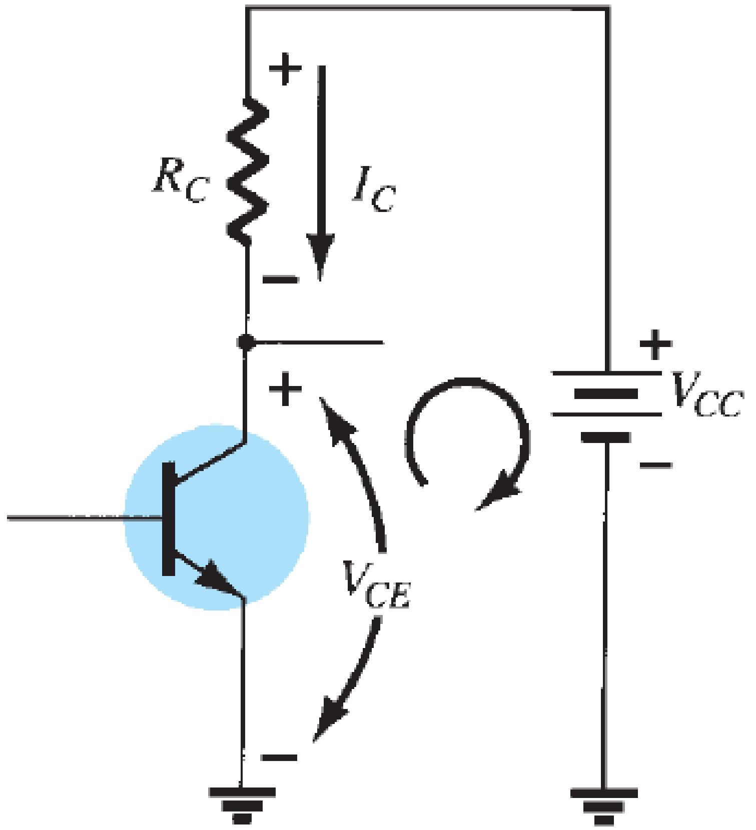
KVL Base emitter loop

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C = \beta I_B$$

Collector–Emitter Loop



$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E$$

$$V_{CE} = V_C$$

$$V_{BE} = V_B - V_E$$

$$V_{BE} = V_B$$

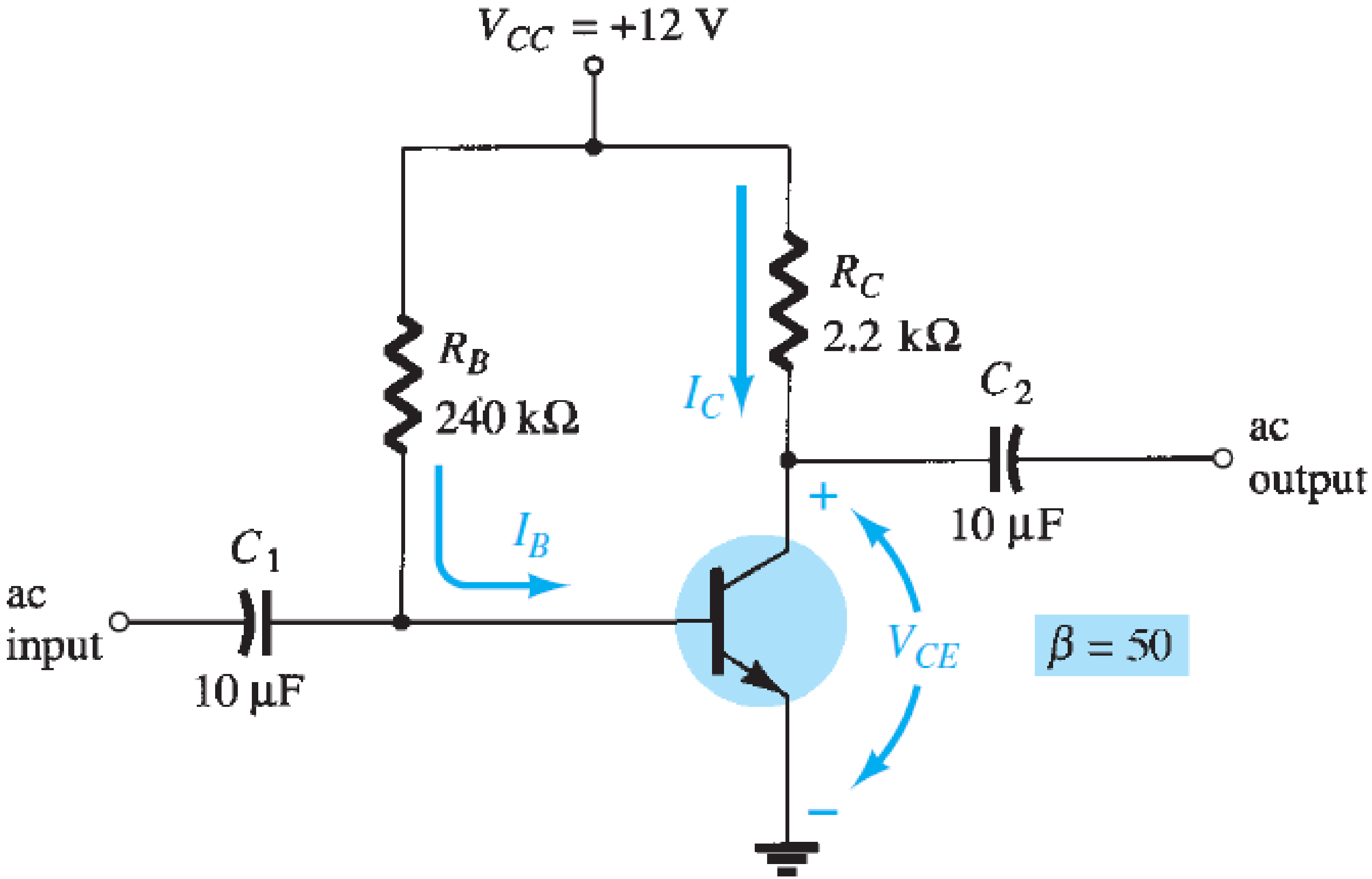
Example 2: Determine the following for the fixed-bias configuration of Fig.

(a) I_{BQ} and I_{CQ}.

(b) V_{CEQ}.

(c) V_B and V_C.

(d) V_{BC}.



Solution:

$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$$

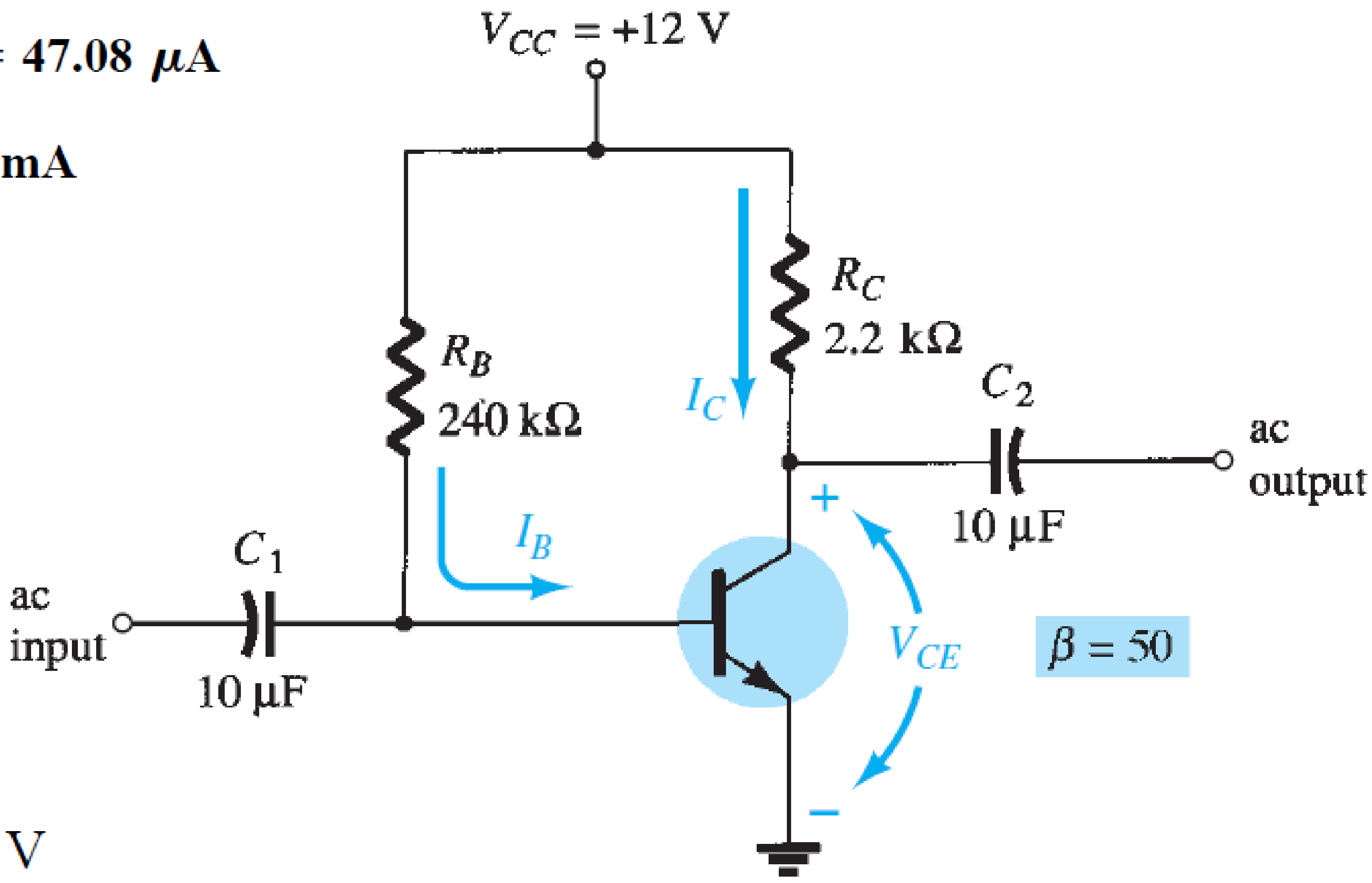
$$I_{C_Q} = \beta I_{B_Q} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\ mA}$$

$$\begin{aligned} V_{CE_Q} &= V_{CC} - I_C R_C \\ &= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega) \\ &= \mathbf{6.83\ V} \end{aligned}$$

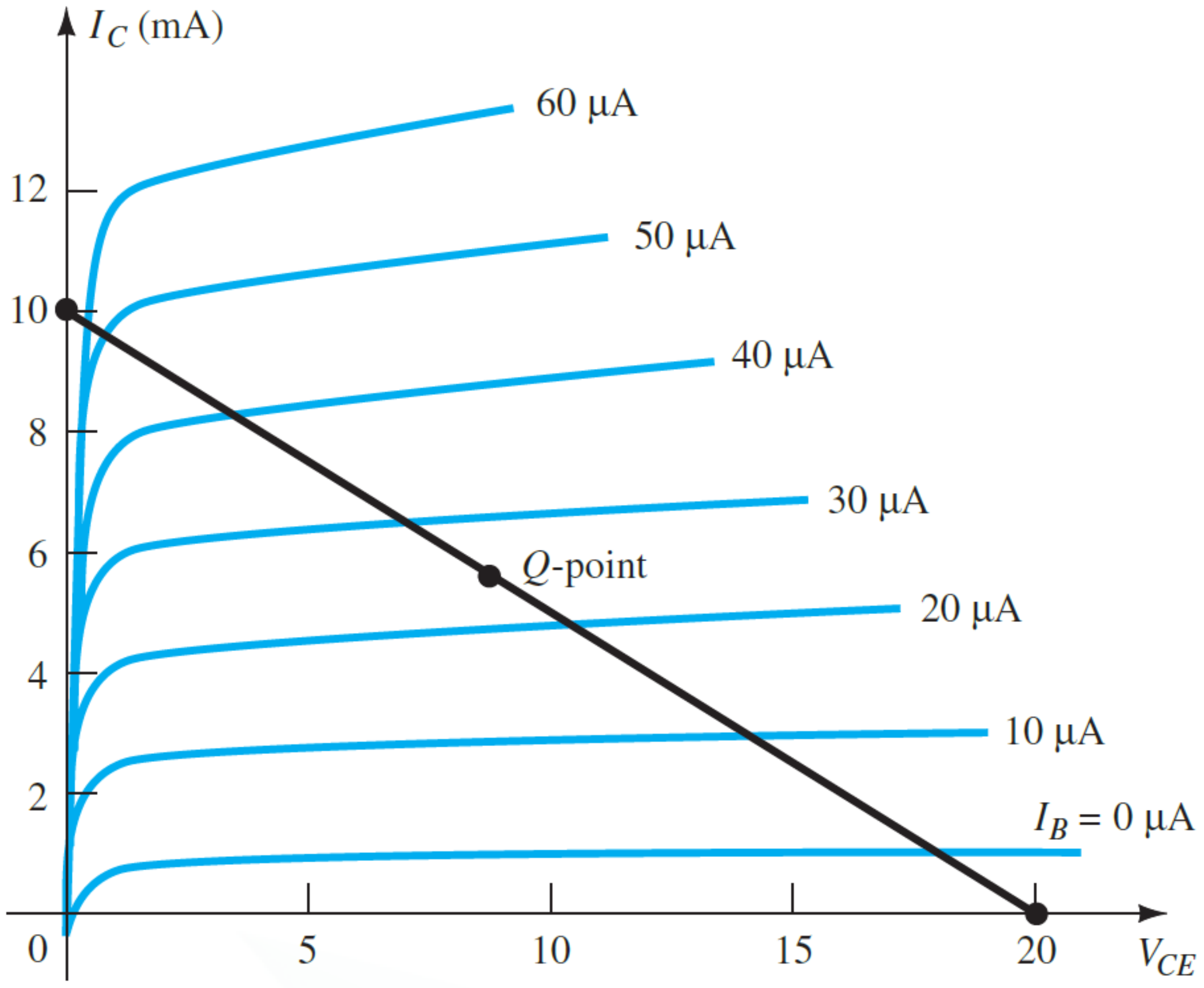
$$V_B = V_{BE} = \mathbf{0.7\ V}$$

$$V_C = V_{CE} = \mathbf{6.83\ V}$$

$$\begin{aligned} V_{BC} &= V_B - V_C = 0.7\text{ V} - 6.83\text{ V} \\ &= \mathbf{-6.13\ V} \end{aligned}$$

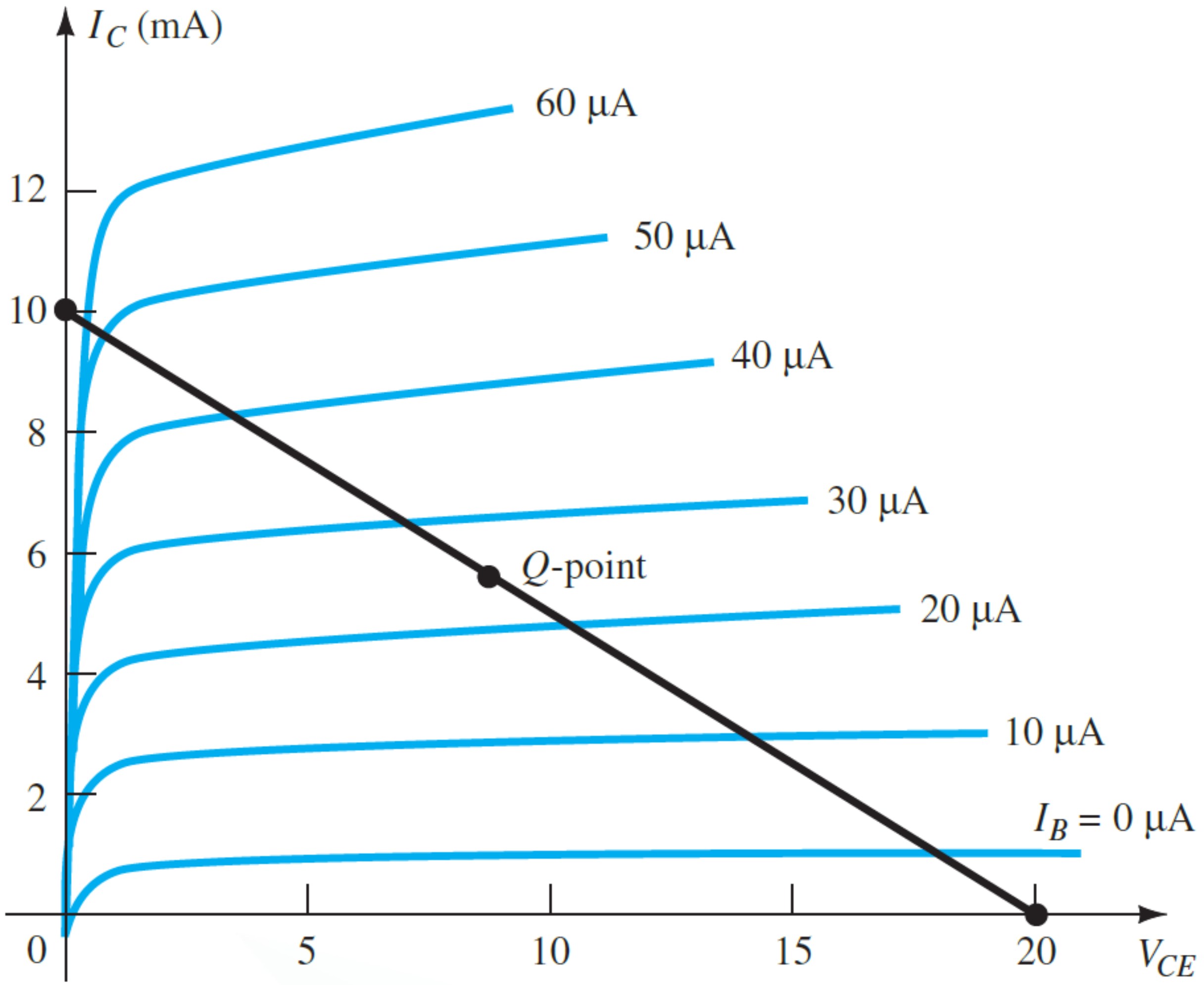


Example 2 Given the load line of Figure below and the defined Q-point, determine the required values of V_C, R_C, and R_B for a fixed-bias configuration.



Example 2 Given the load line of Figure below and the defined Q-point, determine the required values of V_C, R_C, and R_B for a fixed-bias configuration.

Solution:



$$V_{CE} = V_{CC} = \mathbf{20\ V} \text{ at } I_C = 0 \text{ mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0 \text{ V}$$

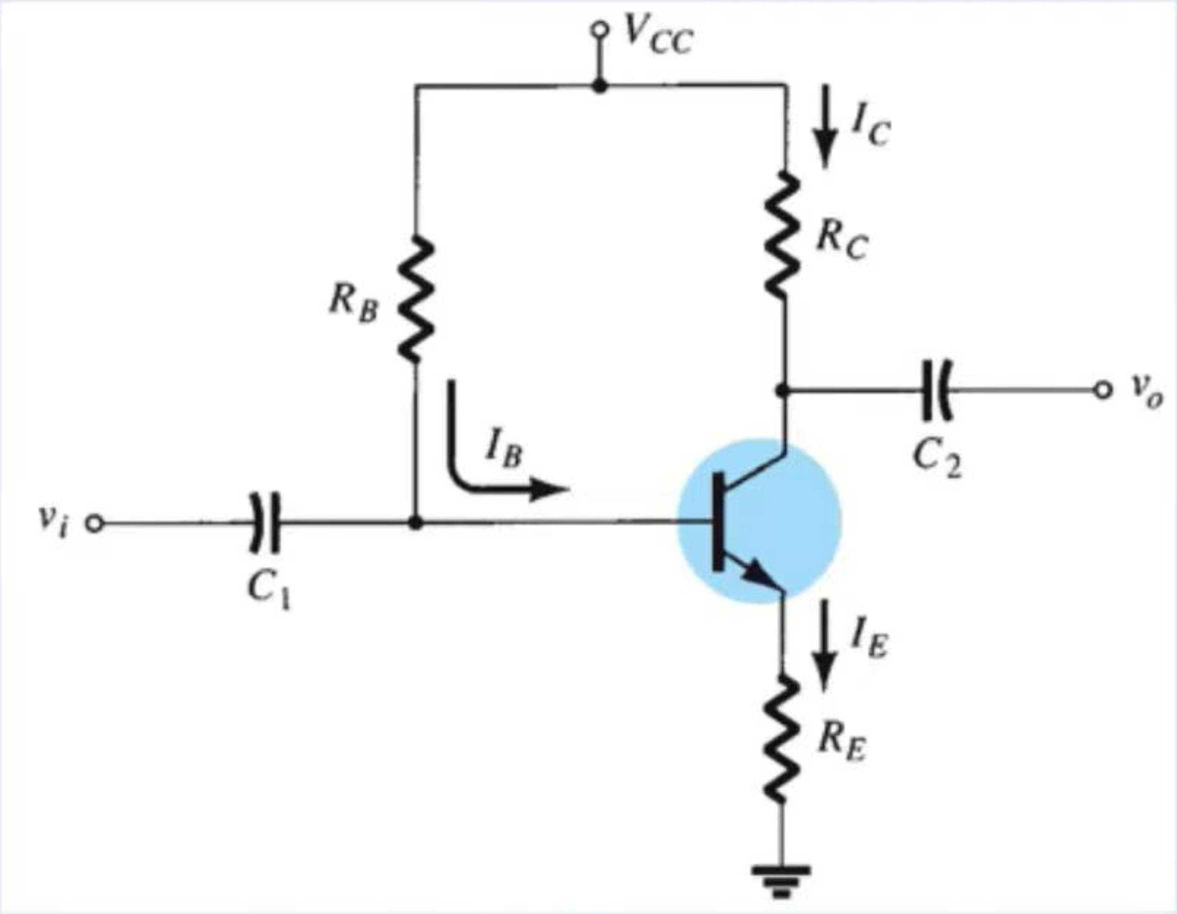
$$R_C = \frac{V_{CC}}{I_C} = \frac{20 \text{ V}}{10 \text{ mA}} = \mathbf{2\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20 \text{ V} - 0.7 \text{ V}}{25\ \mu\text{A}} = \mathbf{772\ k\Omega}$$

Emitter-Bias Configuration

The dc bias network of contains an emitter resistor to improve the stability level over that of the fixed-bias configuration.



BJT bias circuit with emitter resistor

Emitter-Bias Configuration

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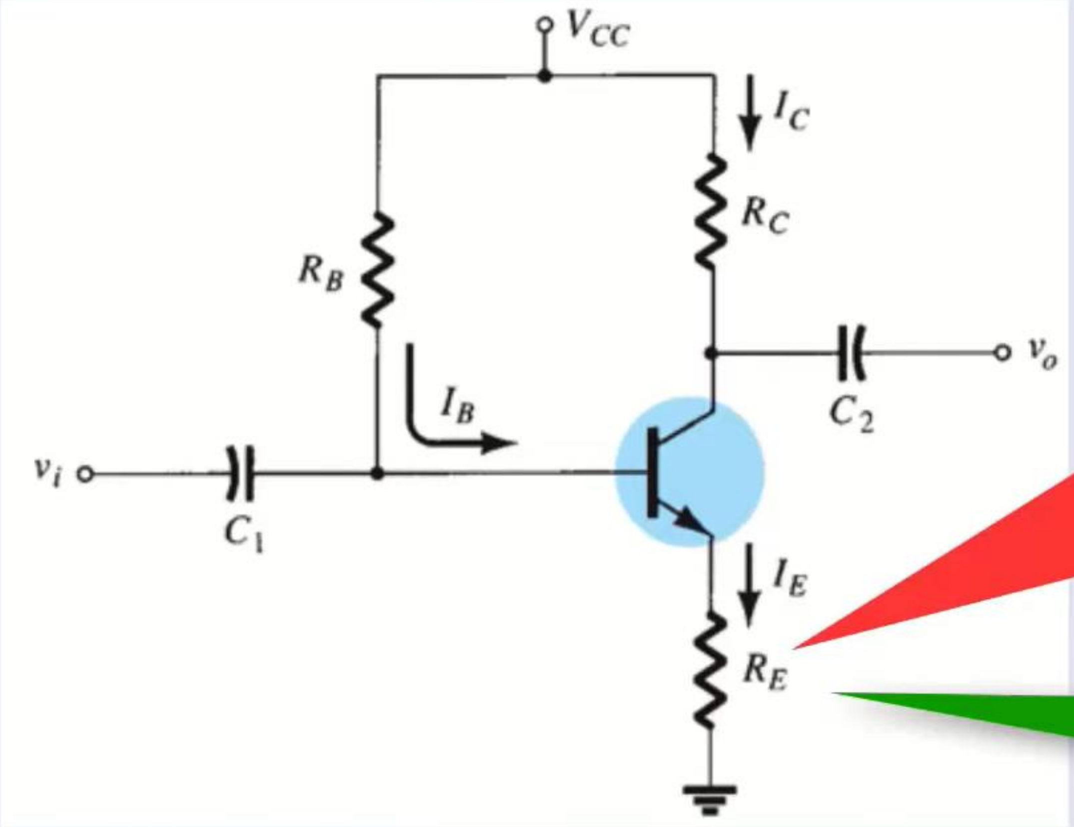


BJT bias circuit with emitter resistor

دائرة انحياز لتشغيل الترانزيستور يجب ان تكون مستقرة ولا تتأثر بالحرارة او اي تغيرات تطرأ على مقدار بيتا، حتى يكون التكبير فقط للاشارة الداخلة

أهم المزايا التي تميز هذا التوصيل

The analysis of Emitter-Bias Configuration

Base–Emitter Loop

Apply Kirchhoff's voltage law

$$-V_{CC} + I_B R_B + V_{BE} + I_E R_E = 0$$

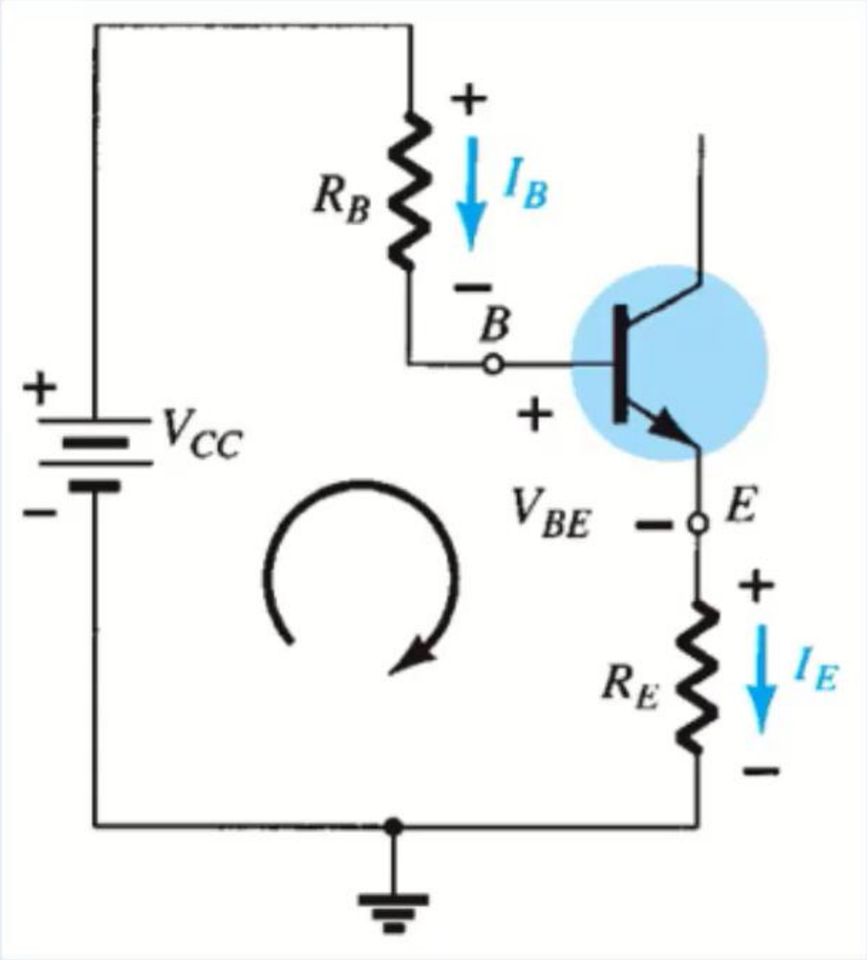
from $I_E = (\beta + 1)I_B$

$$-V_{CC} + I_B R_B + V_{BE} + (\beta + 1)I_B R_E = 0$$

$$I_B(R_B + (\beta + 1)R_E) - V_{CC} + V_{BE} = 0$$

$$I_B(R_B + (\beta + 1)R_E) = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$



The analysis of Emitter-Bias Configuration

Collector–Emitter Loop

The magnitude of the collector current I_C

$$I_C = \beta I_B$$

$$I_C = \frac{\beta(V_{CC} - V_{BE})}{R_B + (\beta + 1)R_E}$$

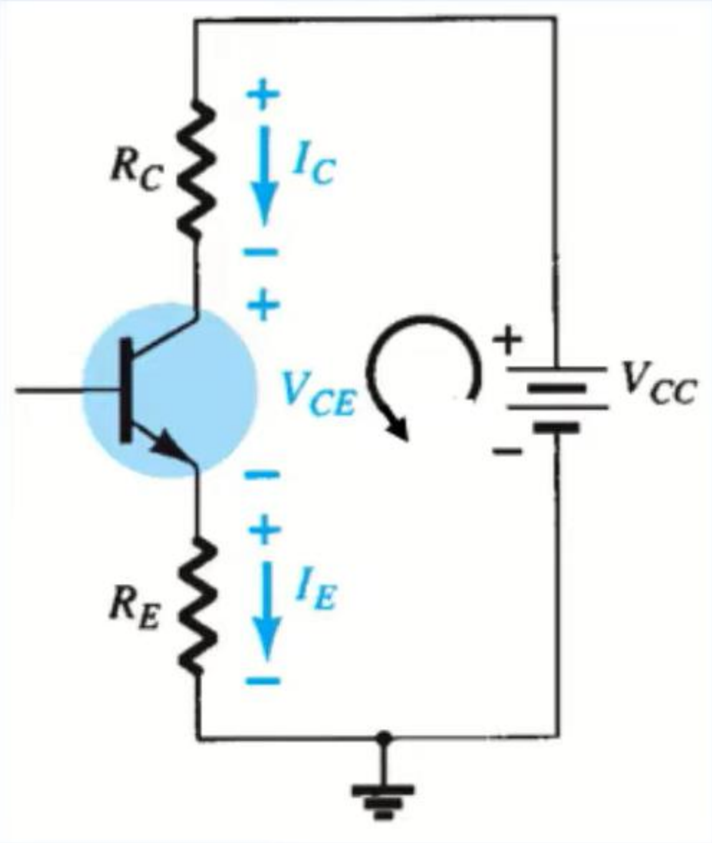
Apply Kirchhoff's voltage law to find V_{CE}

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

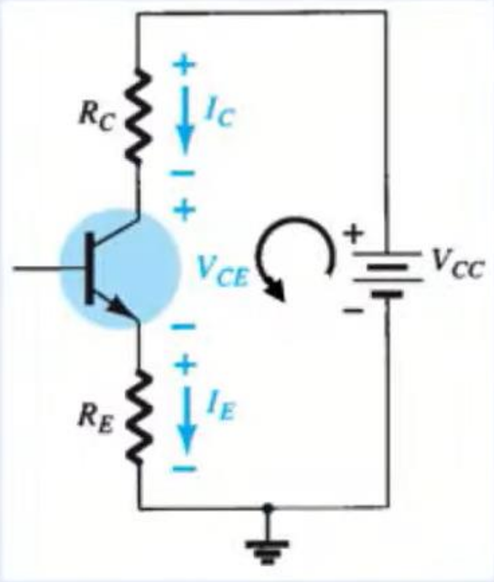
$$I_E \cong I_C$$

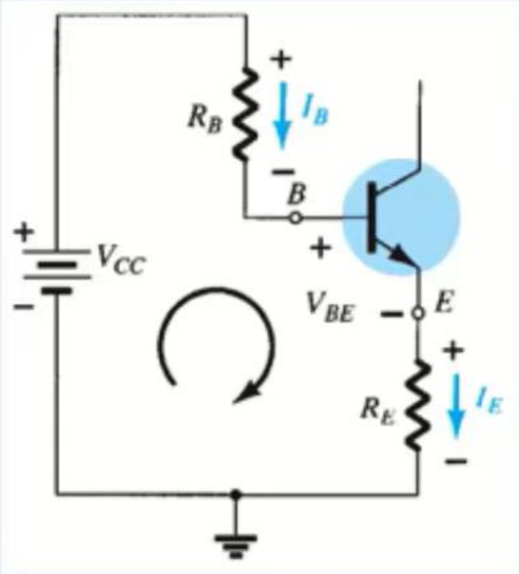
$$V_{CE} - V_{CC} + I_C(R_C + R_E) = 0$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



The voltages V_B, V_C, V_E with respect to the ground





The voltage at the base V_B is the voltage from Base to ground and is determine by

$$V_B = V_{CC} - I_B R_B$$

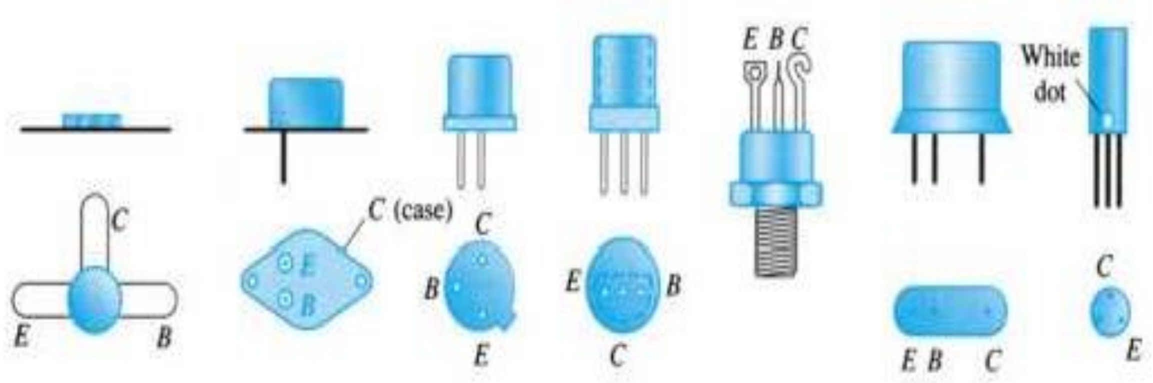
or

$$V_B = V_{BE} + V_E$$

Ninevah University
College of Electronics Engineering
Department of Systems and Control

Electronic I
Lecture 4

BJT Biasing Circuits



2nd Class

by
Rafal Raed Mahmood Alshaker

Outline of Presentation

2. Emitter Bais

3.VOLTAGE-DIVIDER BIAS

- Exact Analysis
- Approximate Analysis

- Examples

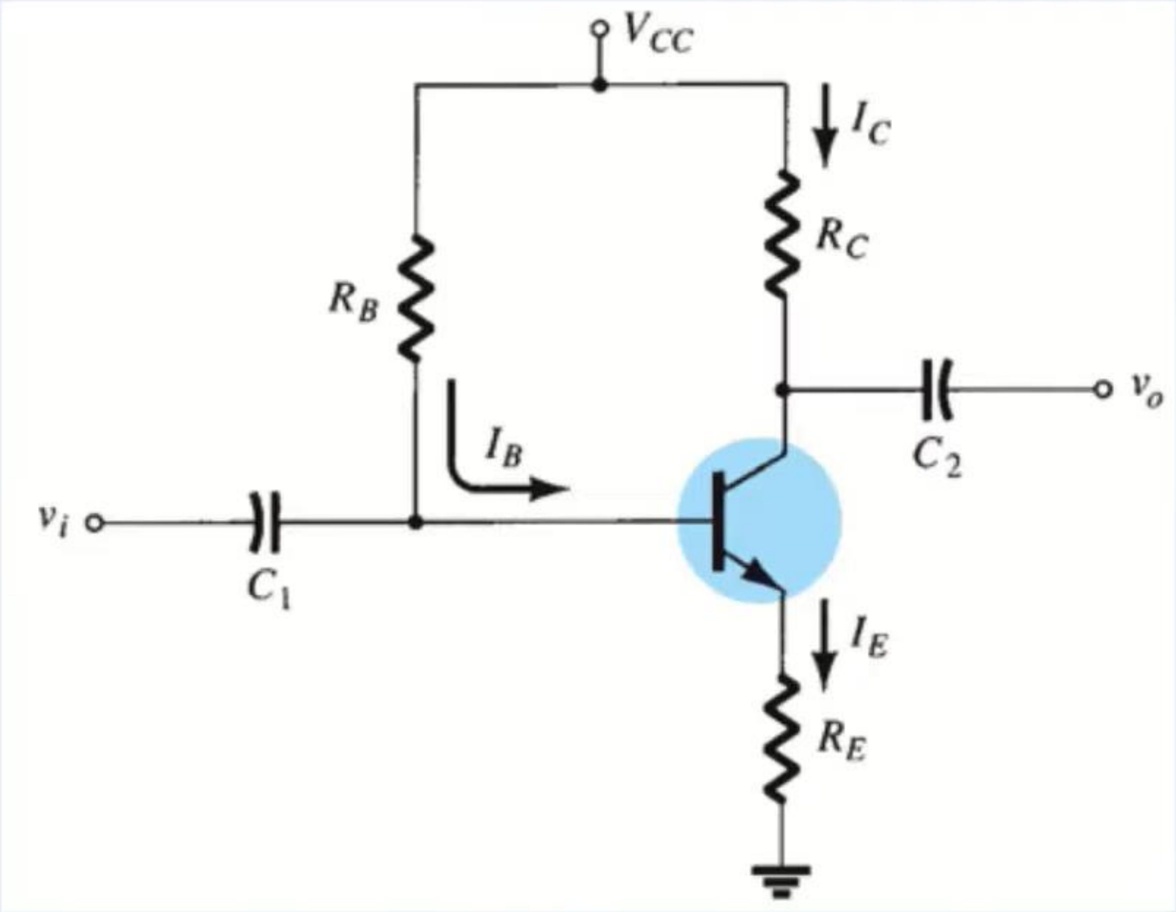
4

4. Collector Feedback Bias

- Examples

Emitter-Bias Configuration

The dc bias network of contains an emitter resistor to improve the stability level over that of the fixed-bias configuration.



BJT bias circuit with emitter resistor

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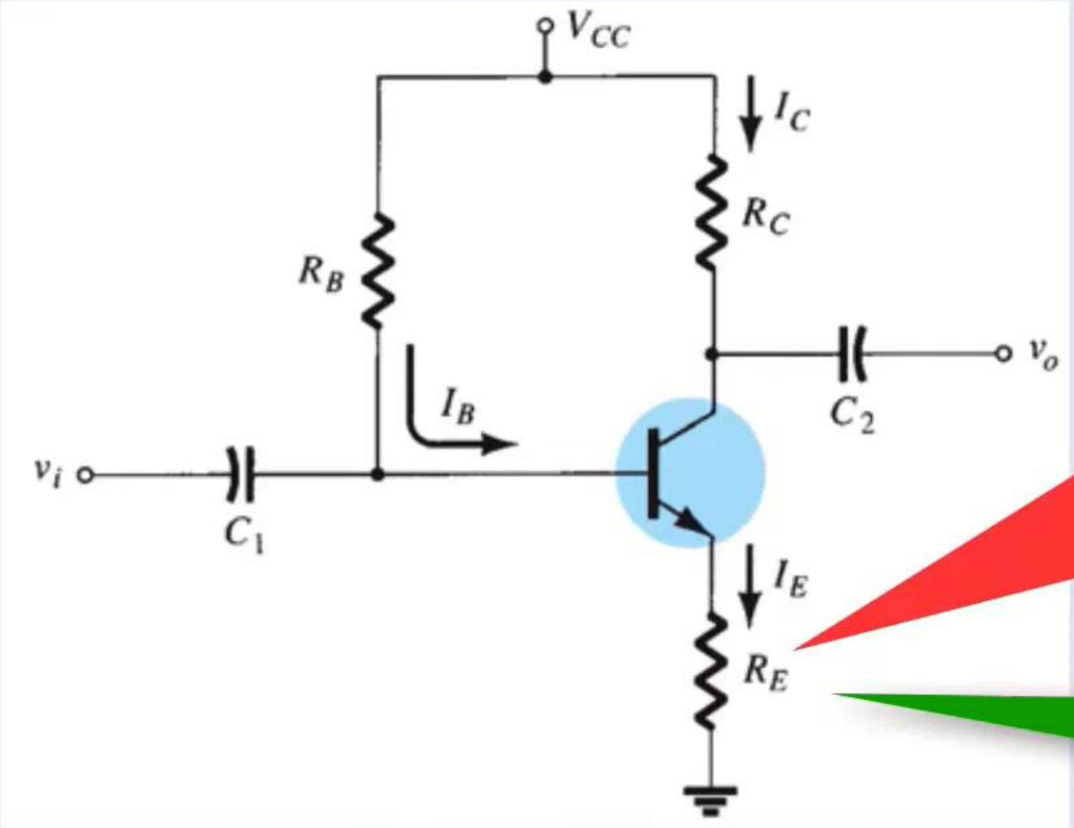

BJT bias circuit with emitter resistor

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$$I_B(R_B + (\beta + 1)R_E) - V_{CC} + V_{BE} = 0$$

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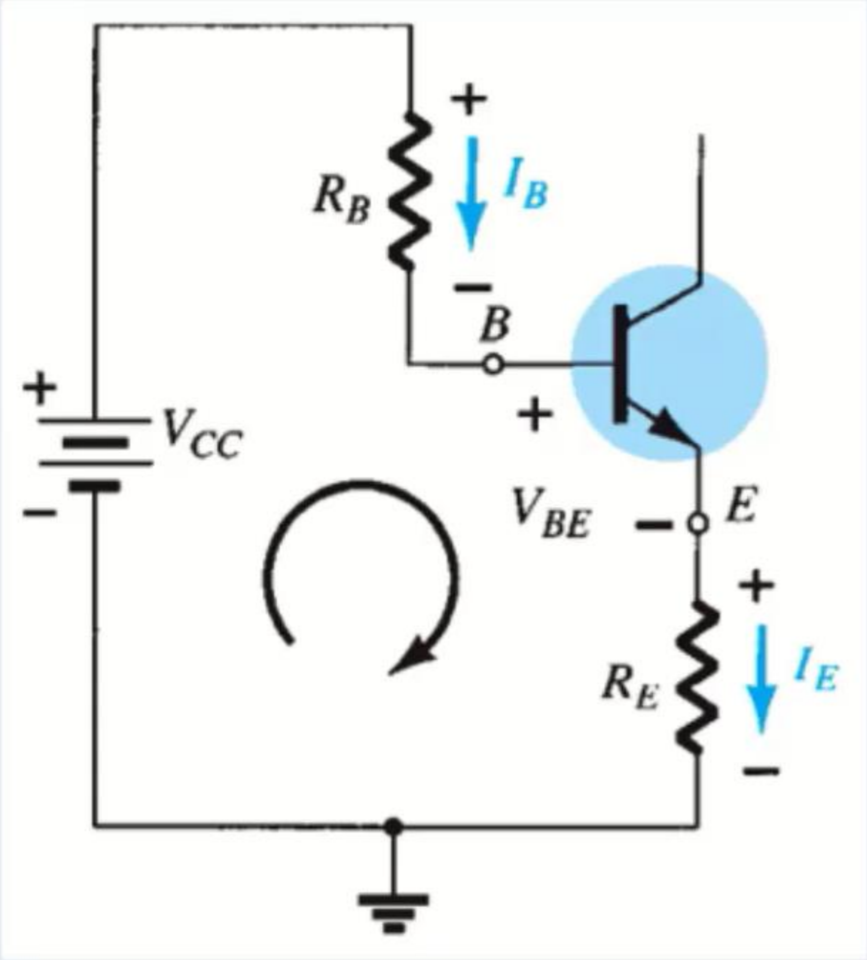
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$



The analysis of Emitter-Bias Configuration

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$$I_C = \frac{\beta(V_{CC} - V_{BE})}{R_B + (\beta + 1)R_E}$$

Apply Kirchhoff's voltage law to find V_{CE}

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

$$I_E \cong I_C$$

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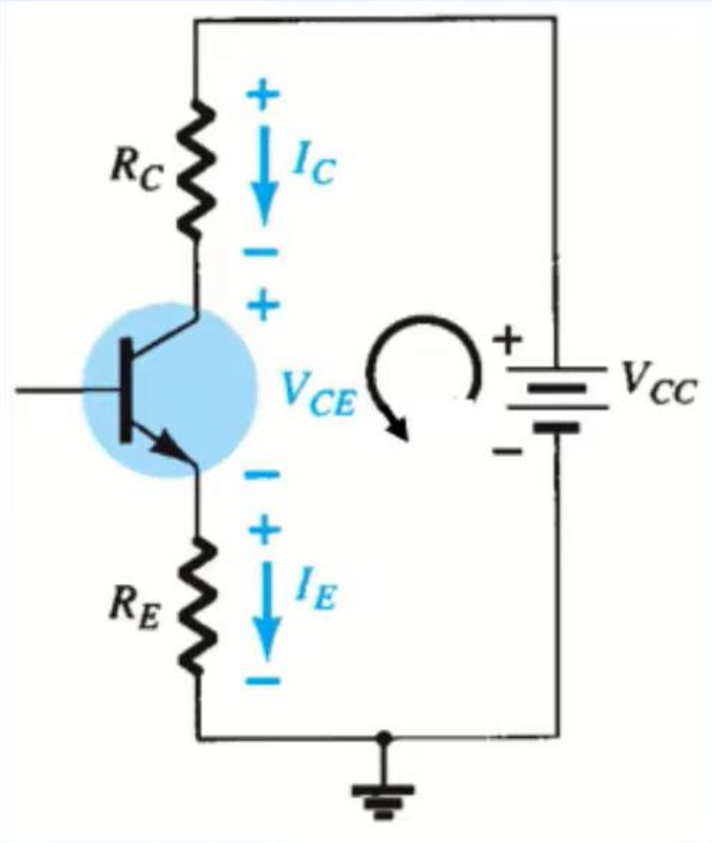
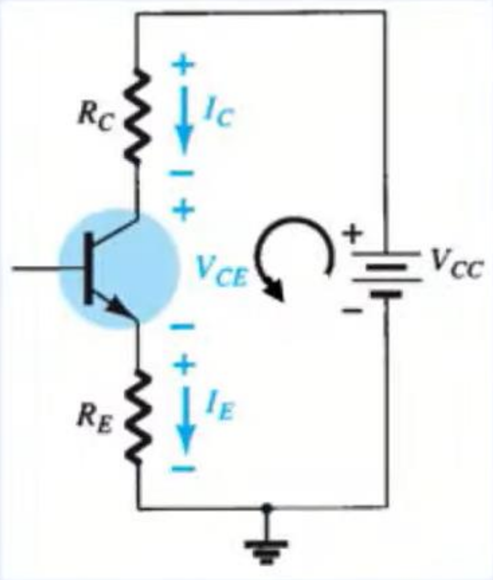
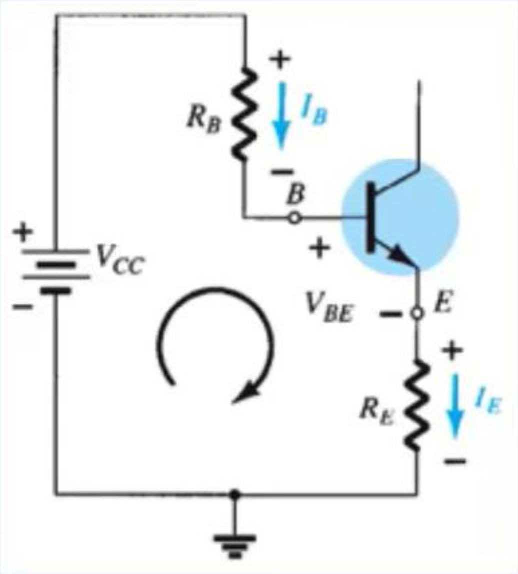
$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



The voltages V_B, V_C, V_E with respect to the ground





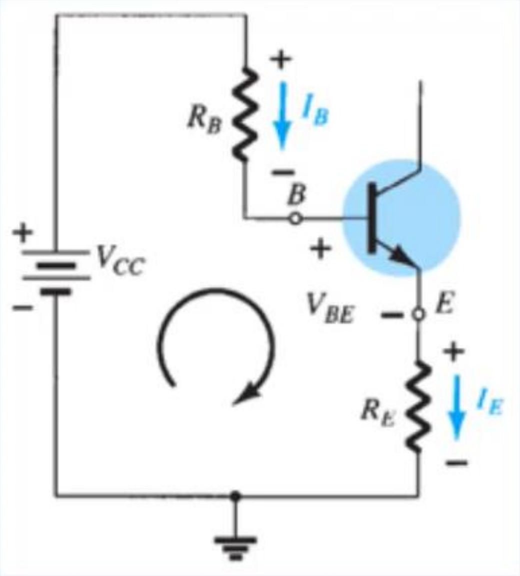
The voltage at the base V_B is the voltage from Base to ground and is determine by

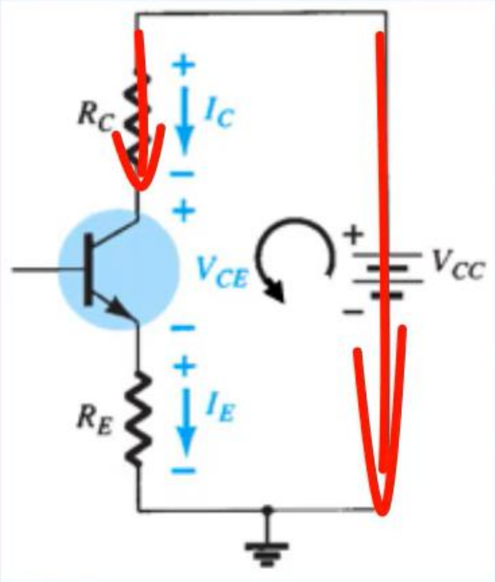
$$V_B = V_{CC} - I_B R_B$$

or

$$V_B = V_{BE} + V_E$$

The voltages V_B, V_C, V_E with respect to the ground





The voltage at the base V_B is the voltage from Base to ground and is determine by

$$V_B = V_{CC} - I_B R_B$$

or

$$V_B = V_{BE} + V_E$$

The voltage V_E is the voltage from emitter to ground and is determine by

$$V_E = I_E R_E$$ or $$V_E = I_E R_E \cong I_C R_E$$

The voltage from V_C collector to ground can be determined from

$$V_C = V_{CE} + V_E$$

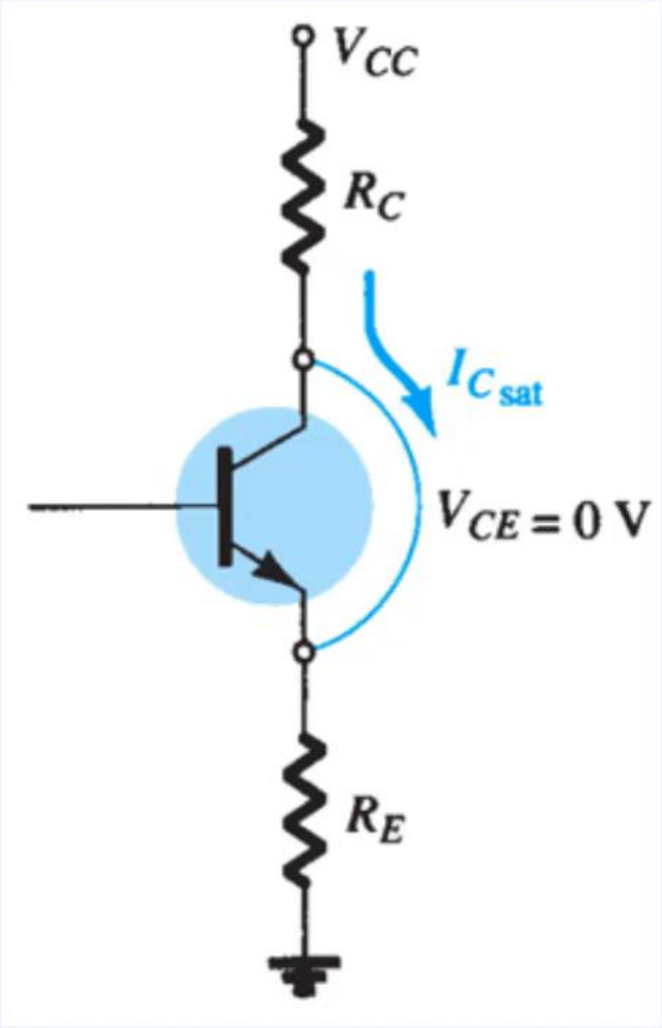
or

$$V_C = V_{CC} - I_C R_C$$

Determining I_{Csat} for the Emitter-bias configuration

The collector saturation level or maximum collector current for an emitter-bias design can be determined by applying a short circuit between the collector–emitter terminals and the resulting collector current

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$



Determining I_{Csat} for the

Load-Line Analysis for the Emitter-bias configuration

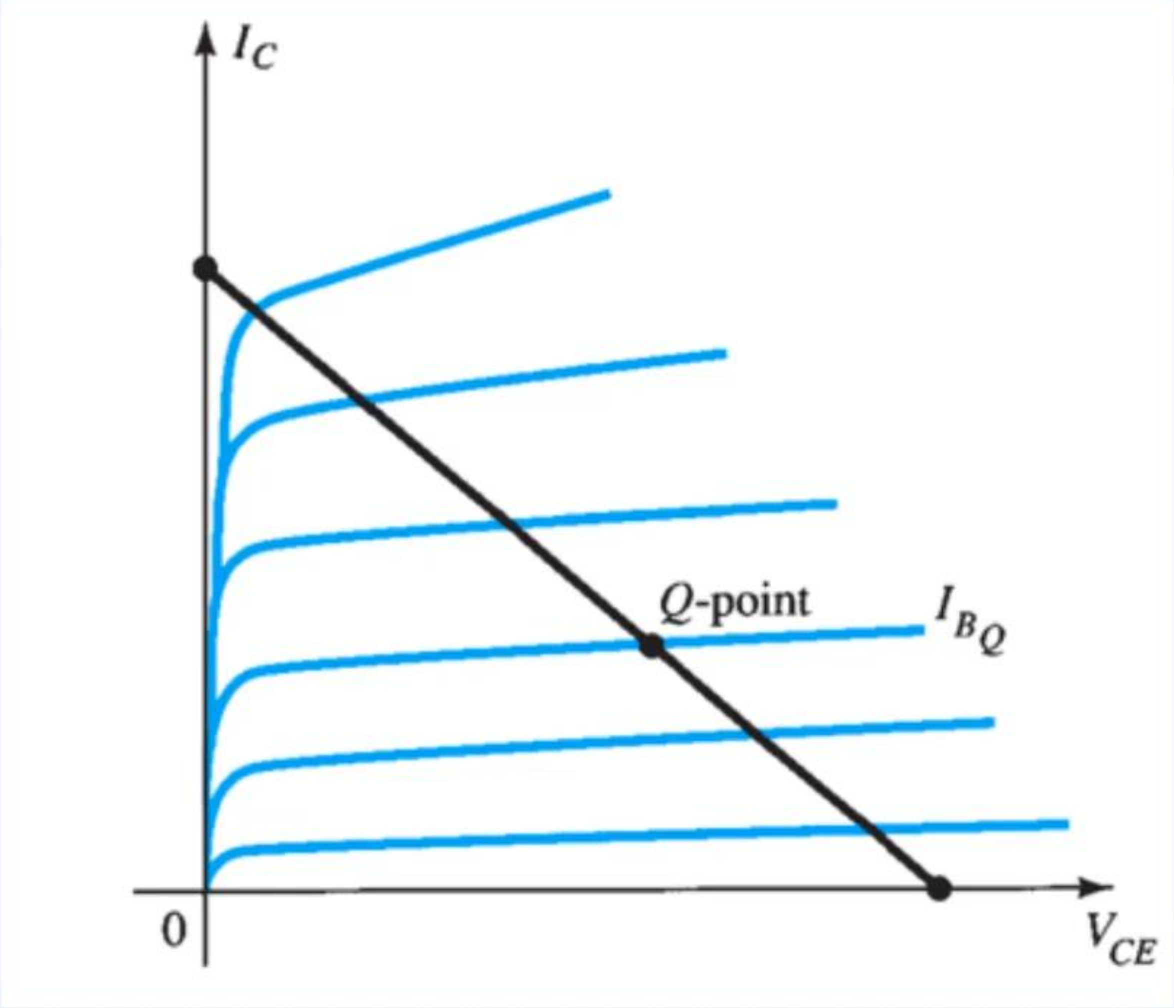
The load-line analysis of the emitter-bias network is only slightly different from that encountered for the fixed-bias configuration.

The level of I_{BQ} as determined by

$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

The collector–emitter loop equation that defines the load line is

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



Load line for the

Load-Line Analysis for the Emitter-bias configuration

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

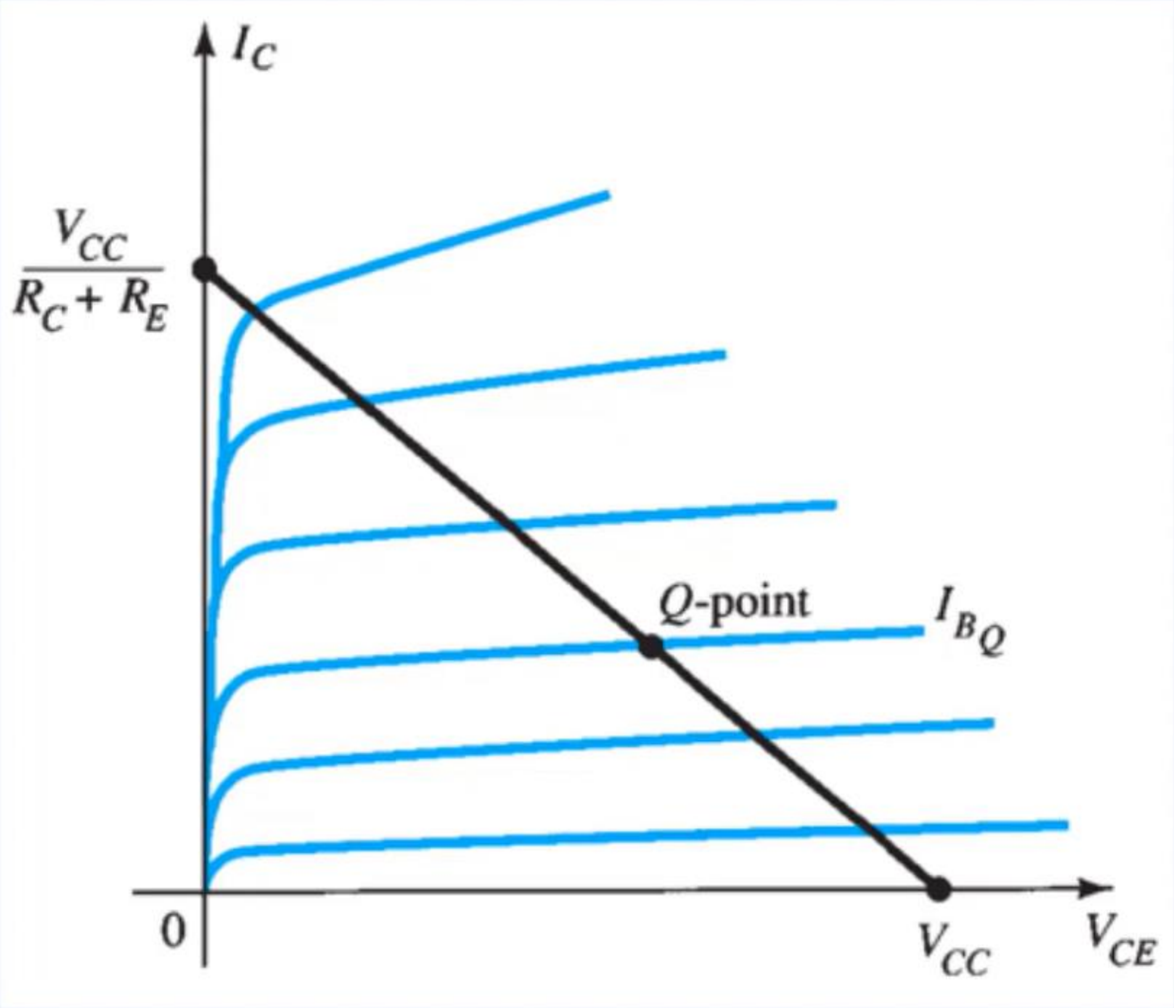
Choosing I_C = 0 mA gives

$$V_{CE} = V_{CC}\big|_{I_C=0\,\text{mA}}$$

Choosing V_{CE} = 0 V gives

$$I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE}=0\,\text{V}}$$

Different levels of I_{BQ} will move the Q - point up or down the load line.



Load line for the emitter-bias configuration

Voltage-Divider Bias Configuration

In the previous bias configurations the bias current I_{CQ} and voltage V_{CEQ} were a function of the current gain β of the transistor.

Fixed-Bias Configuration

$$I_C = \frac{\beta(V_{CC} - V_{BE})}{R_B}$$

$$V_{CE} = V_{CC} - I_C R_C$$

Emitter-Bias Configuration

$$I_C = \frac{\beta(V_{CC} - V_{BE})}{R_B + (\beta + 1)R_E}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

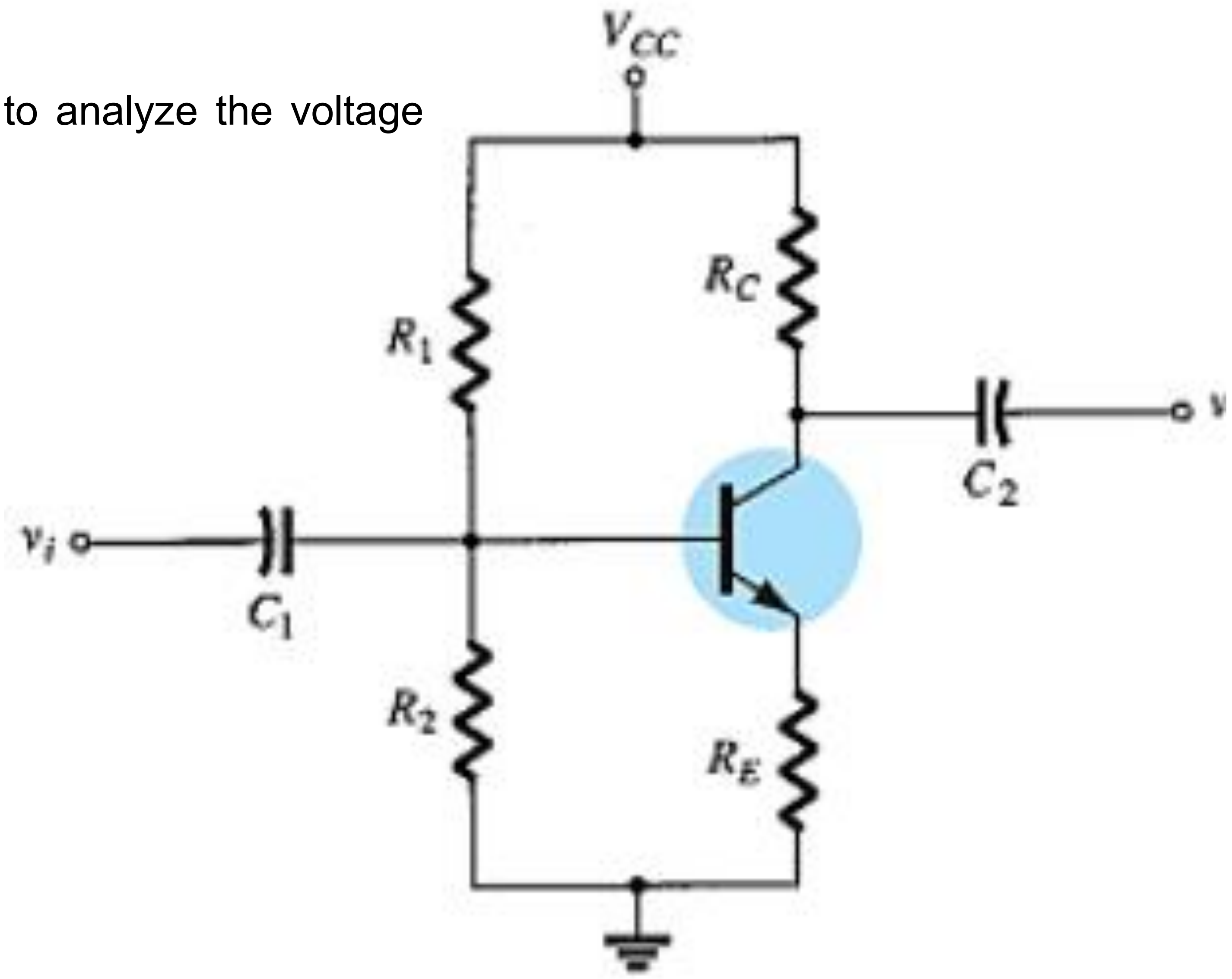
Because β is temperature sensitive, especially for silicon transistor.
Also, because the actual value of β is usually not well defined.

It is desirable to develop a bias circuit that is less dependent on β.

VOLTAGE-DIVIDER BIAS

There are two methods that can be applied to analyze the voltage divider configuration.

1. The **exact** method
2. The **approximate** method



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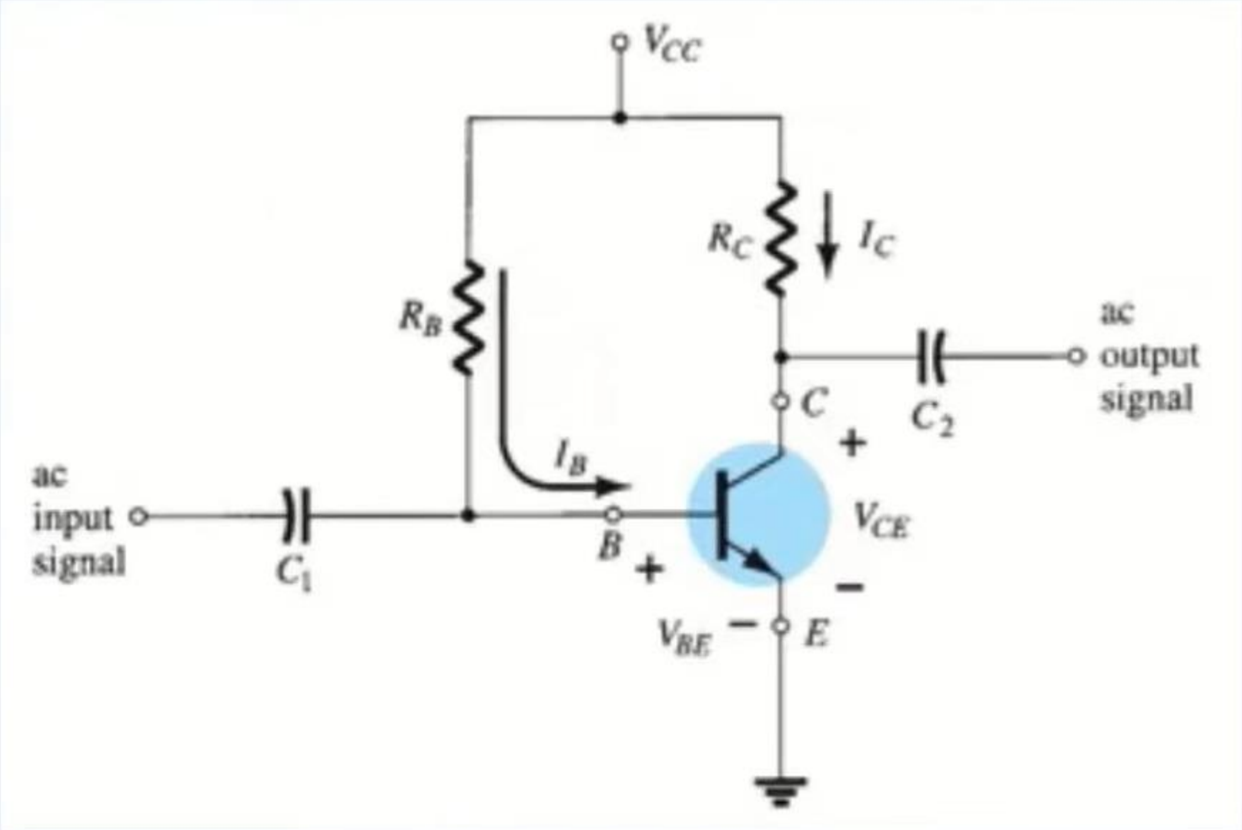

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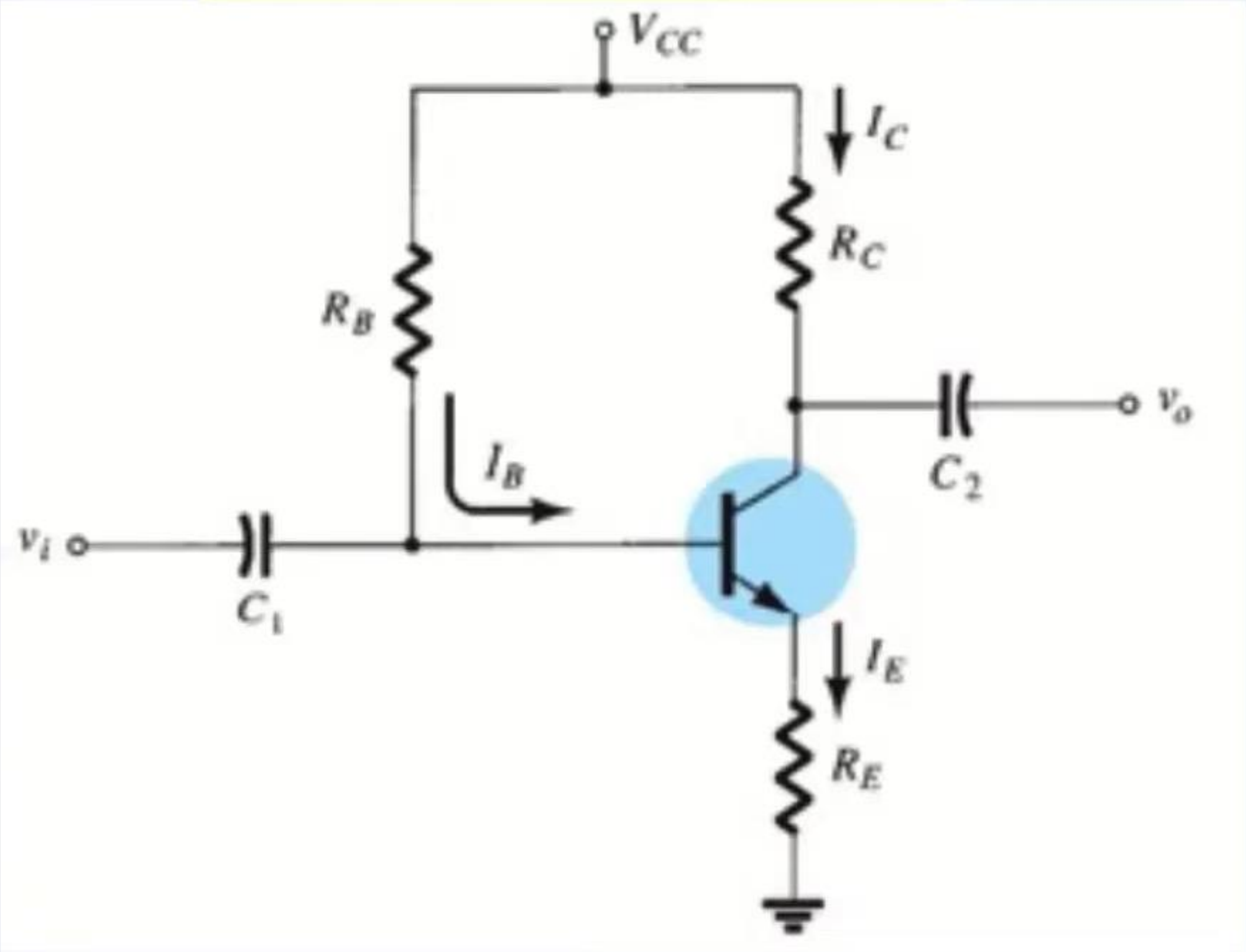

Emitter-Bias Configuration

$$I_C = \frac{\beta(V_{CC} - V_{BE})}{R_B + (\beta + 1)R_E}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

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$$I_C = \frac{\beta(V_{CC} - V_{BE})}{R_B}$$

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$$I_C = \frac{\beta(V_{CC} - V_{BE})}{R_B + (\beta + 1)R_E}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Because β is temperature sensitive, especially for silicon transistor.
Also, because the actual value of β is usually not well defined.

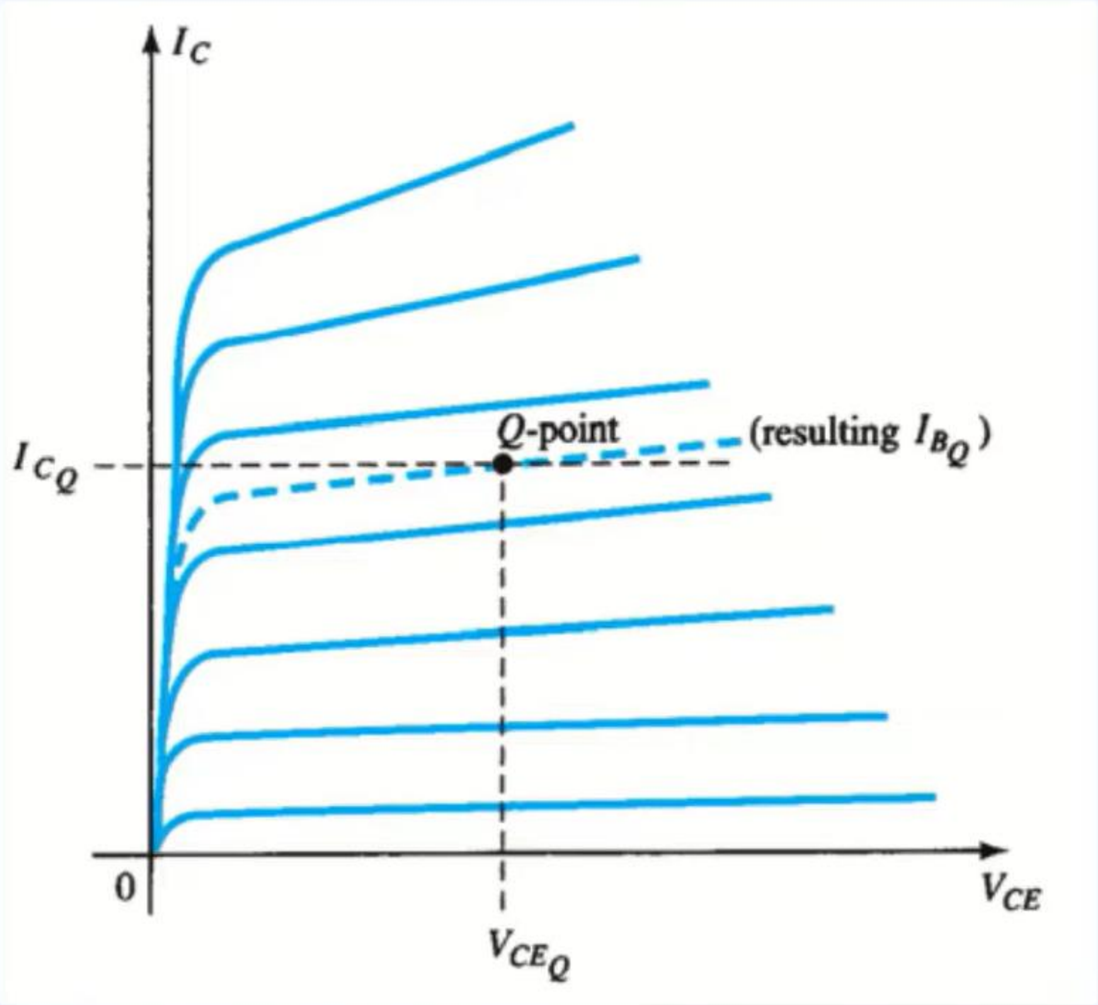
It is desirable to develop a bias circuit that is less dependent on β.

The voltage-divider bias configuration is such a network.

Voltage-Divider Bias Configuration

If the circuit parameters are properly chosen, the resulting levels of I_{CQ} and V_{CEQ} can be almost totally independent of beta.

The level of I_{BQ} will change with the change in β, but the operating point on the characteristics defined by I_{CQ} and V_{CEQ} can remain fixed.

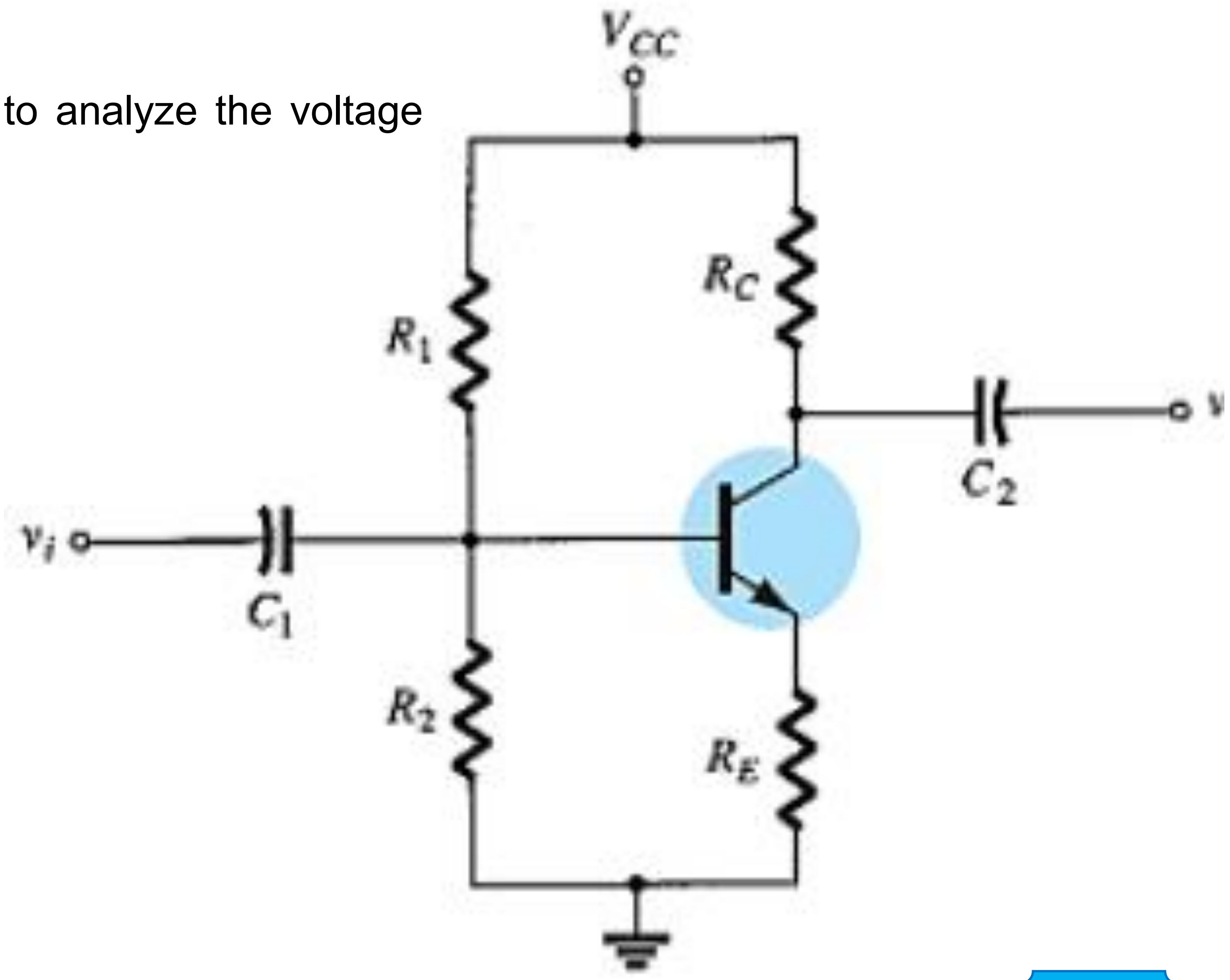


the Q-point for the voltage-divider bias configuration

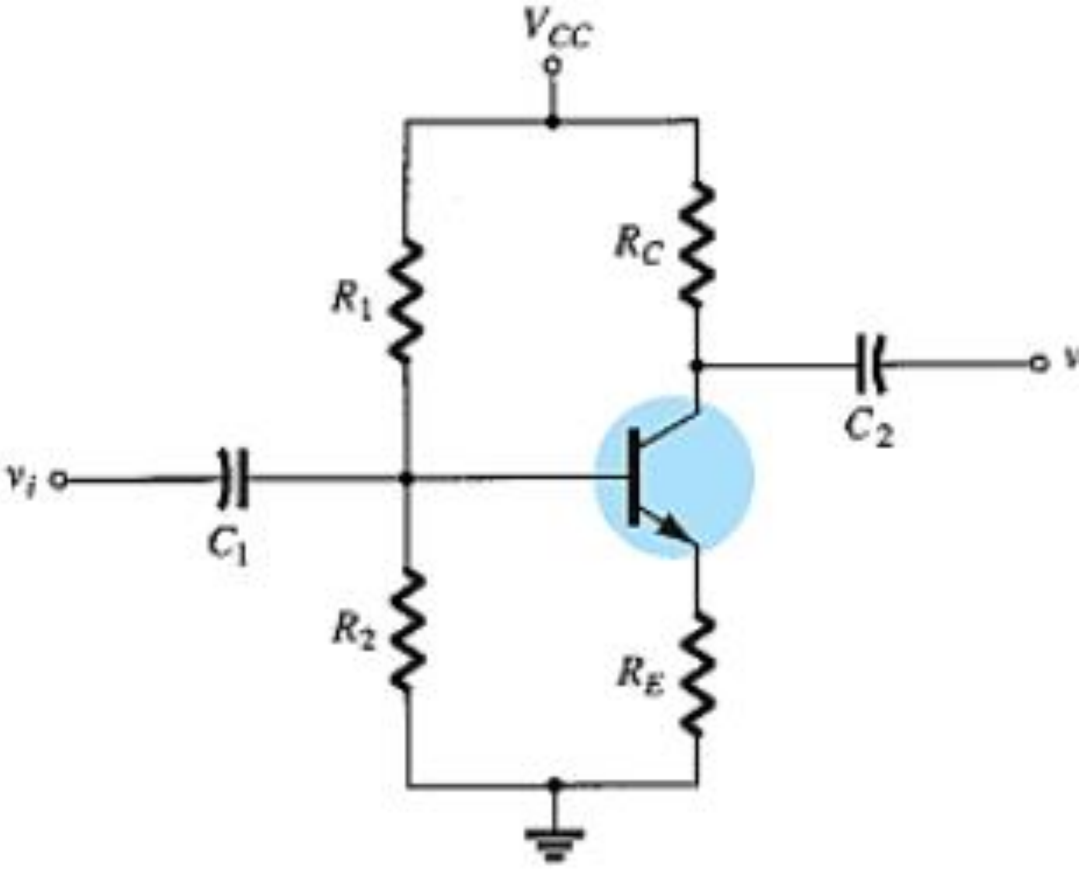
VOLTAGE-DIVIDER BIAS

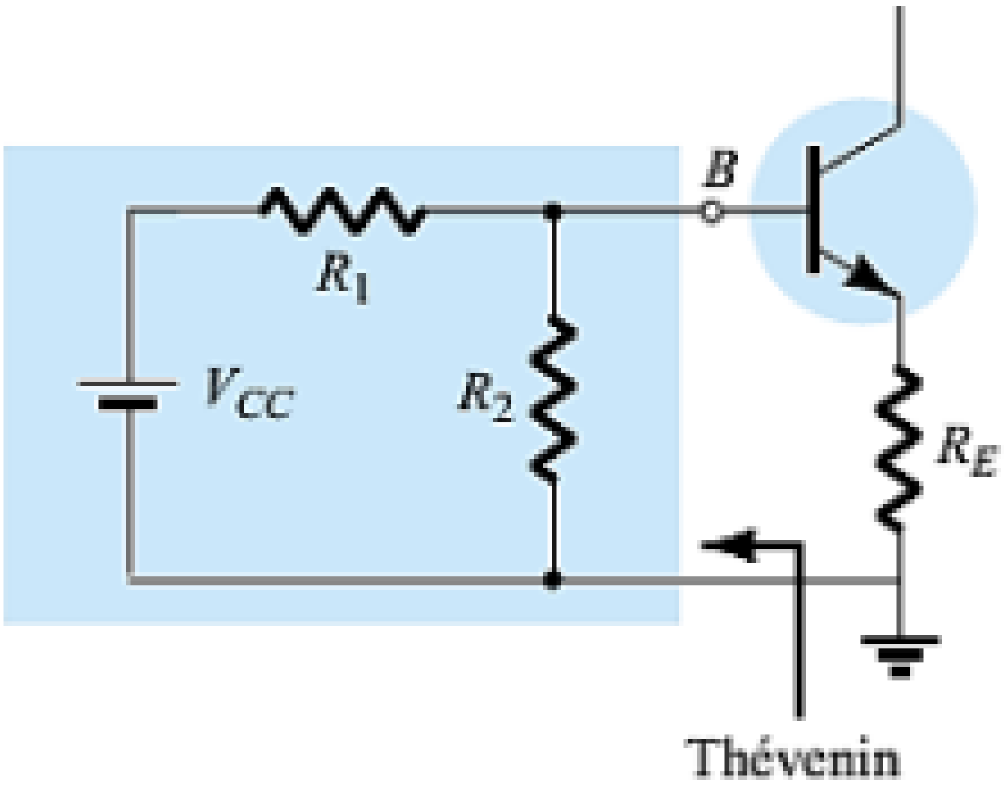
There are two methods that can be applied to analyze the voltage divider configuration.

1. The **exact** method
2. The **approximate** method



Exact Analysis:

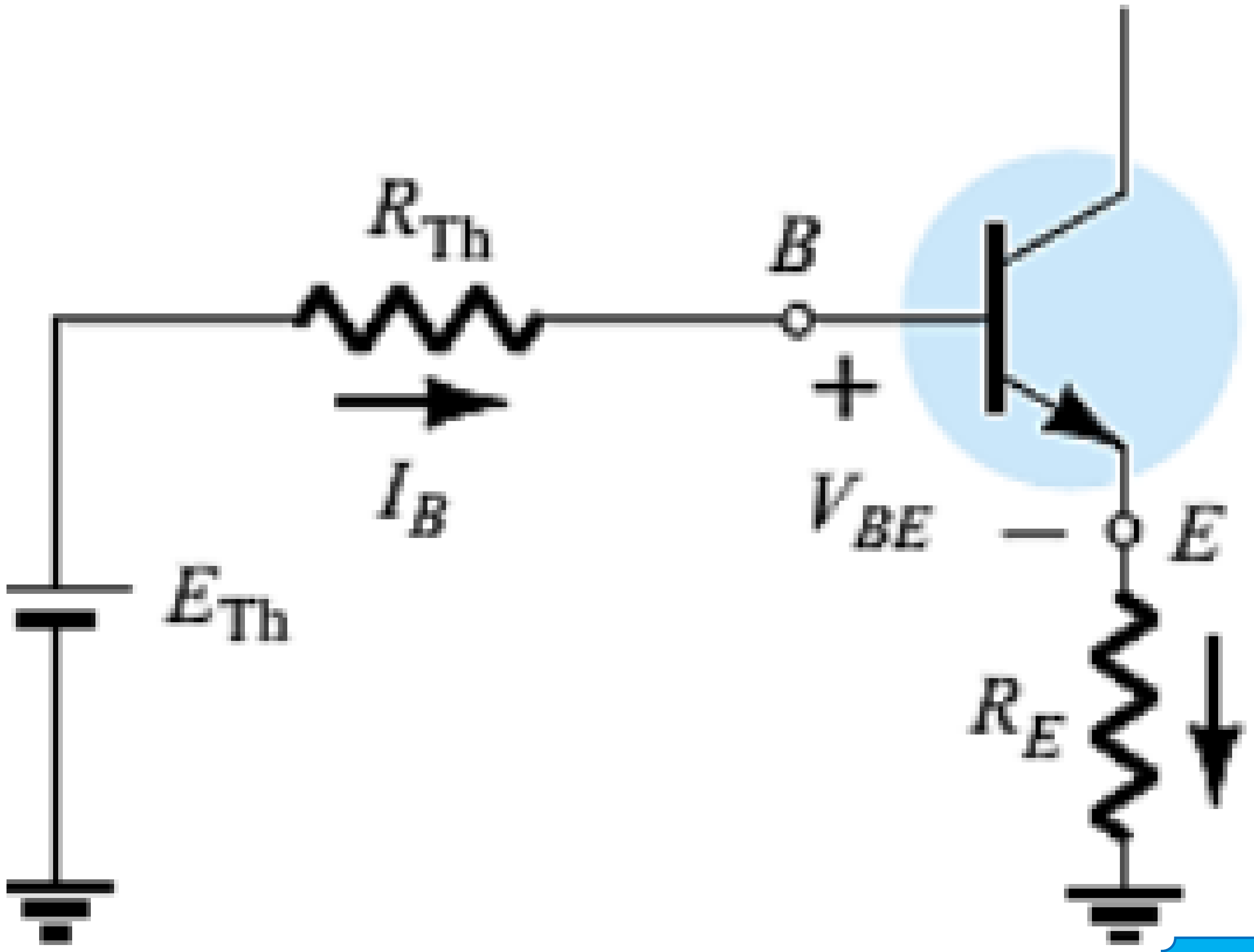




Exact Analysis :

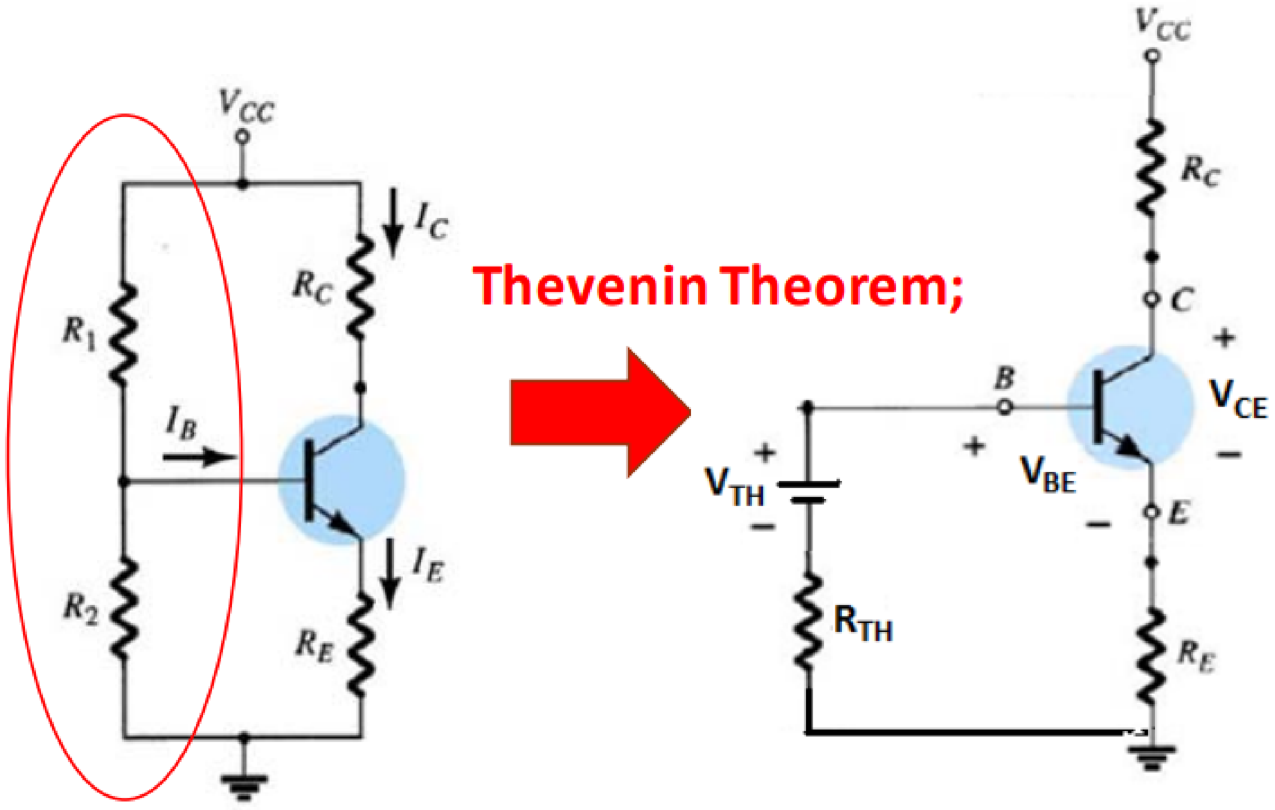
Base emitter loop

Base collector loop



VOLTAGE DIVIDER BIAS CIRCUIT

- 2nd step: : Simplified circuit using **Thevenin Theorem**



Simplified Circuit

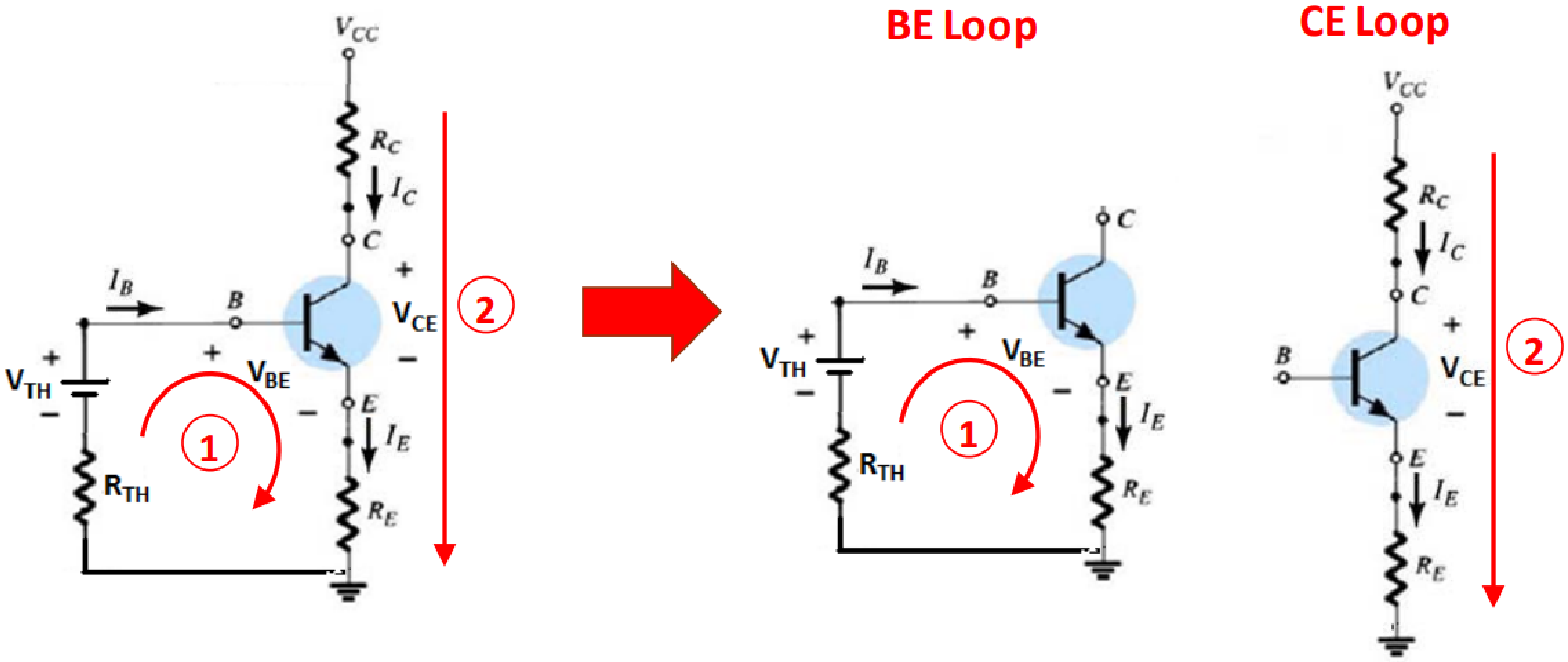
From Thevenin Theorem;

$$R_{TH} = R_1 // R_2 = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC}$$

VOLTAGE DIVIDER BIAS CIRCUIT

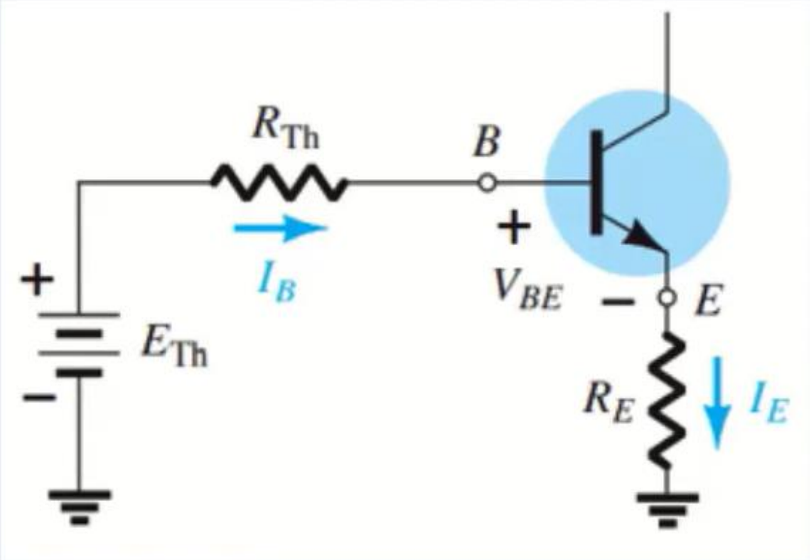
- 2nd step: Locate 2 main loops.



Analysis of Voltage-Divider Bias Configuration

I_{BQ} can be determined by first applying Kirchhoff's voltage law in the clockwise direction for the loop indicated:

$$-E_{Th} + I_B R_{Th} + V_{BE} + I_E R_E = 0$$



The Thevenin network

Substituting $I_E = (\beta + 1)I_B$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

Once I_B is known, the remaining quantities of the network can be found in the same manner as developed for the emitter-bias configuration. That is,

$$I_C = \frac{\beta(V_{Th} - V_{BE})}{R_{Th} + (\beta + 1)R_E}$$

and

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

The remaining equations for V_E, V_C, and V_B are also the same as obtained for the emitter-bias configuration.

Example: Determine the DC bias voltage V_{CE} and the current I_C for the voltage divider configuration of Figure 4.

Solution:

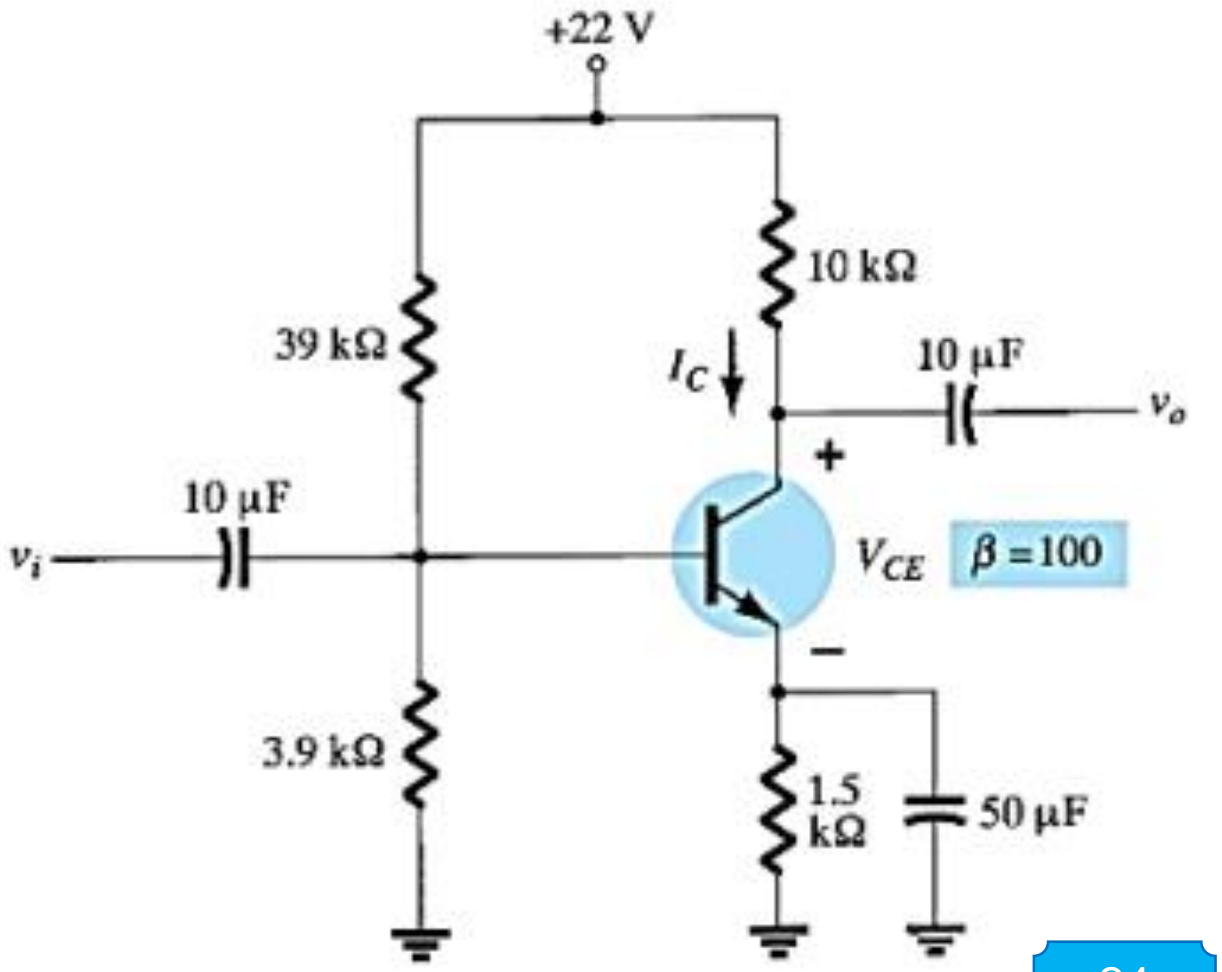
$$R_{Th} = R_1 \| R_2$$
$$= \frac{(39\,k\Omega)(3.9\,k\Omega)}{39\,k\Omega + 3.9\,k\Omega} = 3.55\,k\Omega$$

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$$
$$= \frac{(3.9\,k\Omega)(22\,V)}{39\,k\Omega + 3.9\,k\Omega} = 2\,V$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$
$$= \frac{2\,V - 0.7\,V}{3.55\,k\Omega + (101)(1.5\,k\Omega)} = \frac{1.3\,V}{3.55\,k\Omega + 151.5}$$
$$= 8.38\,\mu A$$

$$I_C = \beta I_B$$
$$= (100)(8.38\,\mu A)$$
$$= \mathbf{0.84\,mA}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 22\,V - (0.84\,mA)(10\,k\Omega + 1.5\,k\Omega)$$
$$= 22\,V - 9.66\,V$$
$$= \mathbf{12.34\,V}$$



Example:

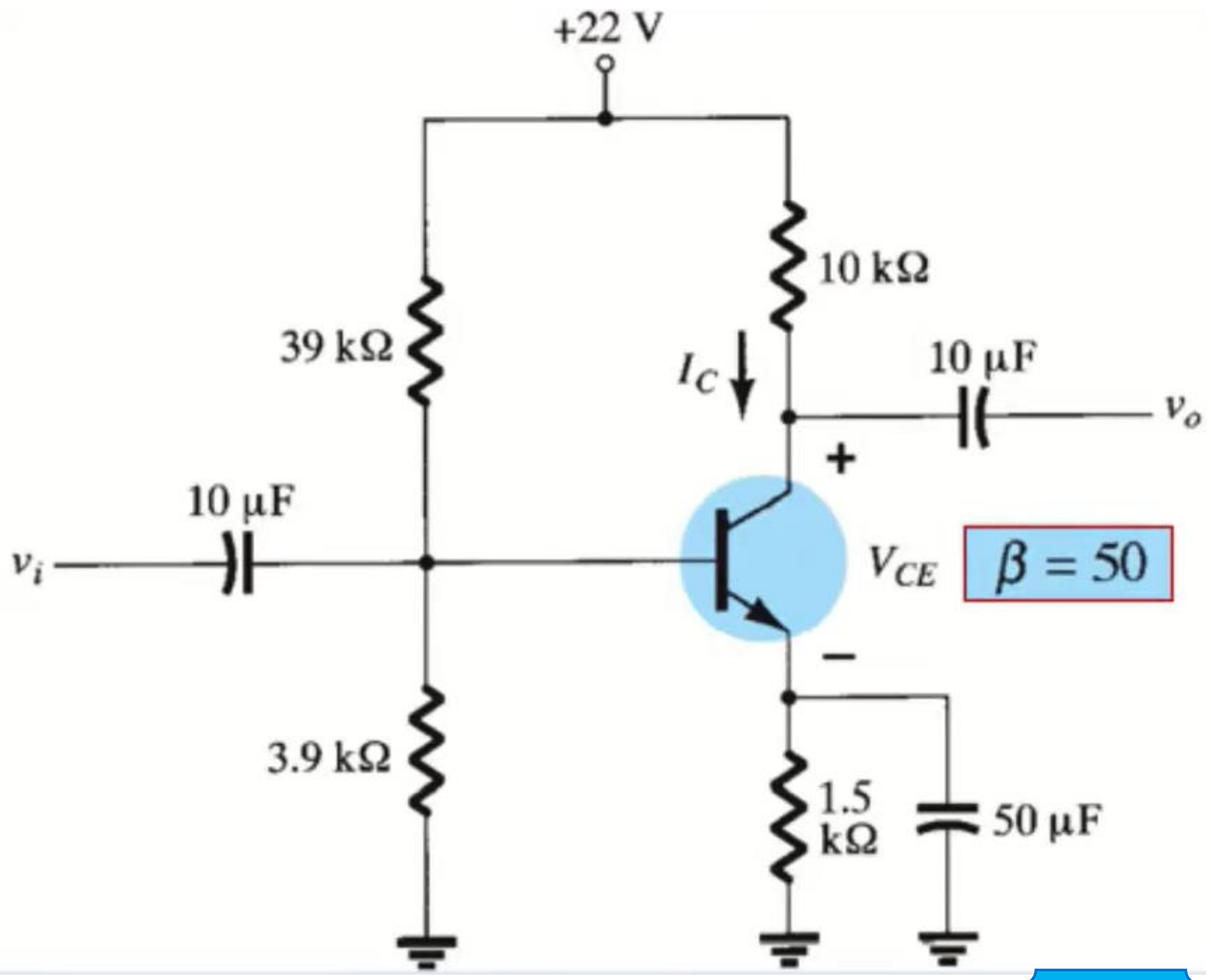
Repeat the exact analysis of the previous example if β is reduced to 50 and compare solutions for ICQ and VCEQ

$$R_{Th} = R_1 \| R_2$$

$$= \frac{(39\ k\Omega)(3.9\ k\Omega)}{39\ k\Omega + 3.9\ k\Omega} = 3.55\ k\Omega$$

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$= \frac{(3.9\ k\Omega)(22\ V)}{39\ k\Omega + 3.9\ k\Omega} = 2\ V$$



Solution:

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$= \frac{2\text{ V} - 0.7\text{ V}}{3.55\text{ k}\Omega + (\boxed{51})(1.5\text{ k}\Omega)}$$

$$= \frac{1.3\text{ V}}{3.55\text{ k}\Omega + 76.5\text{ k}\Omega} = 16.24\ \mu\text{A}$$

$$I_C = \beta I_B$$

$$= (50)(16.24\ \mu\text{A}) \boxed{= \mathbf{0.81\ mA}}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 22\text{ V} - (0.81\text{ mA})(10\text{ k}\Omega + 1.5\text{ k}\Omega)$$

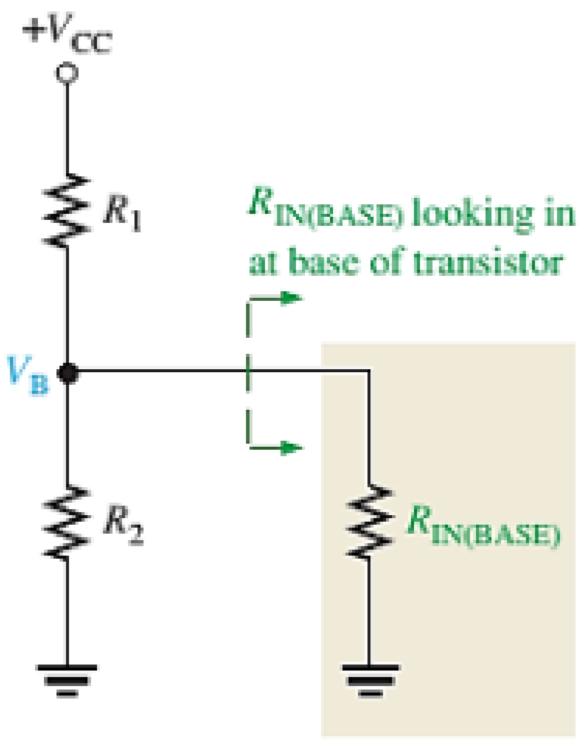
$$\boxed{= \mathbf{12.69\ V}}$$

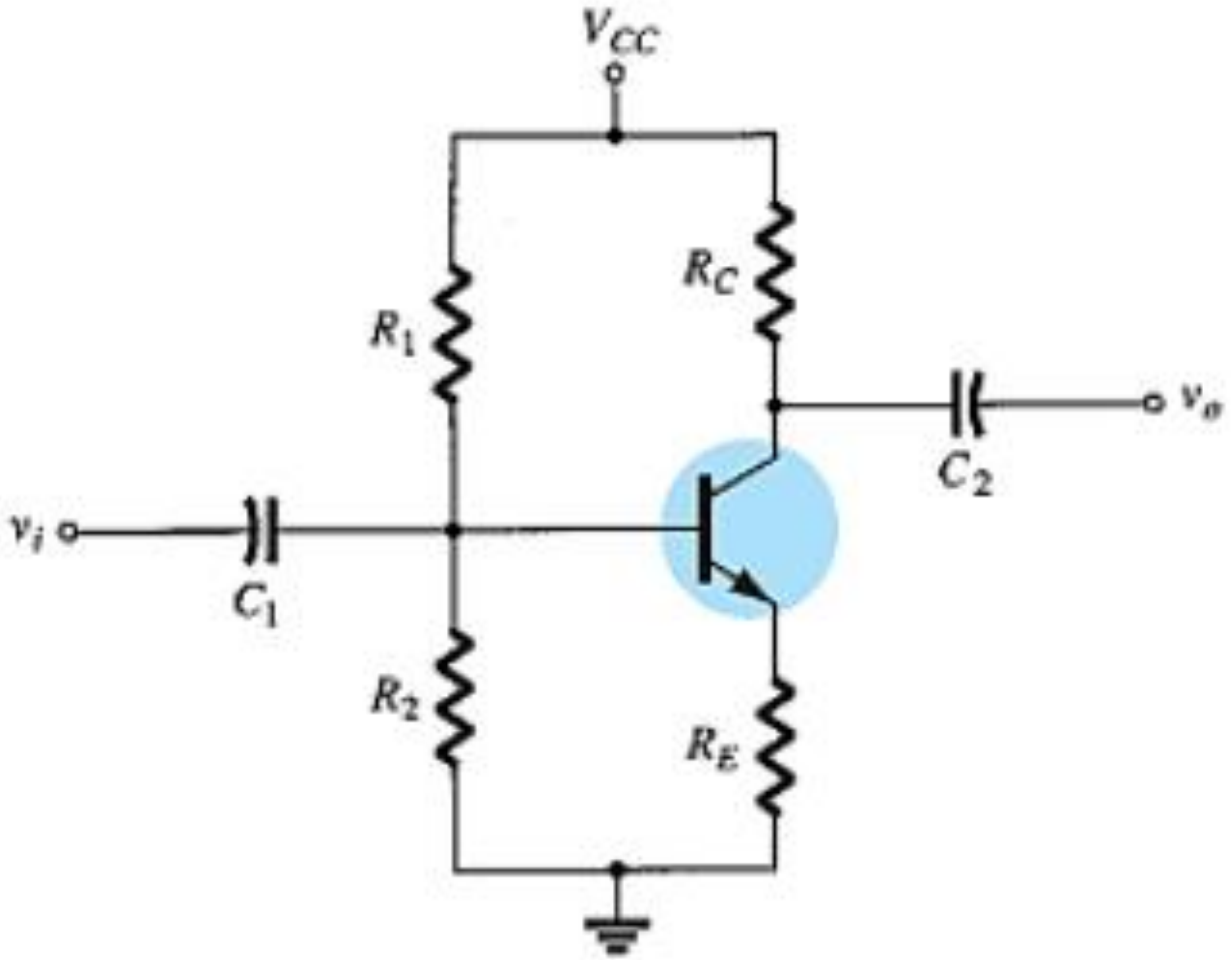
Effect of β variation on the response of the voltage-divider configuration

β	I_{C_Q} (mA)	V_{CE_Q} (V)
100	0.84 mA	12.34 V
50	0.81 mA	12.69 V

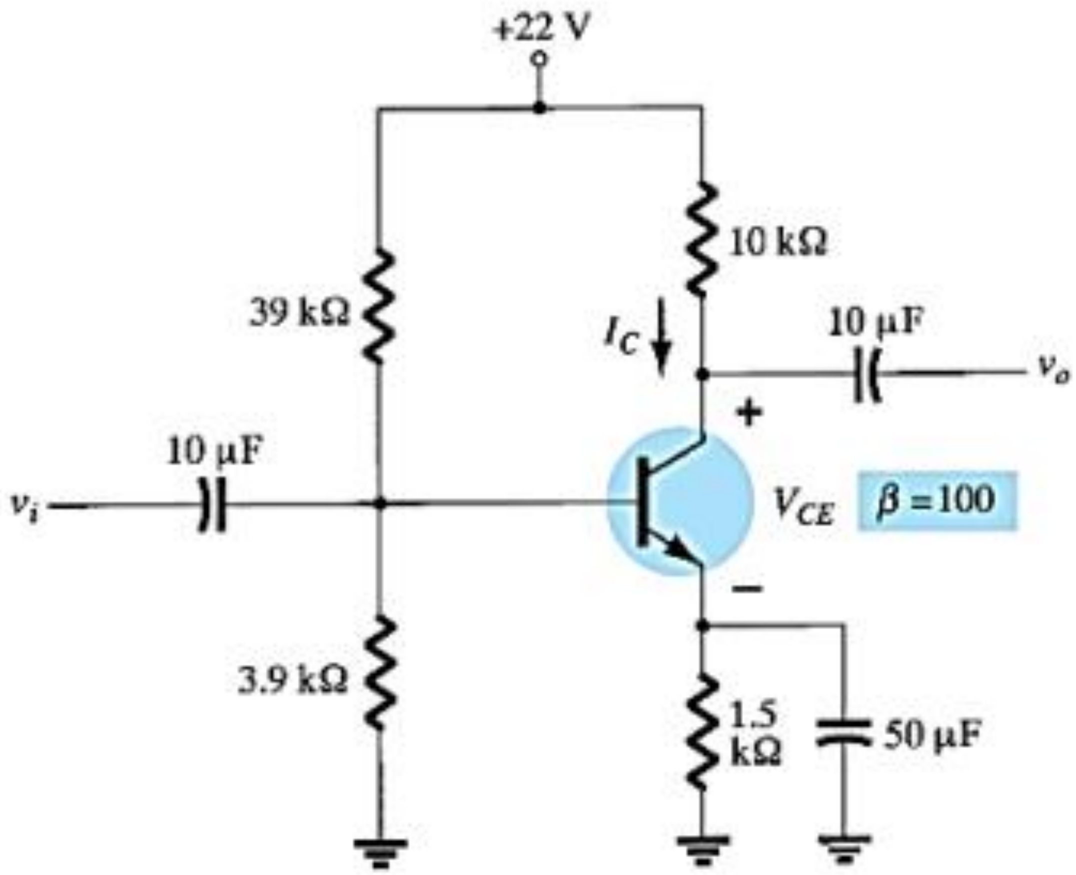
The results clearly show the relative insensitivity of the circuit to the change in β. Even though β is drastically cut in half, from 100 to 50, the levels of I_{CQ} and V_{CEQ} are essentially the same.

Approximate analysis:





Example: Repeat the analysis of figure using the approximate technique and compare solutions for I_{CQ} and V_{CEQ}.

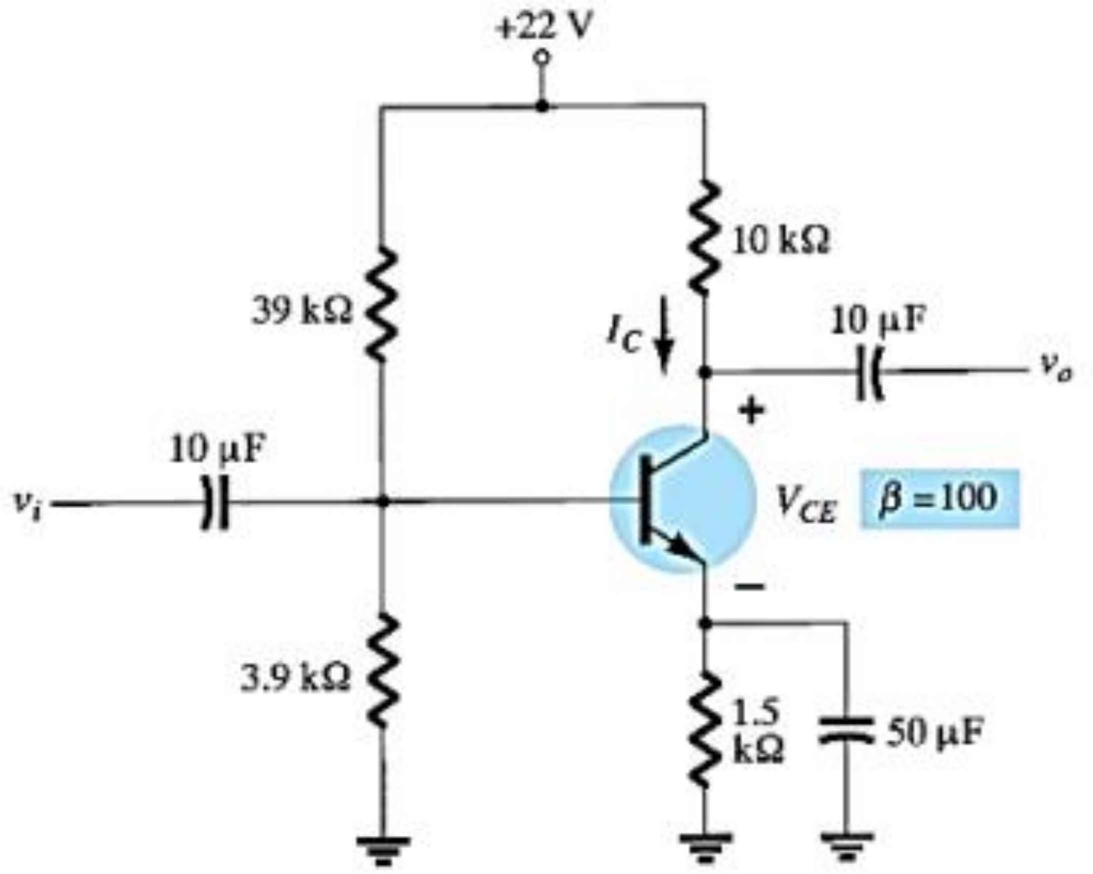


Example: Repeat the analysis of figure using the approximate technique and compare solutions for I_{CQ} and V_{CEQ}.

Solution:

$$\beta R_E \geq 10R_2$$
$$(100)(1.5\text{ k}\Omega) \geq 10(3.9\text{ k}\Omega)$$
$$150\text{ k}\Omega \geq 39\text{ k}\Omega \; (\textit{satisfied})$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(3.9\text{ k}\Omega)(22\text{ V})}{39\text{ k}\Omega + 3.9\text{ k}\Omega} = 2\text{ V}$$



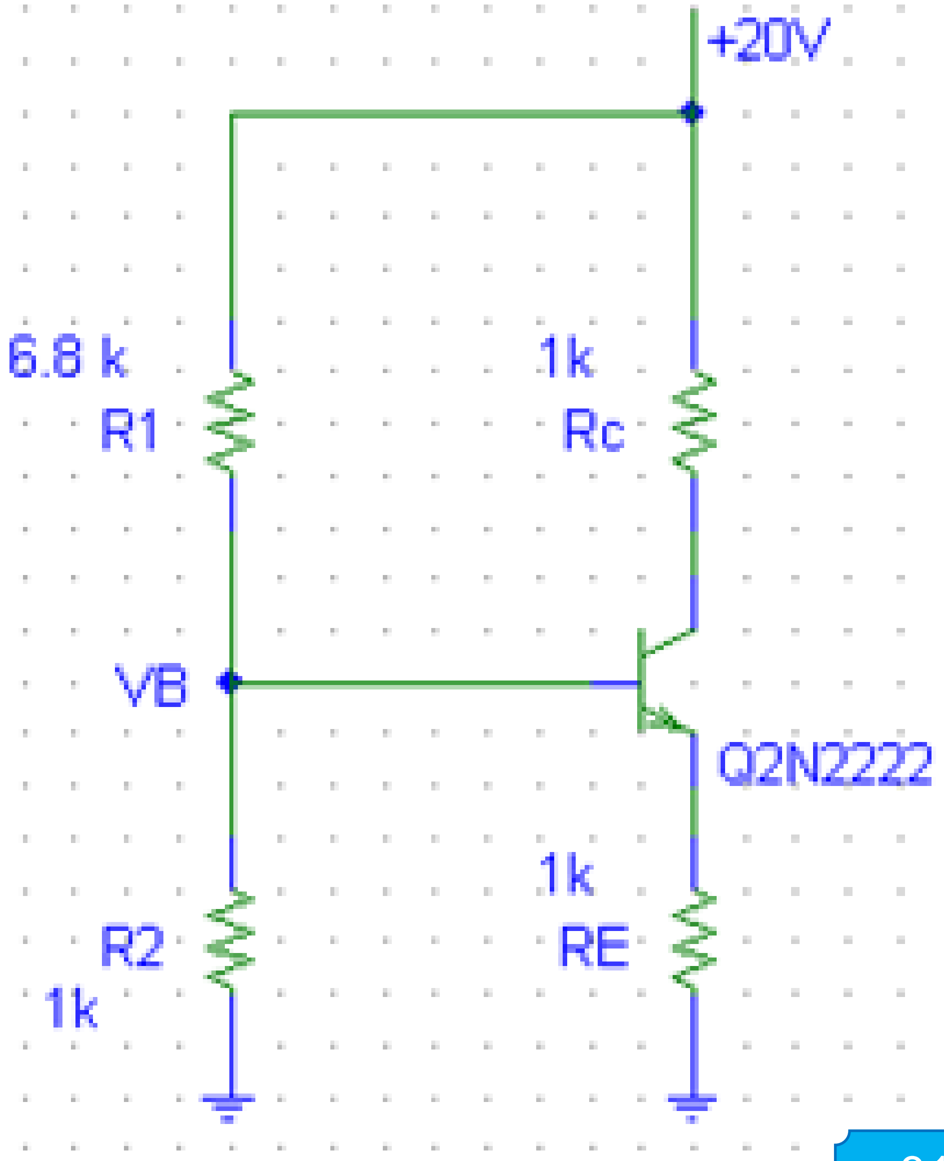
$$V_E = V_B - V_{BE} = 2\text{ V} - 0.7\text{ V} = 1.3\text{ V}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{1.3\text{ V}}{1.5\text{ k}\Omega} = \mathbf{0.867\text{ mA}}$$

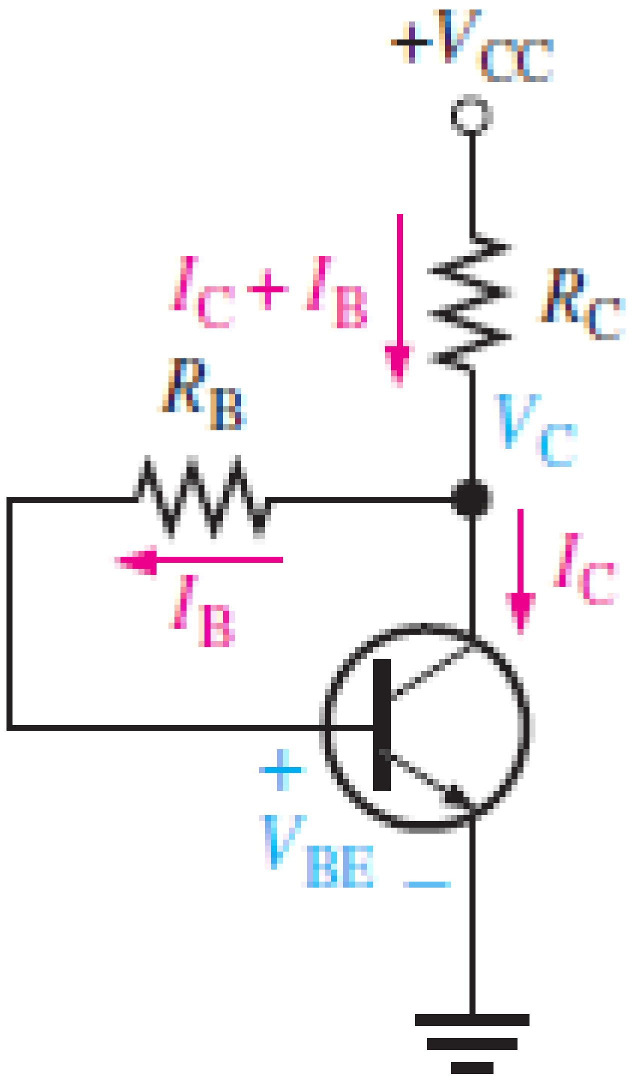
compared to 0.84 mA with the exact analysis. Finally,

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E) = 22\text{ V} - (0.867\text{ mA})(10\text{ kV} + 1.5\text{ k}\Omega) = 22\text{ V} - 9.97\text{ V} = \mathbf{12.03\text{ V}}$$

Home work: Determine V_{CE} and I_C in the voltage-divider biased transistor circuit. Assume β_{DC} = 50 and $I_E = I_B + I_C$.



Collector feedback Bias



Collector feedback Bias

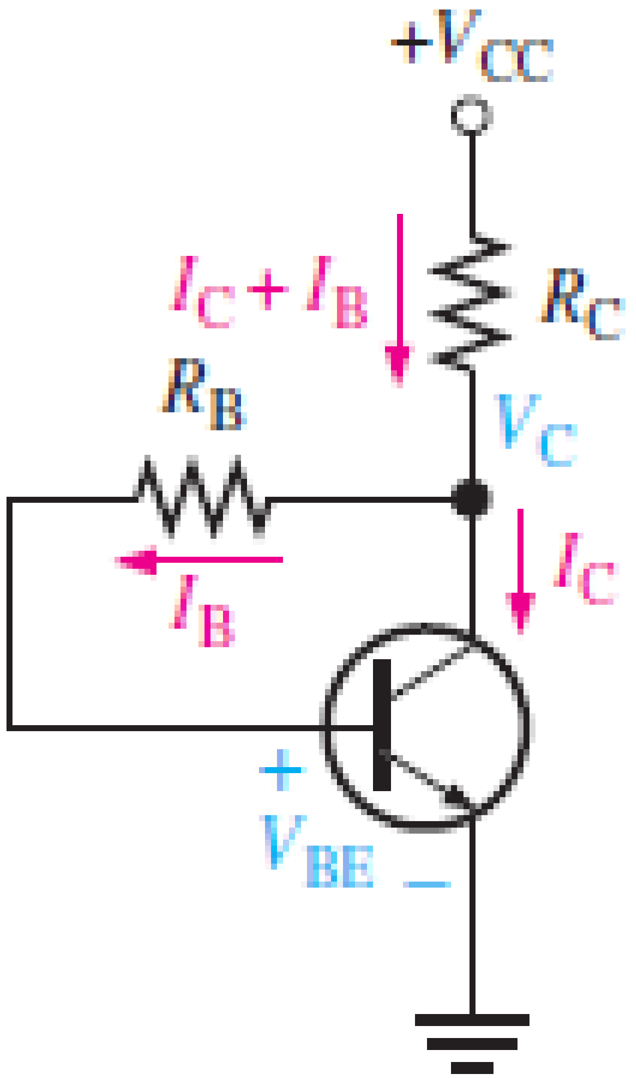
$$V_{CC} = V_{RC} + V_{RB} + V_{BE}$$
$$= (I_C + I_B)R_C + I_B R_B + V_{BE}$$
$$= \beta_{DC} I_B R_C + I_B R_C + I_B R_B + V_{BE}$$
$$= (\beta_{DC} + 1) I_B R_C + I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta_{DC} + 1) R_C}$$

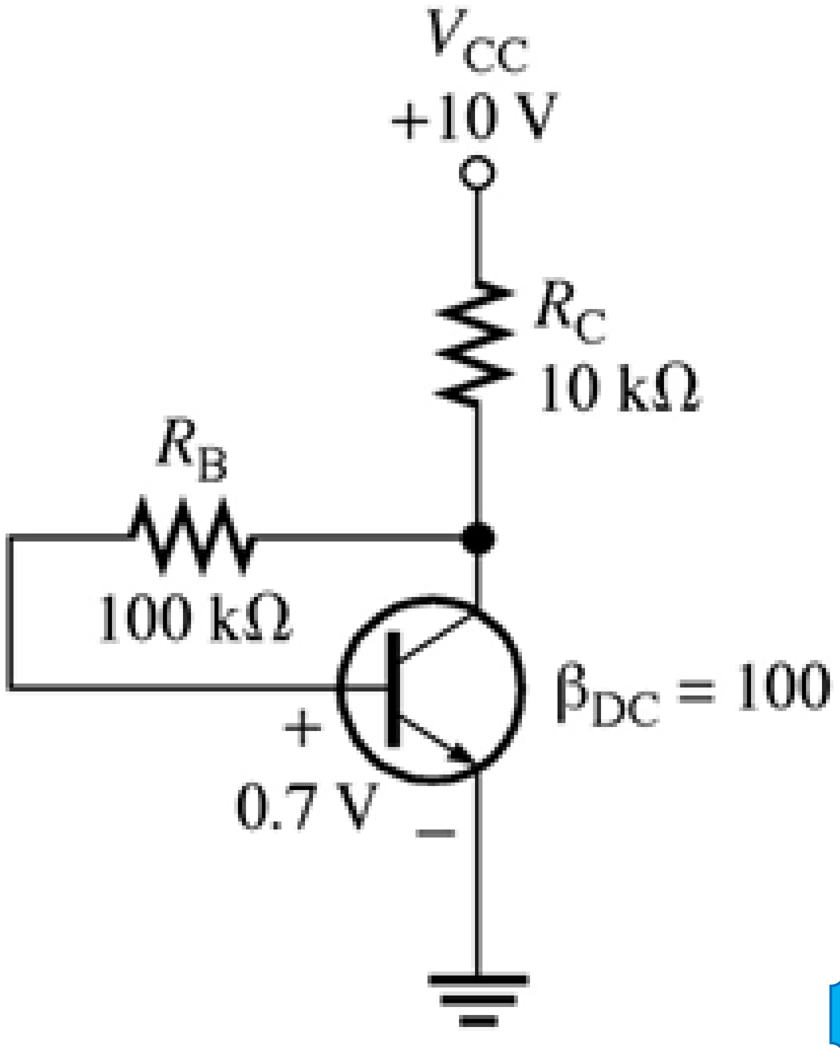
$$I_{CQ} = \frac{\beta_{DC}(V_{CC} - V_{BE})}{R_B + (\beta_{DC} + 1) R_C}$$

$$V_{CEQ} = V_{CC} - (I_{CQ} + I_B) R_C$$
$$\approx V_{CC} - I_{CQ} R_C \quad ; \beta_{DC} >> 1$$

$$\therefore V_{CE} \approx V_{CC} - I_C R_C$$



Example : Calculate the Q-point values (I_C and V_{CE}) for this circuit



Example : Calculate the Q-point values (I_C and V_{CE}) for this circuit

Solution:

at Q-point:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta_{DC} + 1)R_C} = \frac{10 - 0.7}{100 + (100 + 1)} = 8.38\ \mu A$$

$$I_C = \frac{\beta_{DC}(V_{CC} - V_{BE})}{R_B + (\beta_{DC} + 1)R_C} = 100 \times 8.38\ \mu A = 0.838\ \text{mA}$$

$$V_{CE} = V_{CC} - (I_C + I_B)R_C = 10 - (0.838 + 0.00838) \times 10$$
$$= 1.536\ \text{V}$$

$\therefore$ Q-point is at $I_C = 0.838$ mA and $V_{CE} = 1.536$ V

at cut off and saturation mode:

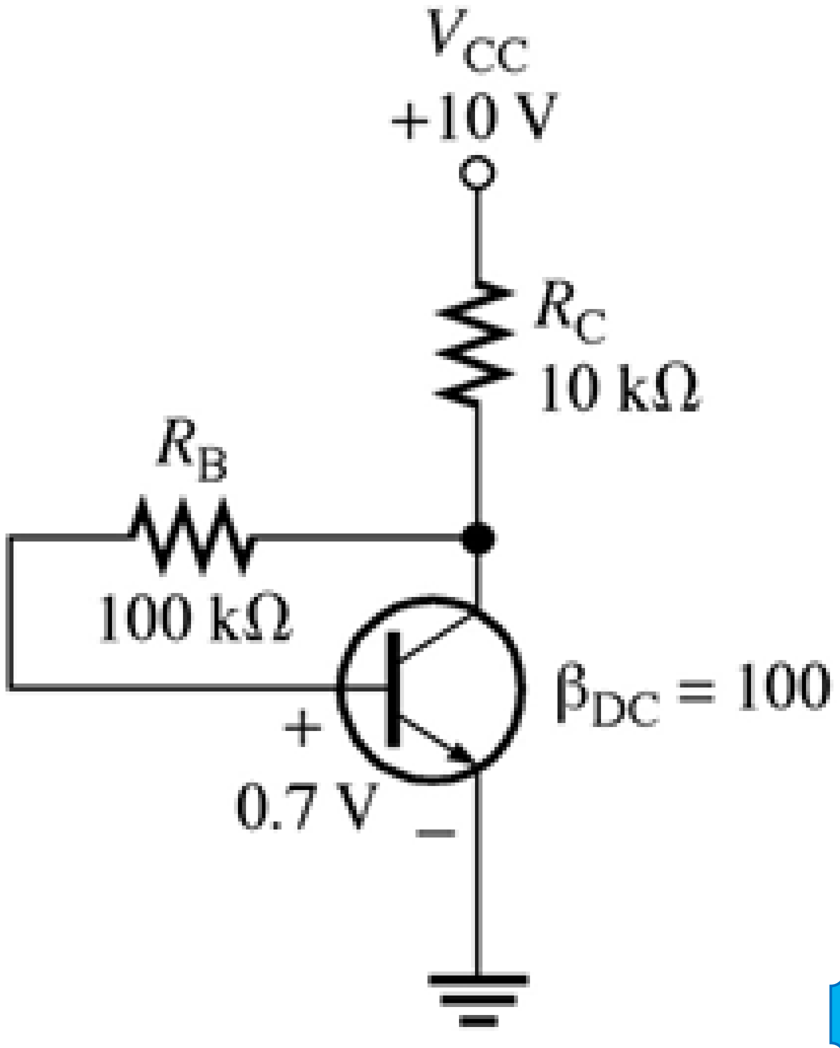
As $V_{CE} = V_{CC} - (I_C + I_B)R_C$

But we usually assume that $I_C >> I_B$ to find $I_{C(sat)}$ and $V_{CE(cutoff)}$

Therefore $V_{CE} \approx V_{CC} - I_C R_C$

$$\therefore\ I_{C(sat)} = \frac{V_{CC}}{R_C} = 1\ \text{mA}$$

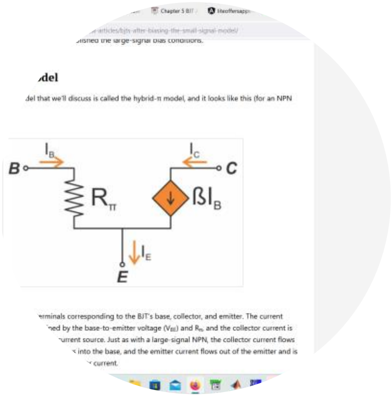
$$V_{CE(cutoff)} = V_{CC} = 10\ \text{V}$$



Ninevah University
College of Electronics Engineering
Department of Systems and Control

Electronic I
Lecture 5

AC analysis of BJT



2nd Class

by
Rafal Raed Mahmood Alshaker

AC analysis of BJT

Outlines of Presentation

BJT Transistor Modeling

- Hybrid equivalent model
- re model

Important Parameters

- Input Impedance Zi
- Output Impedance Z_o
- Voltage gain A_V:
- current gain A_i
- Phase Relationship

THE *re* TRANSISTOR MODEL

- Common Base Configuration
- Common Emitter Configuration
- Common Collector Configuration

BJT Transistor Modeling

A model is a combination of circuit elements, properly chosen, that best approximates the actual behavior of a semiconductor device under specific operating conditions.

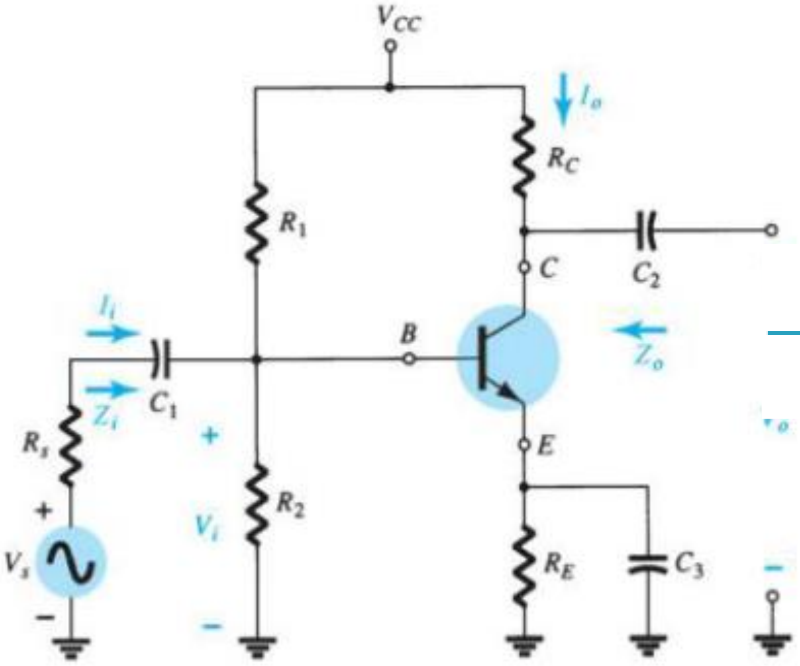
There are 2 models commonly used in small signal AC analysis of a transistor:

- Hybrid equivalent model
- re model

BJT Transistor Modeling

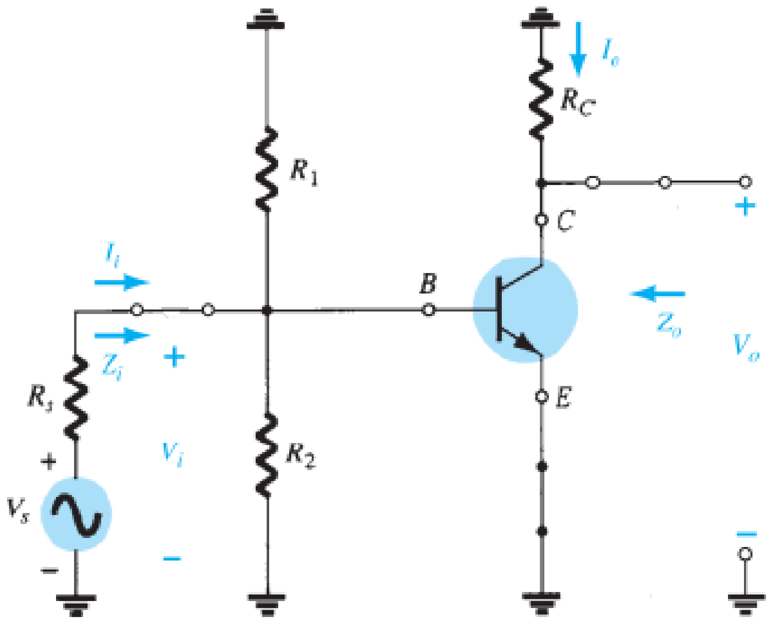
The ac equivalent of a transistor network is obtained by:

1. Setting all dc sources to zero and replacing them by a short-circuit equivalent
2. Replacing all capacitors by a short-circuit equivalent
3. Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 and 2
4. Redrawing the network in a more convenient and logical form

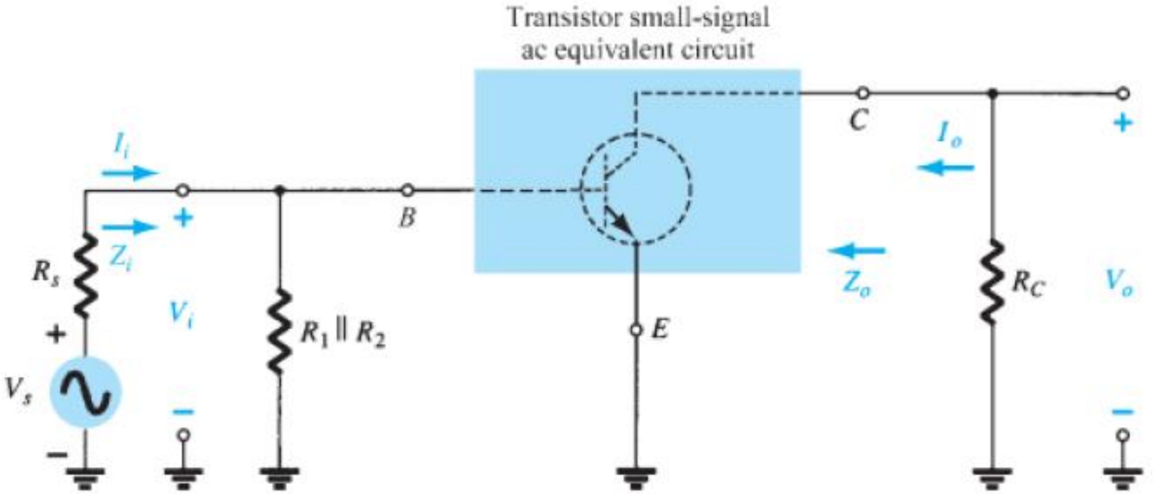


V_{CC}
I_o
R_C
R_1
C_2
C
I_i
B
Z_o
C_1
Z_i
R_s
E
+
V_i
R_2
R_E
C_3
V_s
–

Ac analysis

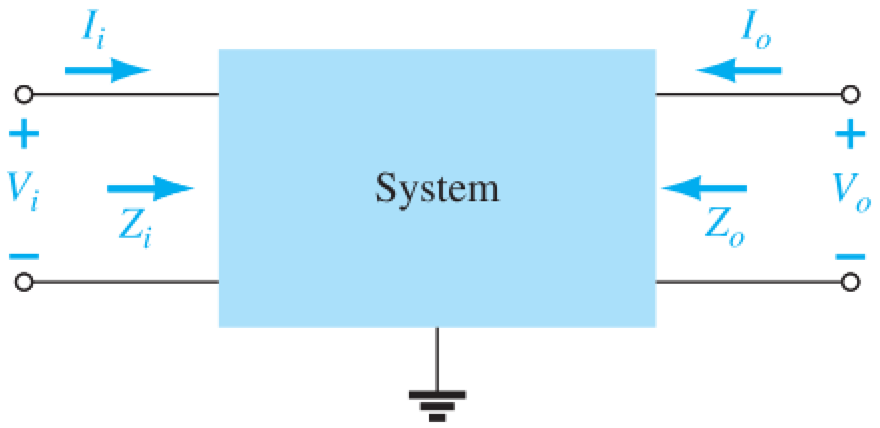


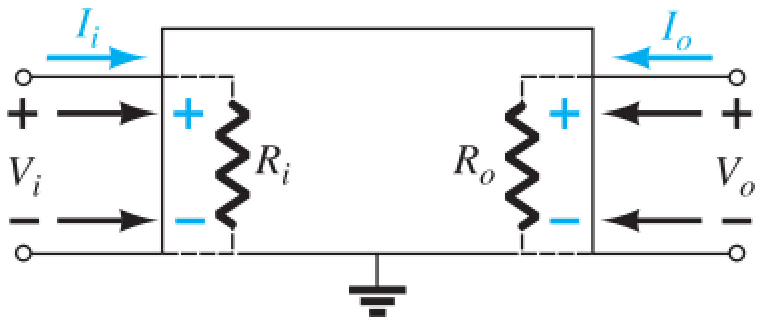
I_o
R_C
R_1
C
+
I_i
B
Z_o
Z_i
V_o
R_s
E
V_i
R_2
V_s
–



Transistor small-signal
ac equivalent circuit
C
I_i
I_o
+
B
Z_i
Z_o
R_s
R_C
V_o
V_i
$R_1 \| R_2$
E
V_s
–

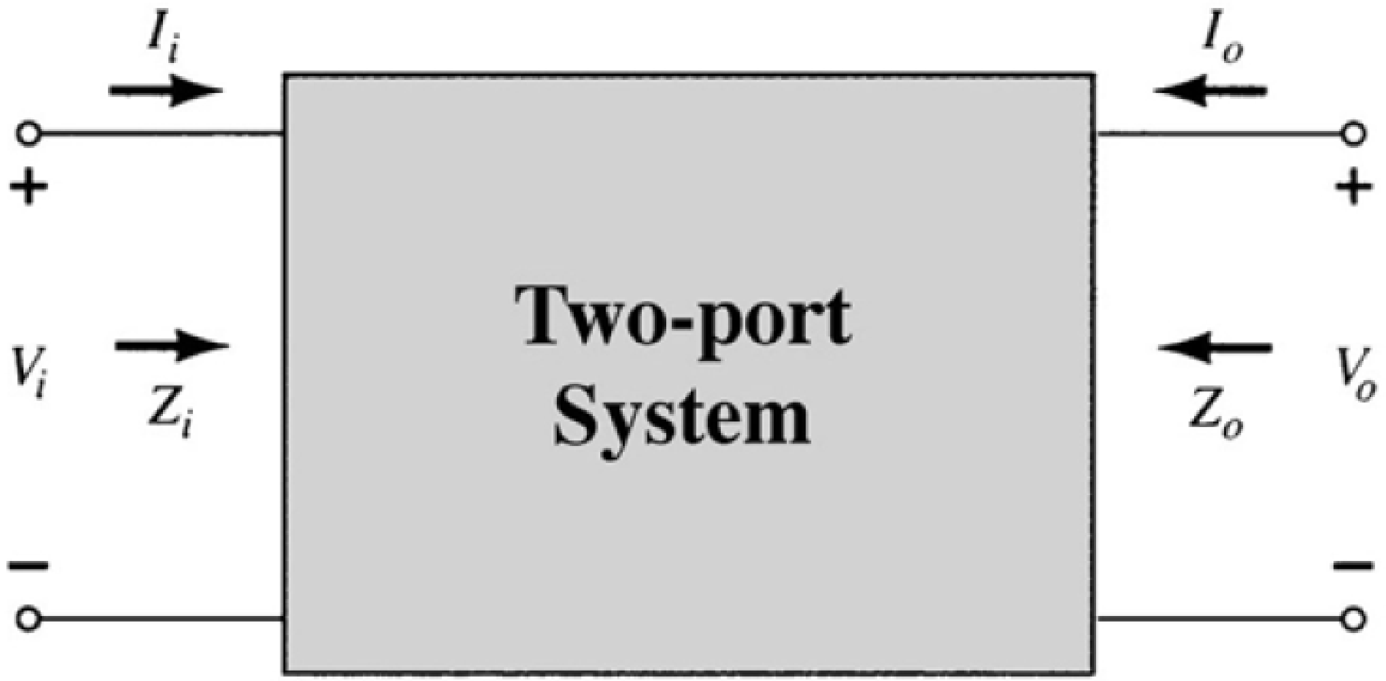
Defining the important parameters of any system.





Important Parameters

Z_i, Z_o, A_v, A_i are important parameters for the analysis of the AC characteristics of a transistor circuit.



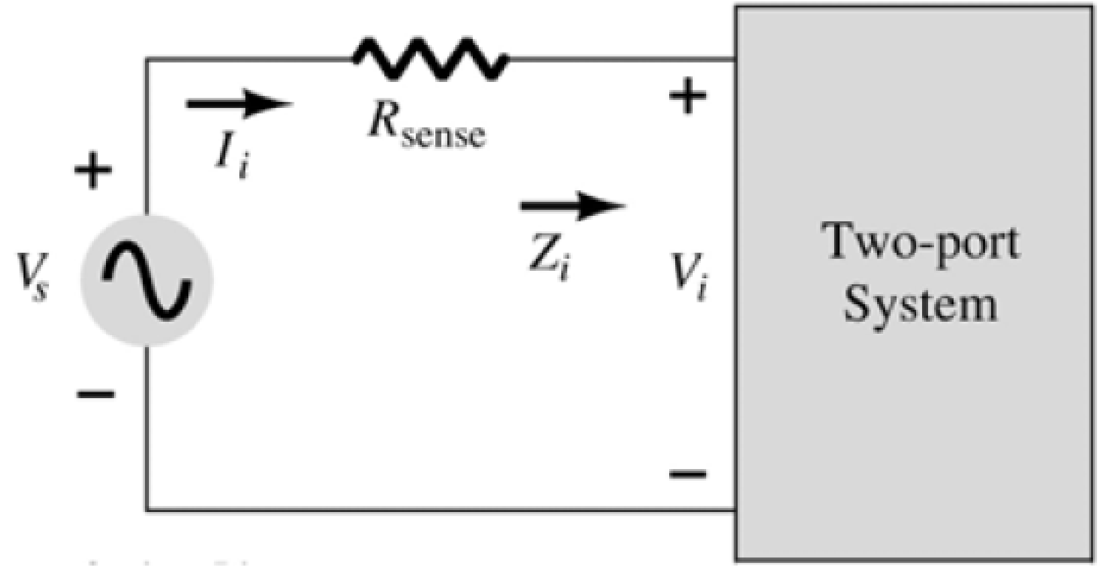
Input Impedance Z_i

To determine I_i: insert a "sensing resistor"

$$Z_i = \frac{V_i}{I_i}$$

then calculate I_i:

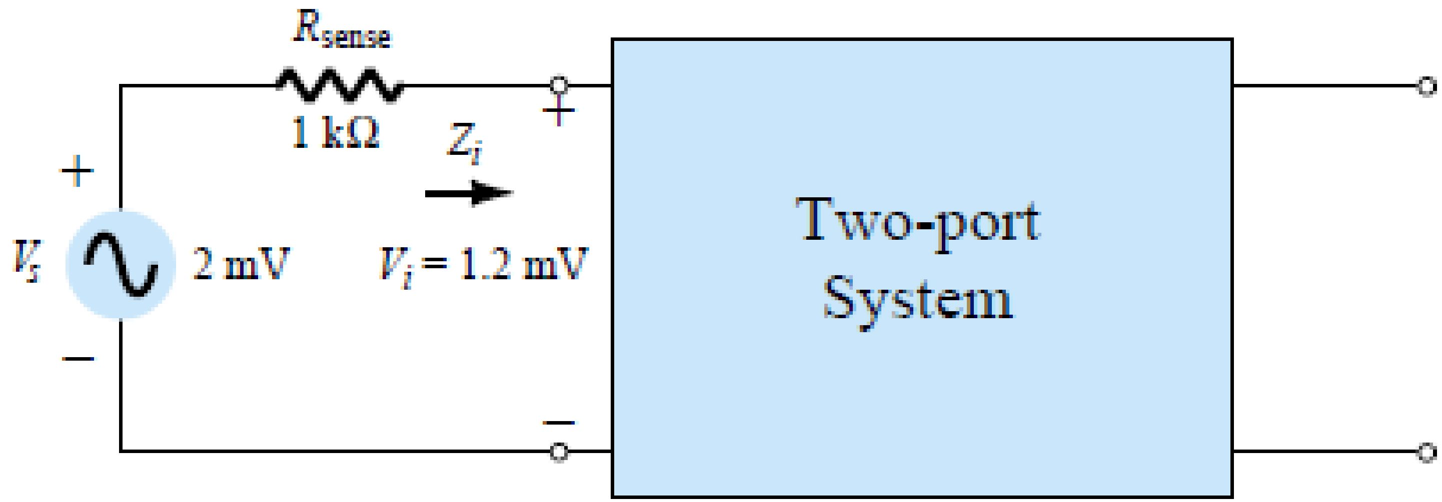
$$I_i = \frac{V_s - V_i}{R_{sense}}$$



The input impedance of a BJT transistor amplifier can vary from a few ohms to megohms.

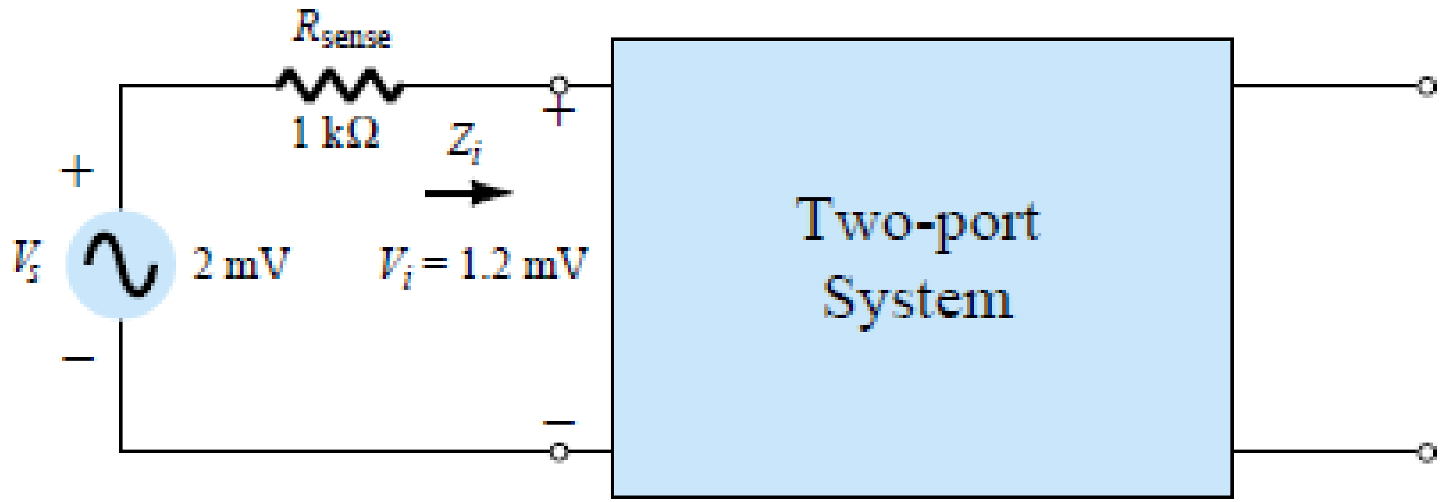
Example: For the system of Figure 1 determine the level of input impedance.

Solution:



Example: For the system of Figure 1 determine the level of input impedance.

Solution:



$$I_i = \frac{V_s - V_i}{R_{sense}} = \frac{2\ \text{mV} - 1.2\ \text{mV}}{1\ \text{k}\Omega} = \frac{0.8\ \text{mV}}{1\ \text{k}\Omega} = 0.8\ \mu\text{A}$$

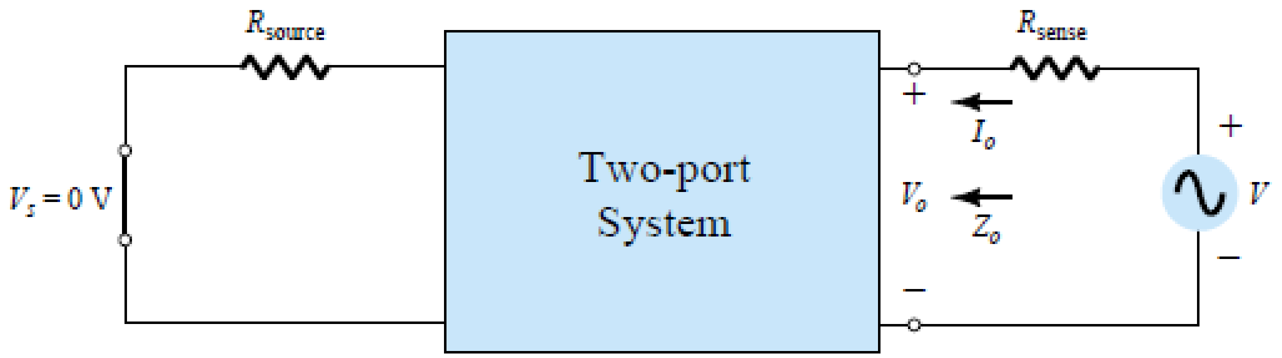
$$Z_i = \frac{V_i}{I_i} = \frac{1.2\ \text{mV}}{0.8\ \mu\text{A}} = 1.5\ \text{k}\Omega$$

Output Impedance Z_o

The output impedance is determined at the output terminals looking back into the system with the applied signal set to zero.

$$I_o = \frac{V - V_o}{R_{sense}}$$

$$Z_o = \frac{V_o}{I_o}$$

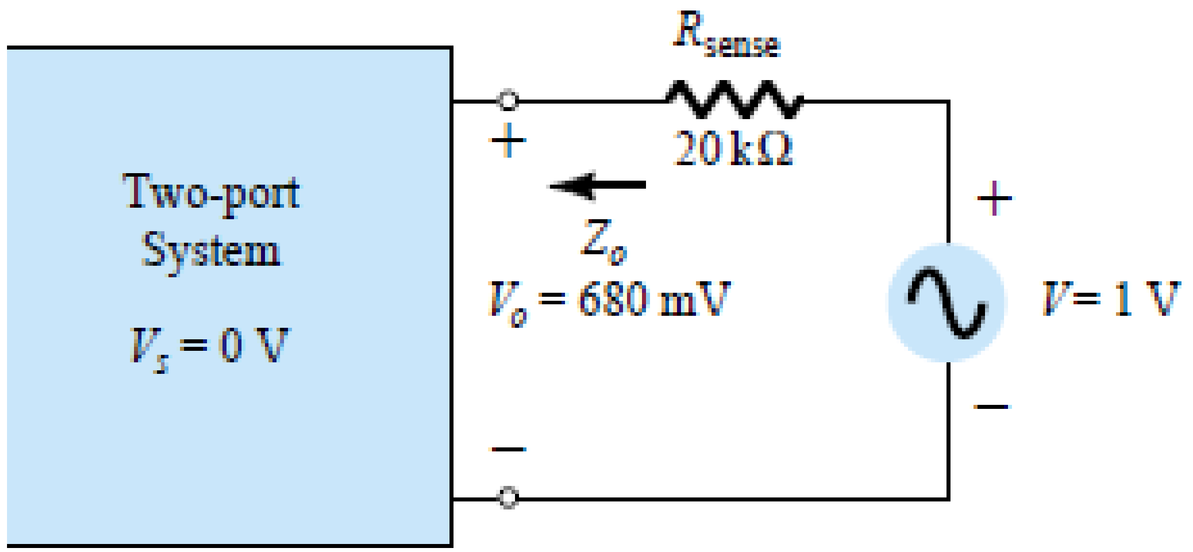


The output impedance of a BJT transistor amplifier is resistive in nature and depending on the configuration and the placement of the resistive elements, Zo, can vary from a few ohms to a level that can exceed 2 MΩ.

Example:

Determine the level of output impedance

Solution:



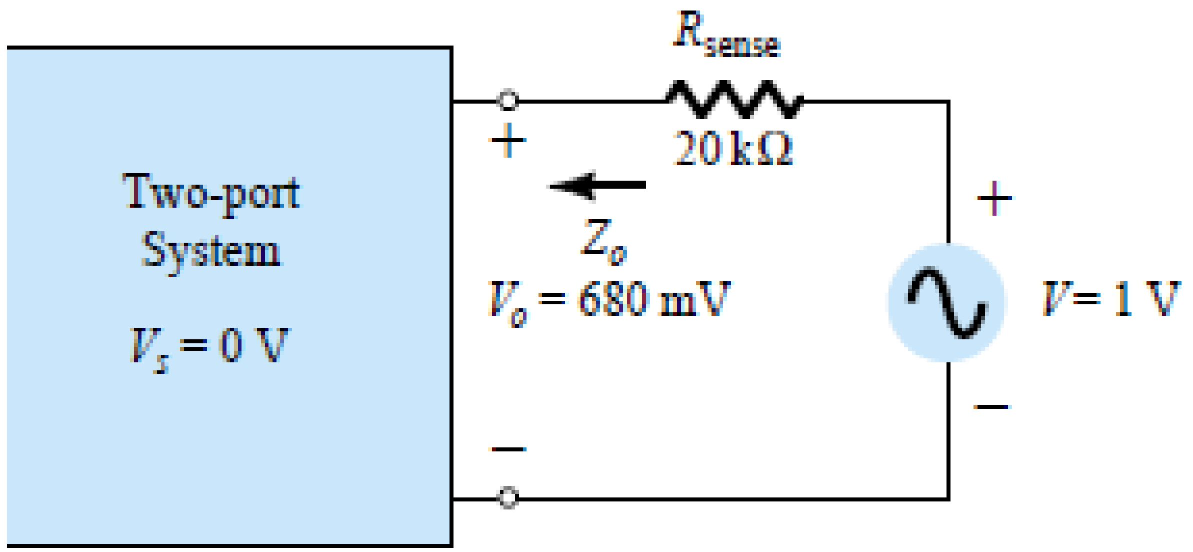
Example:

Determine the level of output impedance

Solution:

$$I_o = \frac{V - V_o}{R_{sense}} = \frac{1\text{ V} - 680\text{ mV}}{20\text{ k}\Omega} = \frac{320\text{ mV}}{20\text{ k}\Omega} = 16\ \mu\text{A}$$

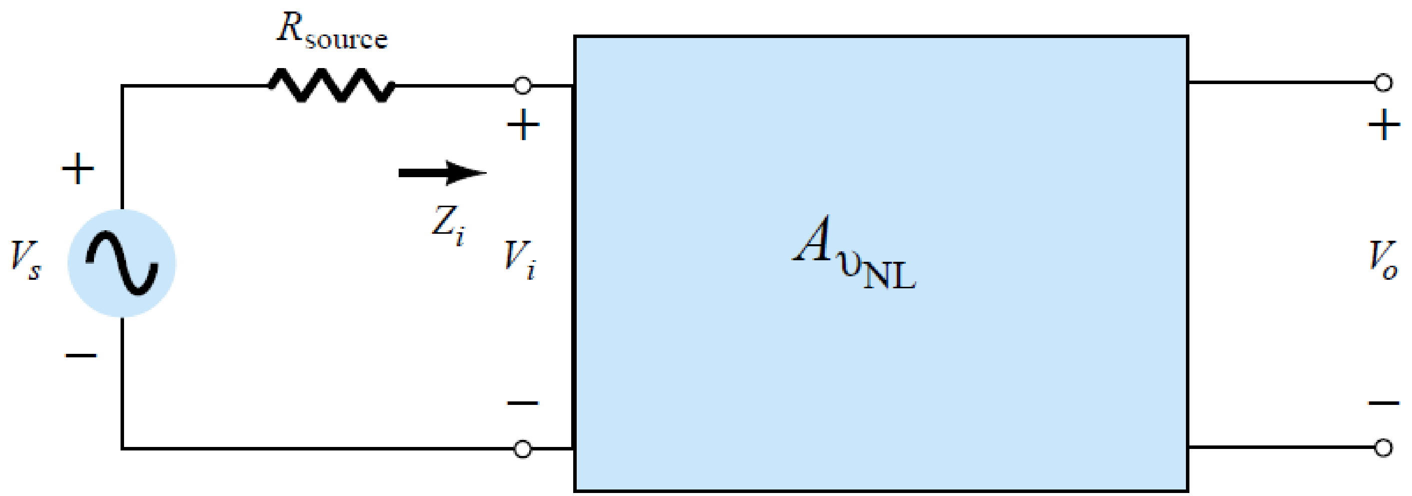
$$Z_o = \frac{V_o}{I_o} = \frac{680\text{ mV}}{16\ \mu\text{A}} = 42.5\text{ k}\Omega$$



Voltage gain AV:

For the transistor amplifier, the no load voltage gain is **greater** than the loaded voltage gain

$$A_v = \frac{V_o}{V_i}$$



$$V_i = \frac{Z_i V_s}{Z_i + R_s}$$

$$\frac{V_i}{V_s} = \frac{Z_i}{Z_i + R_s}$$

$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_i}{V_s} \cdot \frac{V_o}{V_i}$$

$$A_{v_s} = \frac{V_o}{V_s} = \frac{Z_i}{Z_i + R_s} A_{v_{NL}}$$

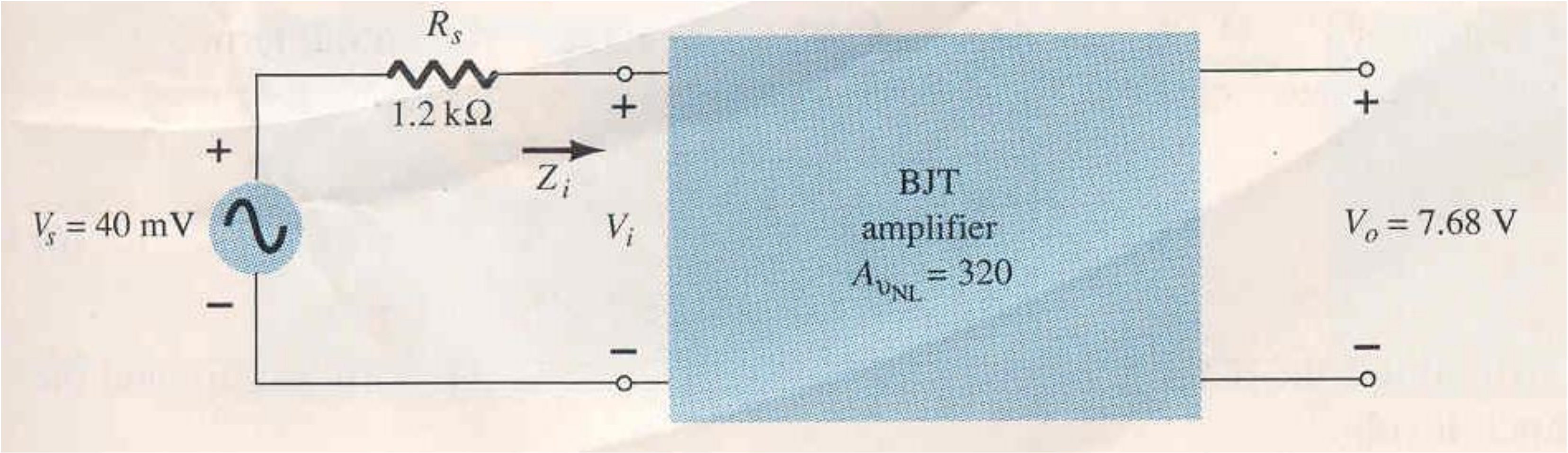
Example: For the BJT amplifier of Figure 2, determine

(a) V_i.

(b) I_i.

(c) Z_i.

(d) A_{vs}.



Solution:

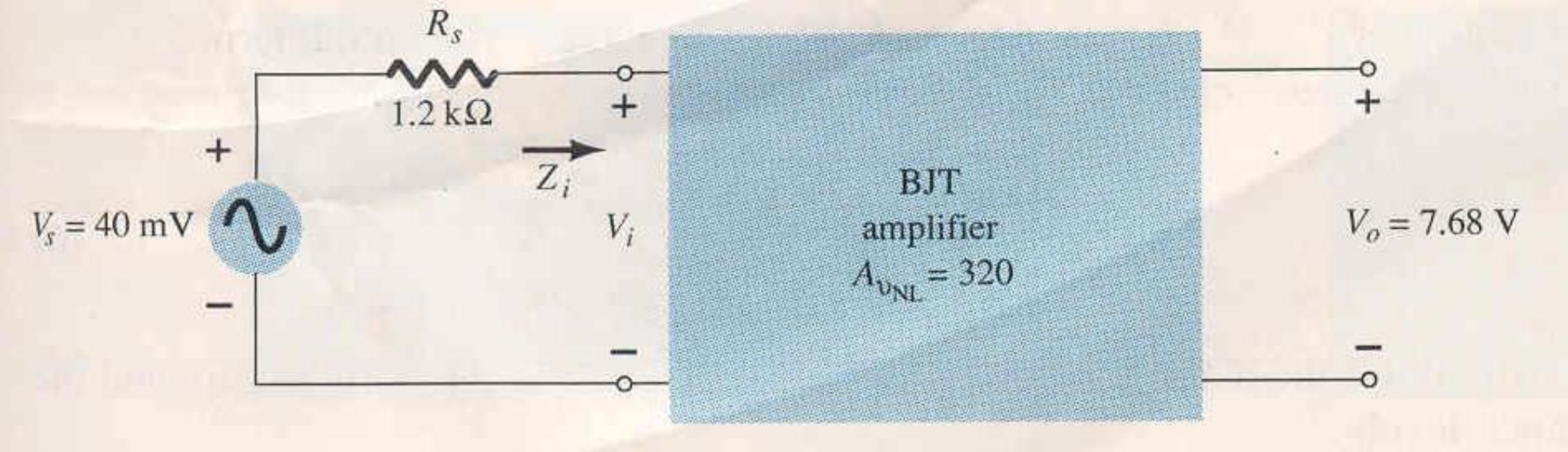
Example: For the BJT amplifier of Figure 2, determine

(a) V_i.

(b) I_i.

(c) Z_i.

(d) A_{vs}.



Solution:

$$\text{(a)}\quad A_{v_{NL}} = \frac{V_o}{V_i} \text{ and } V_i = \frac{V_o}{A_{v_{NL}}} = \frac{7.68\text{ V}}{320} = \mathbf{24\text{ mV}}$$

$$\text{(b)}\quad I_i = \frac{V_s - V_i}{R_s} = \frac{40\text{ mV} - 24\text{ mV}}{1.2\text{ k}\Omega} = \mathbf{13.33\ \mu A}$$

$$\text{(c)}\quad Z_i = \frac{V_i}{I_i} = \frac{24\text{ mV}}{13.33\ \mu\text{A}} = \mathbf{1.8\text{ k}\Omega}$$

$$\text{(d)}\quad A_{v_s} = \frac{Z_i}{Z_i + R_s} A_{v_{NL}}$$

$$= \frac{1.8\text{ k}\Omega}{1.8\text{ k}\Omega + 1.2\text{ k}\Omega}(320)$$

$$= \mathbf{192}$$

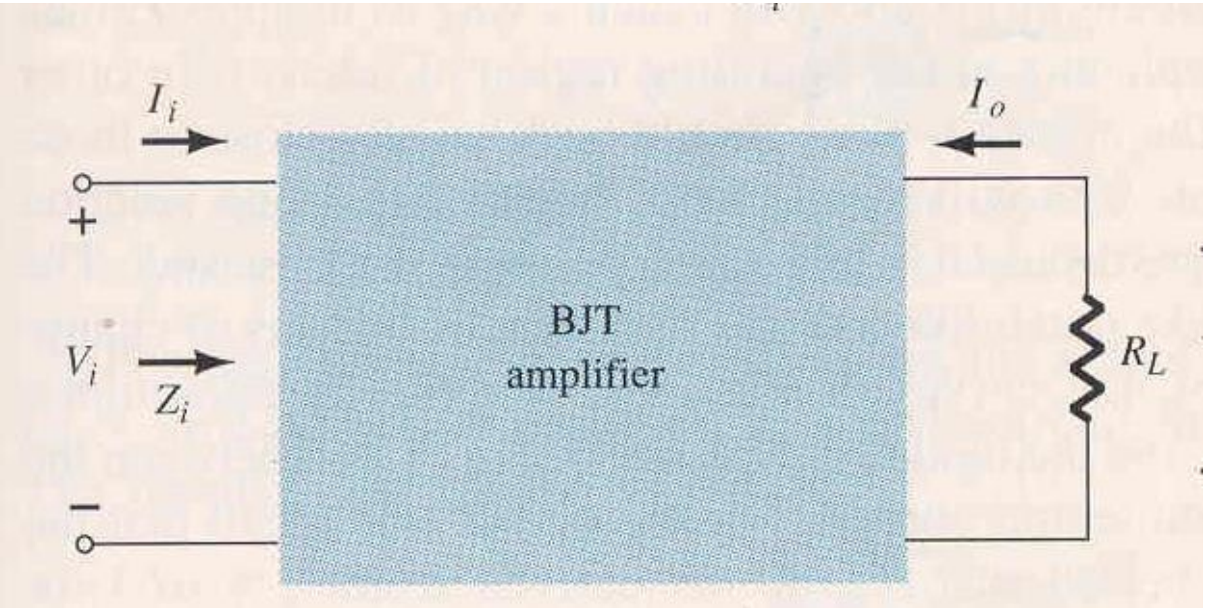
current gain A_i

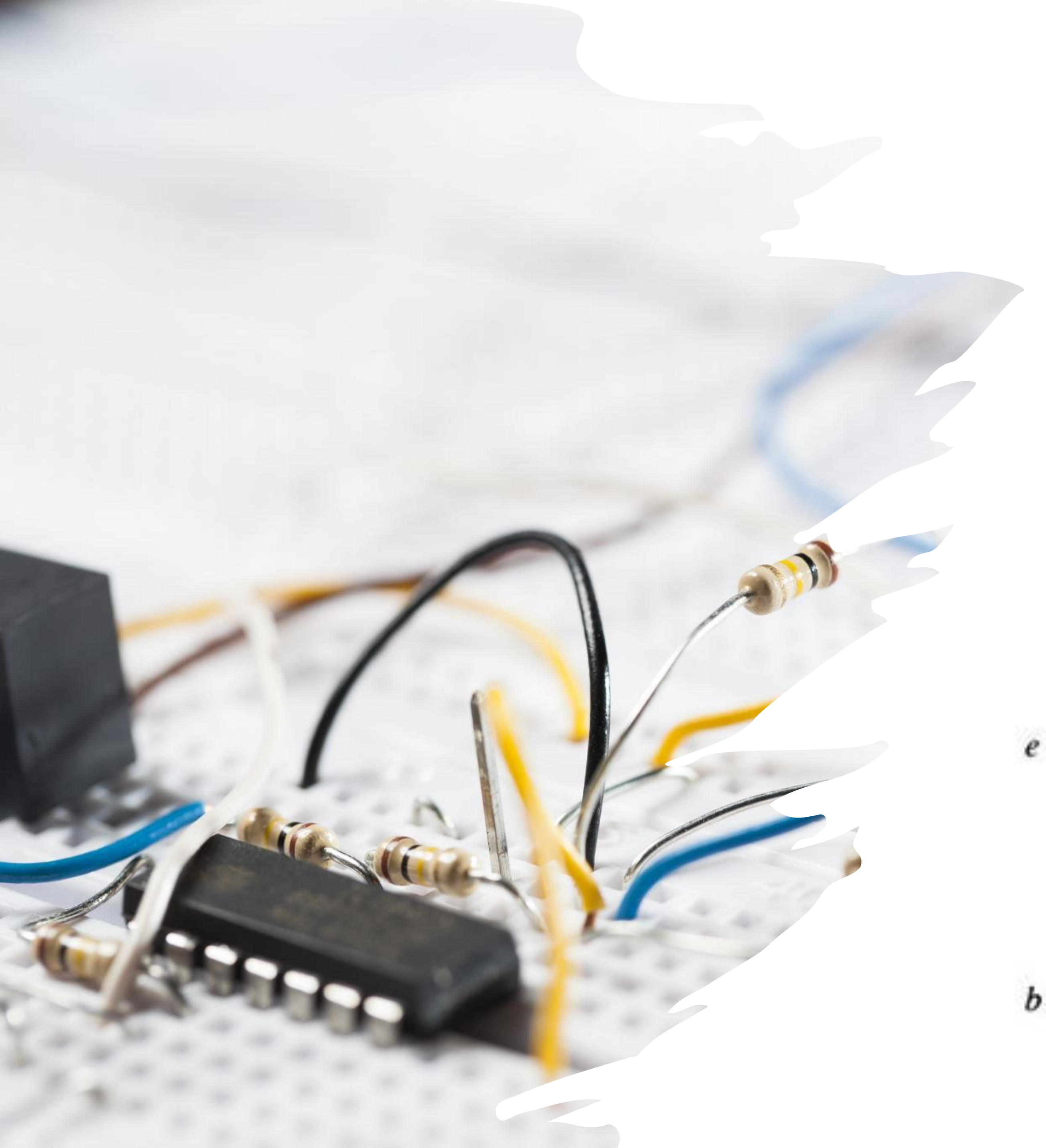
$$A_i = \frac{I_o}{I_i}$$

$$I_i = \frac{V_i}{Z_i} \quad \text{and} \quad I_o = -\frac{V_o}{R_L}$$

$$A_i = \frac{I_o}{I_i} = -\frac{V_o/R_L}{V_i/Z_i} = -\frac{V_o Z_i}{V_i R_L}$$

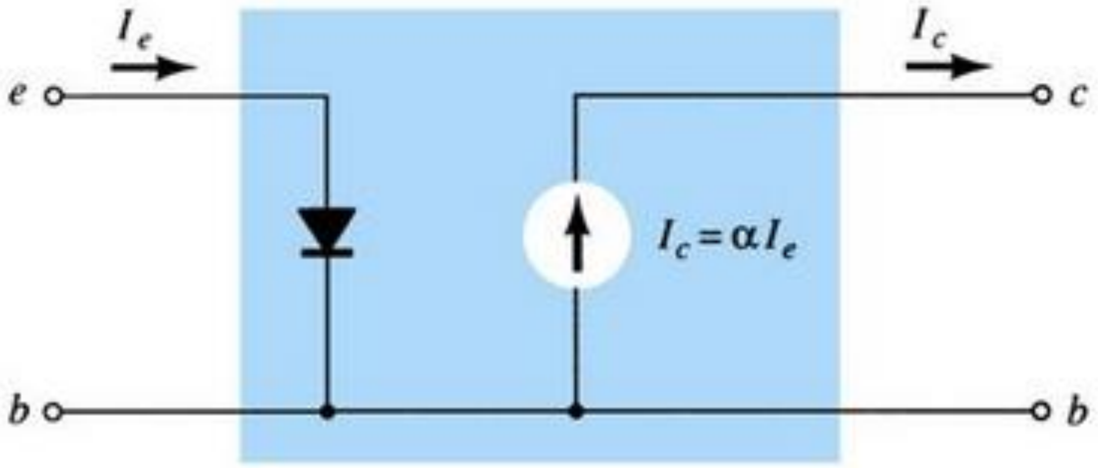
$$A_i = -A_v \frac{Z_i}{R_L}$$





THE *re* TRANSISTOR MODEL

- The re model employs a diode and controlled current source to duplicate the behavior of a transistor in the region of interest. BJT transistor amplifiers are referred to as current-controlled devices.



Common Base Configuration

The ac resistance of a diode can be determined by the equation

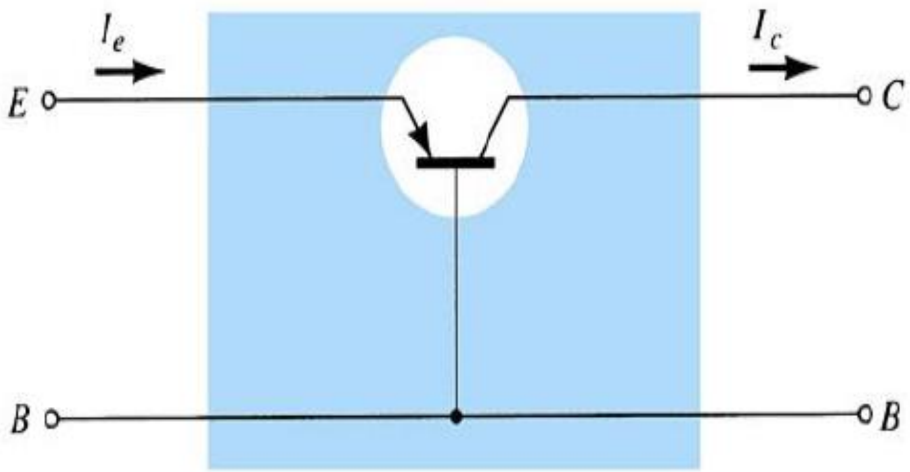
$$r_e = \frac{26\text{ mV}}{I_E}$$

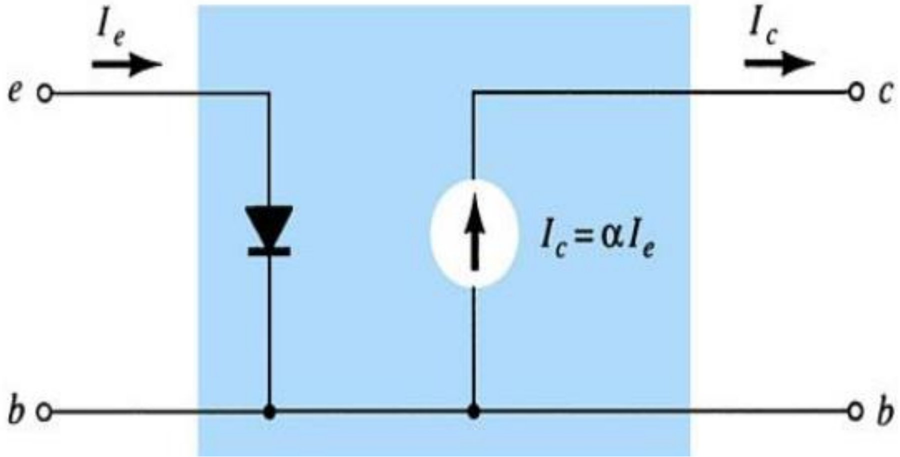
$Zi = re_{CB}$

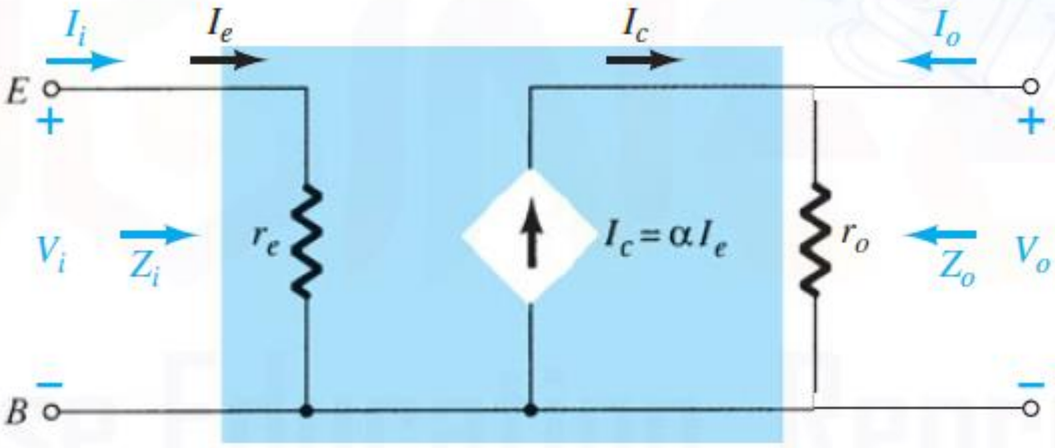
For the output impedance, if we set the signal to zero, then mean I_e= 0 A and I_c=0 where $I_c = \alpha I_e = \alpha (0A) = 0A$ resulting in an open-circuit equivalence at the output terminals.

$$Z_o \cong \infty\ \Omega$$

CB





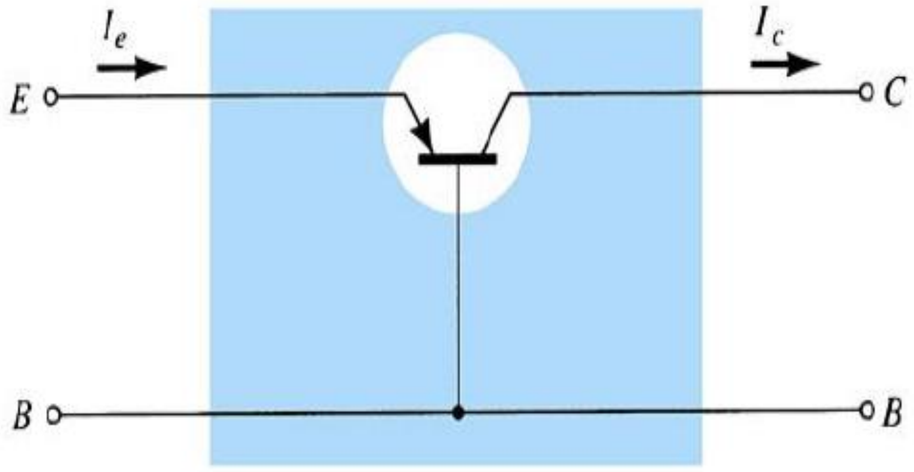


Common Base Configuration

$$r_e = \frac{26\text{ mV}}{I_E}$$

$Zi = re_{CB}$

$$Z_o \cong \infty\ \Omega$$ CB

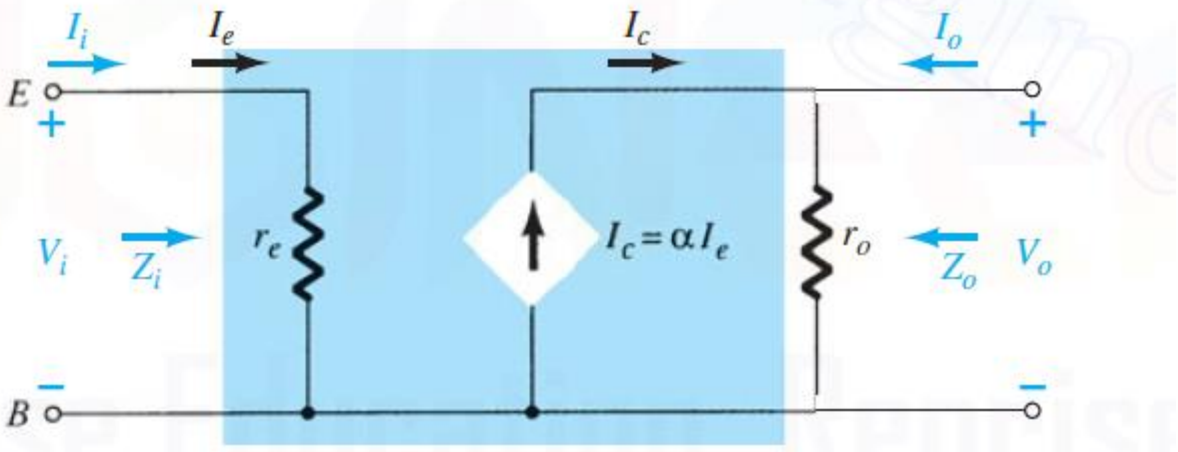


$$V_o = -I_o R_L = -(-I_c)R_L = \alpha I_e R_L$$

$$V_i = I_e Z_i = I_e r_e$$

$$A_v = \frac{V_o}{V_i} = \frac{\alpha I_e R_L}{I_e r_e}$$

$$A_v = \frac{\alpha R_L}{r_e} \cong \frac{R_L}{r_e}$$ CB



$$A_i = \frac{I_o}{I_i} = \frac{-I_c}{I_e} = -\frac{\alpha I_e}{I_e}$$

$$A_i = -\alpha \cong -1$$ CB

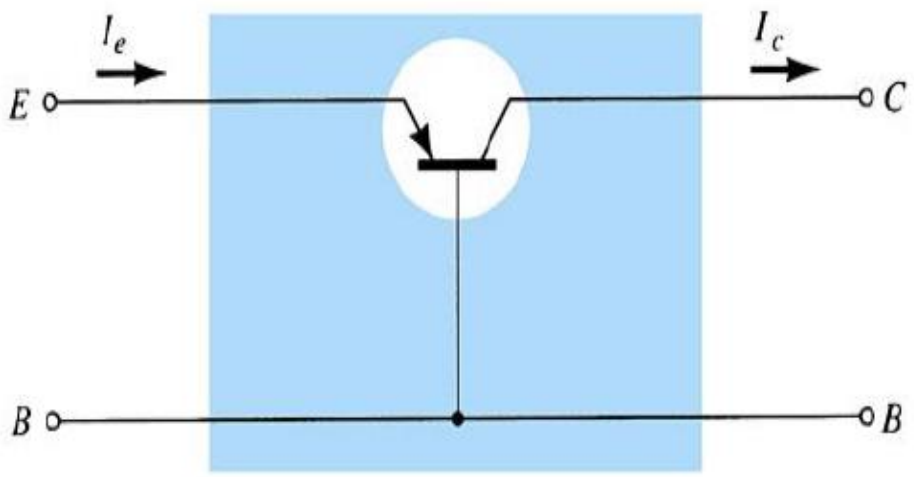
Example : For a common-base configuration of Figure below. with I_E=4 mA, α=0.98, and an ac signal of 2 mV applied between the base and emitter terminals:

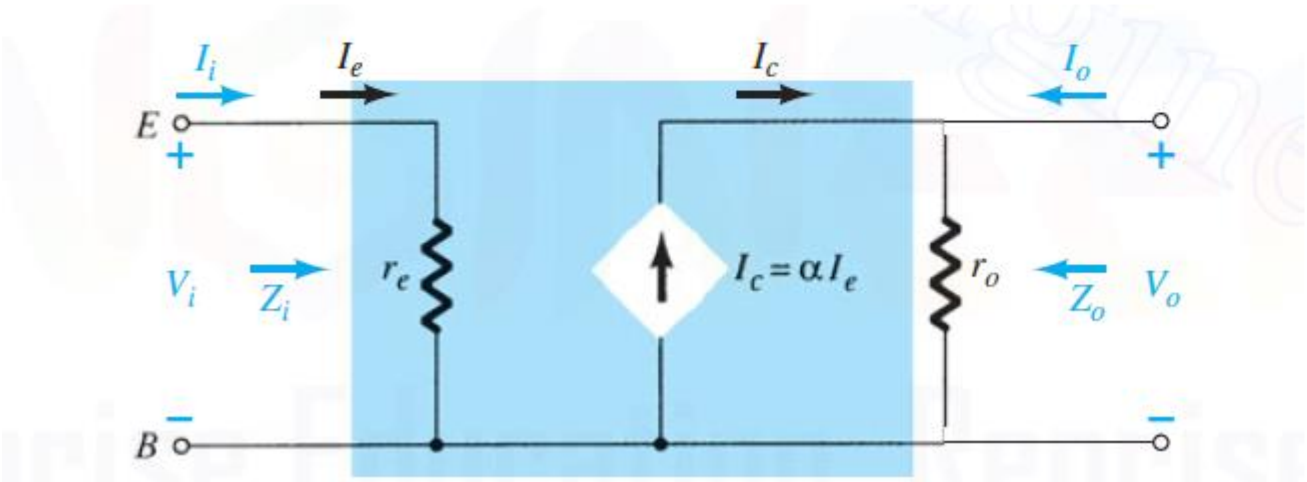
(a) Determine the input impedance.

(b) Calculate the voltage gain if a load of 0.56 kΩ is connected to the output terminals.

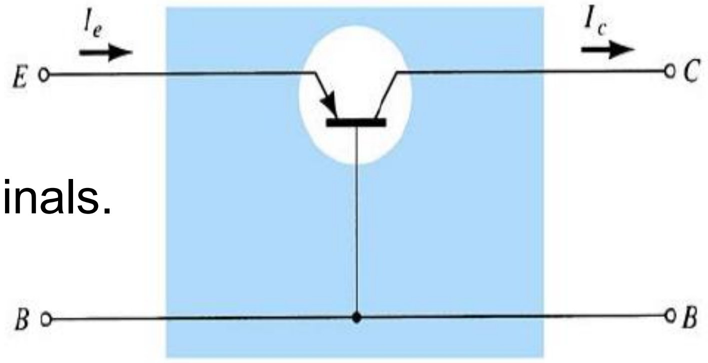
(c) Find the output impedance and current gain.

$$r_e = \frac{26\ \text{mV}}{I_E}$$





Example : For a common-base configuration of Figure below. with I_E=4 mA, α=0.98, and an ac signal of 2 mV applied between the base and emitter terminals:



(a) Determine the input impedance.

(b) Calculate the voltage gain if a load of 0.56 kΩ is connected to the output terminals.

(c) Find the output impedance and current gain.

Solution:

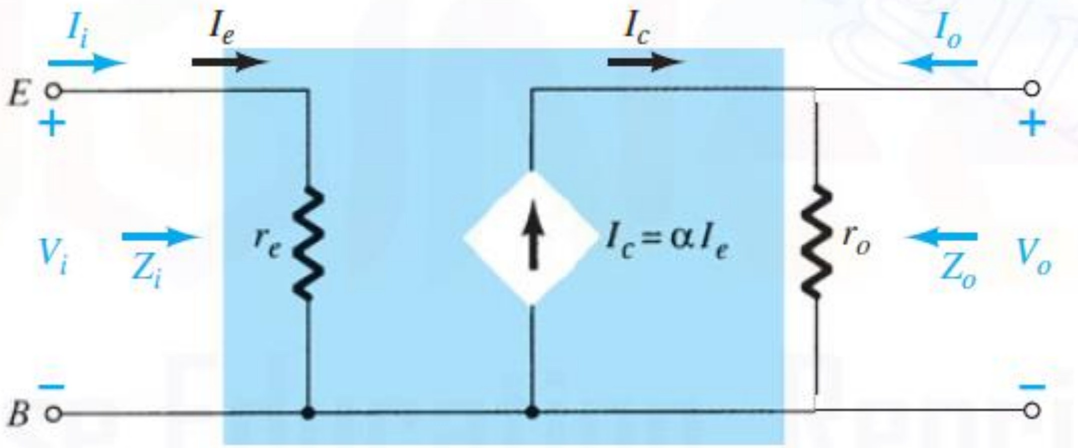
$$\text{(a)}\quad r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{4\text{ mA}} = 6.5\ \Omega$$

$$\text{(b)}\quad I_i = I_e = \frac{V_i}{Z_i} = \frac{2\text{ mV}}{6.5\ \Omega} = 307.69\ \mu\text{A}$$

$$V_o = I_c R_L = \alpha I_e R_L = (0.98)(307.69\ \mu\text{A})(0.56\text{ k}\Omega)$$
$$= 168.86\text{ mV}$$

$$\text{and } A_v = \frac{V_o}{V_i} = \frac{168.86\text{ mV}}{2\text{ mV}} = 84.43$$

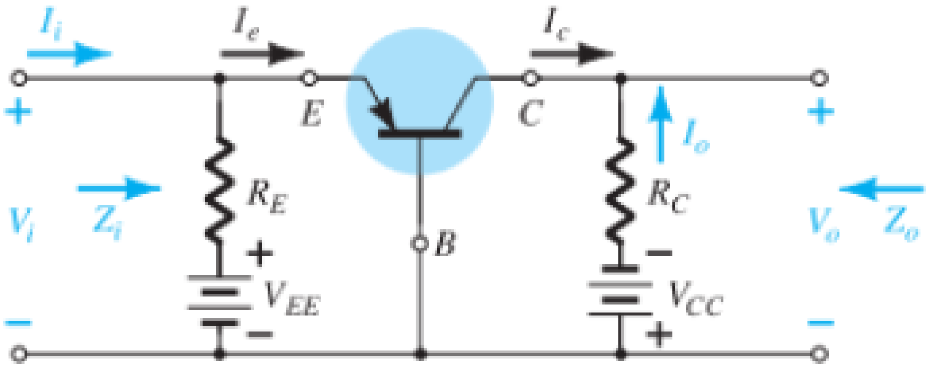
$$A_v = \frac{\alpha R_L}{r_e} = \frac{(0.98)(0.56\text{ k}\Omega)}{6.5\ \Omega} = 84.43$$

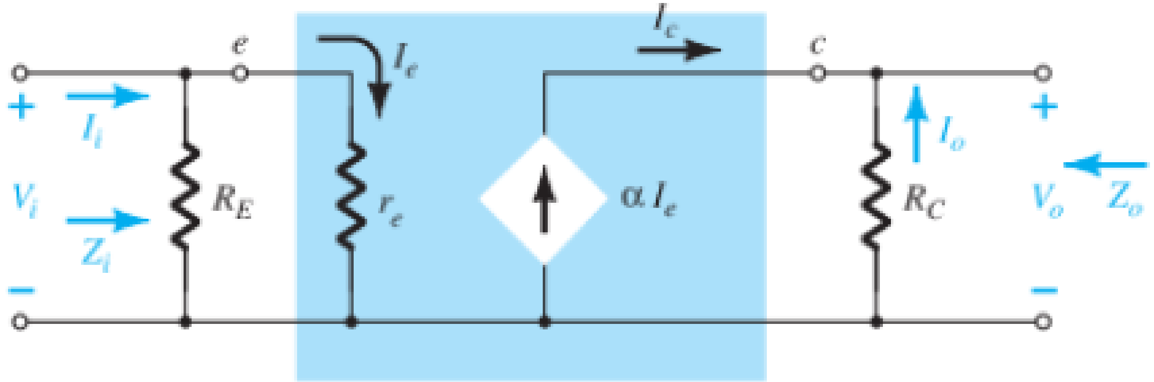


$$\text{(c)}\quad Z_o \cong \infty\ \Omega$$

$$A_i = \frac{I_o}{I_i} = -\alpha = -0.98$$

Common Base Configuration





$$Z_i = R_E \| r_e$$

$$Z_o = R_C$$

$$I_e = I_i$$

$$I_o = -\alpha I_e = -\alpha I_i$$

$$A_i = \frac{I_o}{I_i} = -\alpha \cong -1$$

$$V_o = -I_o R_C = -(-I_c) R_C = \alpha I_e R_C$$

$$I_e = \frac{V_i}{r_e}$$

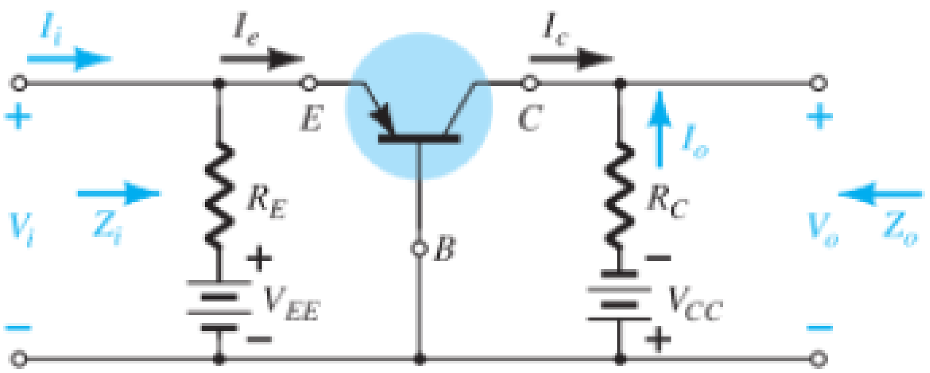
$$V_o = \alpha\left(\frac{V_i}{r_e}\right) R_C$$

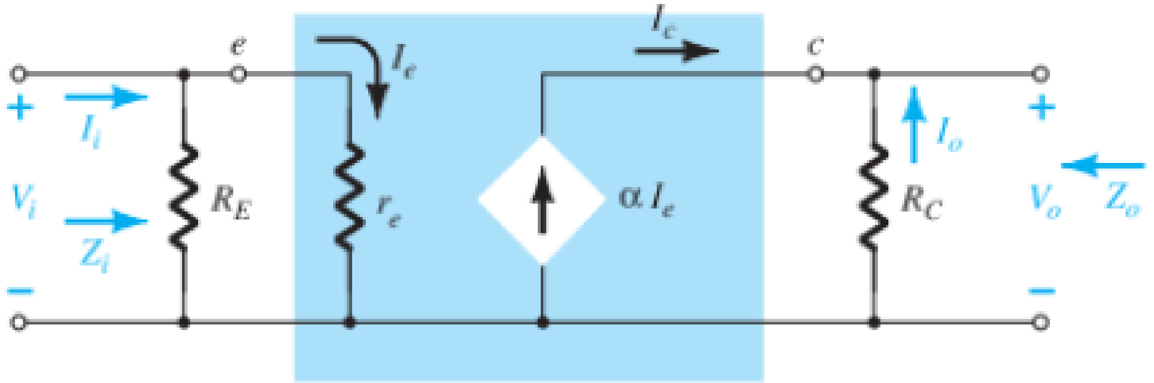
$$A_v = \frac{V_o}{V_i} = \frac{\alpha R_C}{r_e} \cong \frac{R_C}{r_e}$$

Phase Relationship The fact that A_v is a positive number shows that V_o and V_i are in phase for the common-base configuration.

Effect of r_o For the common-base configuration, $r_o = 1/h_{ob}$ is typically in the megohm range and sufficiently larger than the parallel resistance R_C to permit the approximation $r_o \| R_C \cong R_C$.

Common Base Configuration





$$Z_i = R_E \| r_e$$

$$Z_o = R_C$$

$$I_e = I_i$$

$$I_o = -\alpha I_e = -\alpha I_i$$

$$A_i = \frac{I_o}{I_i} = -\alpha \cong -1$$

$$V_o = -I_o R_C = -(-I_c)R_C = \alpha I_e R_C$$

$$I_e = \frac{V_i}{r_e}$$

$$V_o = \alpha\left(\frac{V_i}{r_e}\right)R_C$$

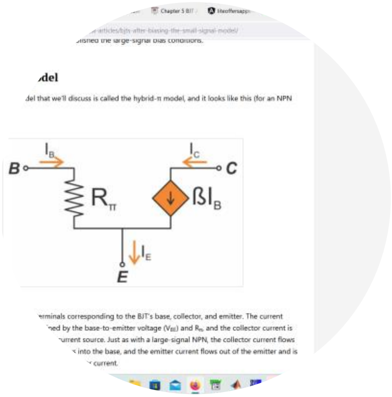
$$A_v = \frac{V_o}{V_i} = \frac{\alpha R_C}{r_e} \cong \frac{R_C}{r_e}$$

Phase Relationship The fact that A_v is a positive number shows that V_o and V_i are in phase for the common-base configuration.

Effect of r_o For the common-base configuration, $r_o = 1/h_{ob}$ is typically in the megohm range and sufficiently larger than the parallel resistance R_C to permit the approximation $r_o \| R_C \cong R_C$.

Ninevah University
College of Electronics Engineering
Department of Systems and Control

Electronic I
Lecture 6
AC analysis of BJT



2nd Class

by
Rafal Raed Mahmood Alshaker

AC analysis of BJT

Outlines of Presentation

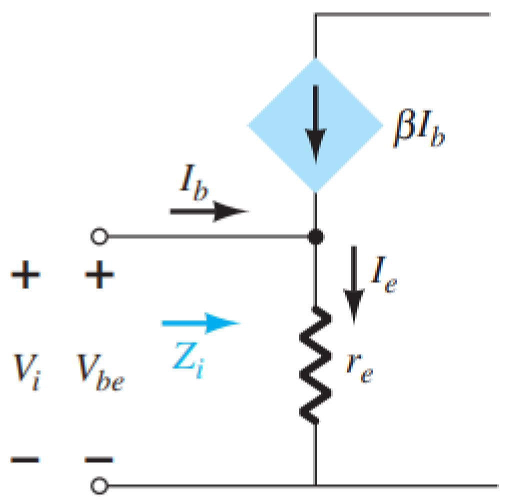
Common Emitter Configuration

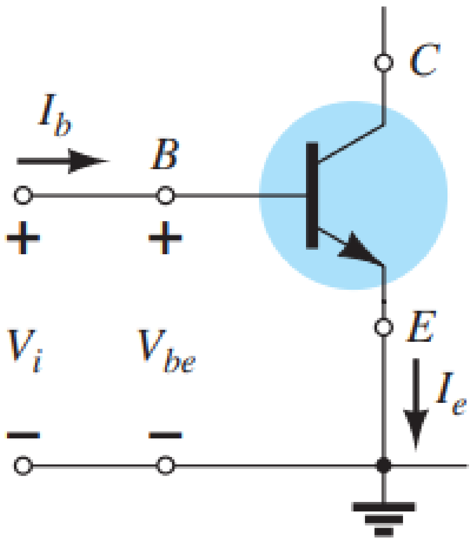
- Input Impedance Zi
- Output Impedance Z_o
- Voltage gain A_V:
- current gain A_i
- Phase Relationship
- Example

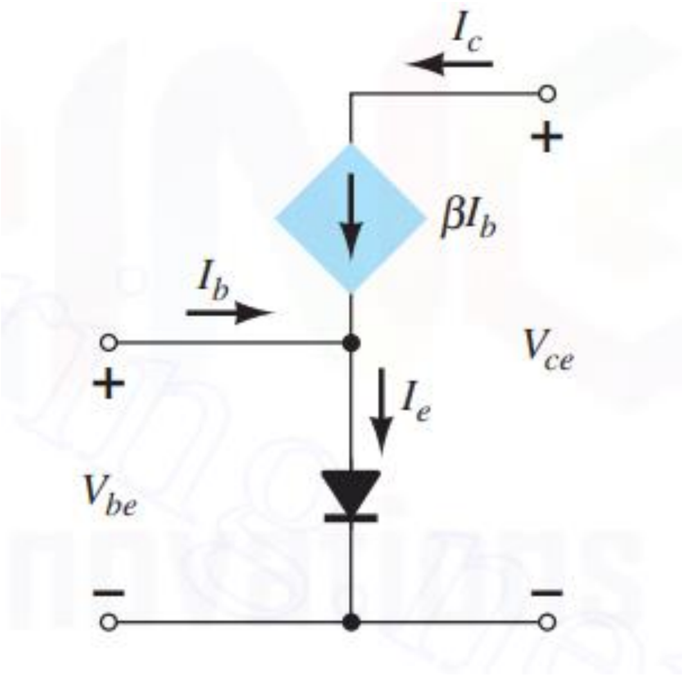
Common Collector Configuration

- Voltage gain A_V
- Input Impedance Zi
- Output Impedance Z_o
- current gain A_i
- Power again

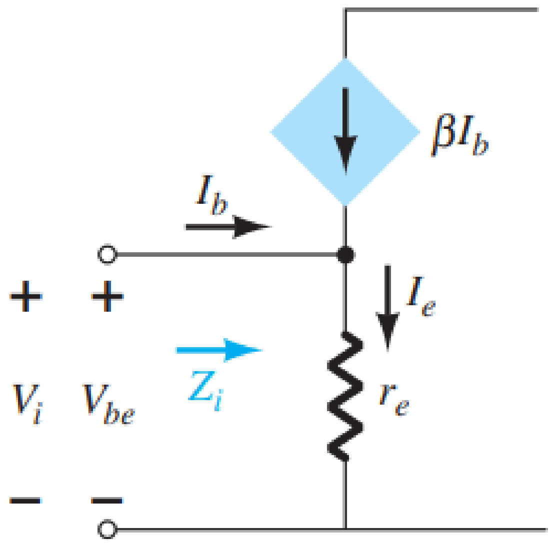
Common-Emitter BJT Transistor

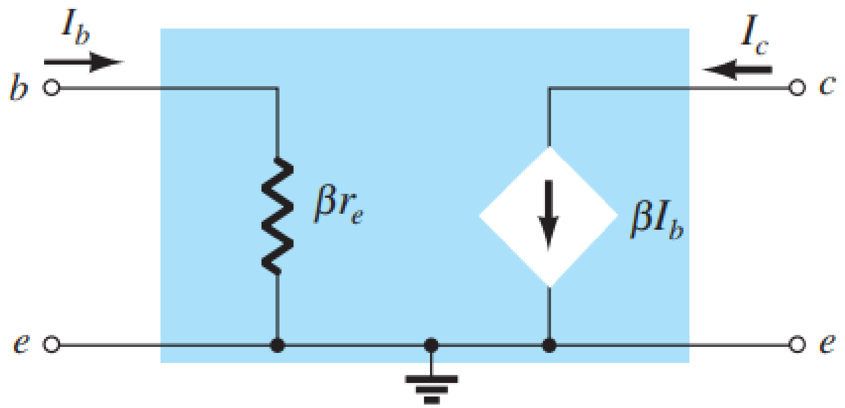






Common-emitter BJT transistor





Common-emitter BJT transistor

$$I_c = \beta I_b$$

$$I_e = I_c + I_b = \beta I_b + I_b$$

$$I_e = (\beta + 1) I_b$$

$$I_e \cong \beta I_b$$

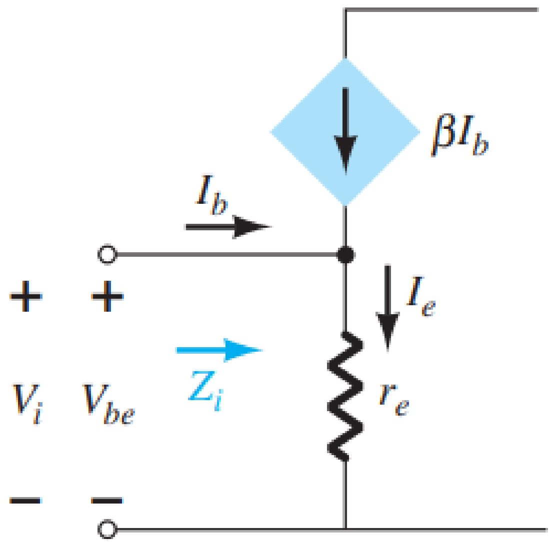
$$Z_i = \frac{V_i}{I_i} = \frac{V_{be}}{I_b}$$

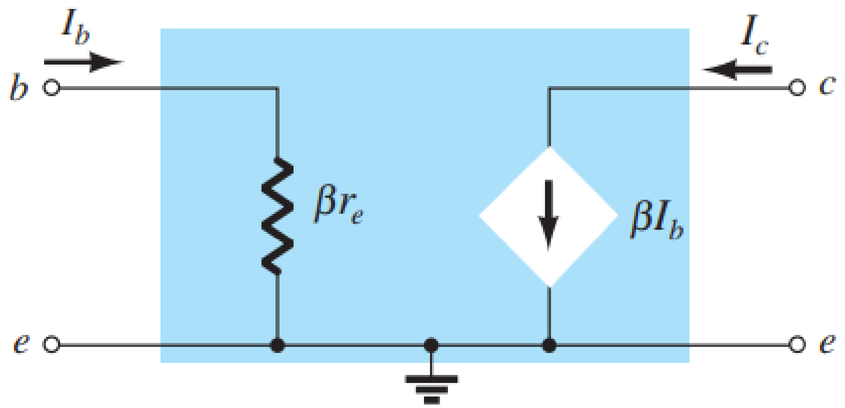
$$V_i = V_{be} = I_e r_e \cong \beta I_b r_e$$

$$Z_i = \frac{V_{be}}{I_b} \cong \frac{\beta I_b r_e}{I_b}$$

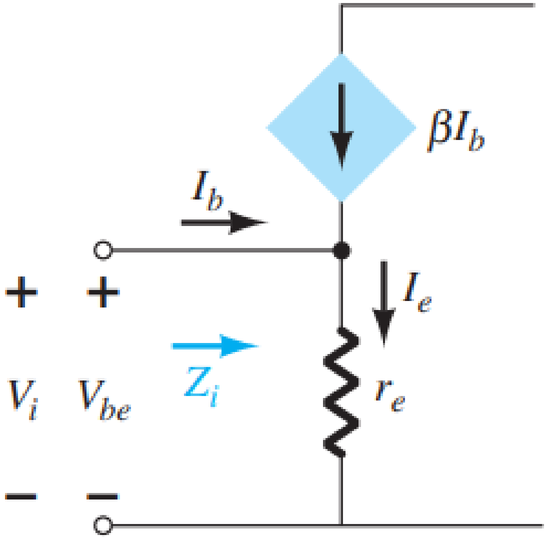
$$Z_i \cong \beta r_e$$

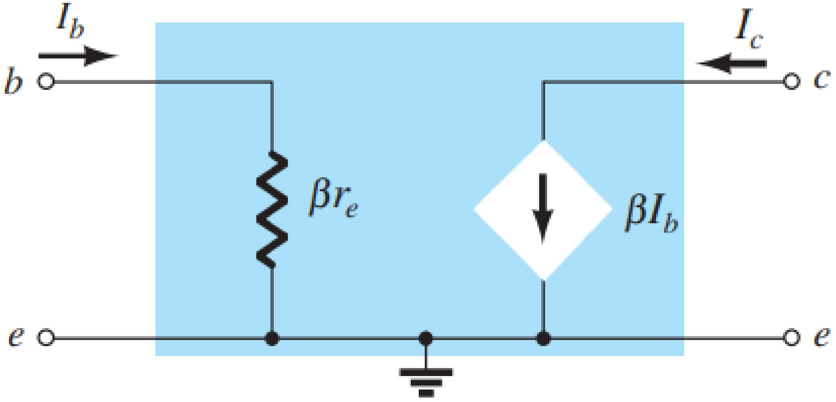
CE

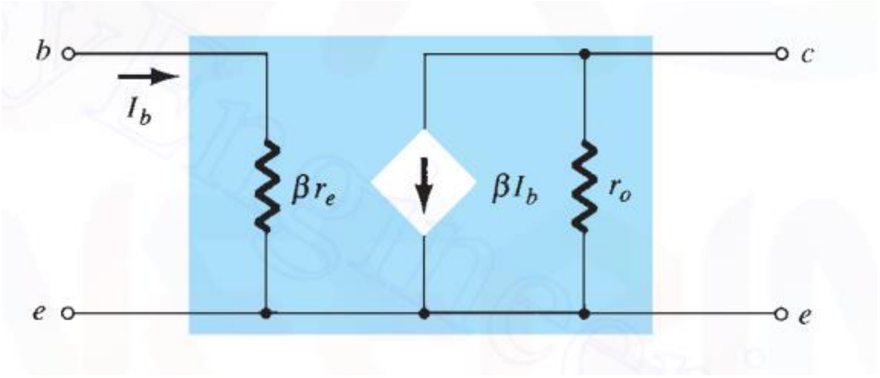




The Input impedance for the common-emitter configuration



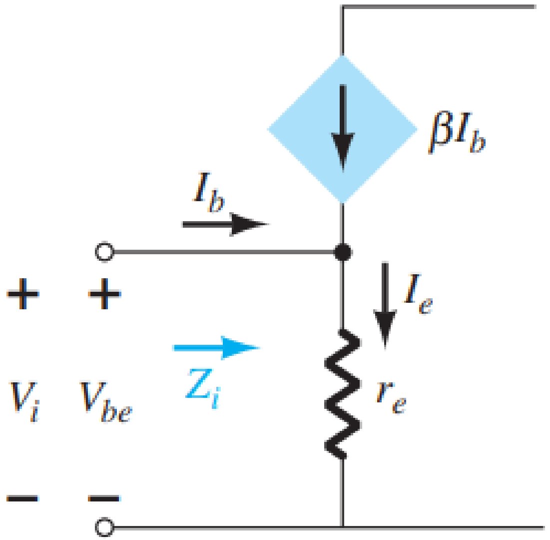


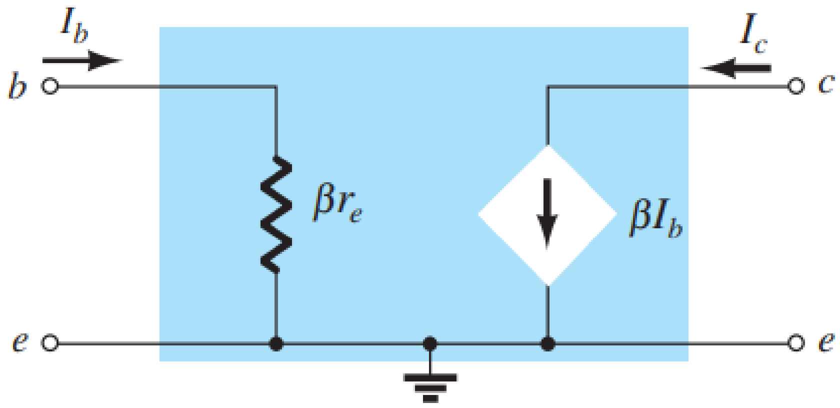


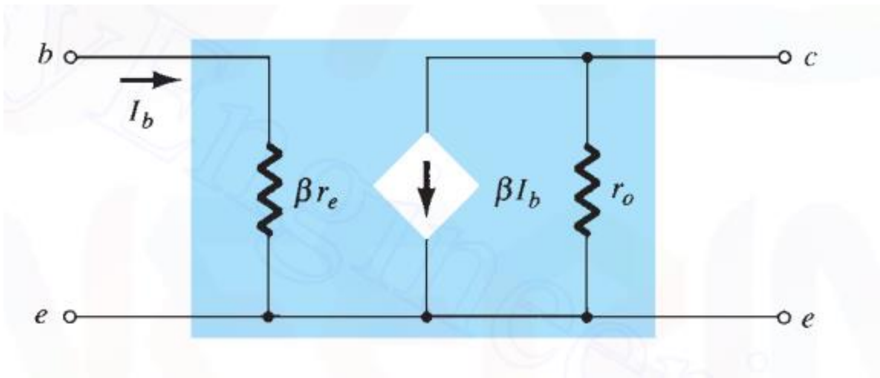
$$Z_i = \frac{V_{be}}{I_b} \cong \frac{\beta I_b r_e}{I_b}$$

$$\boxed{Z_i \cong \beta r_e}_{CE}$$

The output impedance for the common-emitter configuration





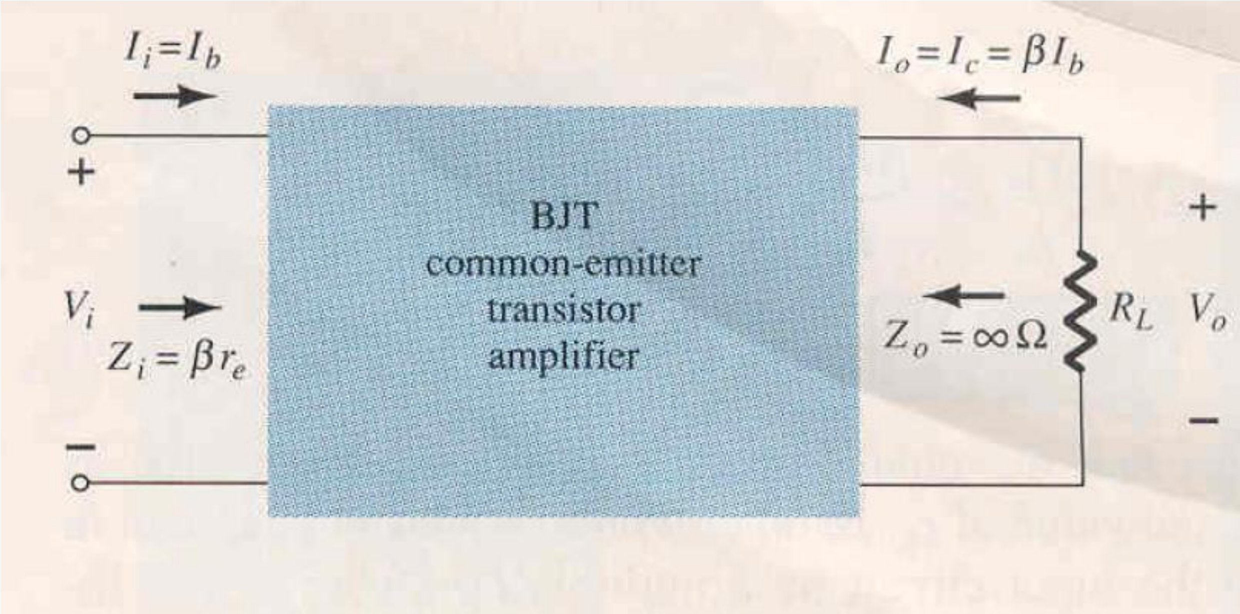


$$Z_o = r_o$$

CE

For the common-emitter configuration, typical values of Z_o are in the range of 40 to 50 kΩ.

The voltage gain for the common-emitter configuration



The voltage gain for the common-emitter configuration

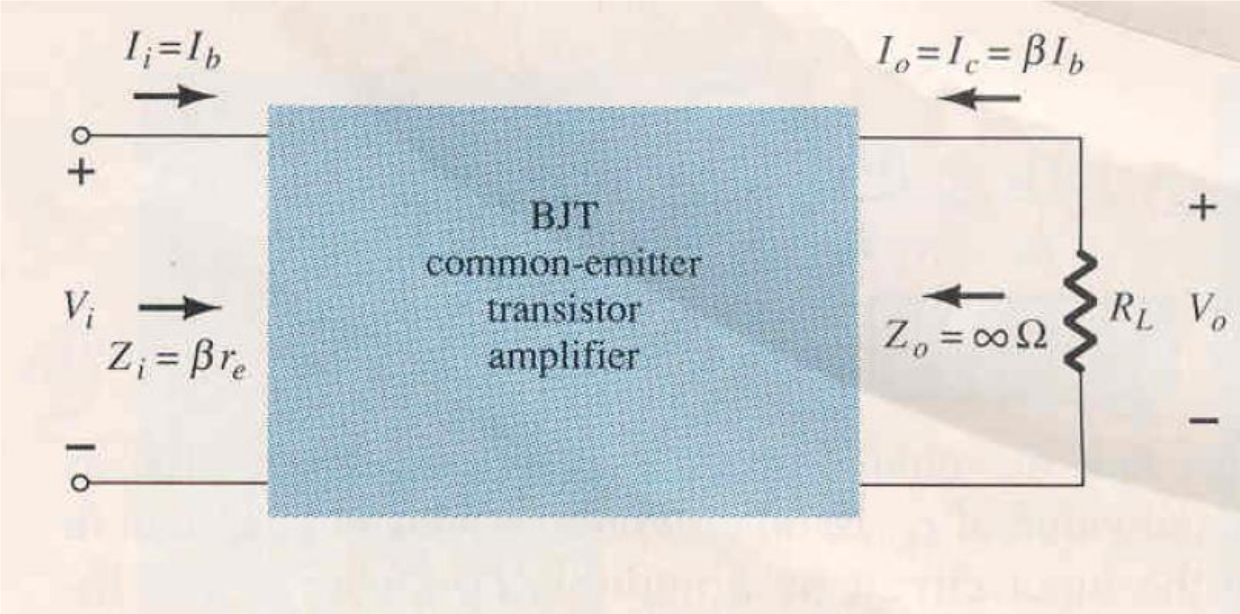
$$V_o = -I_o R_L = -I_c R_L = -\beta I_b R_L$$

$$V_i = I_i Z_i = I_b \beta r_e$$

$$A_v = \frac{V_o}{V_i} = -\frac{\beta I_b R_L}{I_b \beta r_e}$$

$$A_v = -\frac{R_L}{r_e}$$

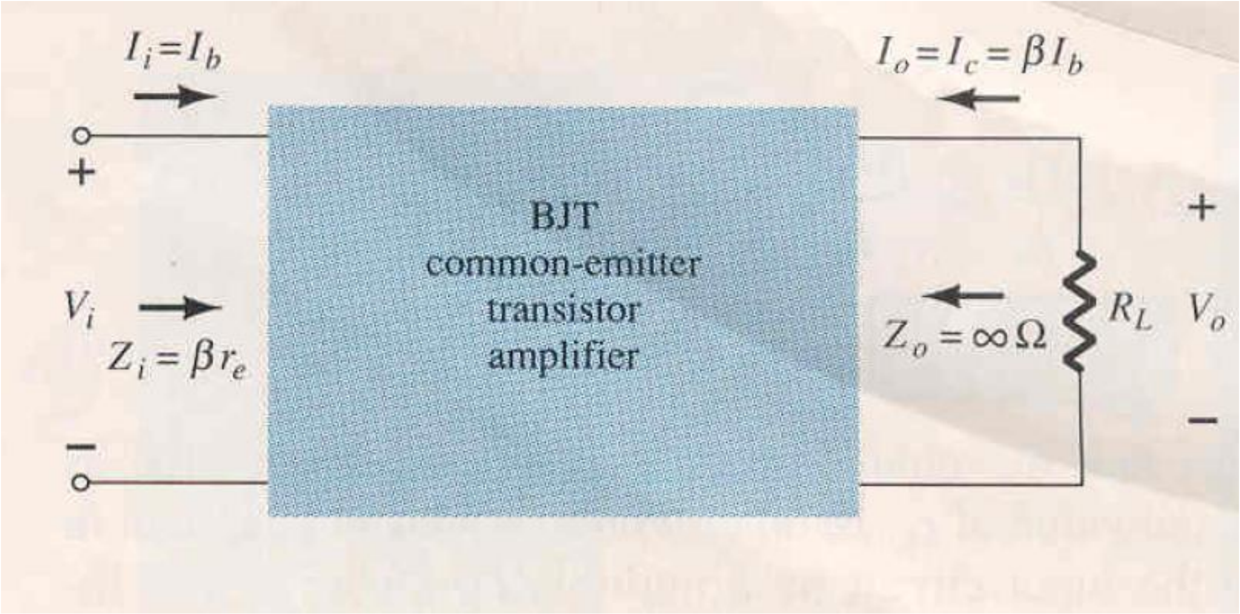
$CE, r_o = \infty\Omega$



The Current gain for the common-emitter configuration

$$A_i = \frac{I_o}{I_i} = \frac{I_c}{I_b} = \frac{\beta I_b}{I_b}$$

$$\boxed{A_i = \beta}_{CE, r_o = \infty\ \Omega}$$



EXAMPLE: Given $\beta = 120$ and $I_E = 3.2$ mA for a common-emitter configuration with $r_o = \infty\Omega$ **determine:**

(a) Z_i.

(b) A_v if a load of 2 kΩ is applied.

(c) A_i with the 2 kΩ load.

Solution:

EXAMPLE: Given $\beta = 120$ and $I_E = 3.2$ mA for a common-emitter configuration with $r_o = \infty\,\Omega$ **determine:**

(a) Z_i.

(b) A_v if a load of 2 kΩ is applied.

(c) A_i with the 2 kΩ load.

Solution:

$$\text{(a)}\quad r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{3.2\text{ mA}} = 8.125\ \Omega$$

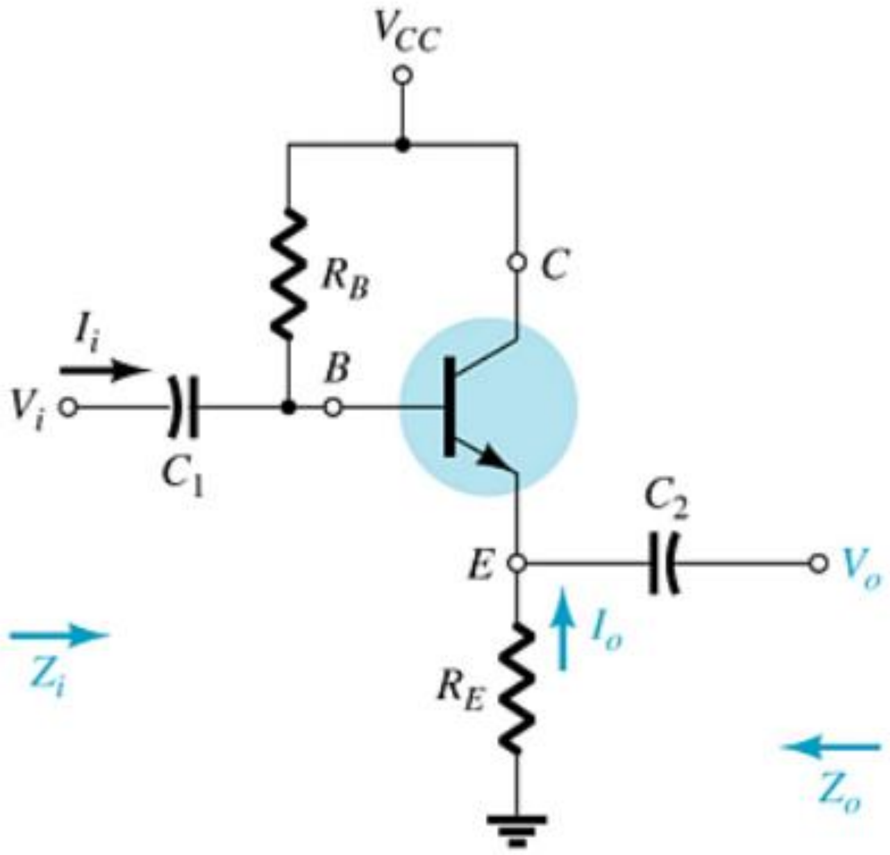
$$\text{and } Z_i = \beta r_e = (120)(8.125\ \Omega) = \mathbf{975\ \Omega}$$

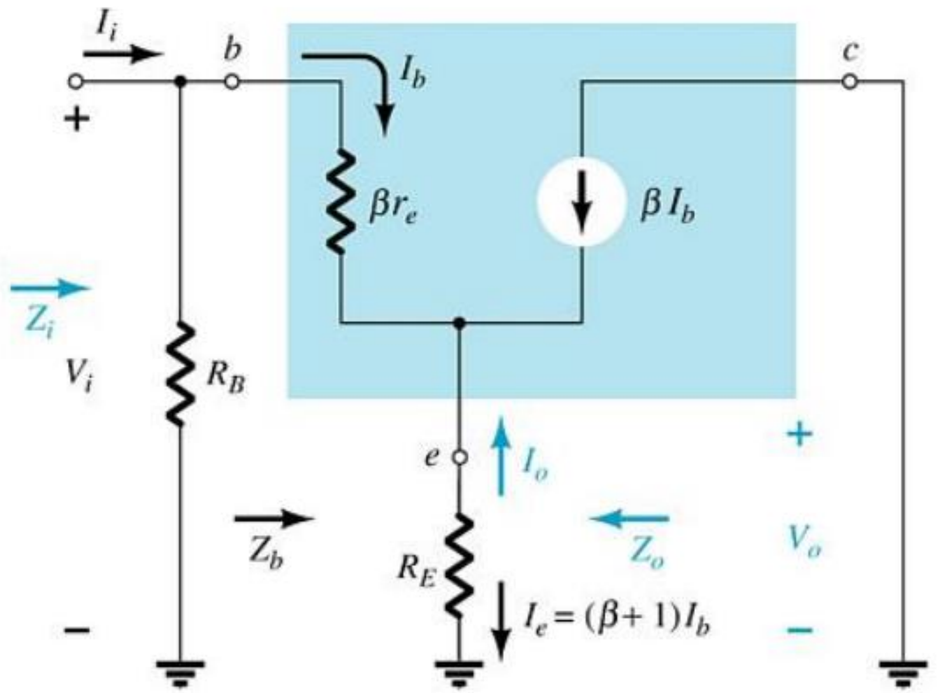
$$A_v = -\frac{R_L}{r_e} = -\frac{2\text{ k}\Omega}{8.125\ \Omega} = \mathbf{-246.15}$$

$$\text{(c)}\quad A_i = \frac{I_o}{I_i} = \beta = \mathbf{120}$$

Common-Collector Configuration.

- This is also known as the common-collector configuration.
- The input is applied to the base and the output is taken from the emitter.
- There is no phase shift between input and output





Voltage gain:

$$A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e}$$

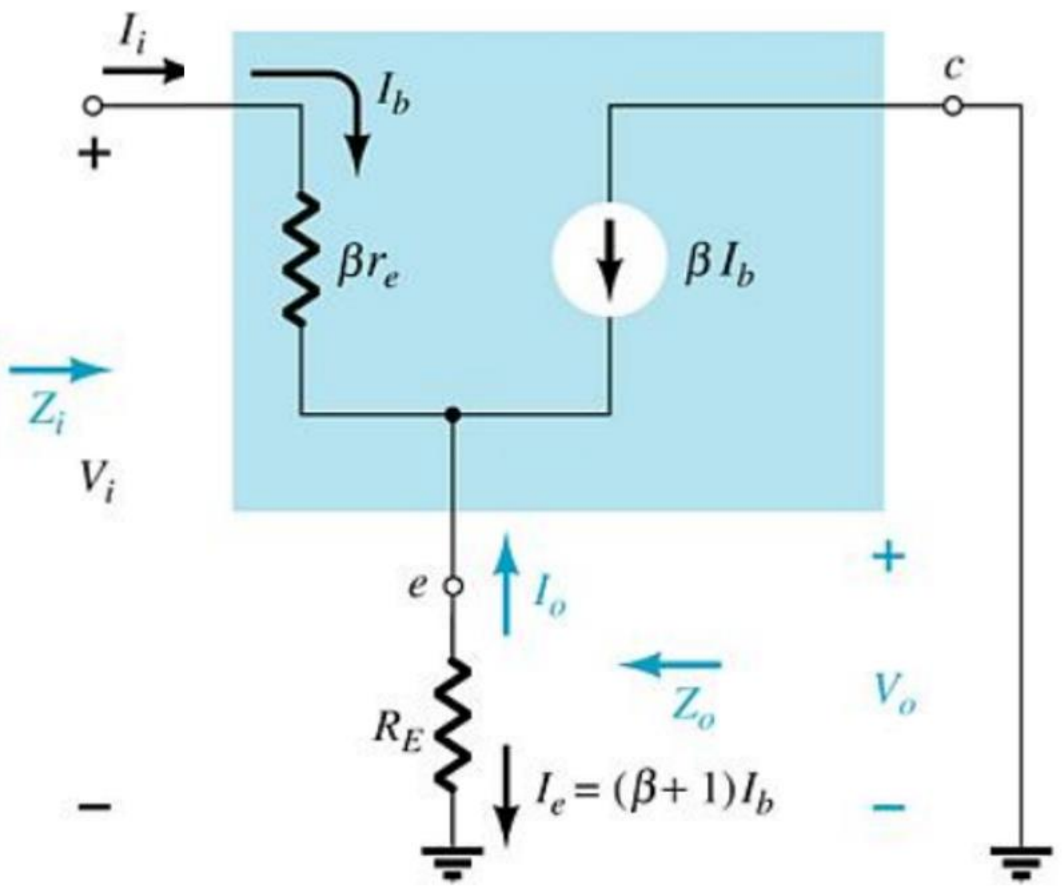
$$A_v = \frac{V_o}{V_i} \simeq 1 |_{R_E >> r_e,\ R_E + r_e \simeq R_E}$$

Current gain:

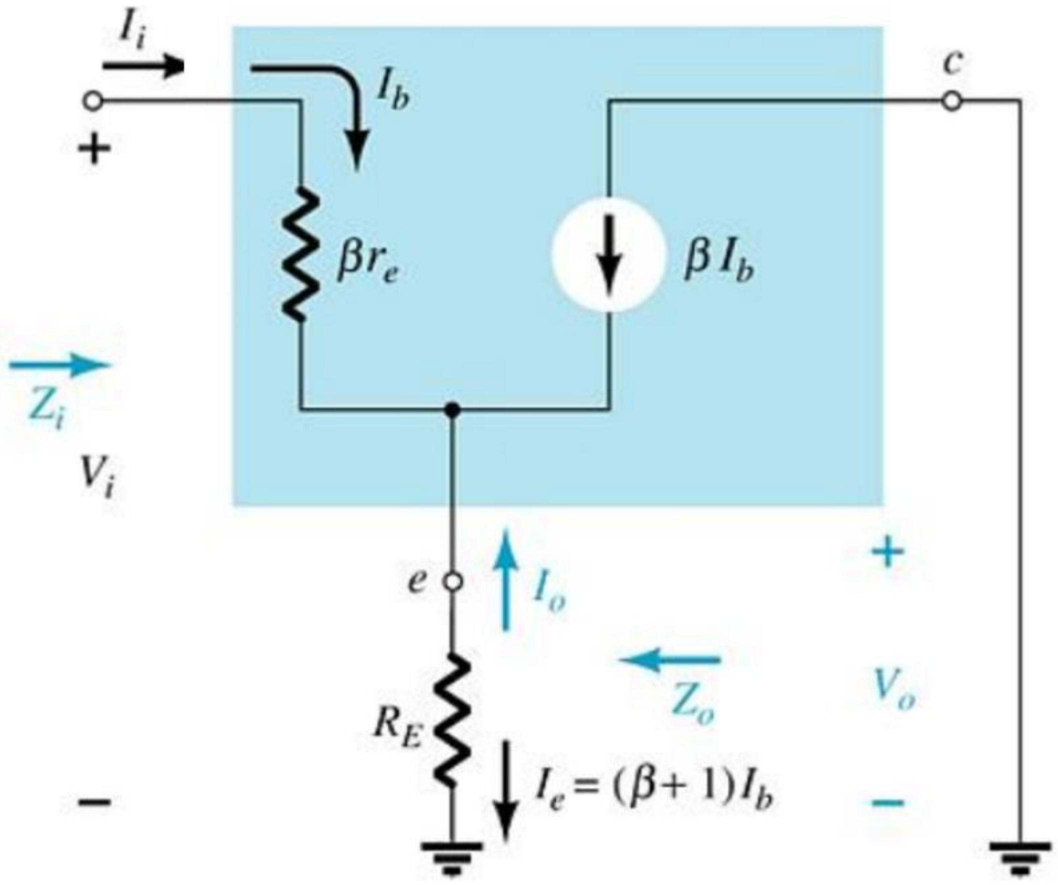
$$A_i \simeq - \frac{\beta R_B}{R_B + Z_b}$$

Current gain from voltage gain:

$$A_i = - A_v \frac{Z_i}{R_E}$$



The voltage gain for the common-collector configuration



The voltage gain for the common-collector configuration

$A_v = V_O / V_{in}$

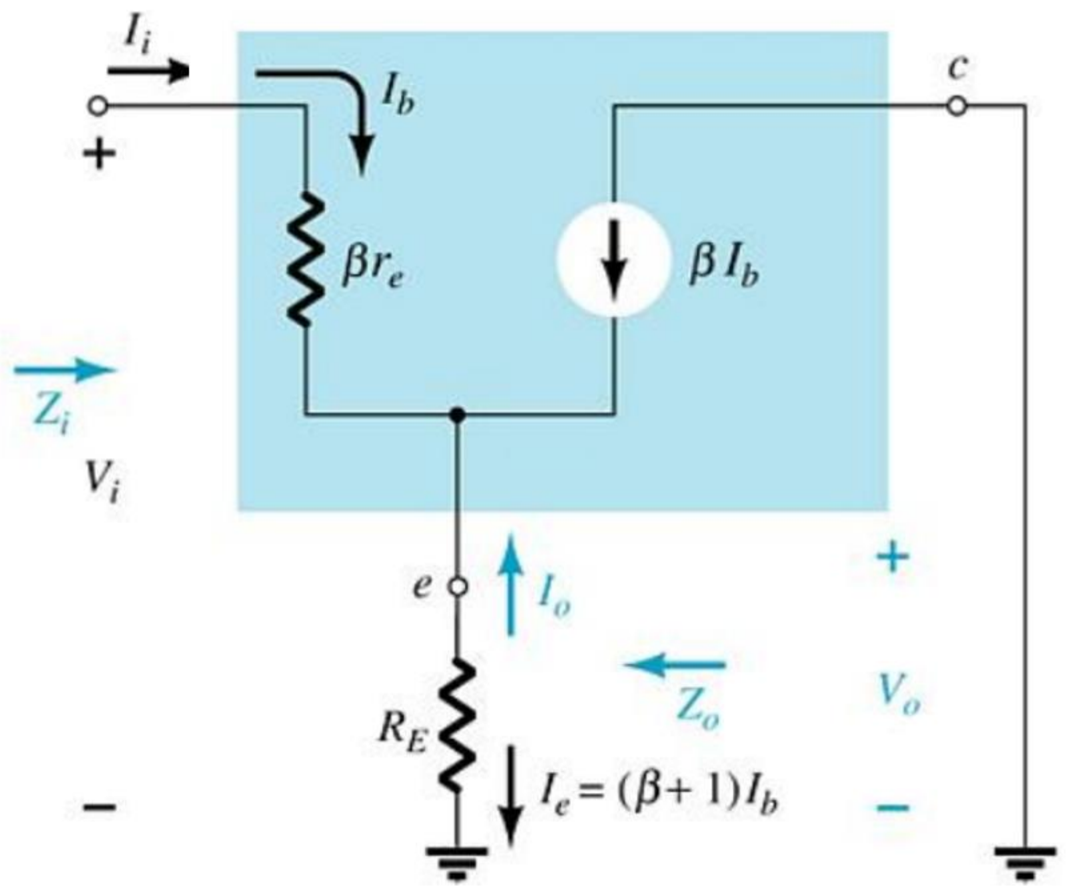
$V_O = I_e R_E = (1+\beta) I_b R_E$

$V_{in} = I_b \beta r_e + I_e R_E$

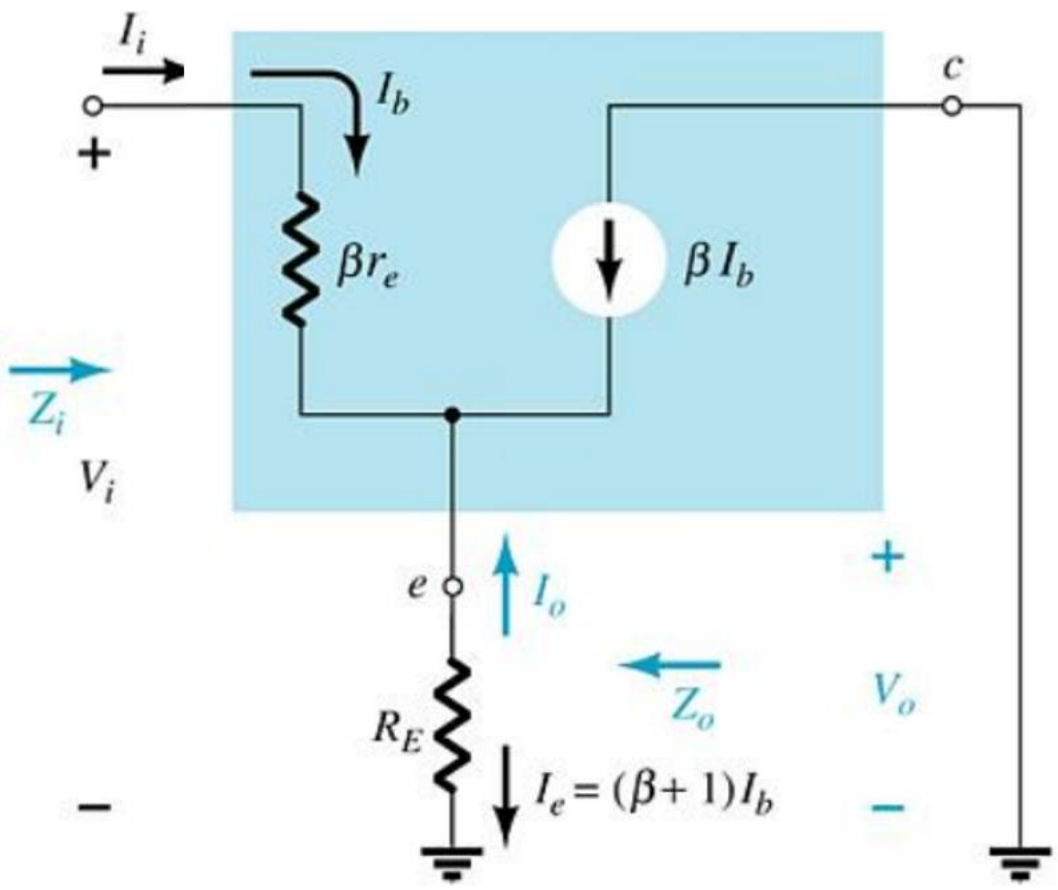
$A_v = R_E / (R_E + r_e)$

$R_E \gg r_e$

$A_v = 1$



The Input Resistance for the common-collector configuration



The Input Resistance for the common-collector configuration

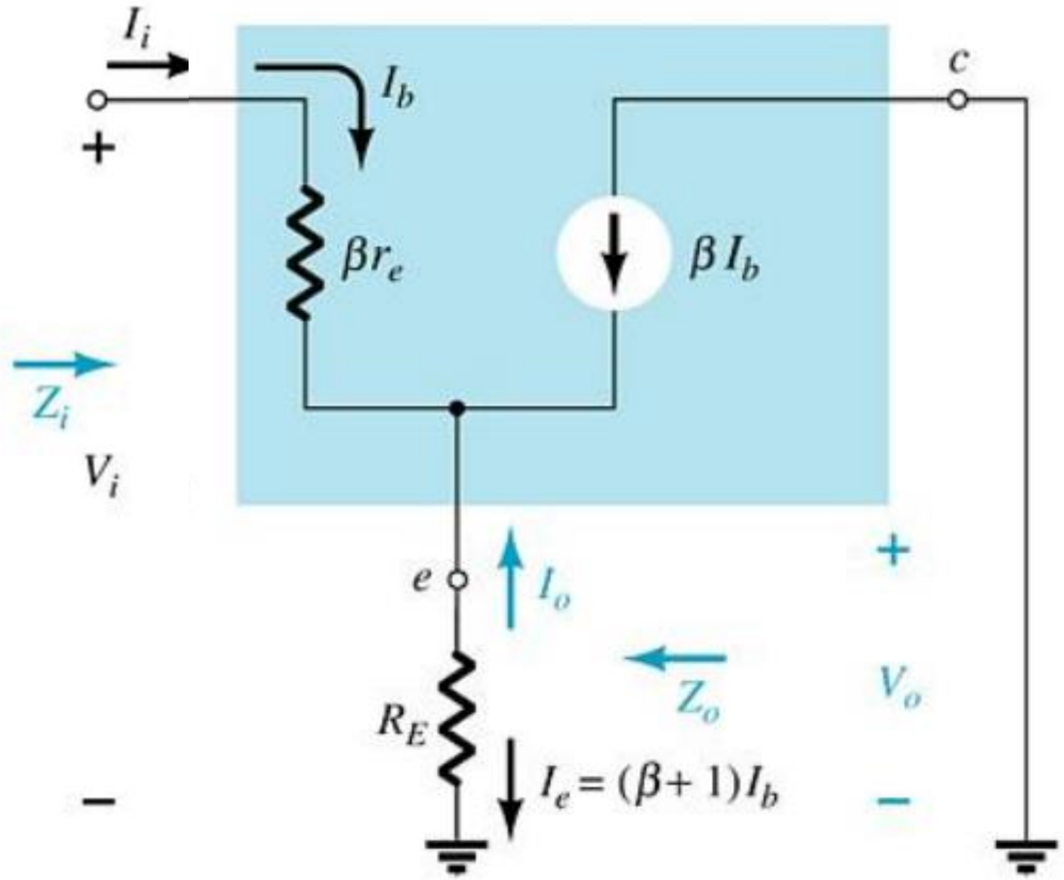
$Z_{in} = V_{in} / I_{in}$

$V_{in} = I_b \beta r_e + I_e R_E$ $\qquad$ $V_{in} = (I_b \beta r_e + I_b (\beta+1) R_E)$

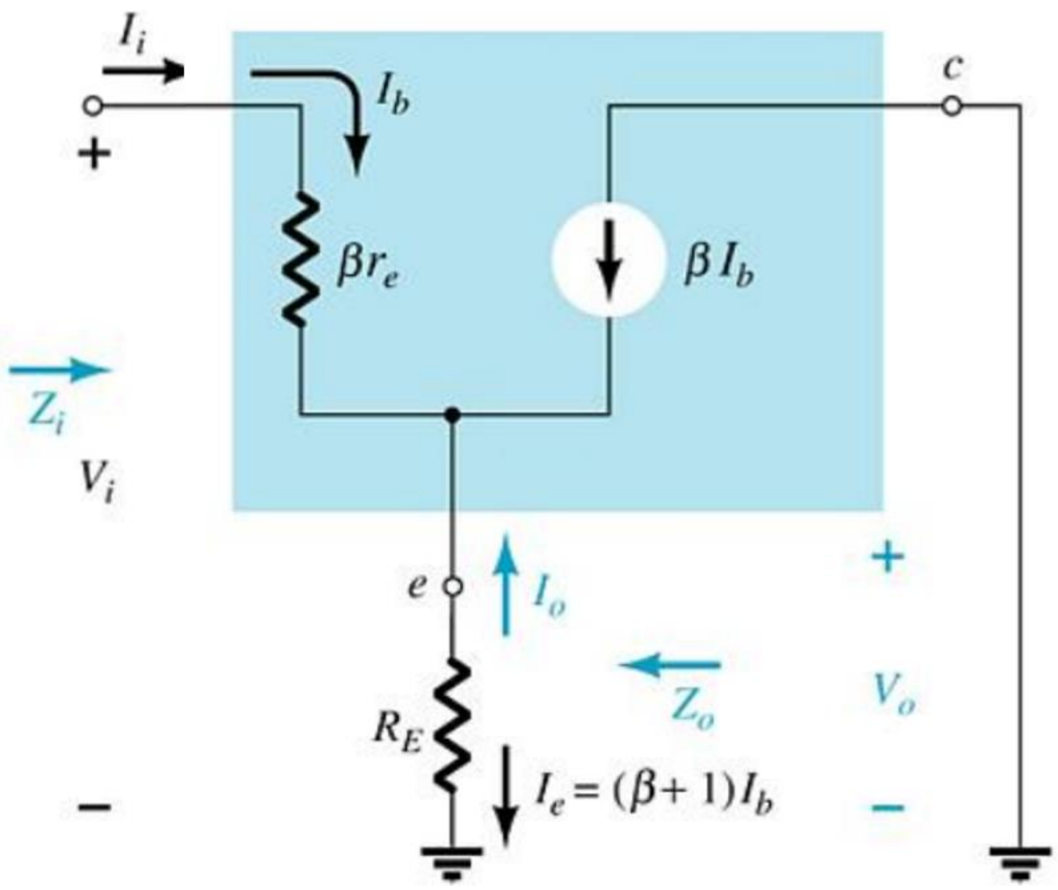
$I_{in} = I_b$

$Z_{in} = (\beta r_e + \beta R_E) = \beta (r_e + R_E) = \beta R_E$

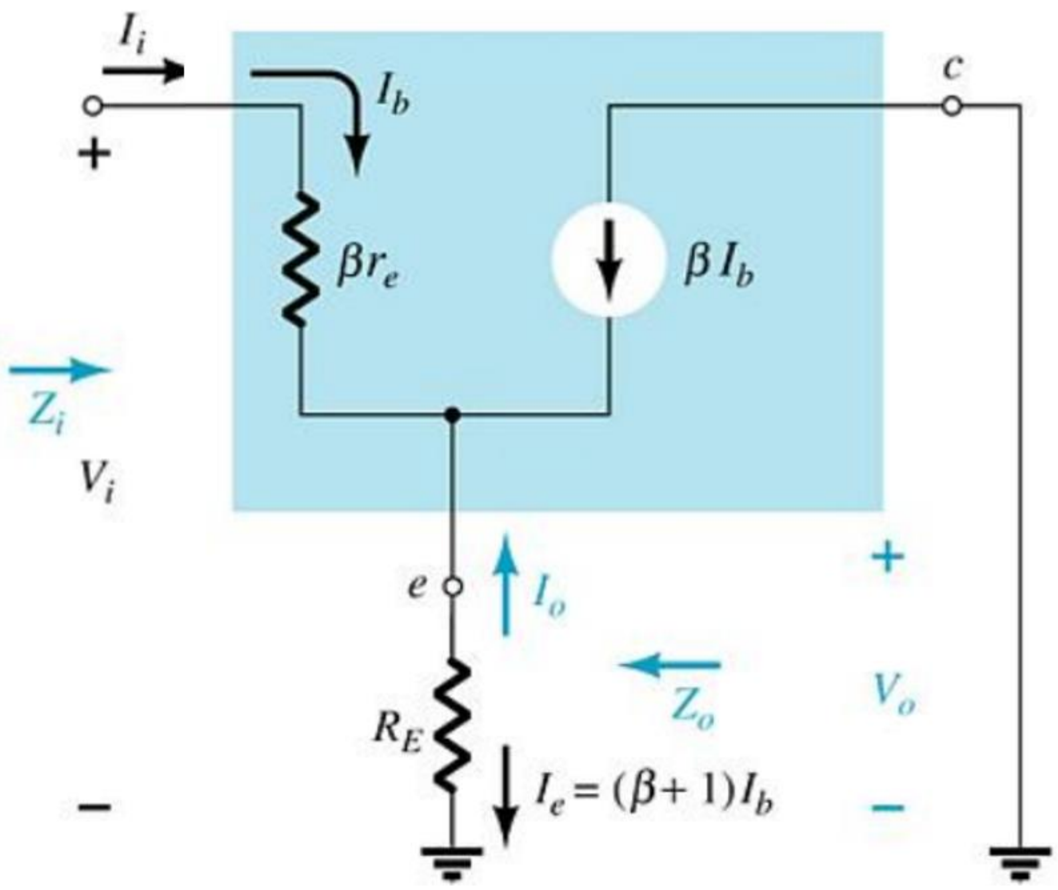
If $R_E >> r_e'$ then the input resistance at the base is simplified to $\boldsymbol{\beta R_E}$



Output Resistance (homework)



Current Gain A_i



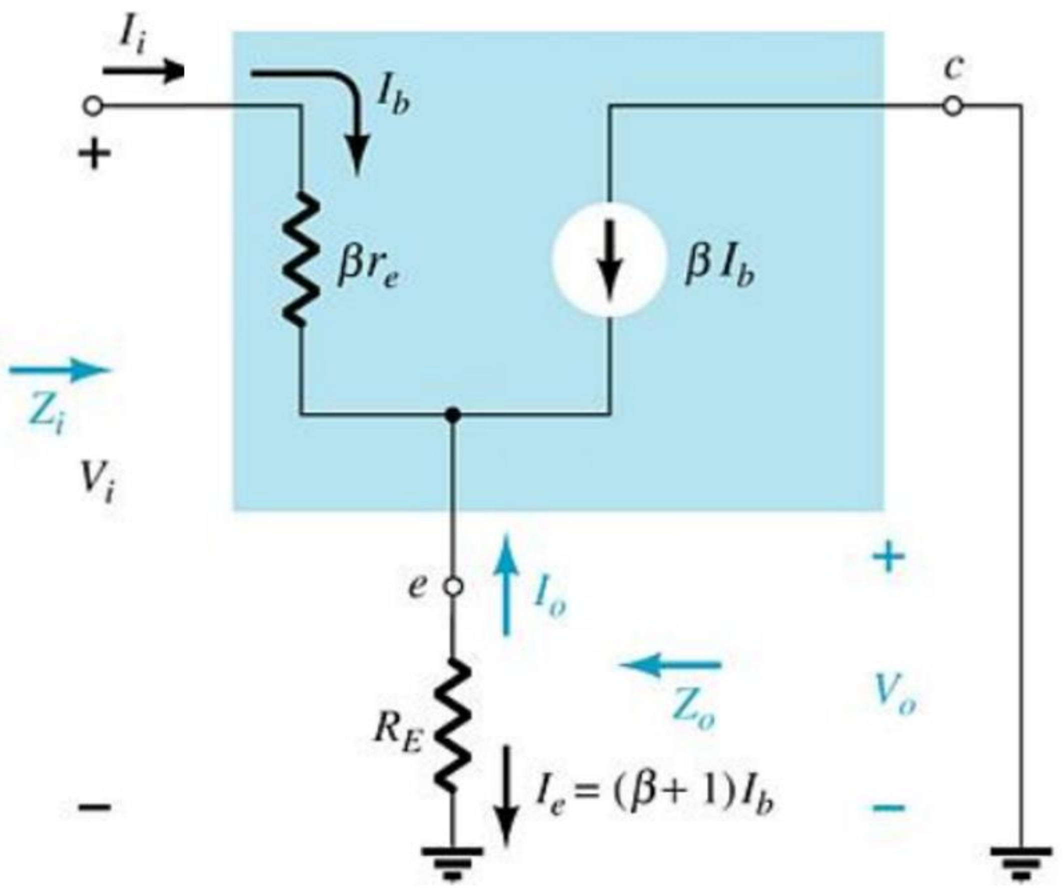
Current Gain A_i

$A_i = I_O / I_{in}$

$I_O = I_e = (1+\beta)\ I_b \approx \beta\ I_b$

$I_{in} = I_b$

$A_i \approx \beta$



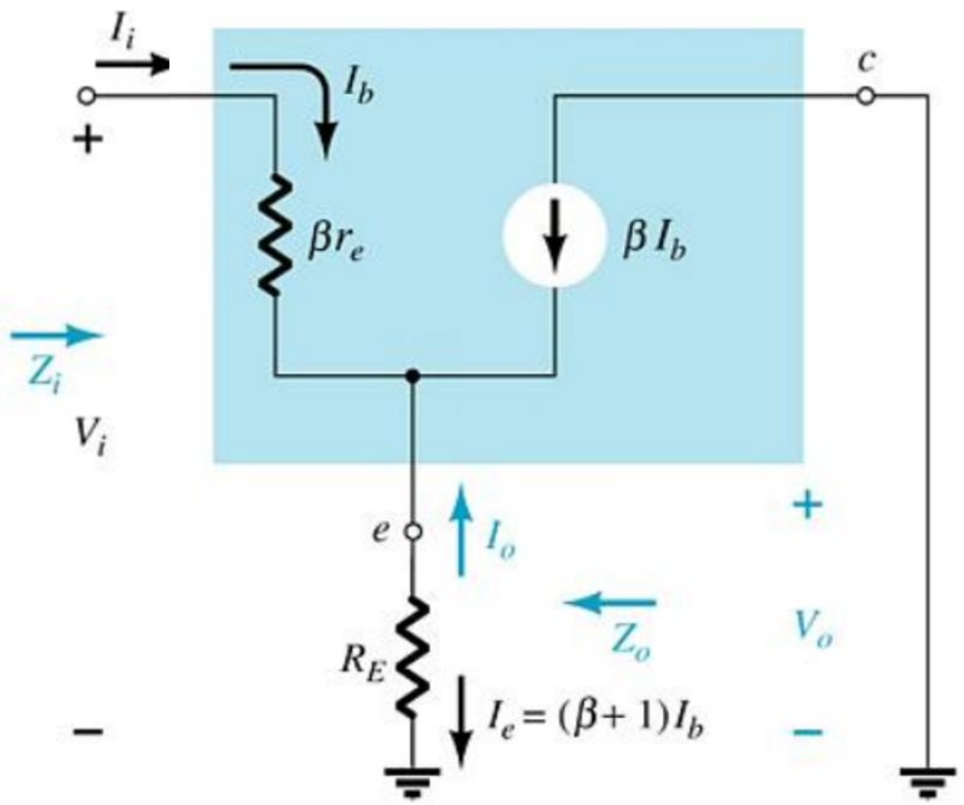
Power Gain

The common-collector power gain is the product of the voltage gain and the current gain. For the emitter-follower, the power gain is approximately equal to the current gain because the voltage gain is approximately 1.

$A_G = A_v * A_i$

$A_v \approx 1$

$A_G = A_i$



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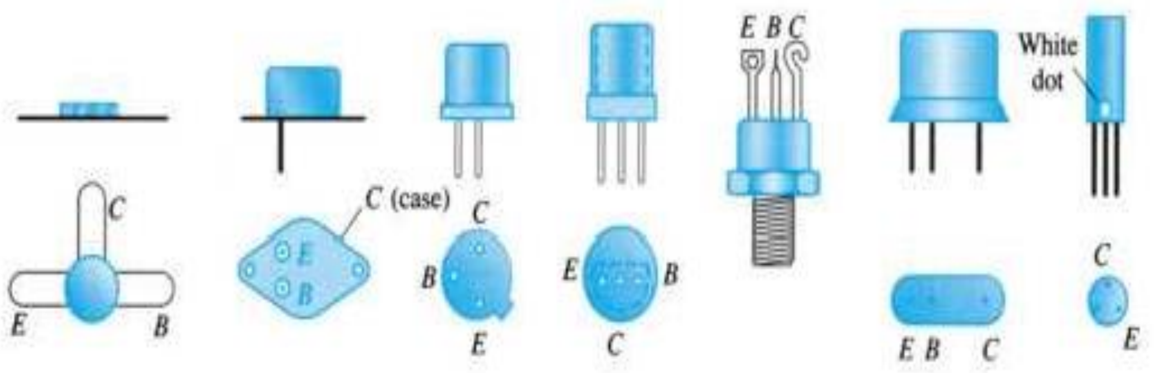
Electronic I

Lecture 6 part 2



2nd Class

by
Rafal Raed Mahmood Alshaker

Outline of Presentation

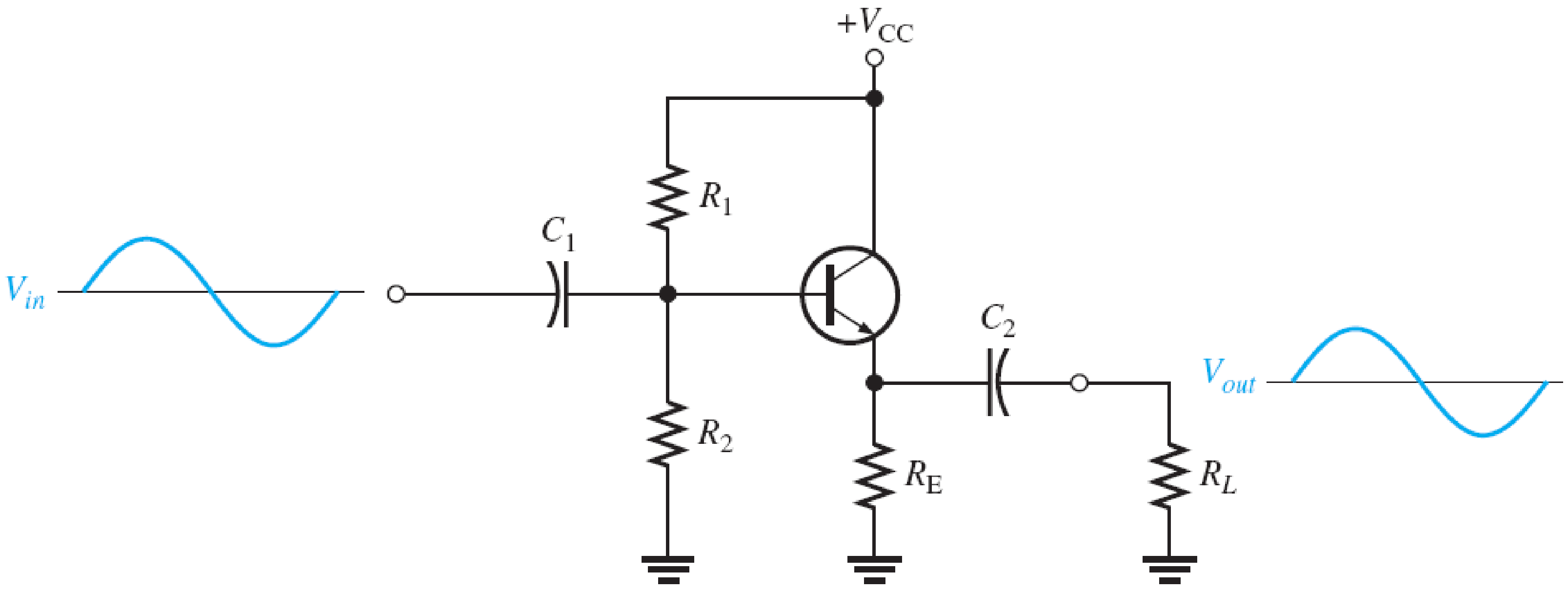
- The Common-collector Amplifier
- Example

Common Base Configuration

- Example

The Common-collector Amplifier

- The **common-collector** (CC) amplifier is usually referred to as an emitter-follower (EF). The input is applied to the base through a coupling capacitor, and the output is at the emitter (no phase change between input and output). The **voltage gain** of a CC amplifier is approximately **1**, and its main advantages are its high input resistance and current gain. The **high input resistance** is very useful to minimize the loading effect specially when circuit is driving a **low-resistance load**→ CC amplifier is used as **a Buffer.**



Example: : For the emitter-follower network of Fig.below, determine:

(a) r_e.

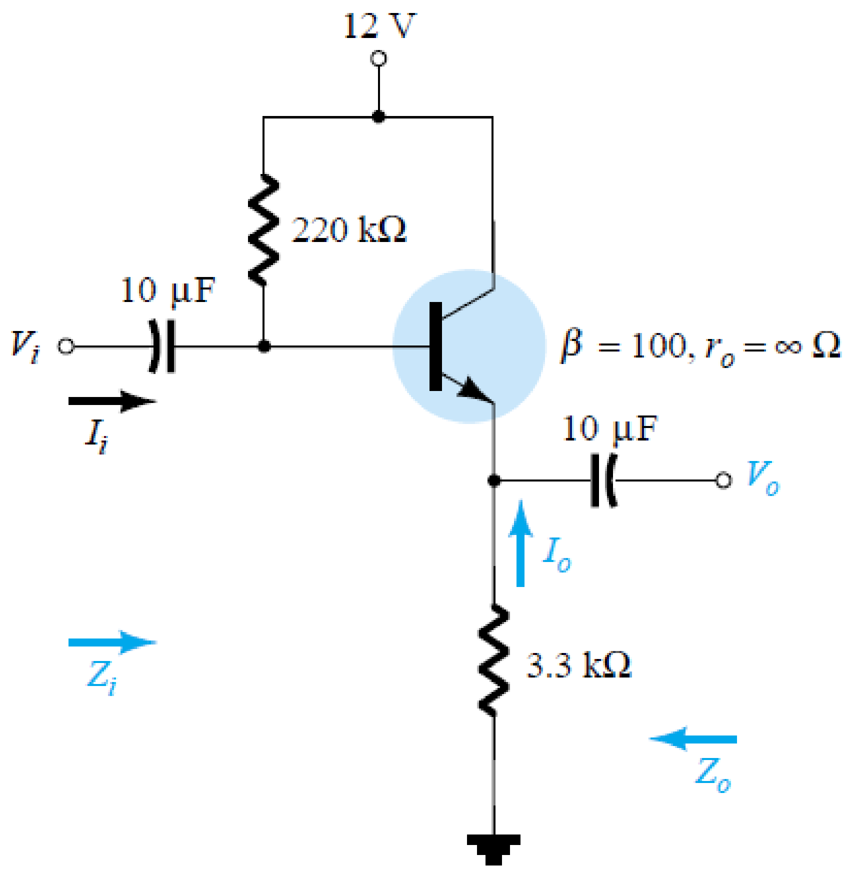
(b) Z_i.

(c) Z_o.

(d) A_v.

(e) A_i.

(f) Repeat parts (b) through (e) with r_o=25 kΩ and compare results.



Solution

(a) $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$= \frac{12\text{ V} - 0.7\text{ V}}{220\text{ k}\Omega + (101)3.3\text{ k}\Omega} = 20.42\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B$$
$$= (101)(20.42\ \mu\text{A}) = 2.062\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.062\text{ mA}} = \mathbf{12.61\ \Omega}$$

(b) $$Z_b = \beta r_e + (\beta + 1)R_E$$
$$= (100)(12.61\ \Omega) + (101)(3.3\text{ k}\Omega)$$
$$= 1.261\text{ k}\Omega + 333.3\text{ k}\Omega$$
$$= 334.56\text{ k}\Omega \cong \beta R_E$$

$$Z_i = R_B \| Z_b = 220\text{ k}\Omega \| 334.56\text{ k}\Omega$$
$$= \mathbf{132.72\text{ k}\Omega}$$

(c) $$Z_o = R_E \| r_e = 3.3\text{ k}\Omega \| 12.61\ \Omega$$
$$= \mathbf{12.56\ \Omega} \cong r_e$$

(d) $A_v = \dfrac{V_o}{V_i} = \dfrac{R_E}{R_E + r_e} = \dfrac{3.3\ \text{k}\Omega}{3.3\ \text{k}\Omega + 12.61\ \Omega} = 0.996 \cong 1$

(e) $A_i \cong -\dfrac{\beta R_B}{R_B + Z_b} = -\dfrac{(100)(220\ \text{k}\Omega)}{220\ \text{k}\Omega + 334.56\ \text{k}\Omega} = -39.67$

$$A_i = -A_v \frac{Z_i}{R_E} = -(0.996)\left(\frac{132.72\ \text{k}\Omega}{3.3\ \text{k}\Omega}\right) = -40.06$$

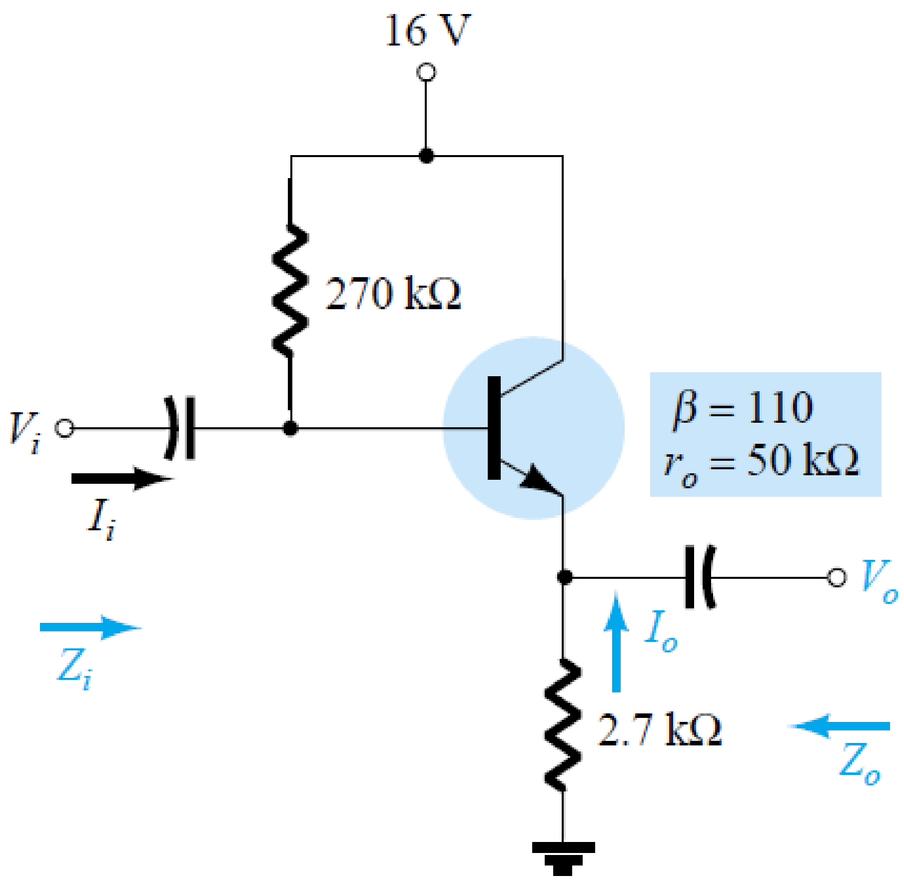
Home work: For the network of Fig below:

(a) Determine the type of configuration.

(b) Determine r_e and βr_e.

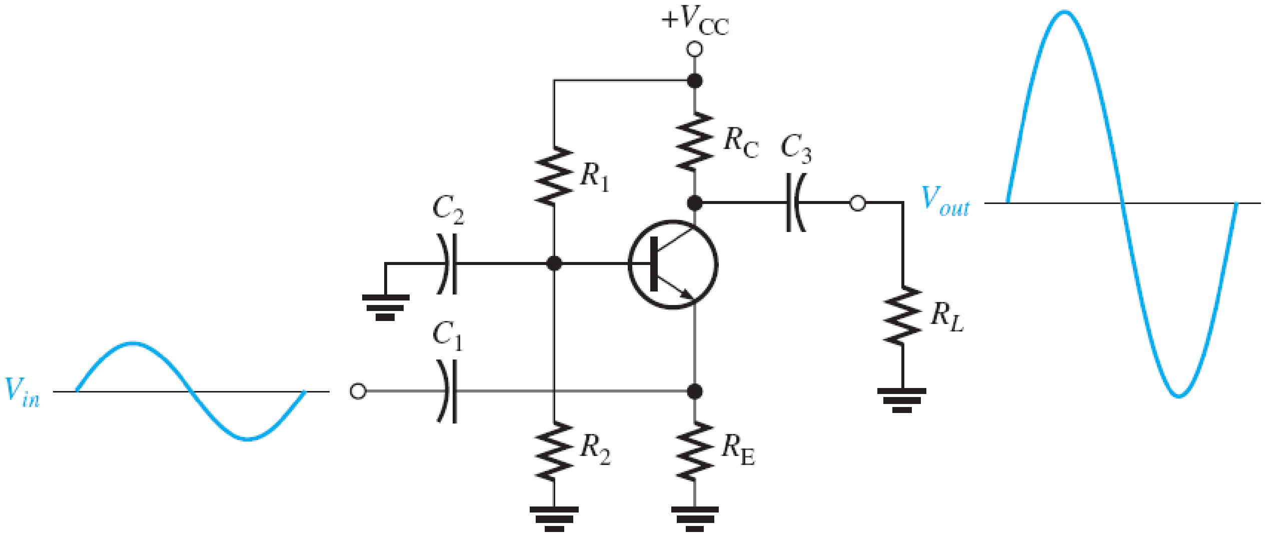
(c) Find Z_i and Z_o.

(d) Calculate A_v and A_i.

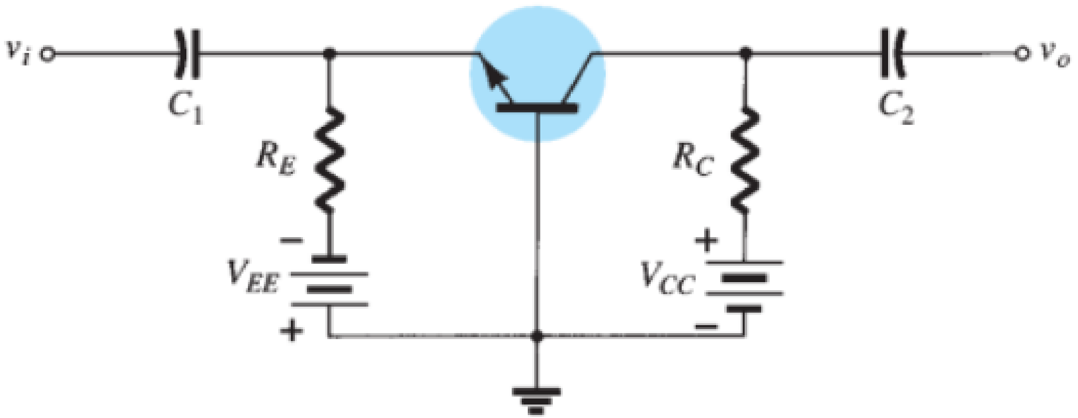


The Common-Base Amplifier

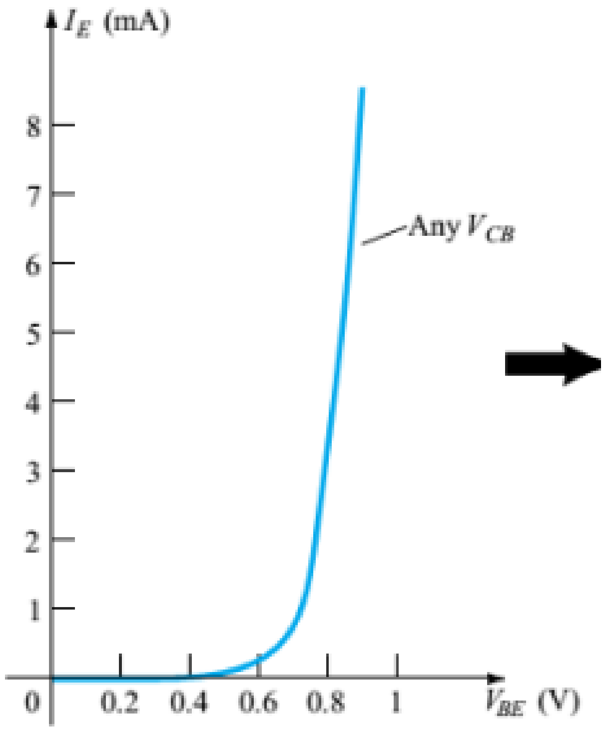
- The common-base (CB) amplifier provides high voltage gain with a maximum current gain of 1. Since it has a low input resistance.
- A typical **common-base** amplifier is shown in figure below. The base is the common terminal and is at ac ground because of capacitor C_2. The input signal is capacitively coupled to the emitter. The output is capacitively coupled from the collector to a load resistor.

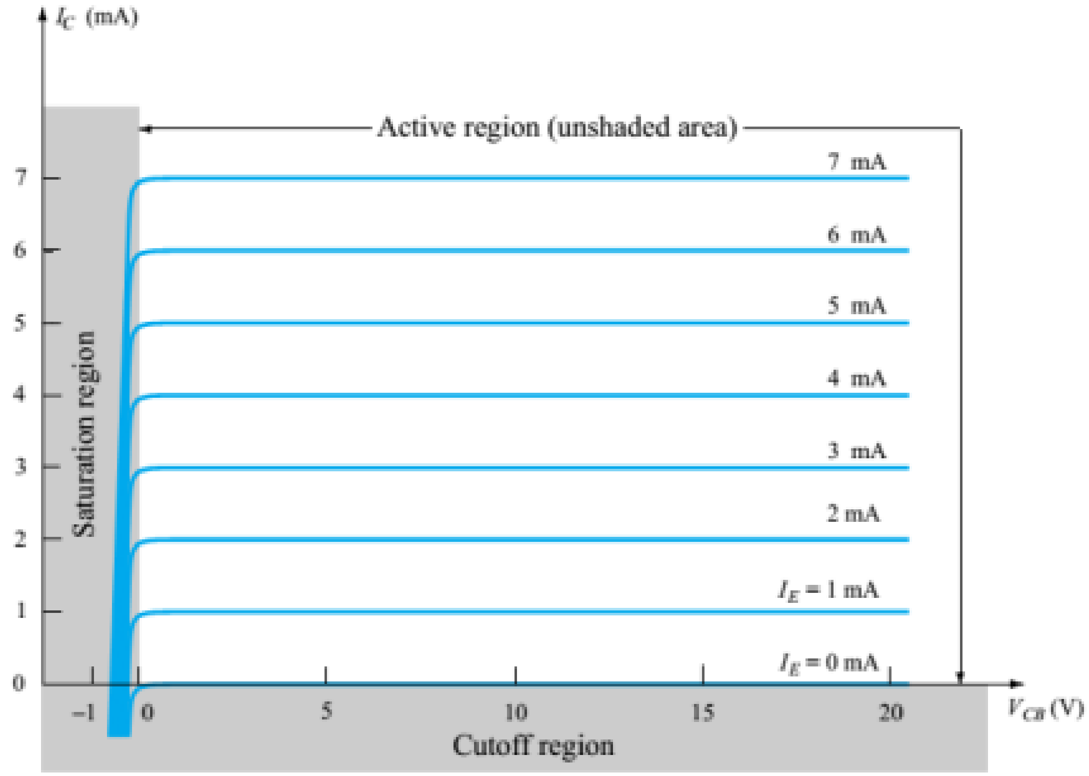


(a) Complete circuit with load



The Common-Base Amplifier characteristic curve

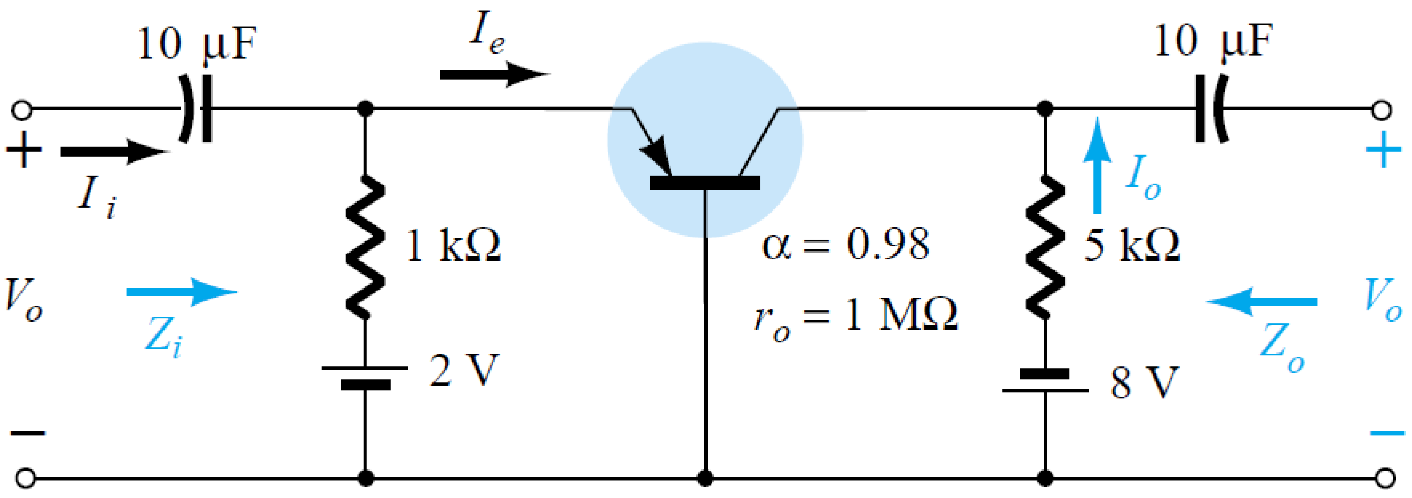




Example:

For the network of Figure below, determine:

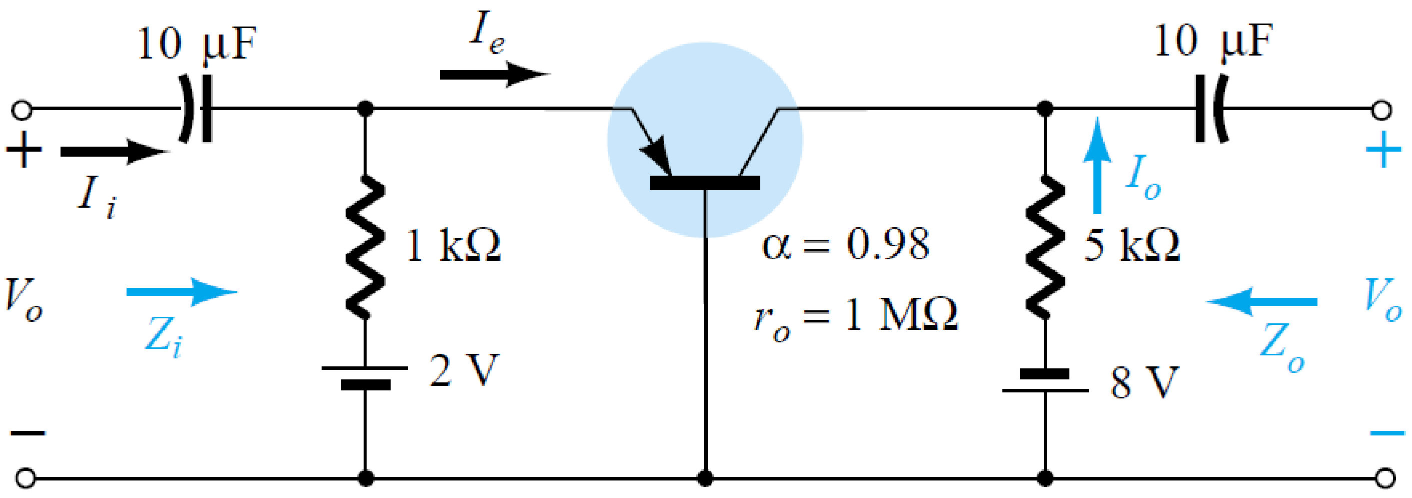
(a) r_e.
(b) Z_i.
(c) Z_o.
(d) A_v.
(e) A_i.



Example:

For the network of Figure below, determine:

(a) r_e.
(b) Z_i.
(c) Z_o.
(d) A_v.
(e) A_i.



Solution:

$$\text{(a)}\quad I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{2\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \frac{1.3\text{ V}}{1\text{ k}\Omega} = 1.3\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{1.3\text{ mA}} = \mathbf{20\ \Omega}$$

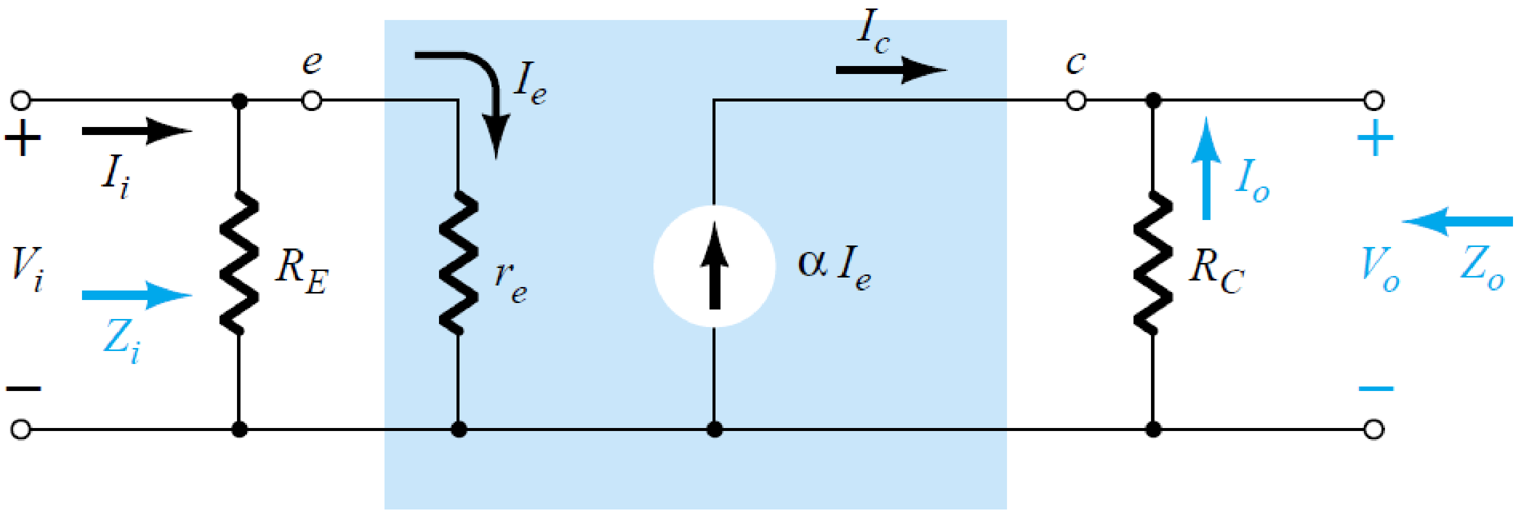
(b) $Z_i = R_E \| r_e = 1\ \text{k}\Omega \| 20\ \Omega$

$= \mathbf{19.61\ \Omega} \cong r_e$

(c) $Z_o = R_C = \mathbf{5\ k\Omega}$

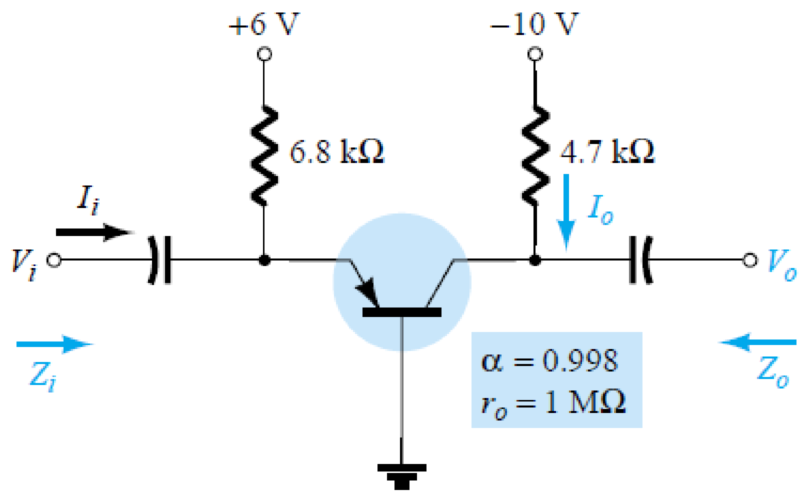
(d) $A_v \cong \dfrac{R_C}{r_e} = \dfrac{5\ \text{k}\Omega}{20\ \Omega} = \mathbf{250}$

(e) $A_i = \mathbf{-0.98} \cong -1$



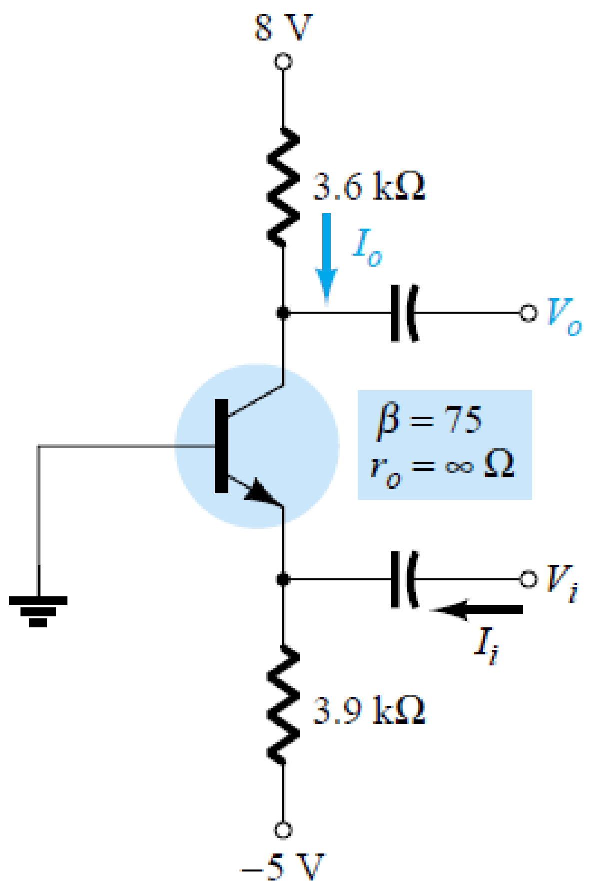
Home Work

- For the common-base configuration of Figure below
- (a) Determine *re*.
- (b) Find *Zi* and *Zo*.
- (c) Calculate *Av* and *Ai*.



Home Work

For the network of Figure below, determine *Av* and *Ai*.



	CE	CC	CB
Voltage gain, A_v	High R_C/r'_e	Low $\cong 1$	High R_C/r'_e
Current gain, $A_{i(max)}$	High β_{ac}	High β_{ac}	Low $\cong 1$
Power gain, A_p	Very high A_iA_v	High $\cong A_i$	High $\cong A_v$
Input resistance, $R_{in(max)}$	Low $\beta_{ac}r'_e$	High $\beta_{ac}R_E$	Very low r'_e
Output resistance, R_{out}	High R_C	Very low $(R_s/\beta_{ac}) \parallel R_E$	High R_C

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Electronic I
Lecture 7
Small-Signal Analysis of Common Emitter Configuration

2nd Class

by
Rafal Raed Mahmood Alshaker

Outlines of Presentation

Common Emitter Fixed bias configuration

- Example

VOLTAGE-DIVIDER BIAS

- Example

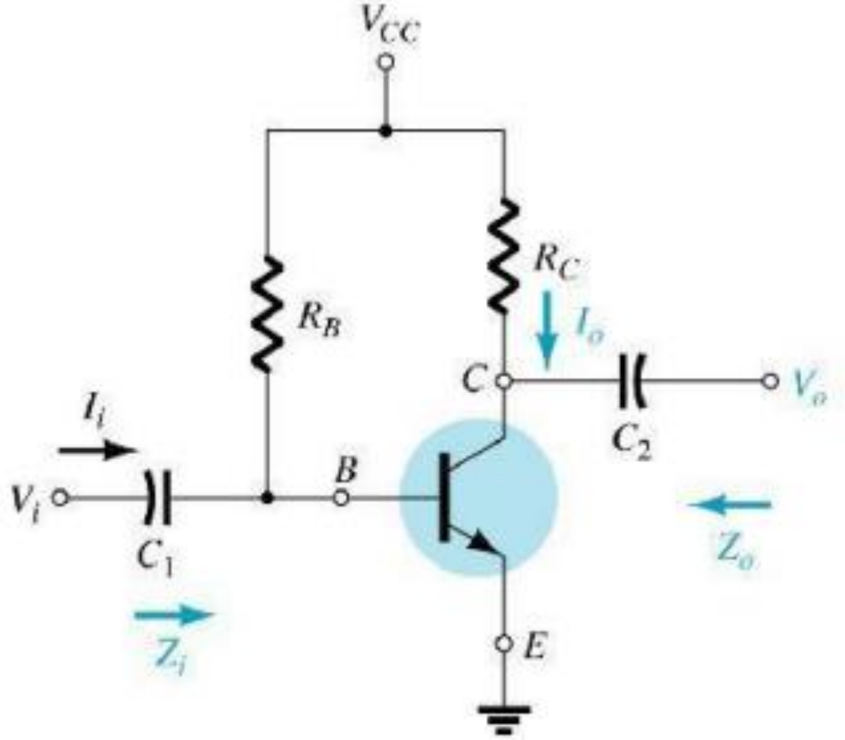
CE Emitter-Bias Configuration (Unbypassed)

- EXAMPLE:

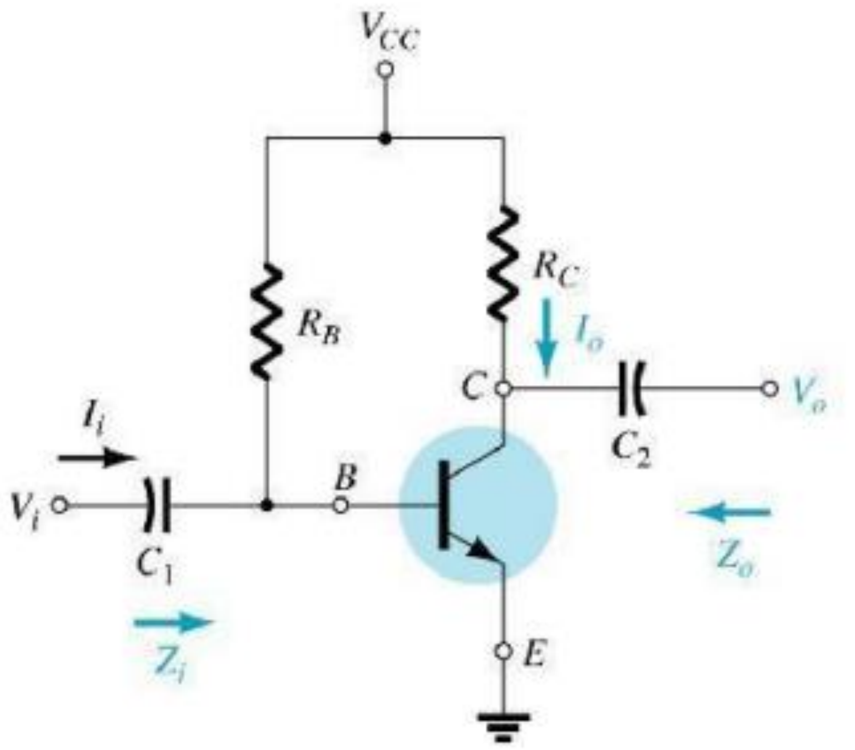
Collector Feedback Configuration

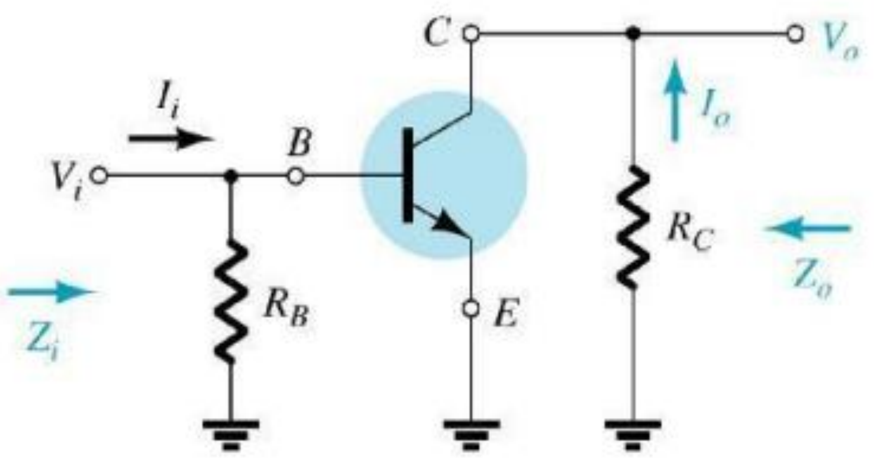
- EXAMPLE:

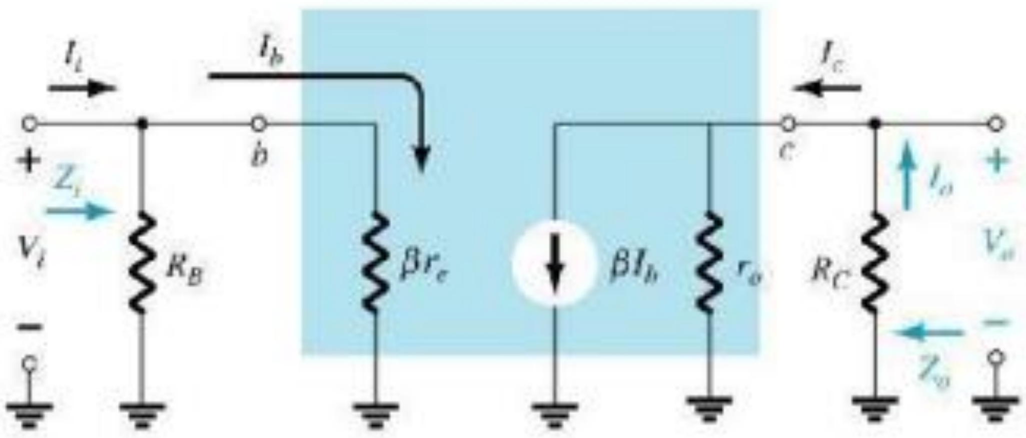
Common Emitter Fixed bias configuration



Common Emitter Fixed bias configuration

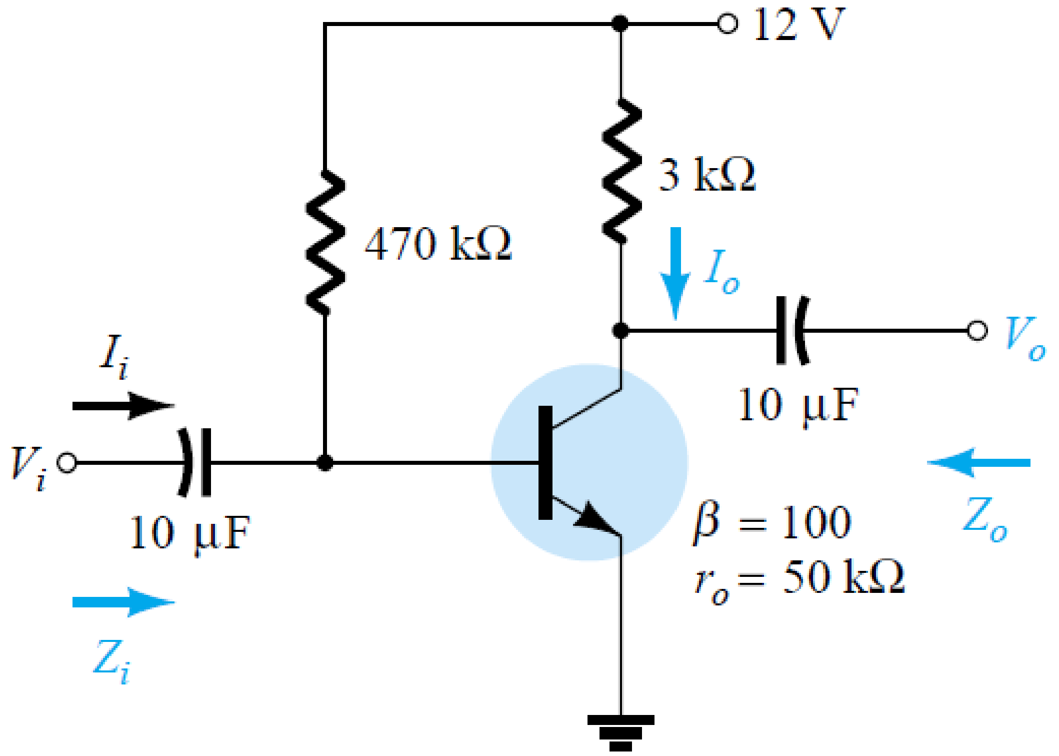






EXAMPLE:

For the network of Fig.



(a) Determine r_e.

(b) Find Z_i (with $r_o = \infty$ Ω).

(c) Calculate Z_o (with $r_o = \infty$Ω).

(d) Determine A_v (with $r_o = \infty$Ω).

(e) Find A_i (with $r_o = \infty$ Ω).

(f) Repeat parts (c) through (e) including r_o = 50 kΩ in all calculations and compare results.

EXAMPLE:

For the network of Fig

(a) DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{470\text{ k}\Omega} = 24.04\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(24.04\ \mu\text{A}) = 2.428\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.428\text{ mA}} = \mathbf{10.71\ \Omega}$$

(b) $\beta r_e = (100)(10.71\ \Omega) = 1.071\text{ k}\Omega$

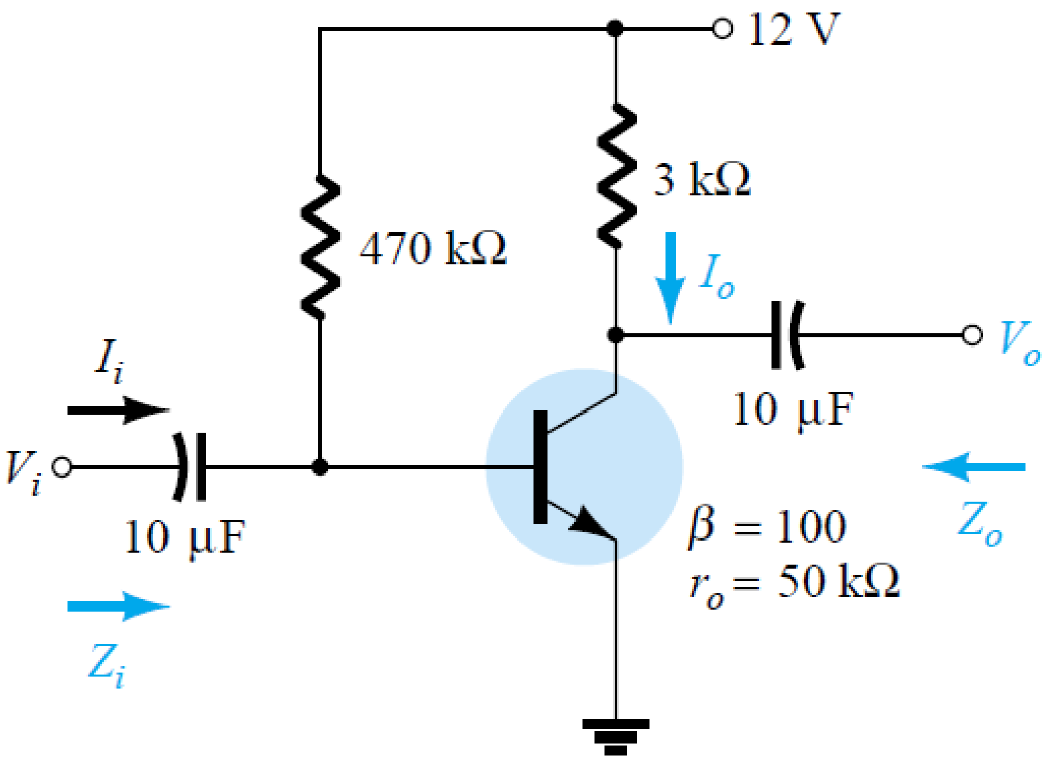
$Z_i = R_B \| \beta r_e = 470\text{ k}\Omega \| 1.071\text{ k}\Omega = \mathbf{1.069\ k\Omega}$

(c) $Z_o = R_C = \mathbf{3\ k\Omega}$

(d) $A_v = -\dfrac{R_C}{r_e} = -\dfrac{3\text{ k}\Omega}{10.71\ \Omega} = \mathbf{-280.11}$

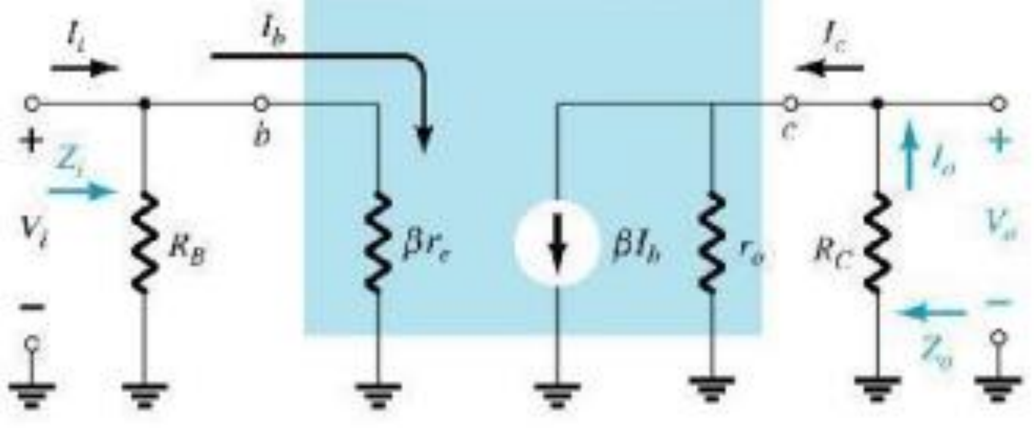
(e) Since $R_B \geq 10\beta r_e (470\text{ k}\Omega > 10.71\text{ k}\Omega)$

$A_i \cong \beta = \mathbf{100}$



EXAMPLE:

Solution:



(f) $Z_o = r_o \| R_C = 50\ \text{k}\Omega \| 3\ \text{k}\Omega = \mathbf{2.83\ k\Omega}$ vs. $3\ \text{k}\Omega$

$$A_v = -\frac{r_o \| R_C}{r_e} = \frac{2.83\ \text{k}\Omega}{10.71\ \Omega} = \mathbf{-264.24} \text{ vs. } -280.11$$

$$A_i = \frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)} = \frac{(100)(470\ \text{k}\Omega)(50\ \text{k}\Omega)}{(50\ \text{k}\Omega + 3\ \text{k}\Omega)(470\ \text{k}\Omega + 1.071\ \text{k}\Omega)}$$

$$= \mathbf{94.13} \text{ vs. } 100$$

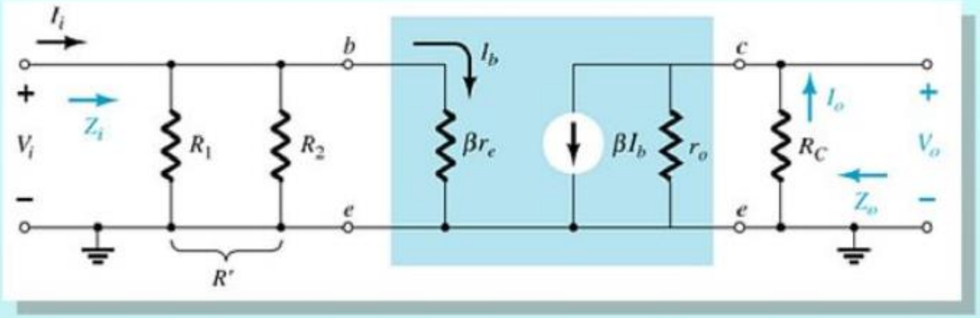
As a check:

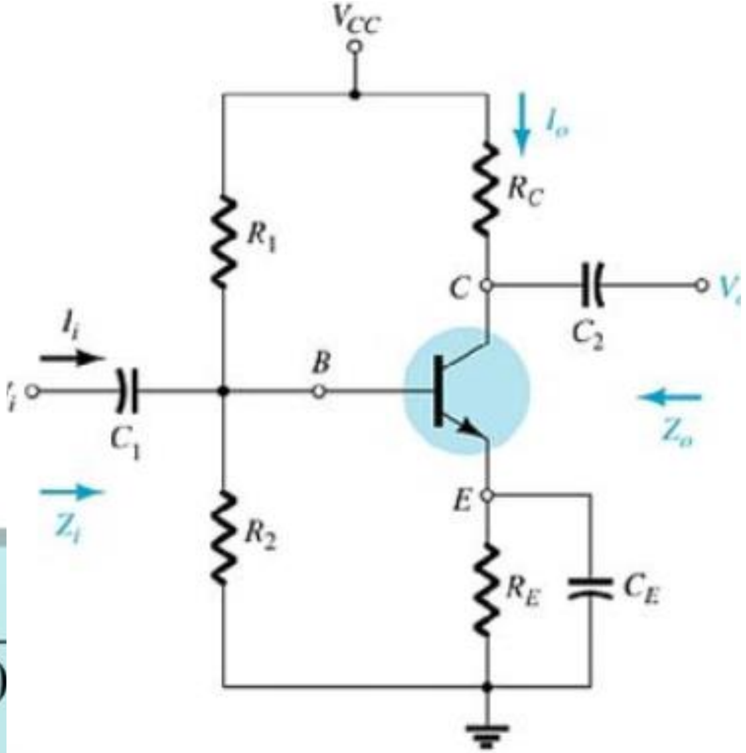
$$A_i = -A_v \frac{Z_i}{R_C} = \frac{-(-264.24)(1.069\ \text{k}\Omega)}{3\ \text{k}\Omega} = \mathbf{94.16}$$

which differs slightly only due to the accuracy carried through the calculations.

Common emitter voltage divider Configuration

r_e model requires you to determine β, r_e, and r_o.





Input impedance:

$$R' = R_1 \| R_2$$

$$Z_i = R' \| \beta r_e$$

Output impedance:

$$Z_o = R_C \| r_o$$

$$Z_o \cong R_C \Big|_{r_o \geq 10R_C}$$

Voltage gain:

$$A_v = \frac{V_o}{V_i} = \frac{-R_C \| r_o}{r_e}$$

$$A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e} \Big|_{r_o \geq 10R_C}$$

Current gain:

$$A_i = \frac{I_o}{I_i} = \frac{\beta R' r_o}{(r_o + R_C)(R' + \beta r_e)}$$

$$A_i = \frac{I_o}{I_i} \cong \frac{\beta R'}{R' + \beta r_e} \Big|_{r_o \geq 10R_C}$$

$$A_i = \frac{I_o}{I_i} \cong \beta \Big|_{r_o \geq 10R_C,\ R' \geq 10\beta r_e}$$

Current gain from voltage gain:

$$A_i = -A_v \frac{Z_i}{R_C}$$

EXAMPLE:

For the network of Fig, determine:

(a) re.

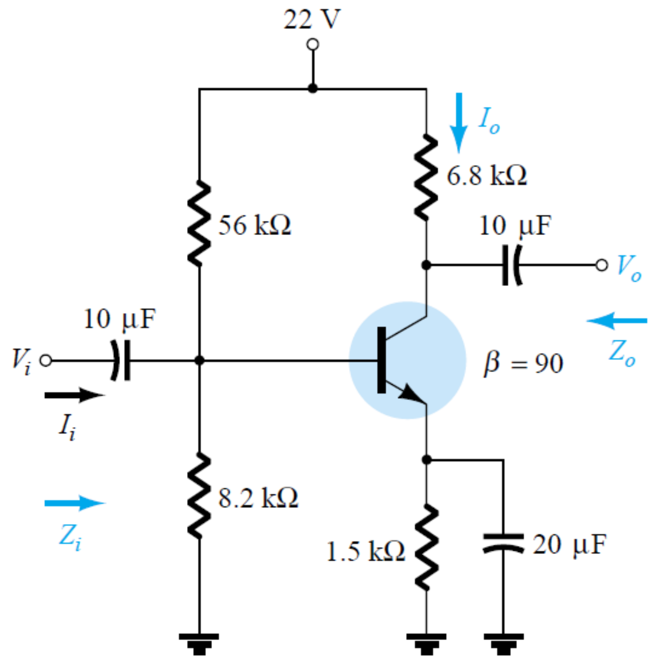
(b) Z_i.

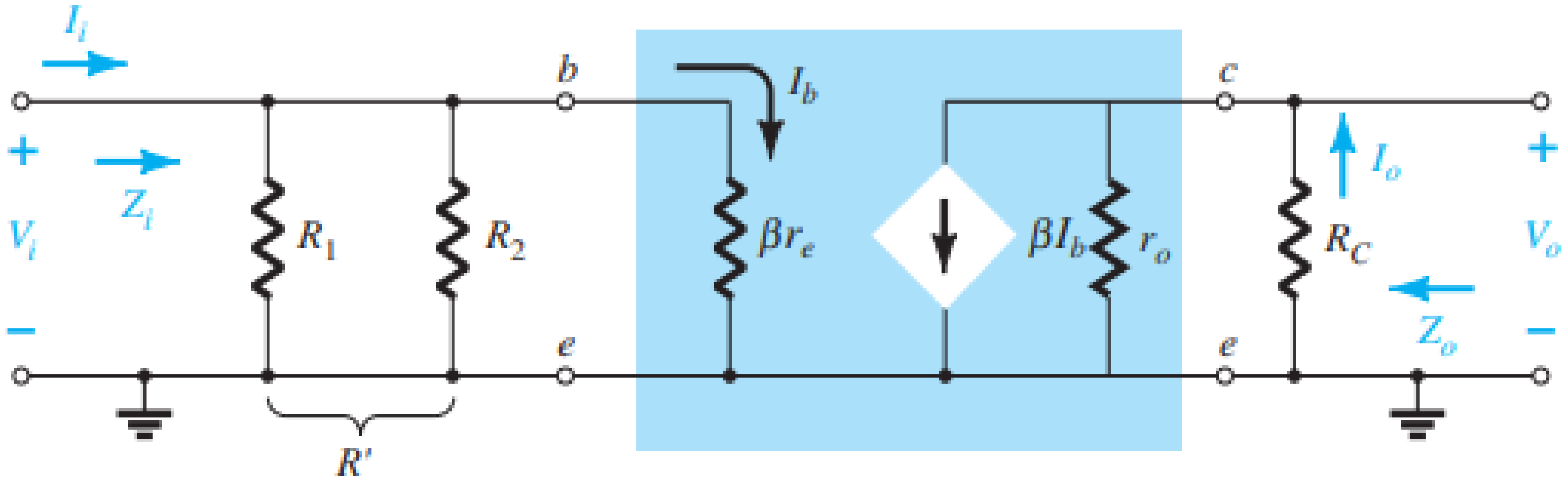
(c) Z_o (with $r_o = \infty\Omega$

(d) A_v (with $r_o = \infty\Omega$

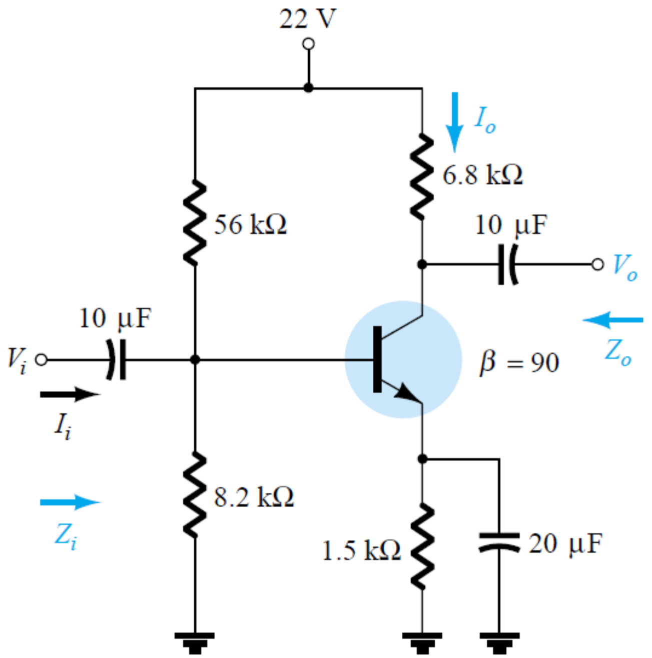
(e) A_i (with $r_o = \infty\Omega$

(f) The parameters of parts (b) through (e) if r_o = 50 kΩ and compare results.





EXAMPLE:



a. DC: Testing $\beta R_E > 10R_2$,

$$(90)(1.5\text{ k}\Omega) > 10(8.2\text{ k}\Omega)$$
$$135\text{ k}\Omega > 82\text{ k}\Omega\ (\textit{satisfied})$$

Using the approximate approach, we obtain

$$V_B = \frac{R_2}{R_1 + R_2}V_{CC} = \frac{(8.2\text{ k}\Omega)(22\text{ V})}{56\text{ k}\Omega + 8.2\text{ k}\Omega} = 2.81\text{ V}$$
$$V_E = V_B - V_{BE} = 2.81\text{ V} - 0.7\text{ V} = 2.11\text{ V}$$
$$I_E = \frac{V_E}{R_E} = \frac{2.11\text{ V}}{1.5\text{ k}\Omega} = 1.41\text{ mA}$$
$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{1.41\text{ mA}} = \mathbf{18.44\ \Omega}$$

b. $R' = R_1 \| R_2 = (56\text{ k}\Omega)\|(8.2\text{ k}\Omega) = 7.15\text{ k}\Omega$

$Z_i = R' \| \beta r_e = 7.15\text{ k}\Omega \| (90)(18.44\ \Omega) = 7.15\text{ k}\Omega \| 1.66\text{ k}\Omega$

$= \mathbf{1.35\text{ k}\Omega}$

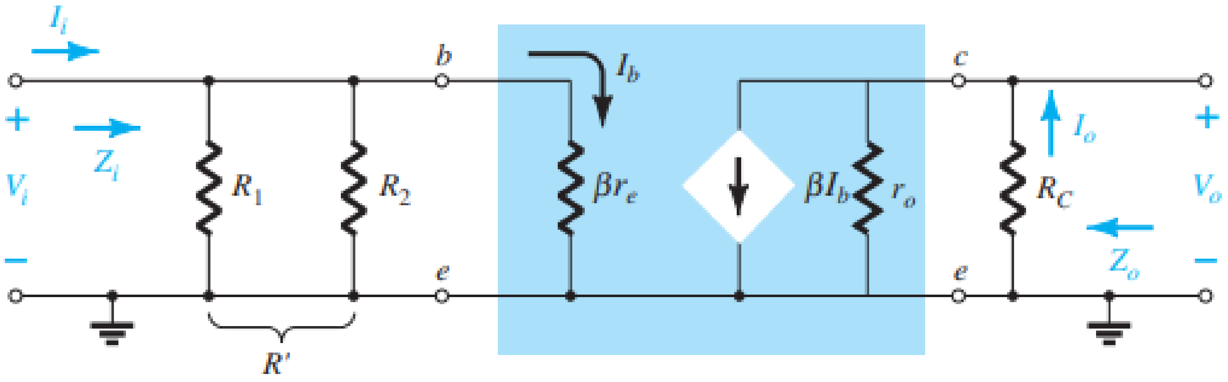
c. $Z_o = R_C = \mathbf{6.8\text{ k}\Omega}$

d. $A_v = -\frac{R_C}{r_e} = -\frac{6.8\text{ k}\Omega}{18.44\ \Omega} = \mathbf{-368.76}$

e. $Z_i = \mathbf{1.35\text{ k}\Omega}$

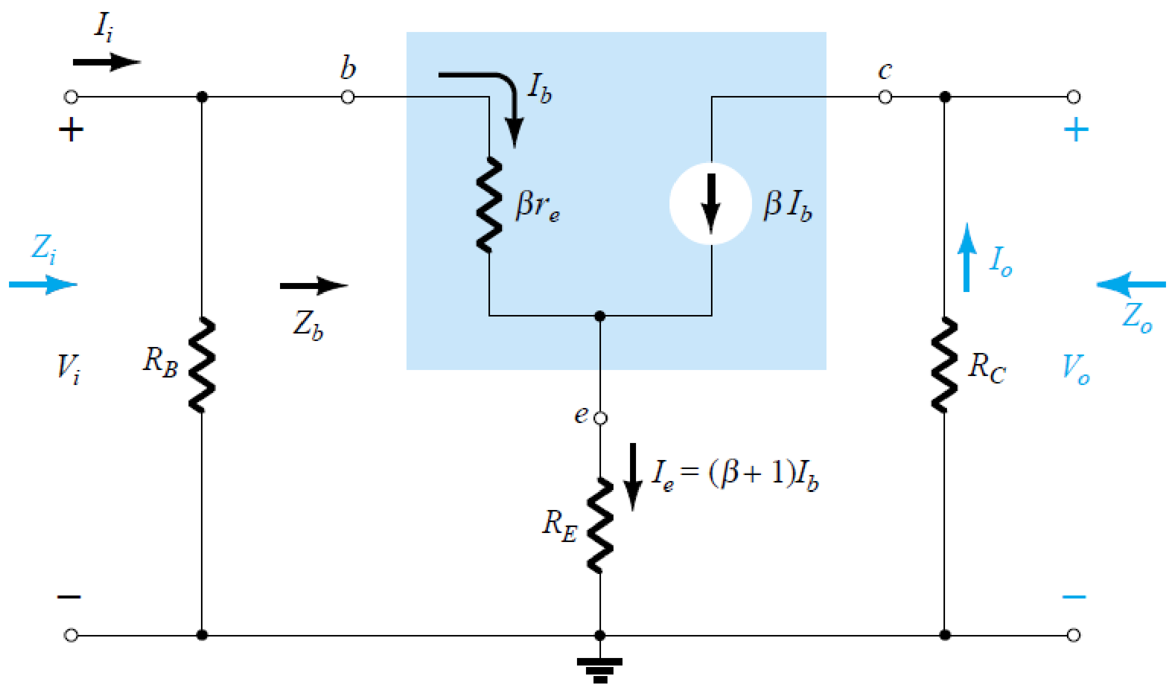
$Z_o = R_C \| r_o = 6.8\text{ k}\Omega \| 50\text{ k}\Omega = \mathbf{5.98\text{ k}\Omega}$ vs. 6.8 kΩ

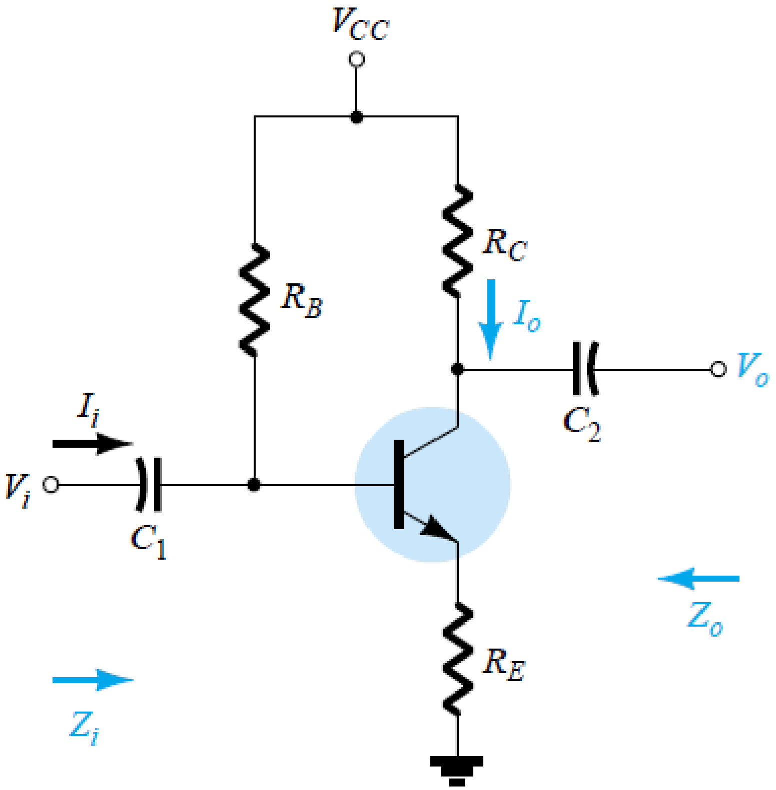
$A_v = -\frac{R_C \| r_o}{r_e} = -\frac{5.98\text{ k}\Omega}{18.44\ \Omega} = \mathbf{-324.3}$ vs. −368.76



There was a measurable difference in the results for Z_o and A_v, b
$r_o \geq 10R_C$ was *not* satisfied.

CE Emitter-Bias Configuration (Unbypassed)





CE Emitter-Bias Configuration (Unbypassed)

EXAMPLE:

For the network shown in the figure below , without C_E (unbypassed), determine:

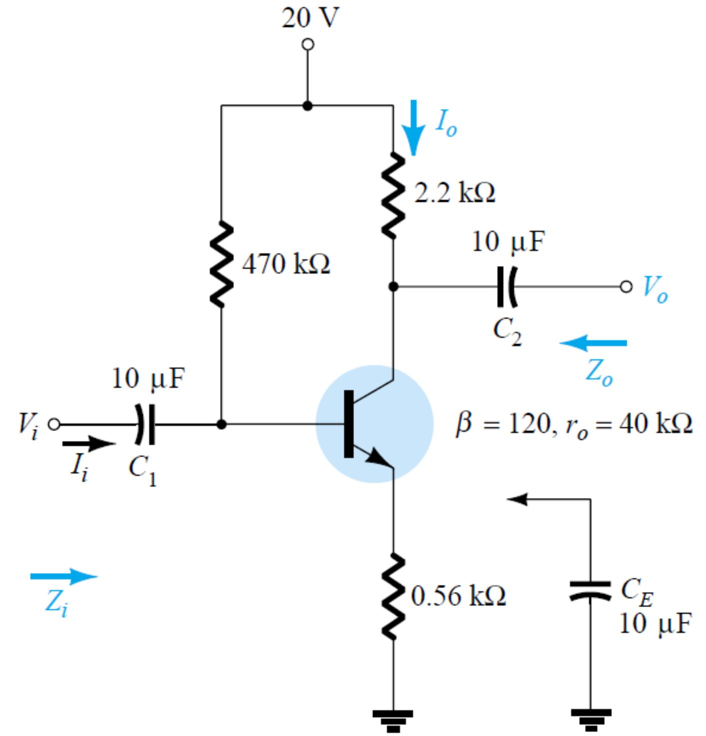
(a) r_e.

(b) Z_i.

(c) Z_o.

(d) A_v.

(e) A_i.



CE Emitter-Bias Configuration (Unbypassed)

EXAMPLE:

For the network shown in the figure below , without C_E (unbypassed), determine:

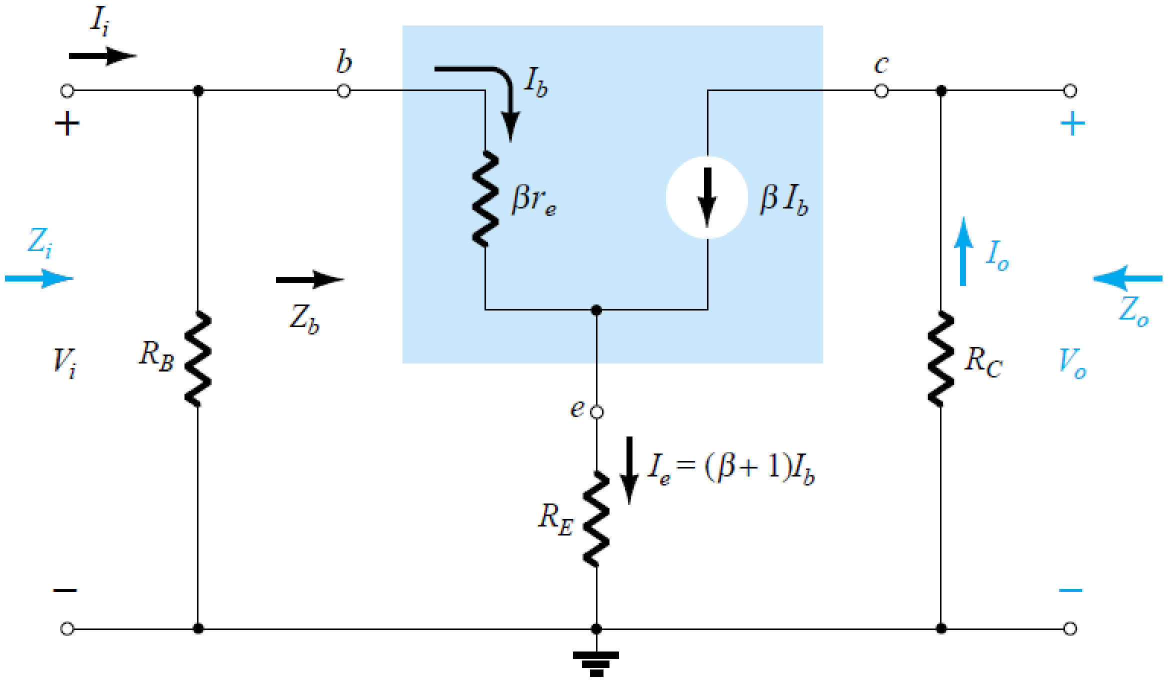
(a) r_e.

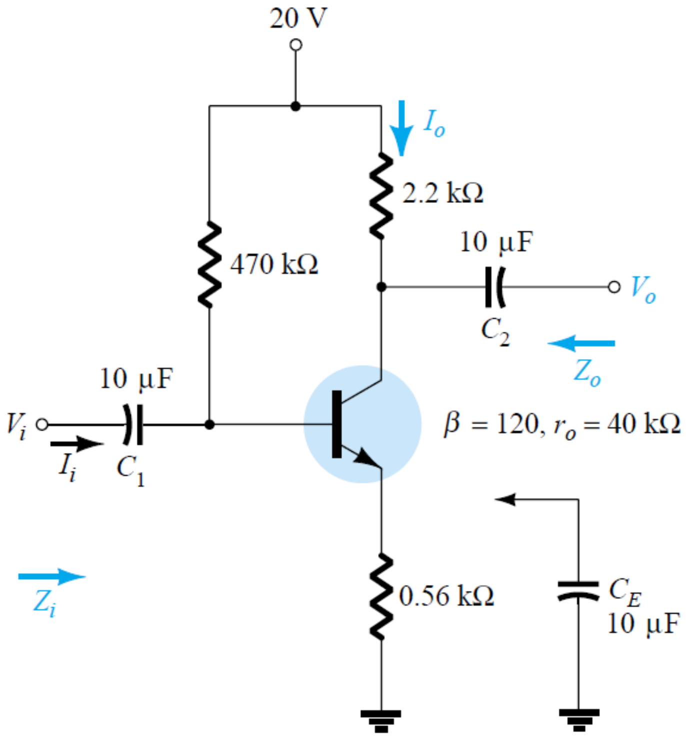
(b) Z_i.

(c) Z_o.

(d) A_v.

(e) A_i.





CE Emitter-Bias Configuration (Unbypassed)

Solution:

a. DC:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{470\text{ k}\Omega + (121)0.56\text{ k}\Omega} = 35.89\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (121)(35.89\ \mu\text{A}) = 4.34\text{ mA}$$

and $$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{4.34\text{ mA}} = \mathbf{5.99\ \Omega}$$

b. Testing the condition $r_o \geq 10(R_C + R_E)$, we obtain

$$40\text{ k}\Omega \geq 10(2.2\text{ k}\Omega + 0.56\text{ k}\Omega)$$
$$40\text{ k}\Omega \geq 10(2.76\text{ k}\Omega) = 27.6\text{ k}\Omega\ (\textit{satisfied})$$

Therefore,

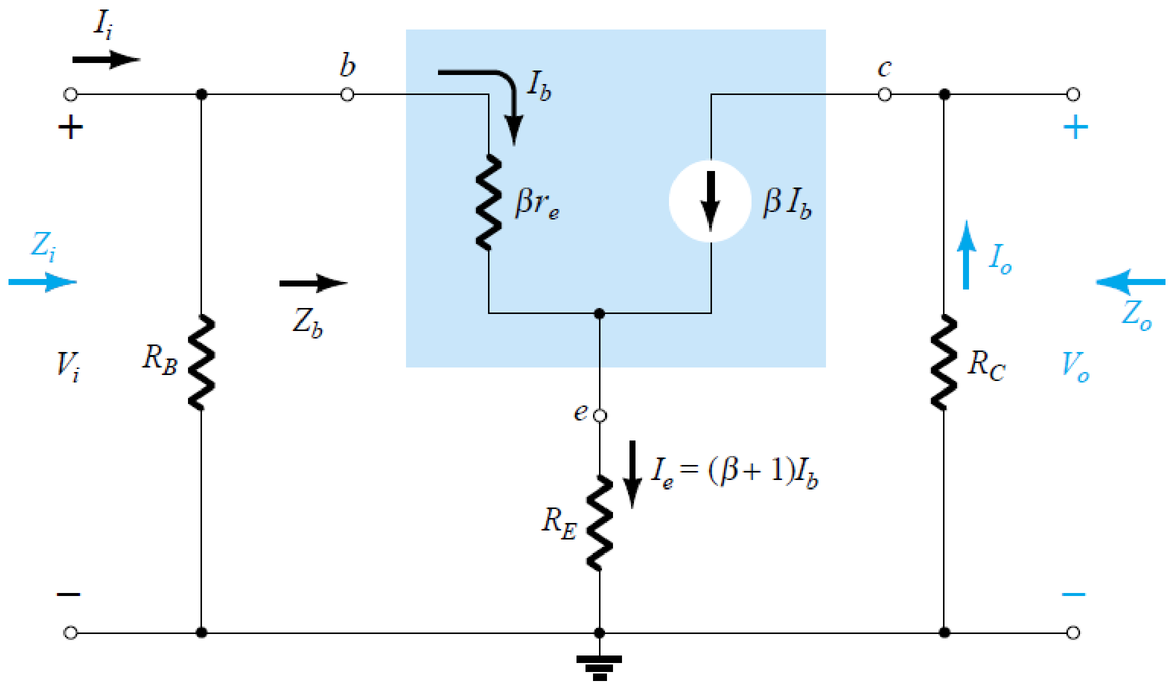
$$Z_b \cong \beta(r_e + R_E) = 120(5.99\ \Omega + 560\ \Omega)$$
$$= 67.92\text{ k}\Omega$$

and $$Z_i = R_B \| Z_b = 470\text{ k}\Omega \| 67.92\text{ k}\Omega$$
$$= \mathbf{59.34\text{ k}\Omega}$$

c. $Z_o = R_C = \mathbf{2.2\text{ k}\Omega}$

d. $r_o \geq 10R_C$ is satisfied. Therefore,

$$A_v = \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b} = -\frac{(120)(2.2\text{ k}\Omega)}{67.92\text{ k}\Omega}$$
$$= \mathbf{-3.89}$$



Home Work

Repeat the analysis of the previous example with CE in place.

Solution

(a) The dc analysis is the same, and $r_e = 5.99\ \Omega$.

(b) R_E is "shorted out" by C_E for the ac analysis. Therefore,

$$Z_i = R_B \| Z_b = R_B \| \beta r_e = 470\ \text{k}\Omega \| (120)(5.99\ \Omega)$$
$$= 470\ \text{k}\Omega \| 718.8\ \Omega \cong \mathbf{717.70\ \Omega}$$

(c) $Z_o = R_C = \mathbf{2.2\ k\Omega}$

(d) $A_v = -\dfrac{R_C}{r_e}$

$$= -\frac{2.2\ \text{k}\Omega}{5.99\ \Omega} = \mathbf{-367.28} \quad \text{(a significant increase)}$$

(e) $A_i = \dfrac{\beta R_B}{R_B + Z_b} = \dfrac{(120)(470\ \text{k}\Omega)}{470\ \text{k}\Omega + 718.8\ \Omega}$

$$= \mathbf{119.82}$$

Collector Feedback Configuration

Input impedance:

$$Z_i = \frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_F}}$$

Output impedance:

$$Z_o \cong R_C \parallel R_F$$

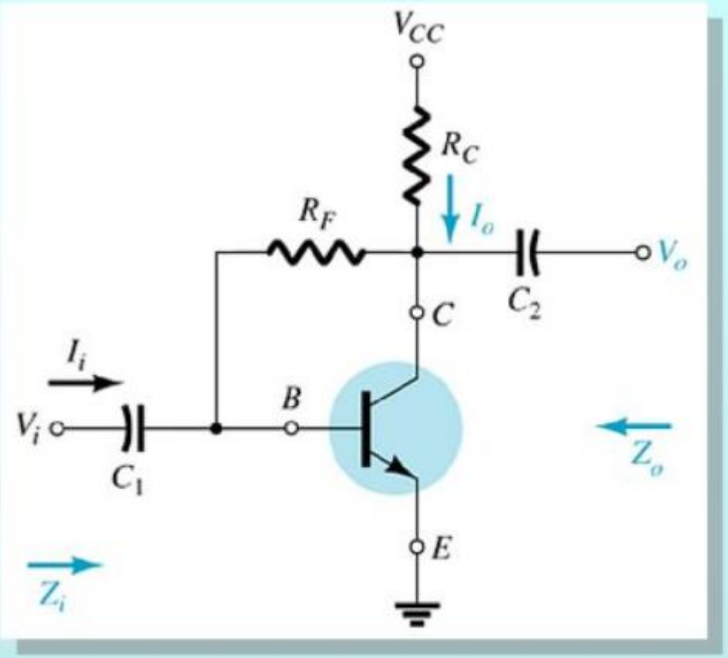
Voltage gain:

$$A_v = \frac{V_o}{V_i} = -\frac{R_C}{r_e}$$

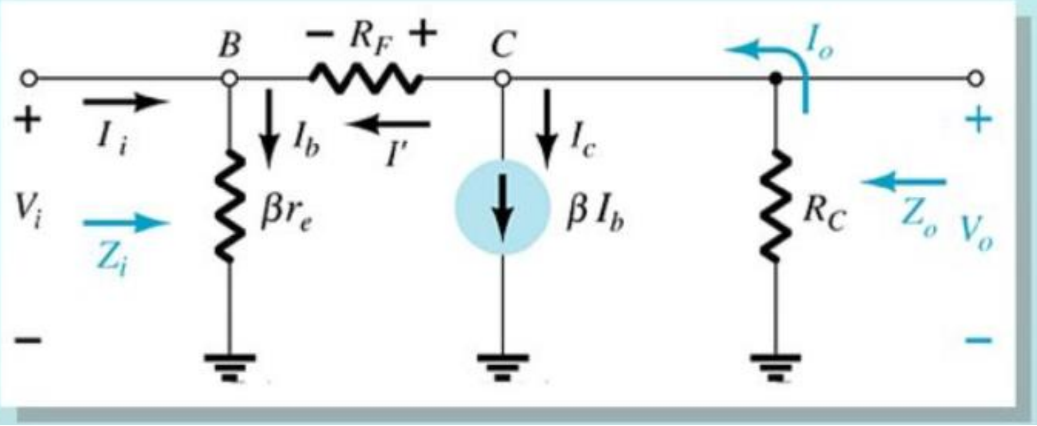
Current gain:

$$A_i = \frac{I_o}{I_i} = \frac{\beta R_F}{R_F + \beta R_C}$$

$$A_i = \frac{I_o}{I_i} \cong \frac{R_F}{R_C}$$



- This is a variation of the common-emitter fixed-bias configuration
- Input is applied to the base
- Output is taken from the collector
- There is a 180° phase shift between input and output



Collector Feedback Configuration

EXAMPLE:

For the network of Fig. , determine:

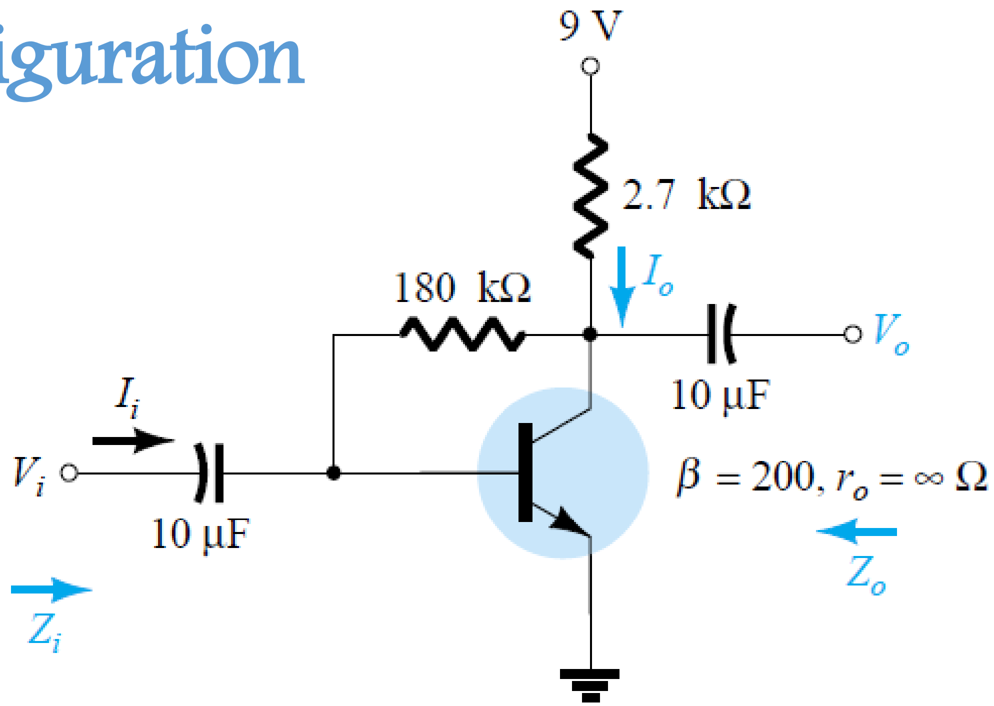
(a) re.

(b) Z_i.

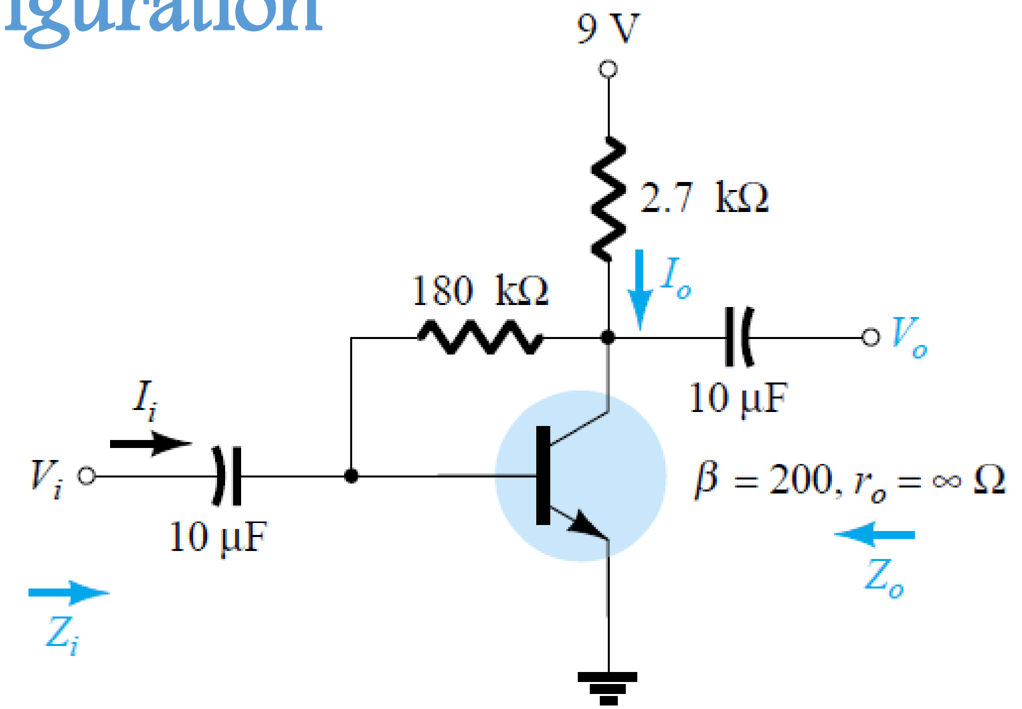
(c) Z_o

(d) A_v

(e) A_i



Collector Feedback Configuration



Solution

(a) $I_B = \dfrac{V_{CC} - V_{BE}}{R_F + \beta R_C} = \dfrac{9\text{ V} - 0.7\text{ V}}{180\text{ k}\Omega + (200)2.7\text{ k}\Omega}$

$= 11.53\ \mu\text{A}$

$I_E = (\beta + 1)I_B = (201)(11.53\ \mu\text{A}) = 2.32\text{ mA}$

$r_e = \dfrac{26\text{ mV}}{I_E} = \dfrac{26\text{ mV}}{2.32\text{ mA}} = \mathbf{11.21\ \Omega}$

(b) $Z_i = \dfrac{r_e}{\dfrac{1}{\beta} + \dfrac{R_C}{R_F}} = \dfrac{11.21\ \Omega}{\dfrac{1}{200} + \dfrac{2.7\text{ k}\Omega}{180\text{ k}\Omega}} = \dfrac{11.21\ \Omega}{0.005 + 0.015}$

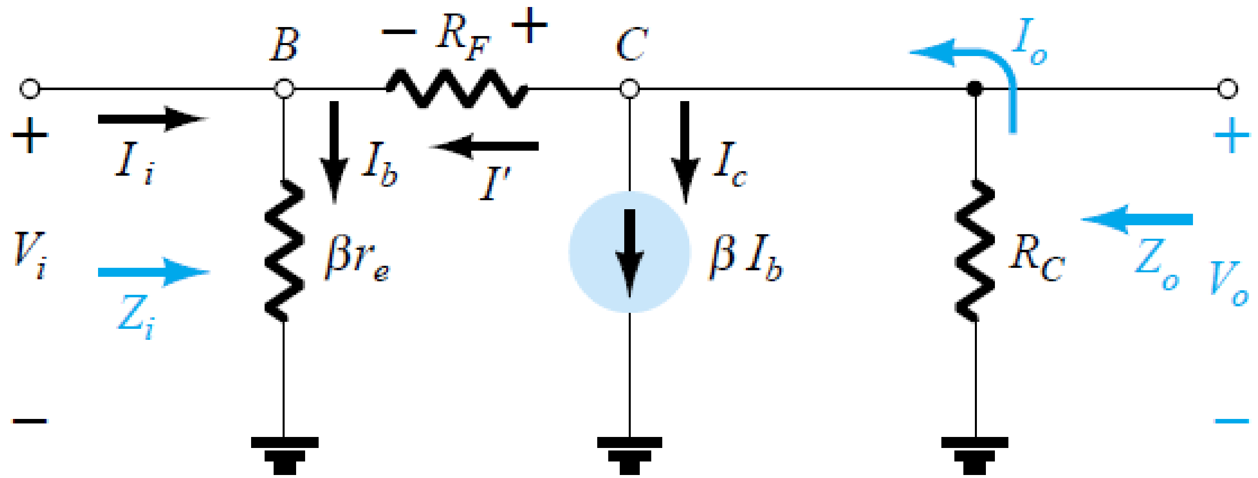
$= \dfrac{11.21\ \Omega}{0.02} = 50(11.21\ \Omega) = \mathbf{560.5\ \Omega}$

(c) $Z_o = R_C \| R_F = 2.7\text{ k}\Omega \| 180\text{ k}\Omega = \mathbf{2.66\text{ k}\Omega}$

(d) $A_v = -\dfrac{R_C}{r_e} = -\dfrac{27\text{ k}\Omega}{11.21\ \Omega} = \mathbf{-240.86}$

(e) $A_i = \dfrac{\beta R_F}{R_F + \beta R_C} = \dfrac{(200)(180\text{ k}\Omega)}{180\text{ k}\Omega + (200)(2.7\text{ k}\Omega)}$

$= \mathbf{50}$



Collector Feedback Configuration

EXAMPLE:

For the network of Fig. , determine:

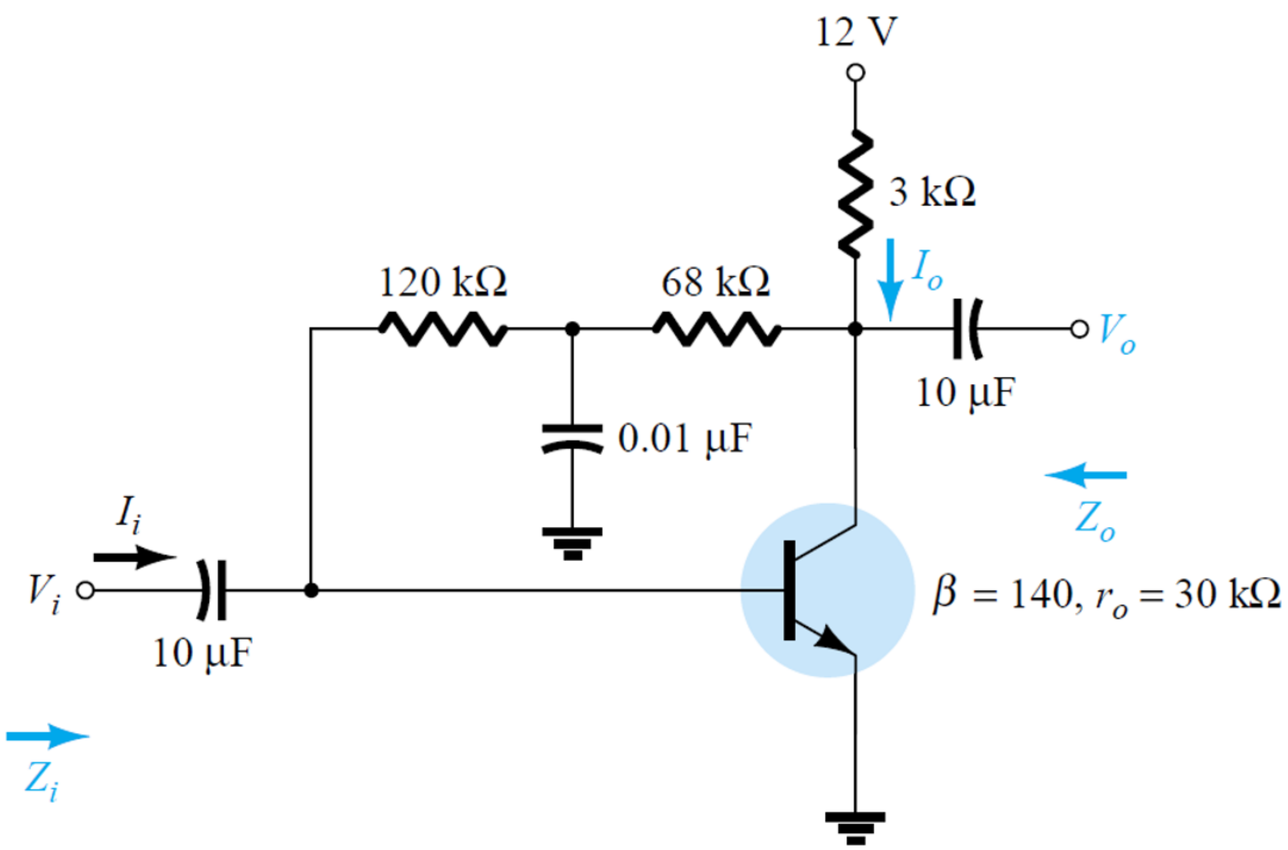
(a) re.

(b) Z_i.

(c) Z_o

(d) A_v

(e) A_i



Solution:

(a) DC: $$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta R_C}$$

$$= \frac{12\text{ V} - 0.7\text{ V}}{(120\text{ k}\Omega + 68\text{ k}\Omega) + (140)3\text{ k}\Omega}$$

$$= \frac{11.3\text{V}}{608\text{ k}\Omega} = 18.6\mu\text{A}$$

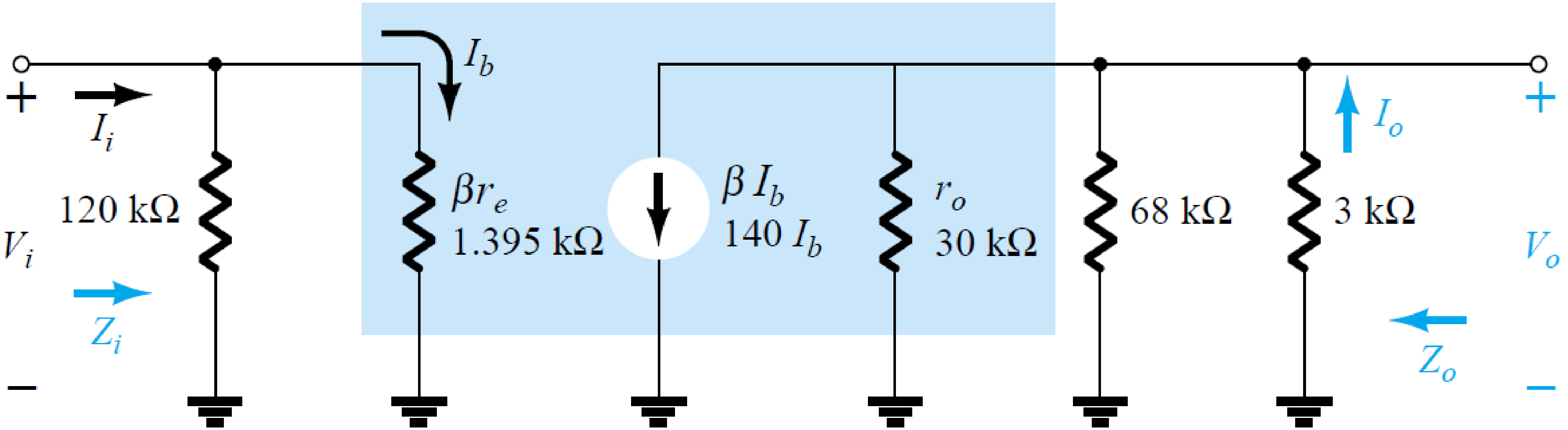
$$I_E = (\beta + 1)I_B = (141)(18.6\mu A)$$
$$= 2.62\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.62\text{ mA}} = \mathbf{9.92\ \Omega}$$

(b) $\beta r_e = (140)(9.92\ \Omega) = 1.39\ \text{k}\Omega$

The AC equivalent network appears in figure below

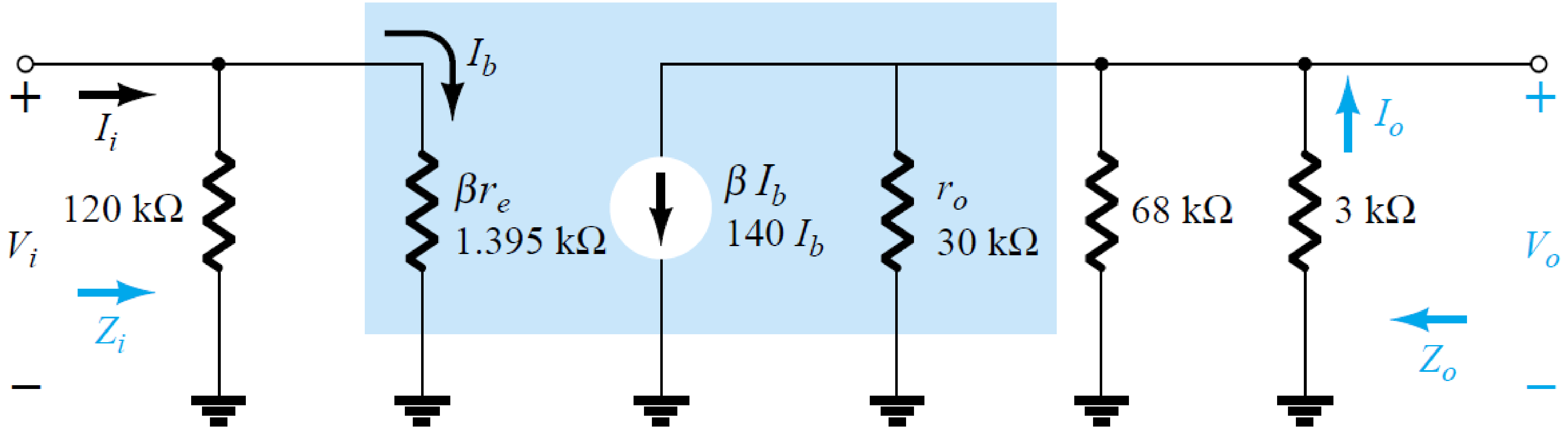
$$Z_i = R_{F_1} \| \beta r_e = 120\ \text{k}\Omega \| 1.39\ \text{k}\Omega$$
$$\cong \mathbf{1.37\ k\Omega}$$



$$Z_o \cong R_C \| R_{F_2} = 3\ \text{k}\Omega \| 68\ \text{k}\Omega$$
$$= \mathbf{2.87\ k\Omega}$$

(d) $r_o \geq 10R_C$, therefore,

$$A_v \cong -\frac{R_{F_2} \| R_C}{r_e} = -\frac{68\ \text{k}\Omega \| 3\ \text{k}\Omega}{9.92\ \Omega}$$
$$\cong -\frac{2.87\ \text{k}\Omega}{9.92\ \Omega}$$
$$\cong \mathbf{-289.3}$$



(e) Since the condition $R_{F_1} \gg \beta r_e$ is satisfied,

$$A_i \cong \frac{\beta}{1 + \dfrac{R_C}{r_o \| R_{F_2}}} = \frac{140}{1 + \dfrac{3\ \text{k}\Omega}{30\ \text{k}\Omega \| 68\ \text{k}\Omega}} = \frac{140}{1 + 0.14} = \frac{140}{1.14}$$

$$\cong \mathbf{122.8}$$

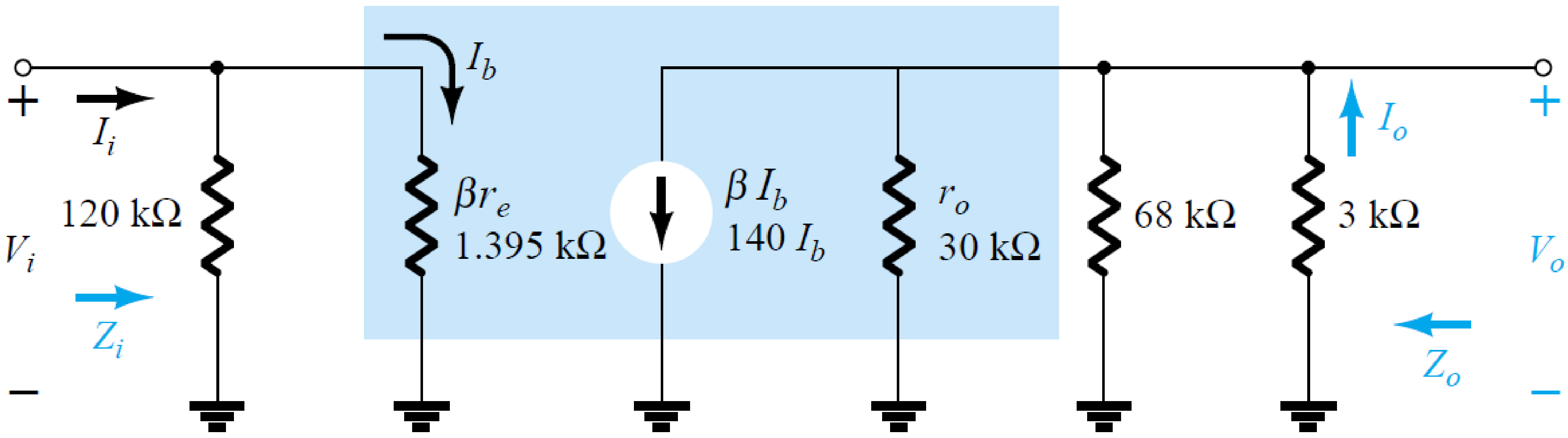
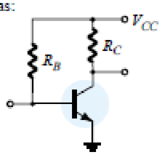
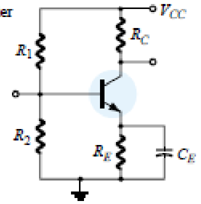
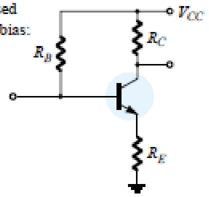
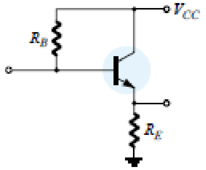
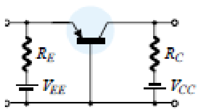
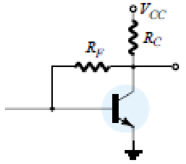


TABLE 8.1 Relative Levels for the Important Parameters of the CE, CB, and CC Transistor Amplifiers

Configuration	Z_i	Z_o	A_v	A_i
Fixed-bias: 	Medium (1 kΩ) $= R_B \| \beta r_e$ $\cong \beta r_e$ $(R_B \geq 10\beta r_e)$	Medium (2 kΩ) $= R_C \| r_o$ $\cong R_C$ $(r_o \geq 10R_C)$	High (−200) $= -\frac{(R_C \| r_o)}{r_e}$ $\cong -\frac{R_C}{r_e}$ $(r_o \geq 10R_C)$	High (100) $= \frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)}$ $\cong \beta$ $(r_o \geq 10R_C,$ $R_B \geq 10\beta r_e)$
Voltage-divider bias: 	Medium (1 kΩ) $= R_1 \| R_2 \| \beta r_e$	Medium (2 kΩ) $= R_C \| r_o$ $\cong R_C$ $(r_o \geq 10R_C)$	High (−200) $= -\frac{R_C \| r_o}{r_e}$ $\cong -\frac{R_C}{r_e}$ $(r_o \geq 10R_C)$	High (50) $= \frac{\beta(R_1 \| R_2)r_o}{(r_o + R_C)(R_1 \| R_2 + \beta r_e)}$ $\cong \frac{\beta(R_1 \| R_2)}{R_1 \| R_2 + \beta r_e}$ $(r_o \geq 10R_C)$
Unbypassed emitter bias: 	High (100 kΩ) $= R_B \| Z_b$ $Z_b \cong \beta(r_e + R_E)$ $\cong R_B \| \beta R_E$ $(R_E \gg r_e)$	Medium (2 kΩ) $= R_C$ (any level of r_o)	Low (−5) $= -\frac{R_C}{r_e + R_E}$ $\cong -\frac{R_C}{R_E}$ $(R_E \gg r_e)$	High (50) $\cong -\frac{\beta R_B}{R_B + Z_b}$
Emitter-follower: 	High (100 kΩ) $= R_B \| Z_b$ $Z_b \cong \beta(r_e + R_E)$ $\cong R_B \| \beta R_E$ $(R_E \gg r_e)$	Low (20 Ω) $= R_E \| r_e$ $\cong r_e$ $(R_E \gg r_e)$	Low ($\cong$ 1) $= \frac{R_E}{R_E + r_e}$ $\cong 1$	High (−50) $\cong -\frac{\beta R_B}{R_B + Z_b}$
Common-base: 	Low (20 Ω) $= R_E \| r_e$ $\cong r_e$ $(R_E \gg r_e)$	Medium (2 kΩ) $= R_C$	High (200) $\cong \frac{R_C}{r_e}$	Low (−1) $\cong -1$
Collector feedback: 	Medium (1 kΩ) $= \frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_F}}$ $(r_o \geq 10R_C)$	Medium (2 kΩ) $\cong R_C \| R_F$ $(r_o \geq 10R_C)$	High (−200) $\cong -\frac{R_C}{r_e}$ $(r_o \geq 10R_C)$ $R_F \gg R_C)$	High (50) $= \frac{\beta R_F}{R_F + \beta R_C}$ $\cong \frac{R_F}{R_C}$

Ninevah University
College of Electronics Engineering
Department of Systems and Control

Electronic I
Lecture 8

Effect of R_L and the R_S

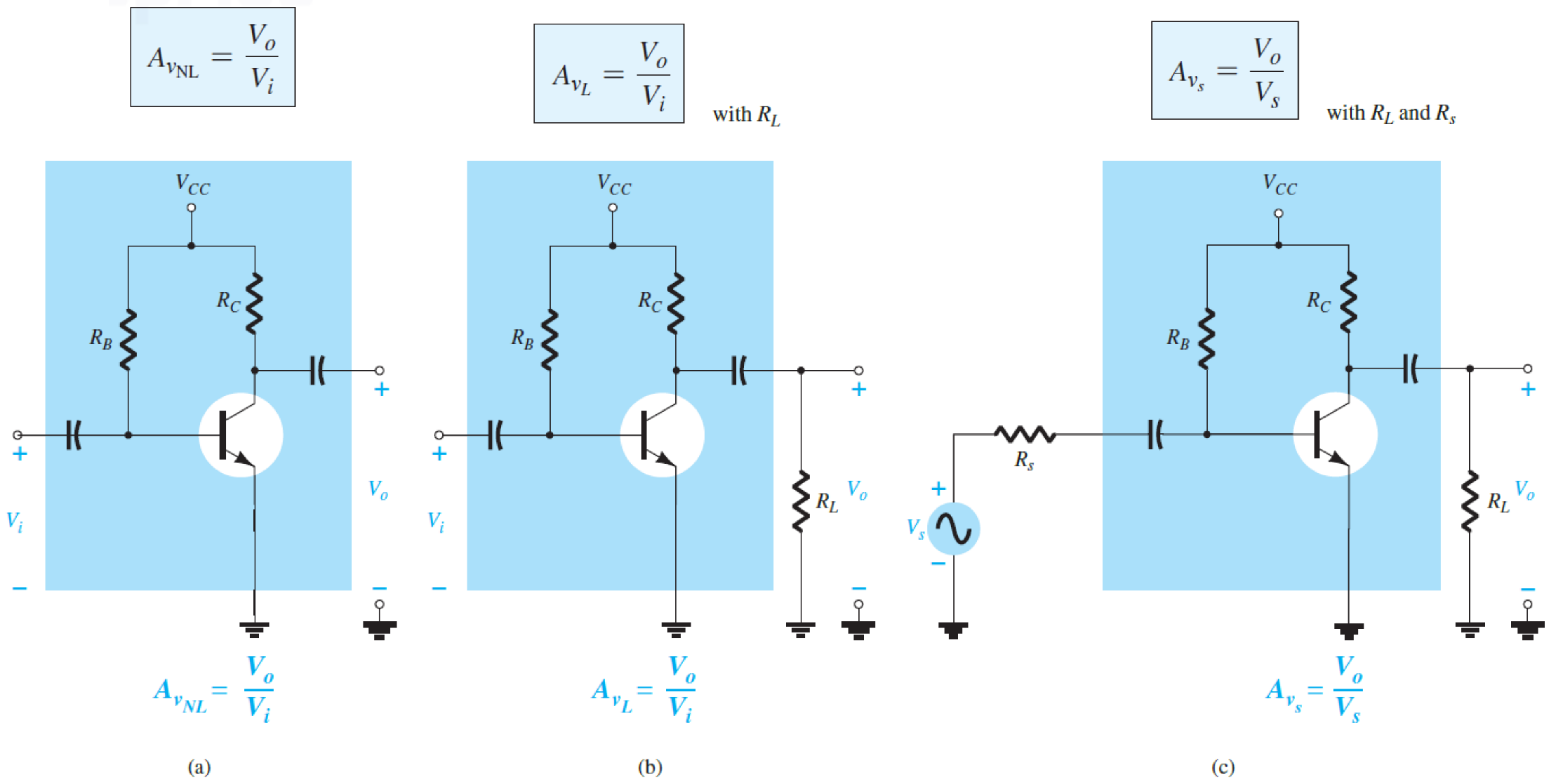
2nd Class

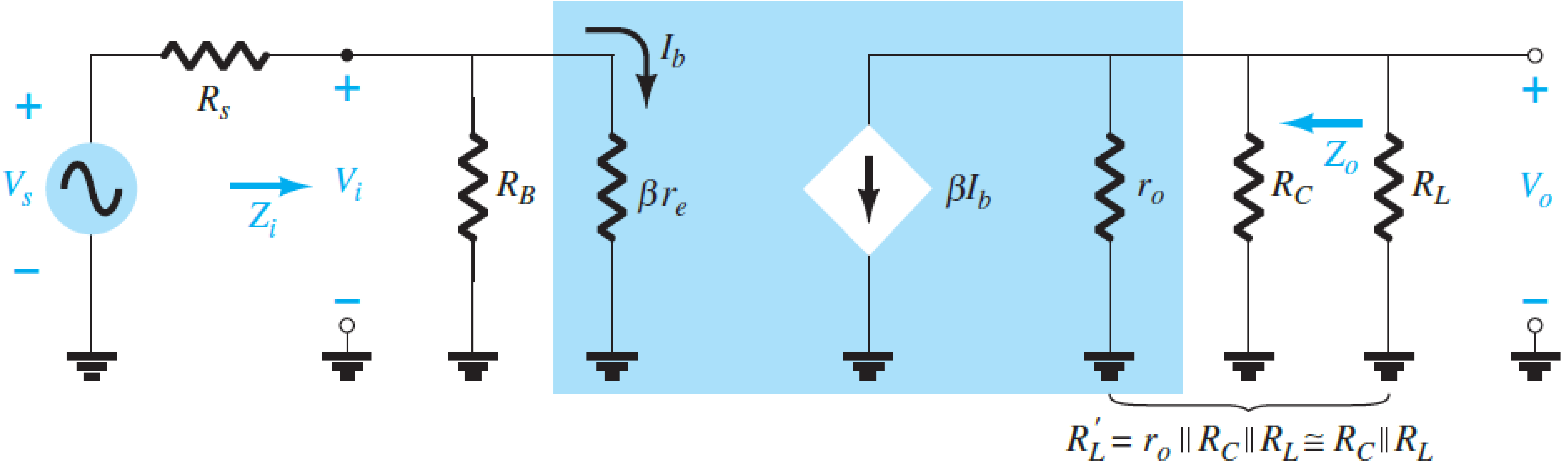
by
Rafal Raed Mahmood Alshaker

Outline of Presentation

- Effect of R_L and the R_S
- The Effect of R_L and R_s in Emitter-Follower Configuration (CC)

Effect of R_L and the R_S





$$Z_i = R_B \| \beta r_e$$

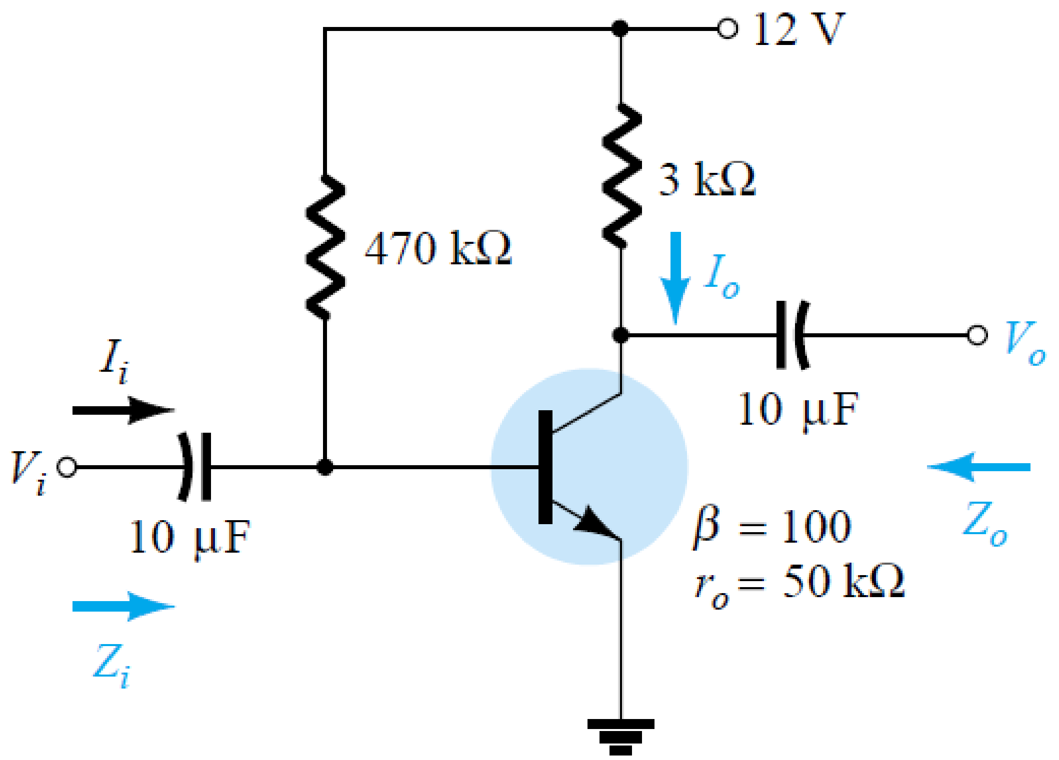
$$Z_o = R_C \| r_o$$

$$A_{v_L} = \frac{V_o}{V_i} = -\frac{R_C \| R_L}{r_e}$$

$$A_{v_S} = \frac{Z_i}{Z_i + R_s} A_{v_L}$$

EXAMPLE:

For the network of Fig



(a) DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{470\text{ k}\Omega} = 24.04\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(24.04\ \mu\text{A}) = 2.428\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.428\text{ mA}} = \mathbf{10.71\ \Omega}$$

(b) $\beta r_e = (100)(10.71\ \Omega) = 1.071\text{ k}\Omega$

$Z_i = R_B \| \beta r_e = 470\text{ k}\Omega \| 1.071\text{ k}\Omega = \mathbf{1.069\ k\Omega}$

(c) $Z_o = R_C = \mathbf{3\ k\Omega}$

(d) $A_v = -\frac{R_C}{r_e} = -\frac{3\text{ k}\Omega}{10.71\ \Omega} = \mathbf{-280.11}$

(e) Since $R_B \geq 10\beta r_e (470\text{ k}\Omega > 10.71\text{ k}\Omega)$

$A_i \cong \beta = \mathbf{100}$

EXAMPLE:

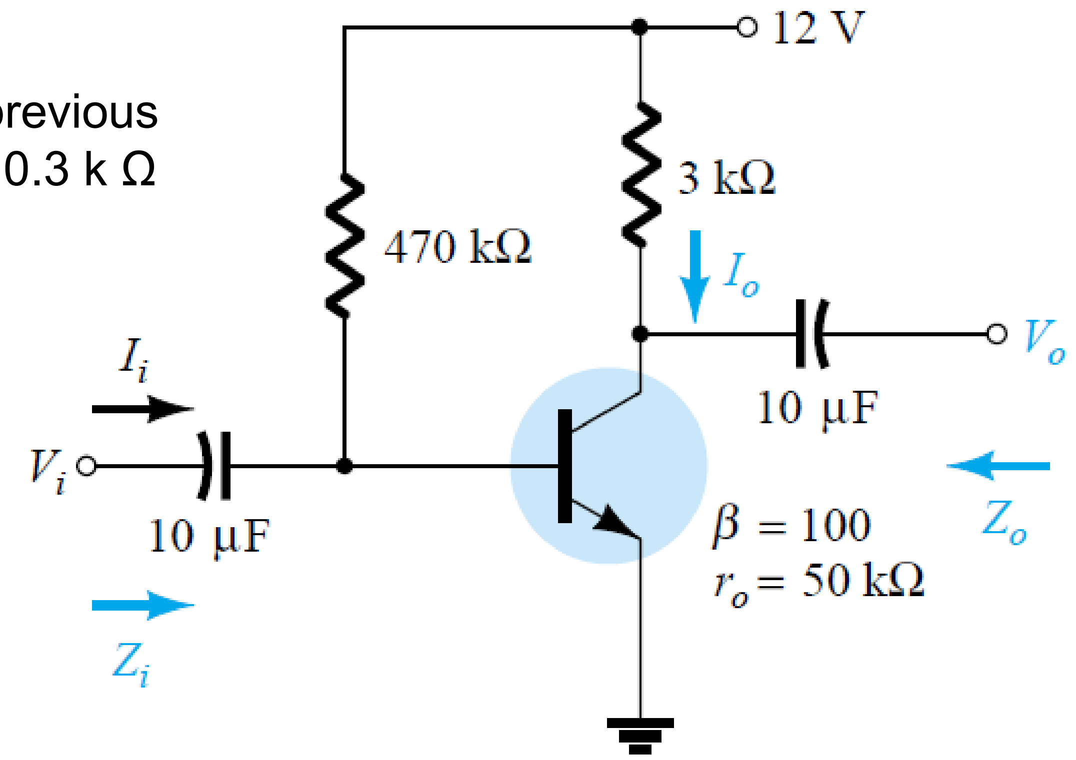
Using the parameter values for the fixed-bias configuration of the previous example with an applied load of 4.7 kΩ and a source resistance of 0.3 k Ω determine the following and compare to the no-load values:

a. A_{vL}.

b. A_{vs}.

c. . Z_i ..

d. Z_o .



EXAMPLE:

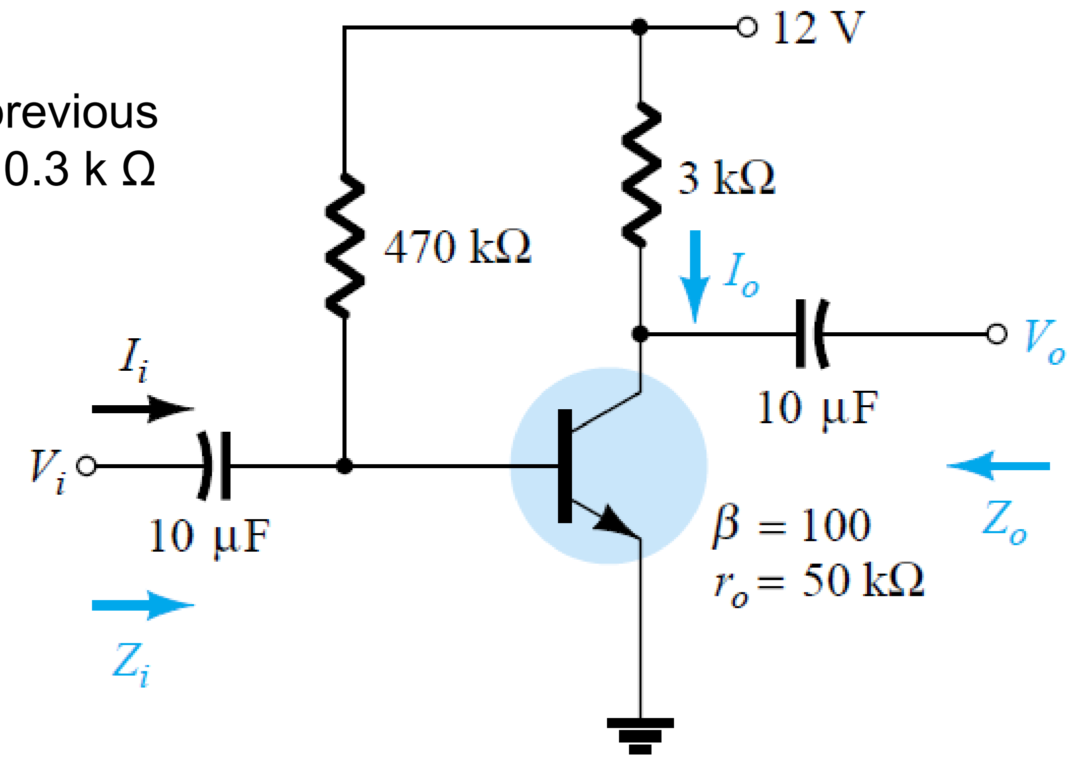
Using the parameter values for the fixed-bias configuration of the previous example with an applied load of 4.7 kΩ and a source resistance of 0.3 k Ω determine the following and compare to the no-load values:

a. A_{vL}.

b. A_{vs}.

c. . Z_i ..

d. Z_o .



Solution:

a. Eq. (5.73): $A_{v_L} = -\frac{R_C \| R_L}{r_e} = -\frac{3\text{ k}\Omega \| 4.7\text{ k}\Omega}{10.71\ \Omega} = -\frac{1.831\text{ k}\Omega}{10.71\ \Omega} = \mathbf{-170.98}$

which is significantly less than the no-load gain of −280.11.

b. Eq. (5.76): $A_{v_s} = \frac{Z_i}{Z_i + R_s} A_{v_L}$

With $Z_i = 1.07$ kΩ from Example 5.1, we have

$$A_{v_s} = \frac{1.07\text{ k}\Omega}{1.07\text{ k}\Omega + 0.3\text{ k}\Omega}(-170.98) = \mathbf{-133.54}$$

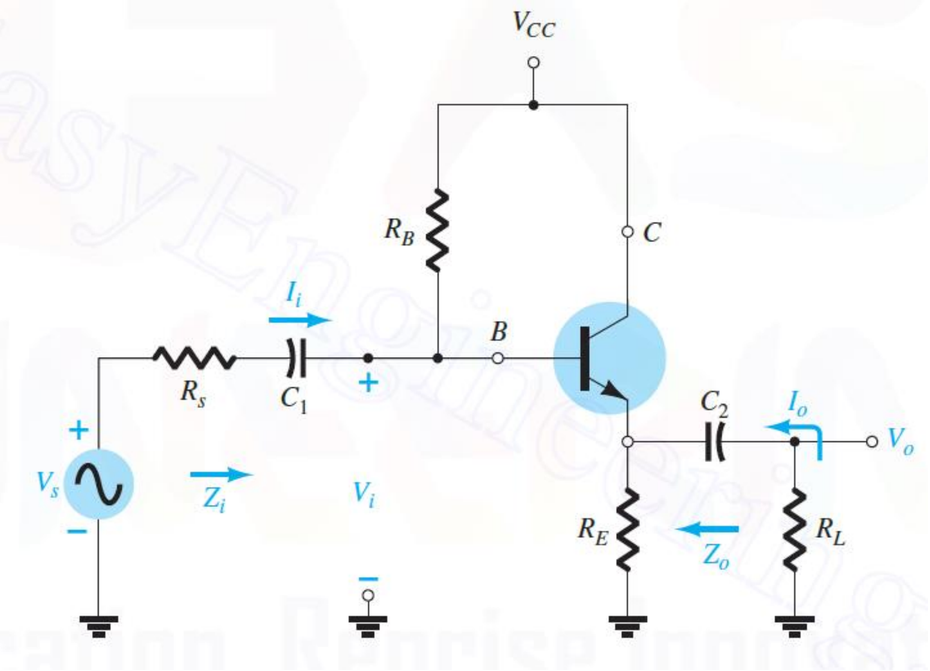
which again is significantly less than $A_{v_{NL}}$ or A_{v_L}.

c. $Z_i = \mathbf{1.07\ k\Omega}$ as obtained for the no-load situation.

d. $Z_o = R_C = \mathbf{3\ k\Omega}$ as obtained for the no-load situation.

The example clearly demonstrates that $A_{v_{NL}} > A_{v_L} > A_{v_s}$.

The Effect of R_L and R_s in Emitter-Follower Configuration (CC)



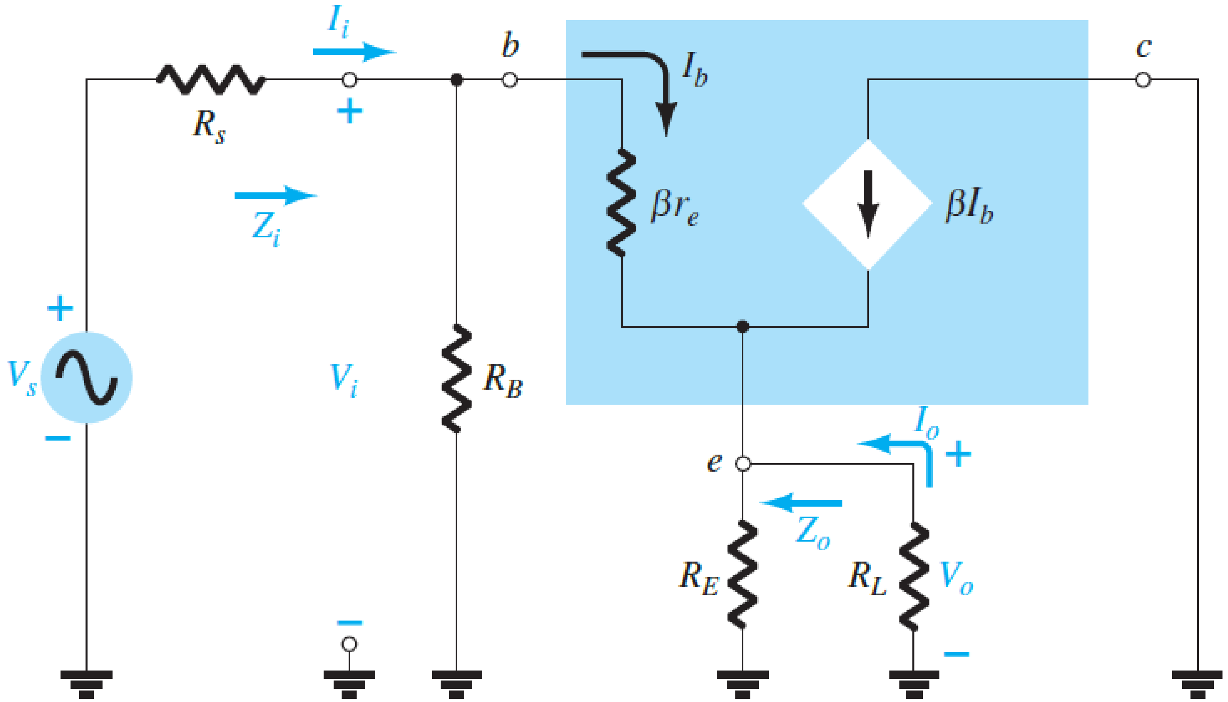
$$Z_i = R_B \| Z_b$$

$$Z_b \cong \beta(R_E \| R_L)$$

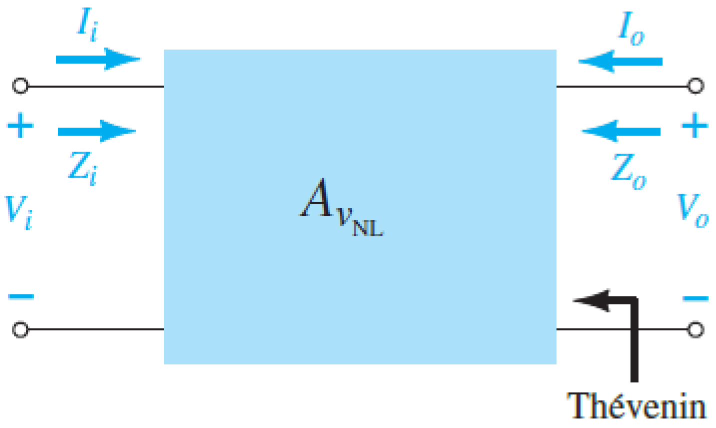
$$Z_o \cong r_e$$

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_E \| R_L}{R_E \| R_L + r_e}$$

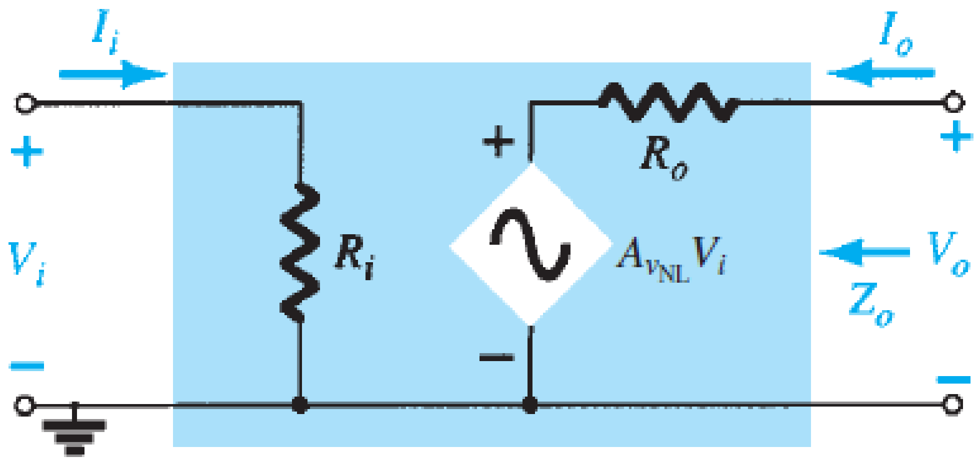
$$A_{i_L} = -A_{v_L}\frac{Z_i}{R_L}$$



The Effect of R_L and R_s in Two Port Network



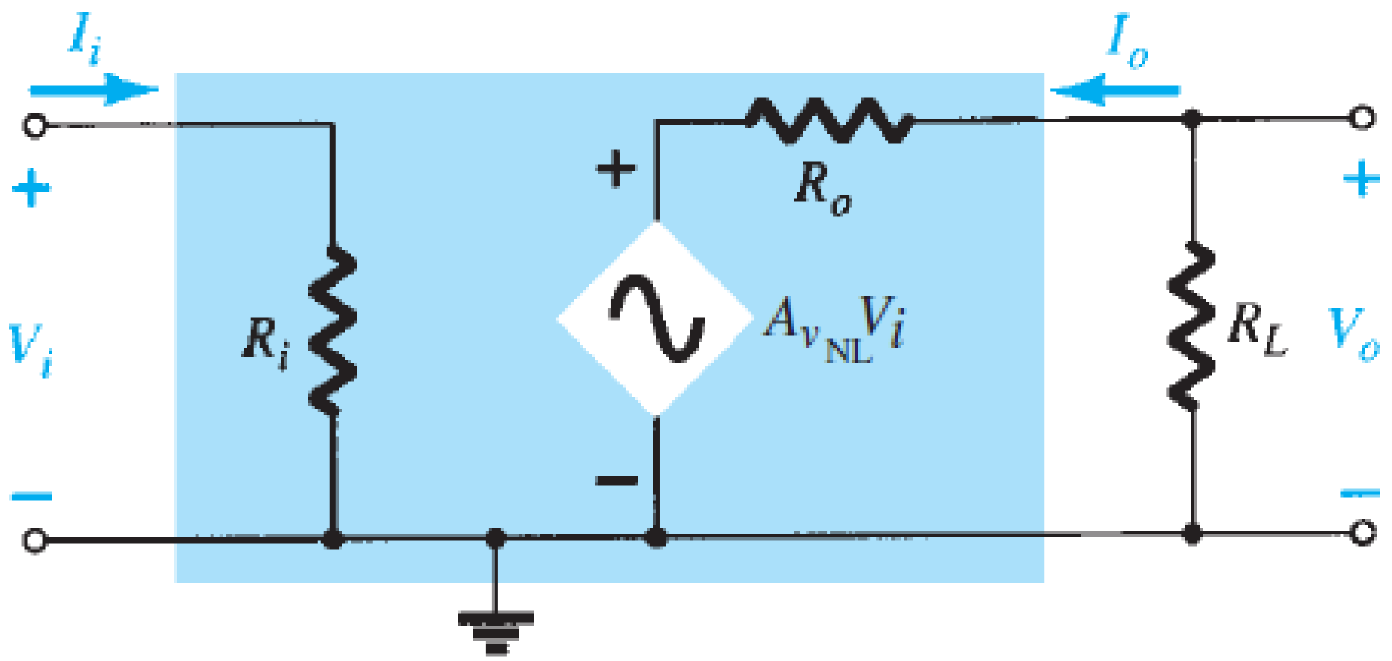
Two-port system.



$$V_o = A_{v_{NL}} V_i$$

$$Z_o = R_o$$

$$Z_i = R_i$$



$$A_{i_L} = \frac{I_o}{I_i} = \frac{-V_o/R_L}{V_i/Z_i} = -\frac{V_o}{V_i}\frac{Z_i}{R_L}$$

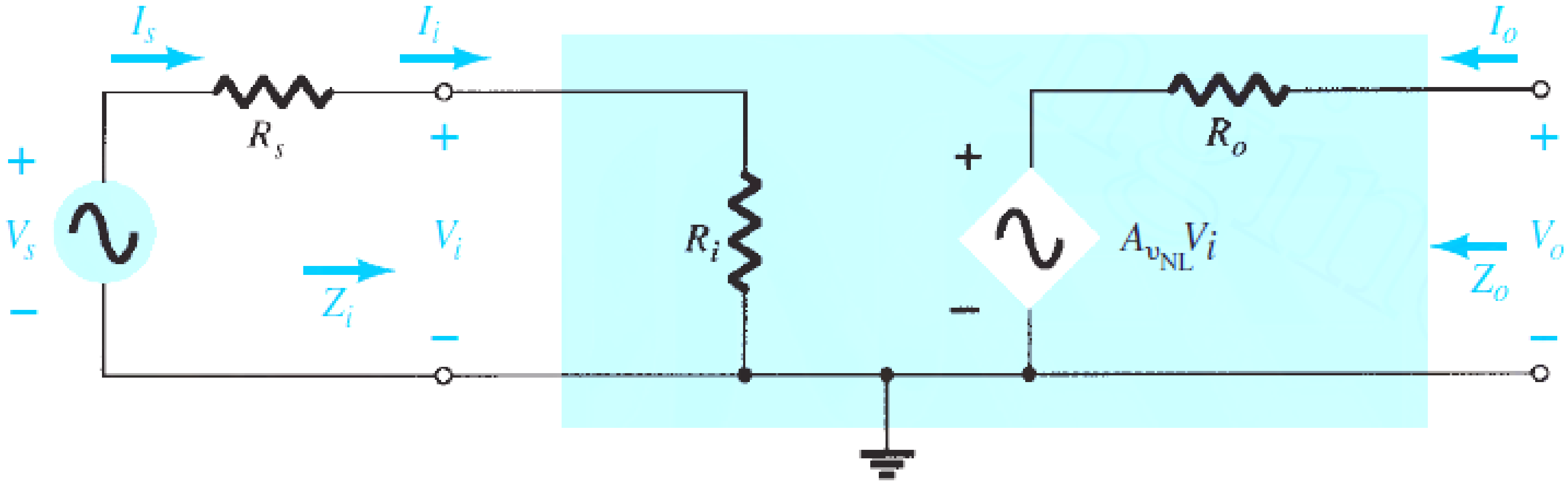
$$A_{i_L} = -A_{v_L}\frac{Z_i}{R_L}$$

$$V_o = \frac{R_L A_{v_{NL}} V_i}{R_L + R_o}$$

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o} A_{v_{NL}}$$

Because the ratio $R_L/(R_L + R_o)$ is always less than 1, the loaded voltage gain of an amplifier is always less than the no-load level.

The parameters Z_i and $A_{v_{NL}}$ of a two-port system are unaffected by the internal resistance of the applied source.



The output impedance may be affected by the magnitude of R s .

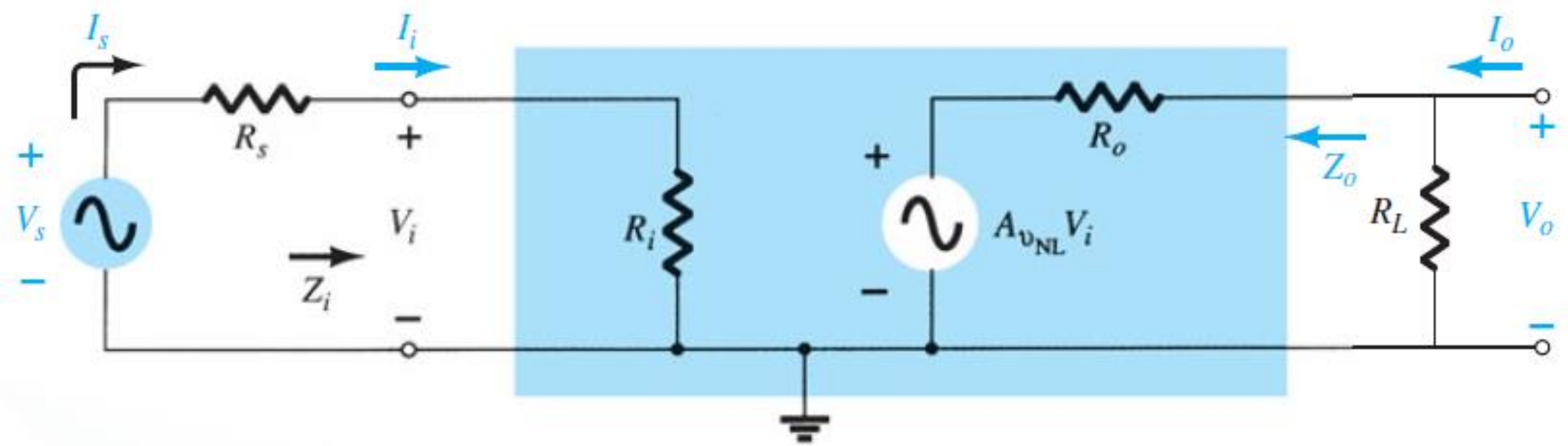
$$V_o = A_{v_{NL}} \frac{R_i}{R_i + R_s} V_s$$

$$V_i = \frac{R_i V_s}{R_i + R_s}$$

$$V_o = A_{v_{NL}} V_i$$

$$V_i = \frac{R_i V_s}{R_i + R_s}$$

$$A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} A_{v_{NL}}$$

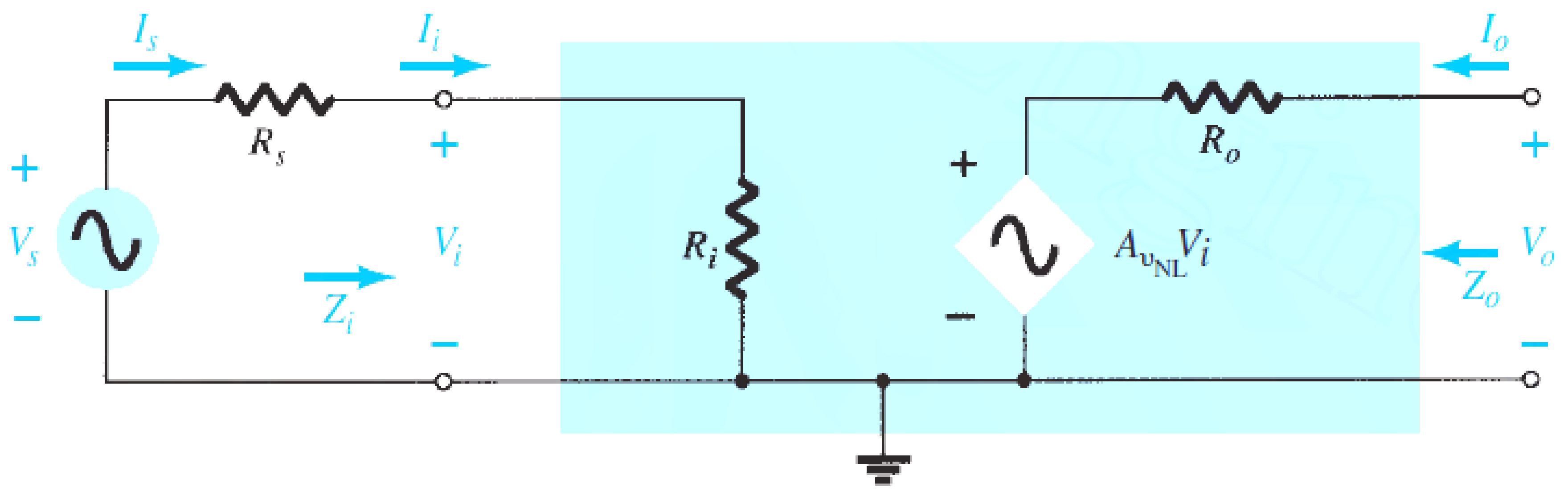


$$V_i = \frac{R_i V_s}{R_i + R_s}$$

$$V_o = \frac{R_L}{R_L + R_o} A_{v_{NL}} V_i$$

$$\boxed{\frac{V_i}{V_s} = \frac{R_i}{R_i + R_s}}$$

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_L A_{v_{NL}}}{R_L + R_o} = \frac{R_L}{R_L + R_o} A_{v_{NL}}$$



$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s}$$

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_L A_{v_{NL}}}{R_L + R_o} = \frac{R_L}{R_L + R_o} A_{v_{NL}}$$

$$V_i = \frac{R_i V_s}{R_i + R_s}$$

$$\frac{V_i}{V_s} = \frac{R_i}{R_i + R_s}$$

$$A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{v_{NL}}$$

$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s}$$

$$A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{v_{\mathrm{NL}}}$$

$$A_{i_L} = -A_{v_L} \frac{R_i}{R_L}$$

$$A_{i_s} = -A_{v_s} \frac{R_s + R_i}{R_L}$$

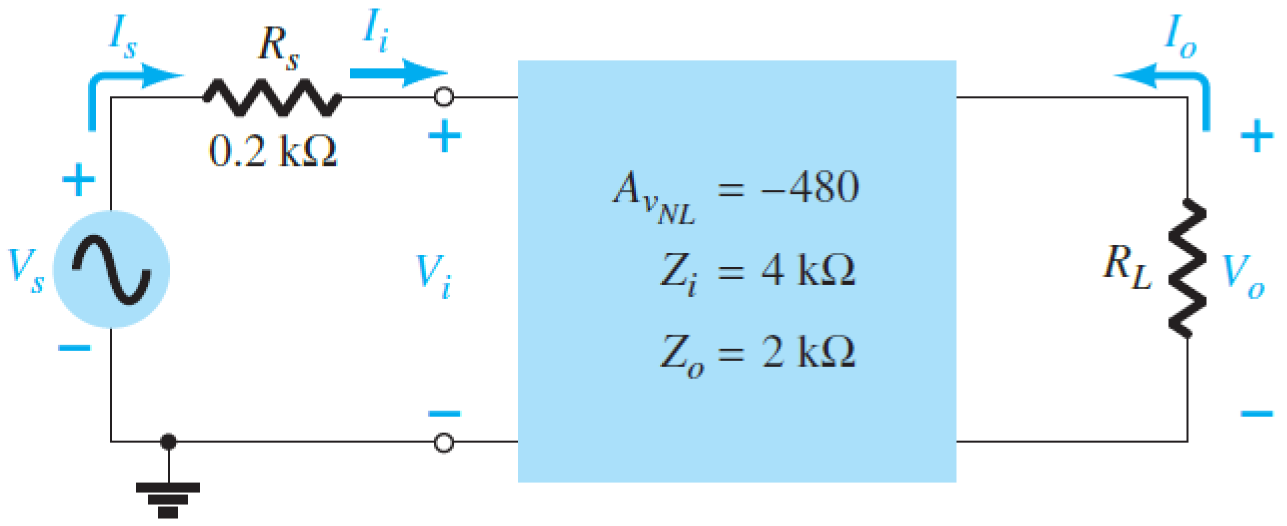
EXAMPLE 5.13 Given the packaged (no-entry-possible) amplifier of figure below

a. Determine the gain A_{vL} and compare it to the no-load value with R_L = 1.2 k.

b. Repeat part (a) with R_L = 5.6 k and compare solutions.

c. Determine A_{vs} with R_L = 1.2 k.

d. Find the current gain $A_i = \frac{I_o}{I_i} = \frac{I_o}{I_s}$ with $R_L = 5.6\ \text{k}\Omega$.



$$A_{v_L} = \frac{R_L}{R_L + R_o} A_{v\text{NL}}$$

$$= \frac{1.2\ \text{k}\Omega}{1.2\ \text{k}\Omega + 2\ \text{k}\Omega}(-480) = (0.375)(-480)$$

$$= \mathbf{-180}$$

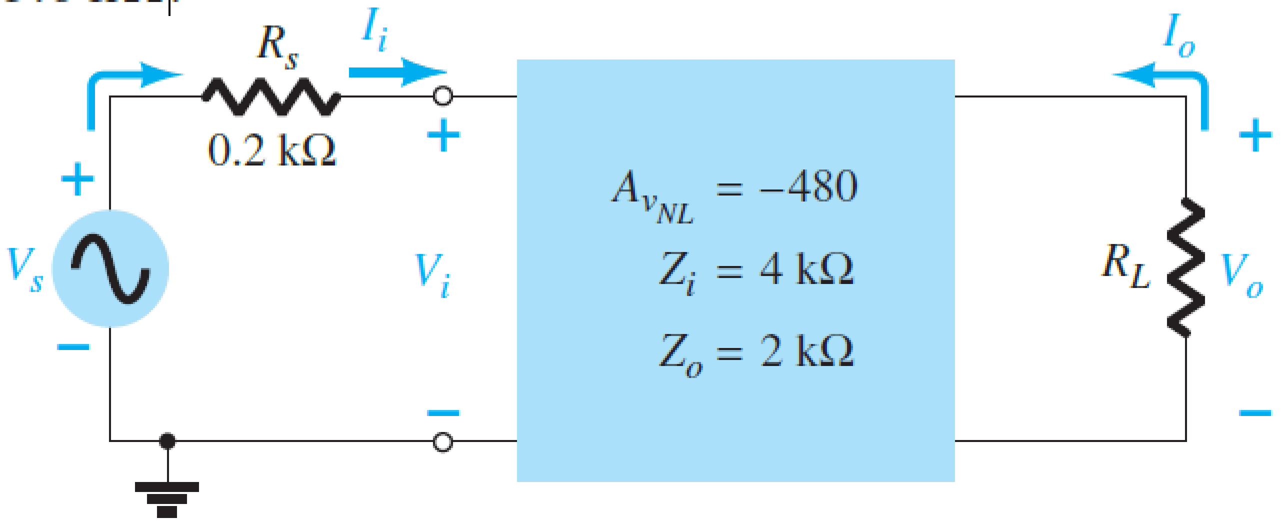
EXAMPLE Given the packaged (no-entry-possible) amplifier of figure below

a. Determine the gain A_{v_L} and compare it to the no-load value with $R_L = 1.2$ k.

b. Repeat part (a) with $R_L = 5.6$ k and compare solutions.

c. Determine A_{v_s} with $R_L = 1.2$ k.

d. Find the current gain $A_i = \frac{I_o}{I_i} = \frac{I_o}{I_s}$ with $R_L = 5.6\ \text{k}\Omega$.



$$A_{v_L} = \frac{R_L}{R_L + R_o} A_{v_{\text{NL}}}$$

$$= \frac{5.6\ \text{k}\Omega}{5.6\ \text{k}\Omega + 2\ \text{k}\Omega}(-480) = (0.737)(-480)$$

$$= \mathbf{-353.76}$$

$$A_{v_s} = \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{v_{\text{NL}}}$$

$$= \frac{4\ \text{k}\Omega}{4\ \text{k}\Omega + 0.2\ \text{k}\Omega} \cdot \frac{1.2\ \text{k}\Omega}{1.2\ \text{k}\Omega + 2\ \text{k}\Omega}(-480)$$

$$= (0.952)(0.375)(-480)$$

$$= \mathbf{-171.36}$$

d. $$A_{i_L} = \frac{I_o}{I_i} = \frac{I_o}{I_s} = -A_{v_L}\frac{Z_i}{R_L}$$

$$= -(-353.76)\left(\frac{4\ \text{k}\Omega}{5.6\ \text{k}\Omega}\right) = -(-353.76)(0.714)$$

$$= \mathbf{252.6}$$

$$A_{v_L} = \frac{R_L}{R_L + Z_o} A_{v_{NL}}$$

R_L

$R \downarrow \rightarrow A_{v_L} \downarrow$

$$A_{i_L} = -A_{v_L} \frac{Z_i}{R_L}$$

$$A_{v_s} = \frac{Z_i}{Z_i + R_s} A_{v_L}$$

R_s, R_L

$A_{v_s} \uparrow \rightarrow A_{v_L} \uparrow$

$$A_{i_s} = -A_{v_s} \frac{Z_i + R_s}{R_L}$$

$R_s \downarrow - A_{v_s} \uparrow$

$R_L \uparrow - A_{v_s} \uparrow$

$$A_{v_s} = \frac{Z_i}{Z_i + R_s} A_{v_{NL}}$$

R_s

$A_{v_{NL}} > A_{v_L} > A_{v_s}$

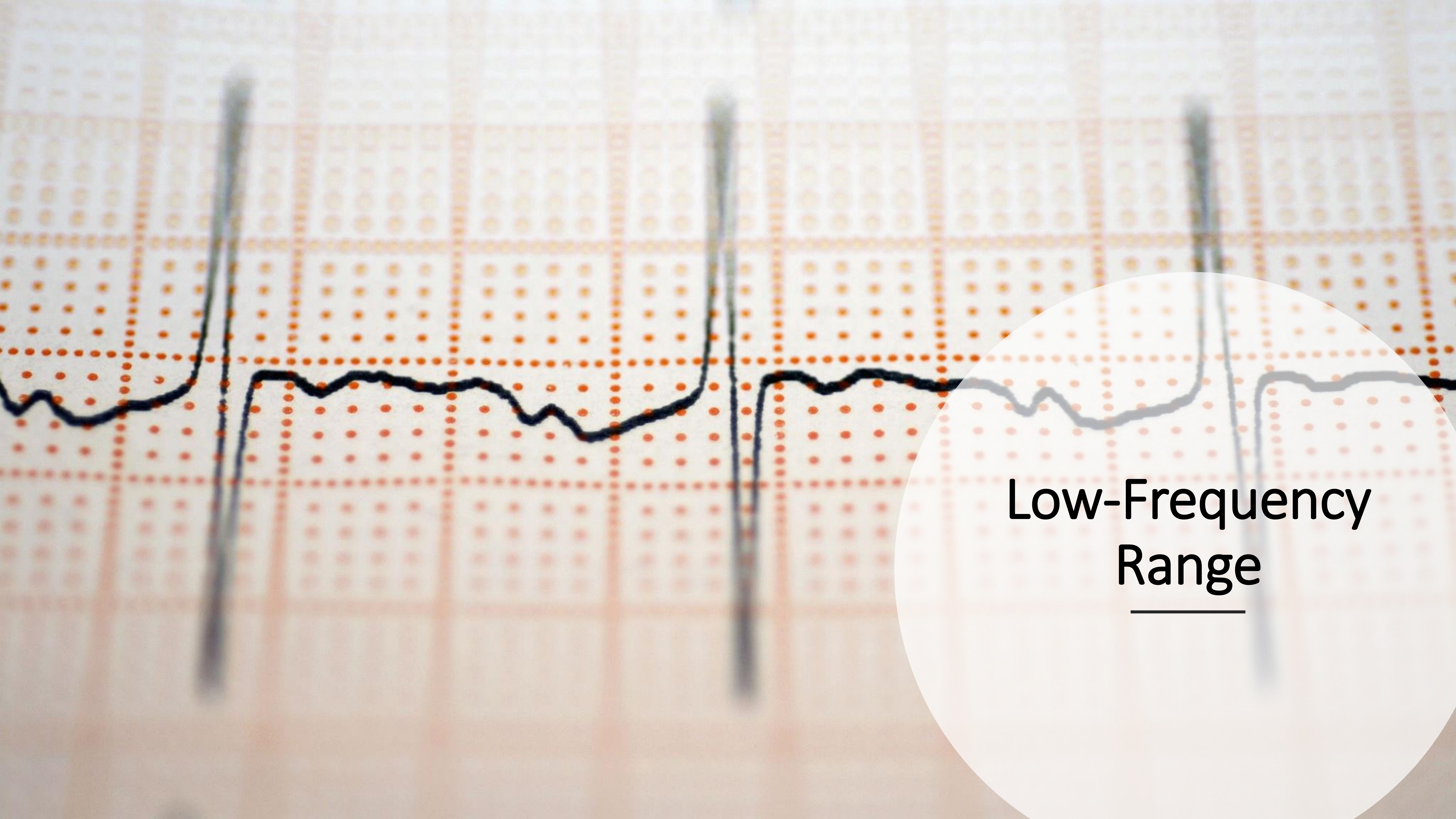
Ninevah University
College of Electronics Engineering
Department of Systems and Control

Electronic I
Lecture 9

Frequency Response

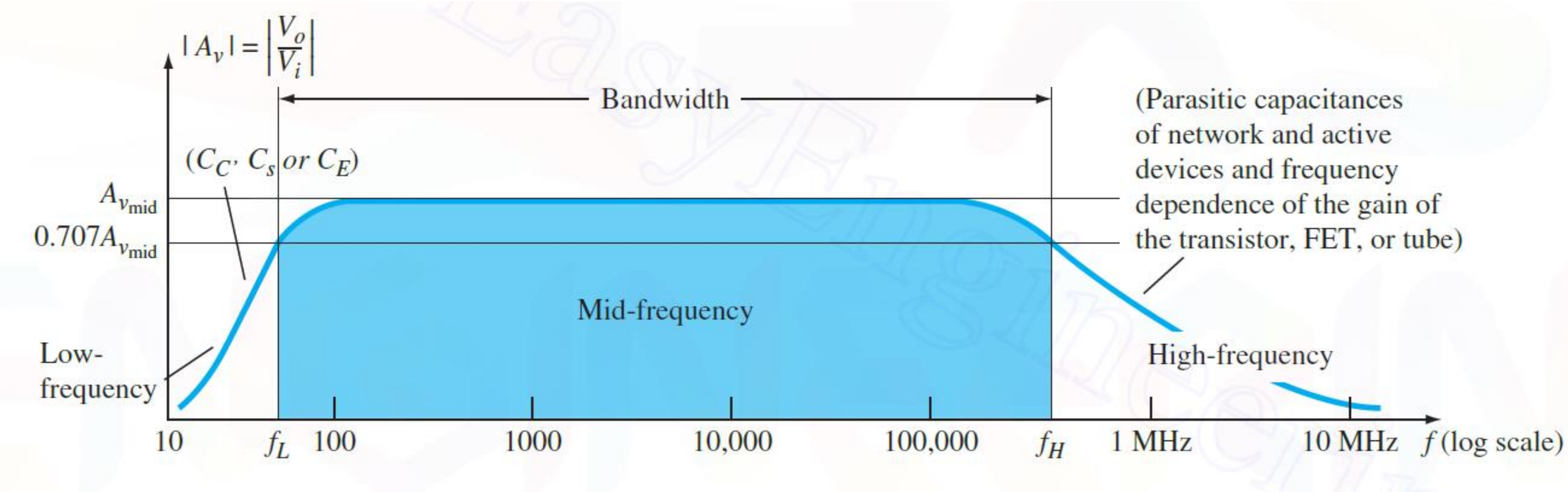
2nd Class

by
Rafal Raed Mahmood Alshaker



Low-Frequency Range

Typical Frequency Response



Low-Frequency Range

Variation in $X_C = \dfrac{1}{2\pi f C}$ *with frequency for a 1-μF capacitor*

f	X_C	
10 Hz	15.91 kΩ	Range of possible effect
100 Hz	1.59 kΩ	
1 kHz	159 Ω	
10 kHz	15.9 Ω	
100 kHz	1.59 Ω	Range of lesser concern (≅ short-circuit equivalence)
1 MHz	0.159 Ω	
10 MHz	15.9 mΩ	
100 MHz	1.59 mΩ	

the larger capacitors of a system will have an important impact on the response of a system in the low-frequency range and can be ignored for the high-frequency region.

High-Frequency Range

Variation in $X_C = \dfrac{1}{2\pi f C}$ *with frequency for a 5 pF capacitor*

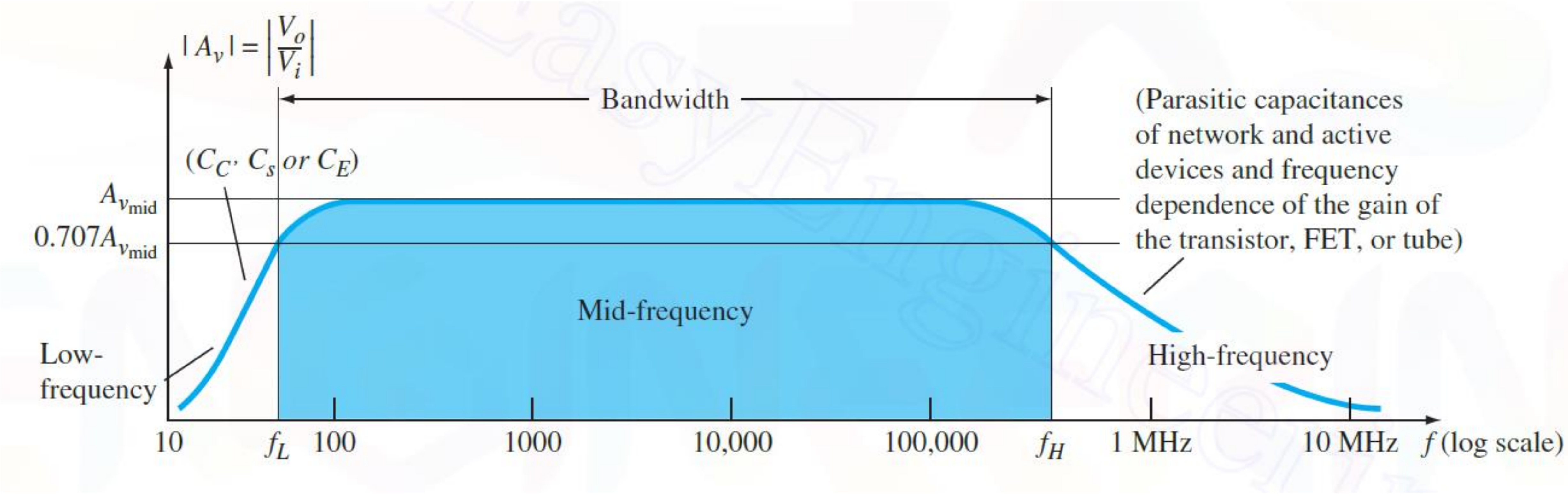
f	X_C	
10 Hz	3,183 MΩ	Range of lesser concern (≅ open-circuit equivalent)
100 Hz	318.3 MΩ	
1 kHz	31.83 MΩ	
10 kHz	3.183 MΩ	
100 kHz	318.3 kΩ	Range of possible effect
1 MHz	31.83 kΩ	
10 MHz	3.183 kΩ	
100 MHz	318.3 Ω	

the smaller capacitors of a system will have an important impact on the response of a system in the high-frequency range and can be ignored for the low-frequency region.

Mid-Frequency Range

the effect of the capacitive elements in an amplifier are ignored for the mid-frequency range when important quantities such as the gain and impedance levels are determined.

Typical Frequency Response



Typical Frequency Response

$$P_{o_{\text{mid}}} = \frac{|V_o^2|}{R_o} = \frac{|A_{v_{\text{mid}}} V_i|^2}{R_o}$$

and at the half-power frequencies,

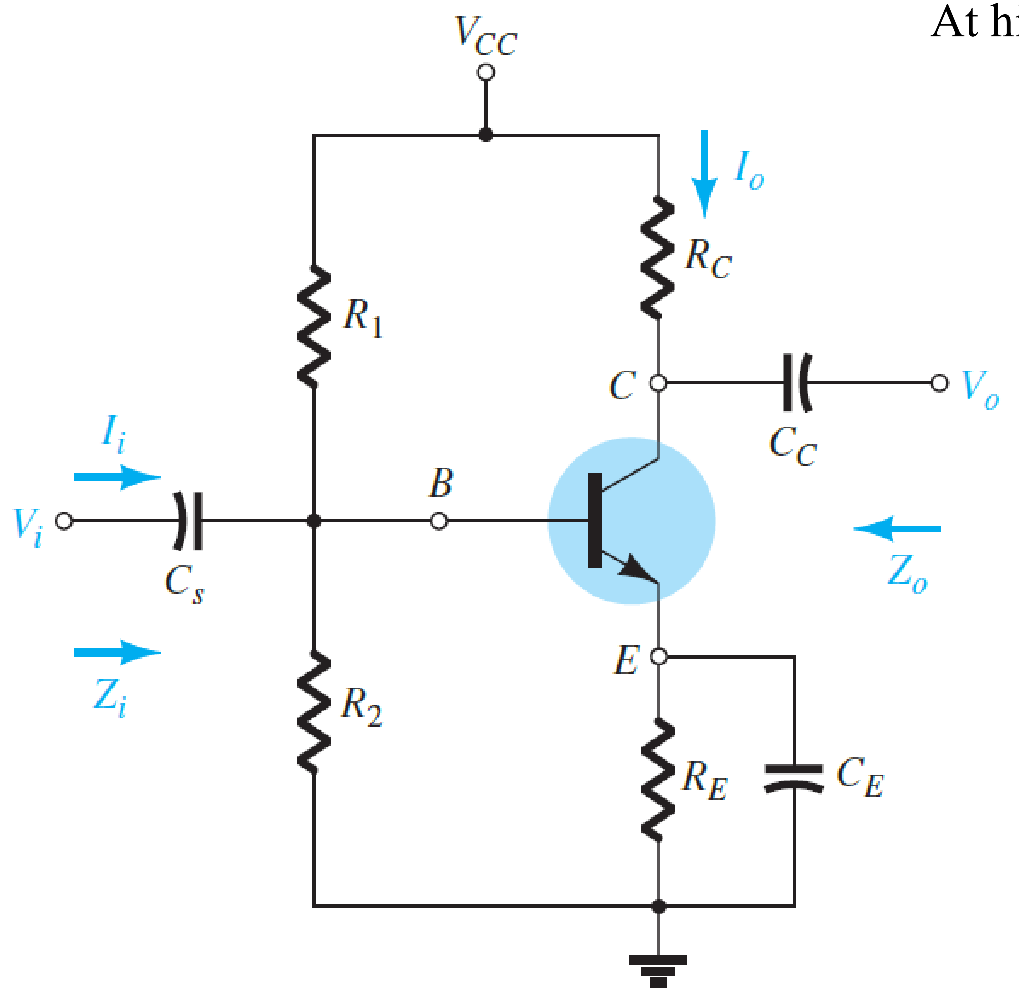
$$P_{o_{HPF}} = \frac{|0.707\, A_{v_{\text{mid}}} V_i|^2}{R_o} = 0.5\, \frac{|A_{v_{\text{mid}}} V_i|^2}{R_o}$$

$$\boxed{P_{o_{HPF}} = 0.5\, P_{o_{\text{mid}}}}$$

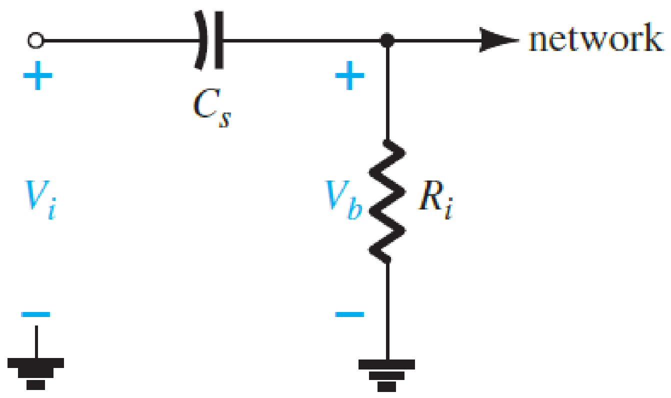
The multiplier 0.707 was chosen because at this level the output power is half the midband power output, that is, at midfrequencies

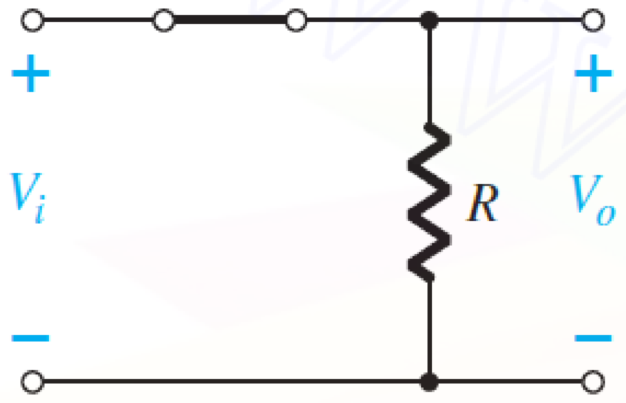
$$\boxed{\text{bandwidth (BW)} = f_H - f_L}$$

LOW-FREQUENCY ANALYSIS—BODE PLOT



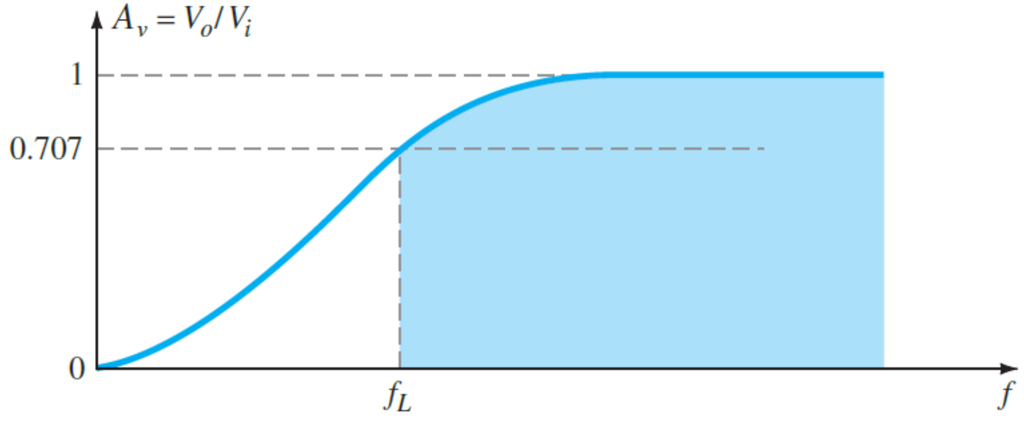
At high frequencies, the reactance of the capacitor of



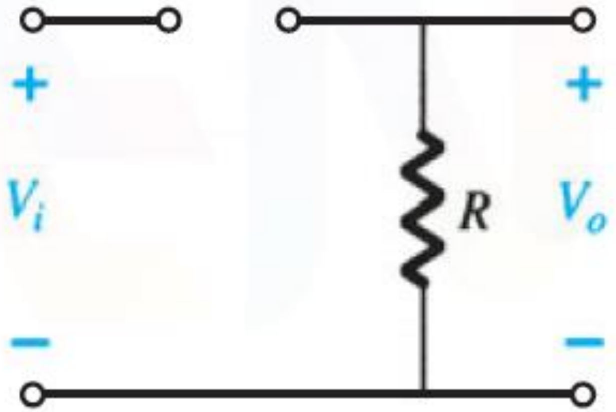


$$X_C = \frac{1}{2\pi f C} \cong 0\ \Omega$$

RC circuit at very high frequencies



Low-frequency response for the RC circuit .



$$X_C = \frac{1}{2\pi f C} = \frac{1}{2\pi(0)C} = \infty\ \Omega$$

RC circuit at Zero frequency

5. LOW-FREQUENCY ANALYSIS—BODE PLOT

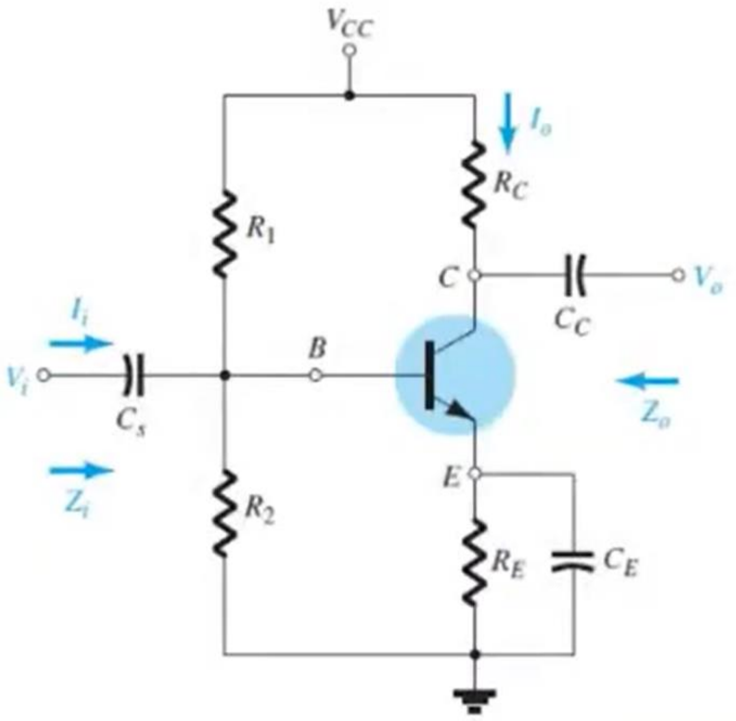


FIG. 9.15
Voltage-divider bias configuration.

$$Z_i = R_i = R_1 \| R_2 \| \beta r_e$$

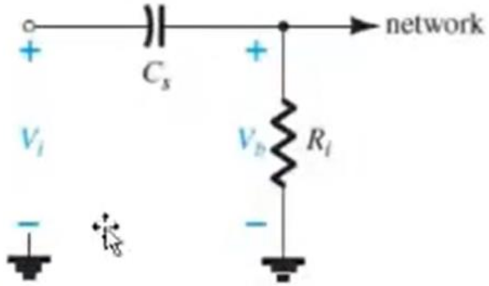
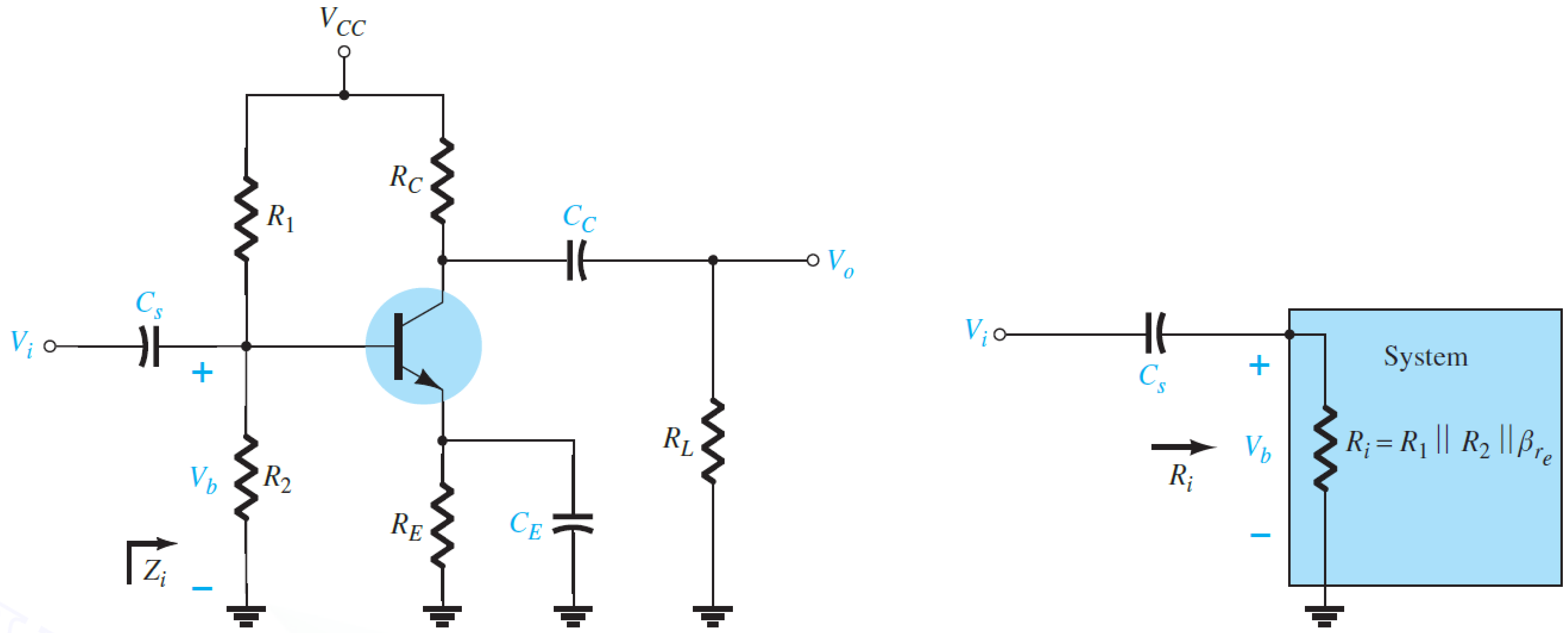


FIG. 9.16
Equivalent input circuit for the network of Fig. 9.15.

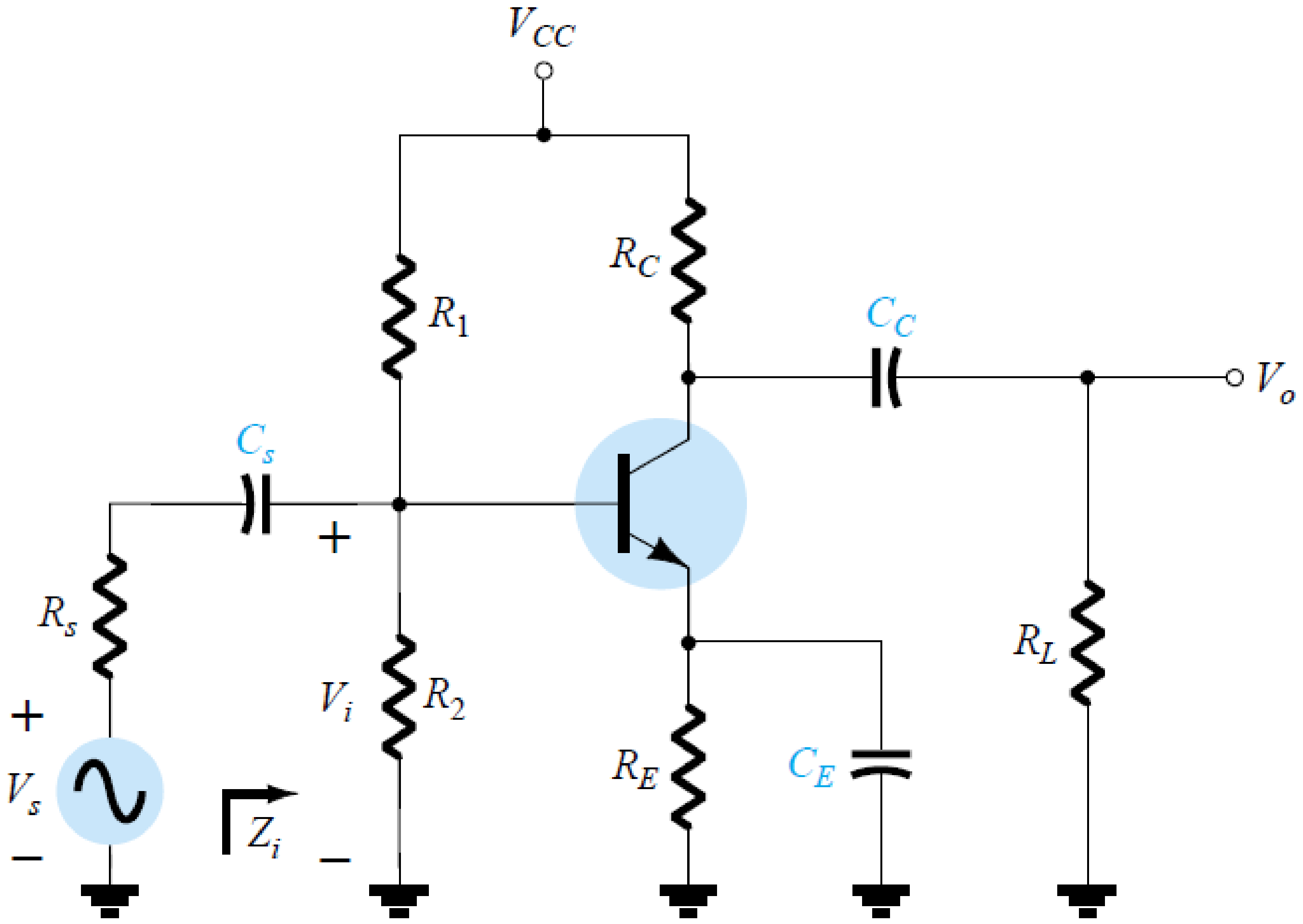
LOW-FREQUENCY RESPONSE—BJT AMPLIFIER WITH R_L

The capacitors C_s, C_C, and C_E will determine the low-frequency response



LOW-FREQUENCY RESPONSE—BJT AMPLIFIER WITH R_L

The capacitors C_s, C_C, and C_E will determine the low-frequency response



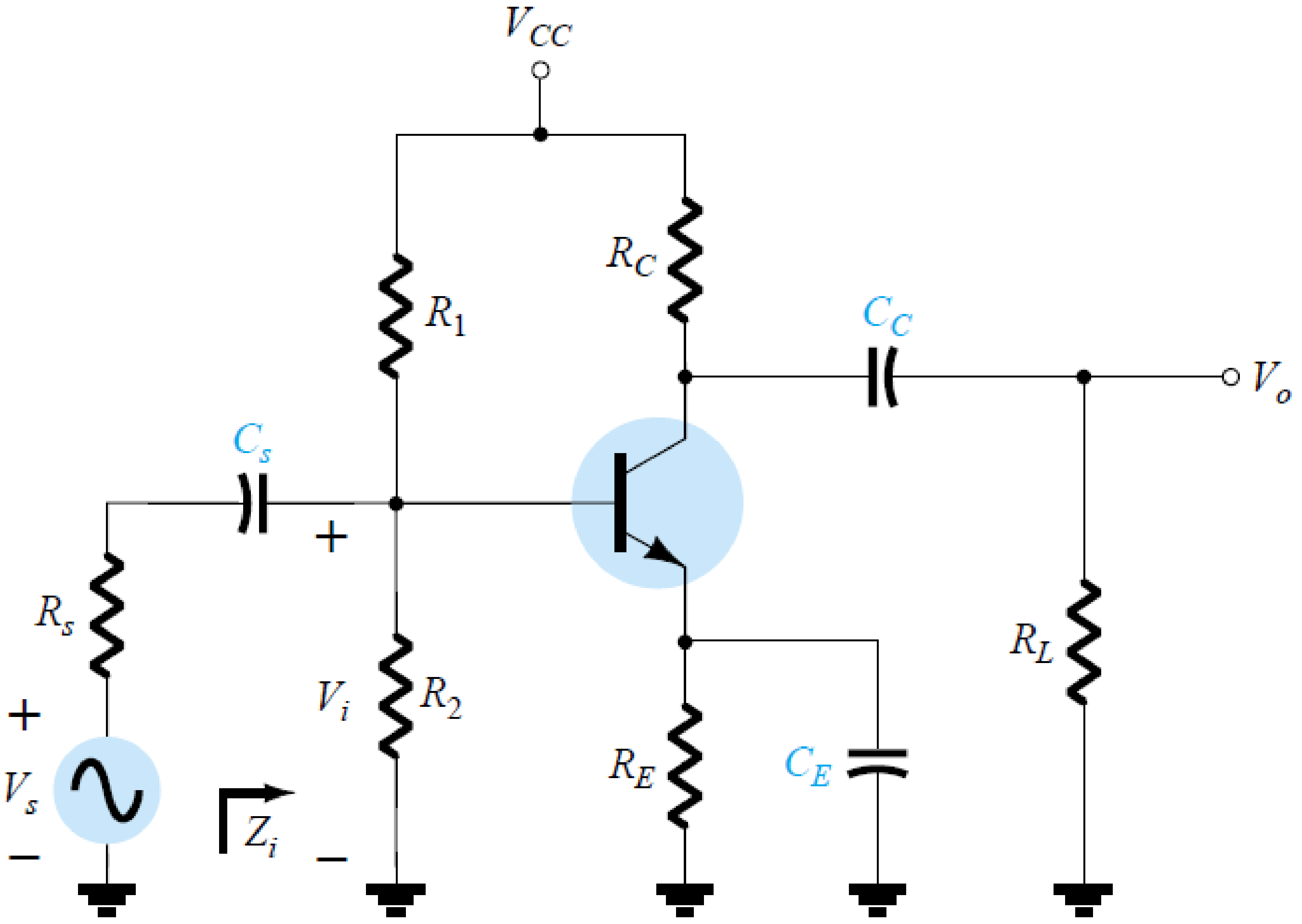
LOW-FREQUENCY RESPONSE—BJT AMPLIFIER WITH R_L

C_s

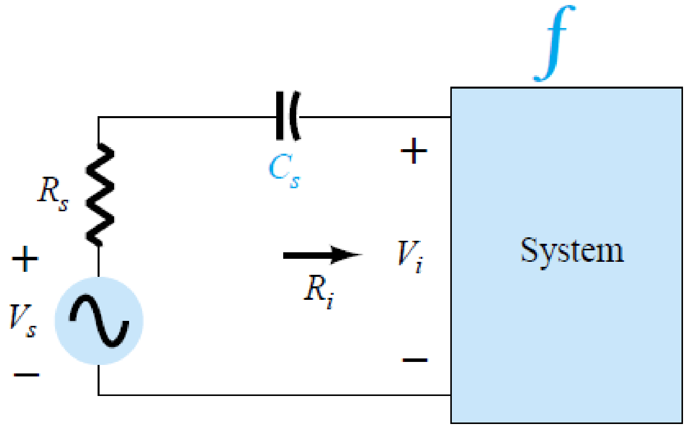
Since C_s is normally connected between the applied source and the active device, the general form of the *R-C* configuration is established by the network of Figure below

The total resistance is now R_s R_i, and the cutoff frequency is

$$f_{L_s} = \frac{1}{2\pi (R_s + R_i)C_s}$$

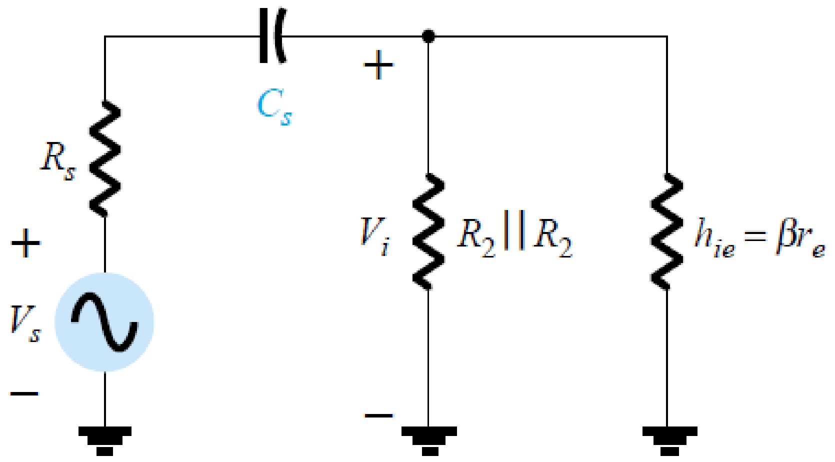


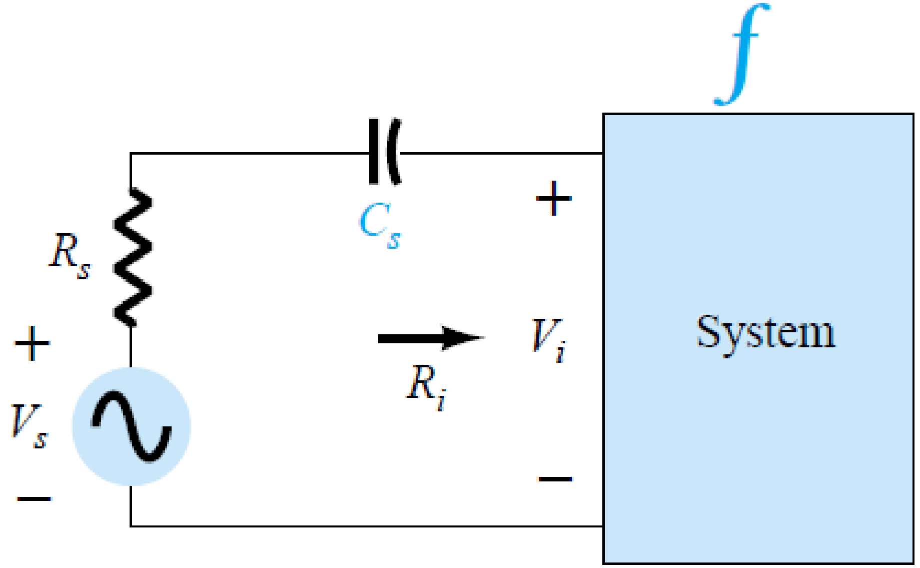
$$V_i\big|_{\text{mid}} = \frac{R_i V_s}{R_i + R_s}$$



LOW-FREQUENCY RESPONSE—BJT AMPLIFIER WITH R_L

C_s





$$R_i = R_1 || R_2 || \beta r_e$$

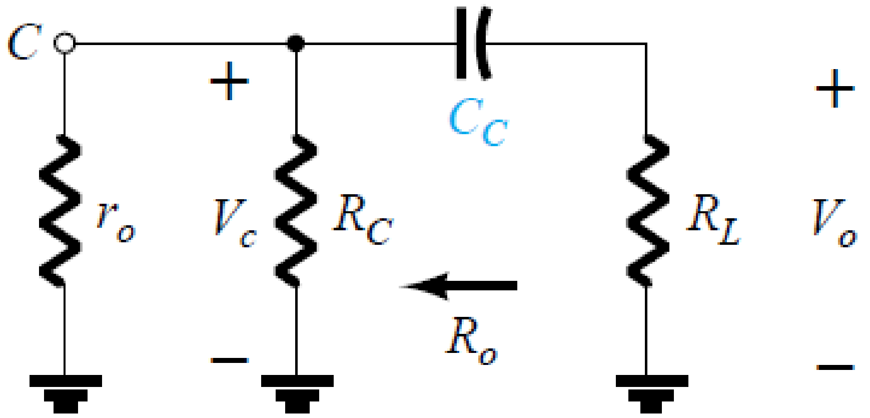
$$\mathbf{V}_i = \frac{R_i \mathbf{V}_s}{R_s + R_i - jX_{C_S}}$$

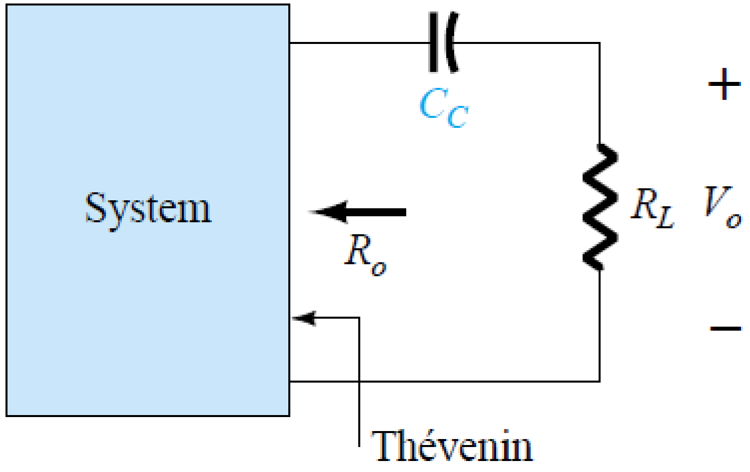
C_C

LOW-FREQUENCY RESPONSE—BJT AMPLIFIER WITH R_L

Since the coupling capacitor is normally connected between the output of the active device and the applied load, the *R*-*C* configuration that determines the low cutoff frequency due to C_C appears in figure below, the total series resistance is now $R_o + R_L$ and the cutoff frequency due to C_C is determined by

$$f_{L_C} = \frac{1}{2\pi (R_o + R_L) C_C}$$





Ignoring the effects of C_s and C_E, the output voltage V_o will be 70.7% of its midband value at f_{LC}. , the ac equivalent network for the output section with V_i = 0 V . The resulting value for R_o is

$$R_o = R_C \| r_o$$

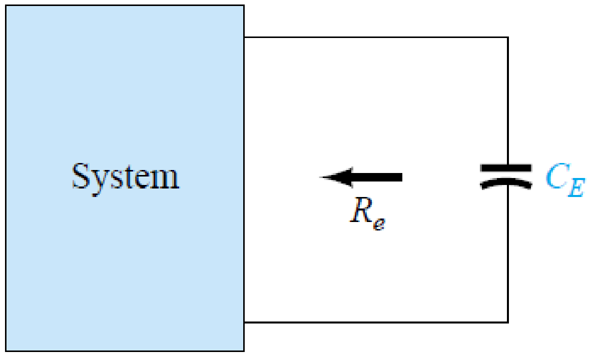
LOW-FREQUENCY RESPONSE—BJT AMPLIFIER WITH R_L

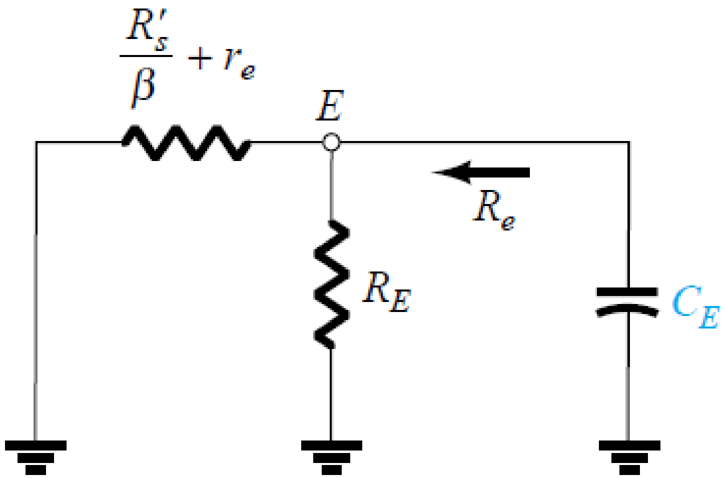
C_E

To determine f_{L_E}, the network "seen" by C_E must be determined as shown in Figure below
Once the level of R_e is established, the cutoff frequency due to C_E can be determined using the following equation:

$$f_{L_E} = \frac{1}{2\pi R_e C_E}$$

f





$$R_e = R_E \| \left(\frac{R_s'}{\beta} + r_e\right)$$

$$A_v = \frac{-R_C}{r_e + R_E}$$

where $R_s' = R_s \| R_1 \| R_2$.

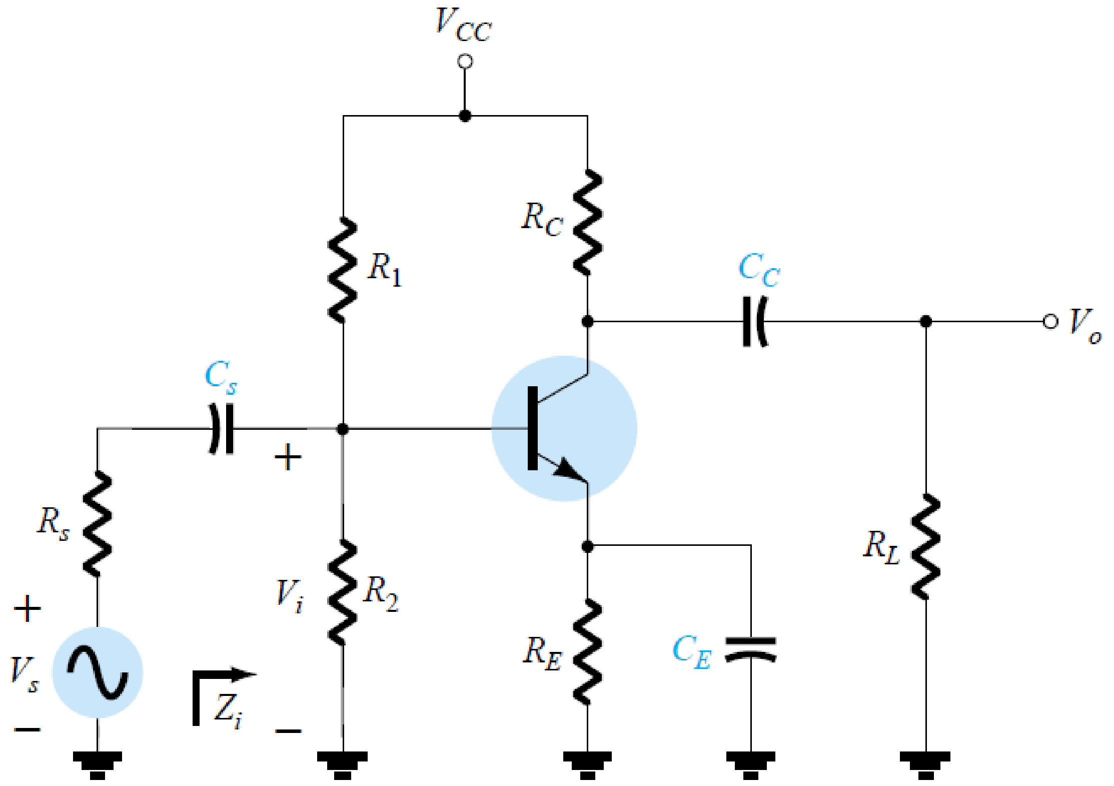
EXAMPLE:

Determine the lower cutoff frequency for the network of figure below using the following parameters:

$C_s = 10\ \mu\text{F}$, $C_E = 20\ \mu\text{F}$, $C_C = 1\ \mu\text{F}$

$R_s = 1\ \text{k}\Omega$, $R_1 = 40\ \text{k}\Omega$, $R_2 = 10\ \text{k}\Omega$, $R_E = 2\ \text{k}\Omega$, $R_C = 4\ \text{k}\Omega$,
$R_L = 2.2\ \text{k}\Omega$

$\beta = 100$, $r_o = \infty\ \Omega$, $V_{CC} = 20\ \text{V}$



Solution

(a) Determining r_e for dc conditions:

$$\beta R_E = (100)(2\ \text{k}\Omega) = 200\ \text{k}\Omega \gg 10R_2 = 100\ \text{k}\Omega$$

The result is:

$$V_B \cong \frac{R_2 V_{CC}}{R_2 + R_1} = \frac{10\ \text{k}\Omega(20\ \text{V})}{10\ \text{k}\Omega + 40\ \text{k}\Omega} = \frac{200\ \text{V}}{50} = 4\ \text{V}$$

with
$$I_E = \frac{V_E}{R_E} = \frac{4\ \text{V} - 0.7\ \text{V}}{2\ \text{k}\Omega} = \frac{3.3\ \text{V}}{2\ \text{k}\Omega} = 1.65\ \text{mA}$$

so that
$$r_e = \frac{26\ \text{mV}}{1.65\ \text{mA}} \cong \mathbf{15.76\ \Omega}$$

and
$$\beta r_e = 100(15.76\ \Omega) = 1576\ \Omega = \mathbf{1.576\ k\Omega}$$

Midband Gain

$$A_v = \frac{V_o}{V_i} = \frac{-R_C \| R_L}{r_e} = -\frac{(4\ \text{k}\Omega)\|(2.2\ \text{k}\Omega)}{15.76\ \Omega} \cong -90$$

The input impedance

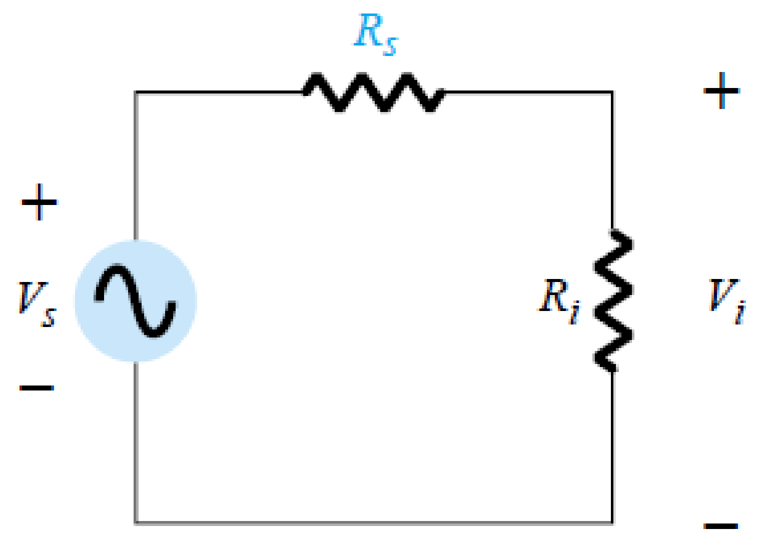
$$\begin{aligned} Z_i = R_i &= R_1 \| R_2 \| \beta r_e \\ &= 40\ \text{k}\Omega \| 10\ \text{k}\Omega \| 1.576\ \text{k}\Omega \\ &\cong 1.32\ \text{k}\Omega \end{aligned}$$

$$V_i = \frac{R_i V_s}{R_i + R_s}$$

$$\frac{V_i}{V_s} = \frac{R_i}{R_i + R_s} = \frac{1.32\ \text{k}\Omega}{1.32\ \text{k}\Omega + 1\ \text{k}\Omega} = 0.569$$

$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_o}{V_i}\,\frac{V_i}{V_s} = (-90)(0.569)$$

$$= \mathbf{-51.21}$$



C_s

$$R_i = R_1 \| R_2 \| \beta r_e = 40\ \text{k}\Omega \| 10\ \text{k}\Omega \| 1.576\ \text{k}\Omega \cong 1.32\ \text{k}\Omega$$

$$f_{L_s} = \frac{1}{2\pi\,(R_s + R_i)C_s} = \frac{1}{(6.28)(1\ \text{k}\Omega + 1.32\ \text{k}\Omega)(10\ \mu\text{F})}$$

$$f_{L_s} \cong \mathbf{6.86\ Hz}$$

C_C

$$f_{L_C} = \frac{1}{2\pi(R_C + R_L)C_C}$$

$$= \frac{1}{(6.28)(4\ \text{k}\Omega + 2.2\ \text{k}\Omega)(1\ \mu\text{F})}$$

$$\cong \mathbf{25.68\ Hz}$$

C_E

$$R_s' = R_s \| R_1 \| R_2 = 1\ \text{k}\Omega \| 40\ \text{k}\Omega \| 10\ \text{k}\Omega \cong 0.889\ \text{k}\Omega$$

$$R_e = R_E \left\| \left(\frac{R'_s}{\beta} + r_e \right) = 2\ \text{k}\Omega \right\| \left(\frac{0.889\ \text{k}\Omega}{100} + 15.76\ \Omega \right)$$

$$= 2\ \text{k}\Omega \| (8.89\ \Omega + 15.76\ \Omega) = 2\ \text{k}\Omega \| 24.65\ \Omega \cong 24.35\ \Omega$$

$$f_{L_E} = \frac{1}{2\pi R_e C_E} = \frac{1}{(6.28)(24.35\ \Omega)(20\ \mu\text{F})} = \frac{10^6}{3058.36} \cong \mathbf{327\ Hz}$$

Ninevah University
College of Electronics Engineering
Department of Systems and Control

Electronic I
Lecture 10

Multistage Amplifiers

2nd Class

by
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Outlines of Presentation

CASCADED SYSTEMS

- Example

R-C Coupled BJT Amplifiers

- Example

Direct-Coupled Multistage Amplifiers

- Example

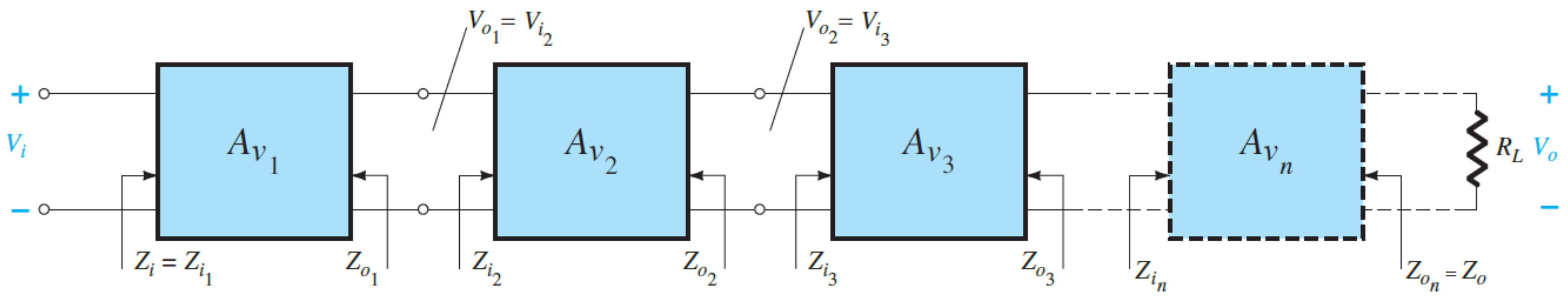
Cascaded System

The two-port systems approach is particularly useful for cascaded systems such as that appearing in Figure below , where A_{v1}, A_{v2}, A_{v3}, and so on, are the voltage gains of each stage *under loaded conditions.* The total gain of the system is then determined by the product of the individual gains as follows:

$$A_{v_T} = A_{v_1} \cdot A_{v_2} \cdot A_{v_3} \cdots$$

and the total current gain is given by

$$A_{i_T} = -A_{v_T} \frac{Z_{i_1}}{R_L}$$

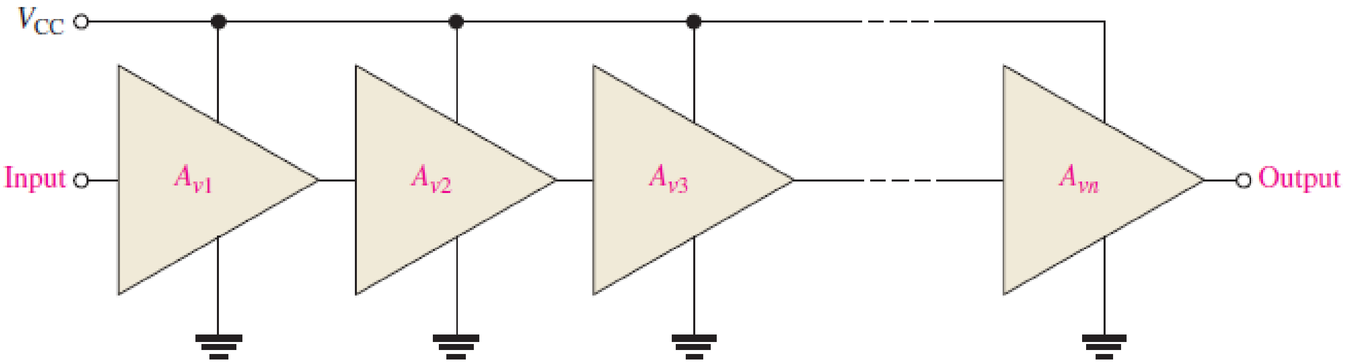


Cascaded System

Multistage Amplifiers

- Two or more amplifiers can be connected in a **cascaded** arrangement with the output of one amplifier driving the input of the next. The basic purpose of a multistage arrangement is to ***increase the overall voltage gain***
- The overall voltage gain, of cascaded amplifie A'_v as shown in the figure, is the product of the individual voltage gains.

$$A'_v = A_{v1}A_{v2}A_{v3}\ldots A_{vn}$$



- Also amplifier voltage gain is often expressed in **decibels** (dB) as follows:

$$A_{v(\mathrm{dB})} = 20 \log A_v$$

This is particularly useful in **multistage** systems because the overall voltage gain in dB is the *sum* of the individual voltage gains in dB.

$$A'_{v(\mathrm{dB})} = A_{v1(\mathrm{dB})} + A_{v2(\mathrm{dB})} + \cdots + A_{vn(\mathrm{dB})}$$

Example: A given amplifier arrangement has the following voltage gains. $A_{v1}=10$, $A_{v2}=20$ and $A_{v3}=40$. What is the overall gain? Also express each gain in dB and determine the total dB voltage gain.

Solution:

Given: $A_{v_1} = 10$; $A_{v_2} = 20$ and $A_{v_3} = 40$

Overall voltage gain

We know that the overall voltage gain,

$$A_v = A_{v_1} \times A_{v_2} \times A_{v_3} = 10 \times 20 \times 40 = 8000 \text{ Ans.}$$

Total dB voltage gain

We know that dB voltage gain of the first stage

$$G_{v_1} = 20 \log_{10} A_{v_1} = 20 \log_{10} 10 = 20 \text{ dB}$$

Similarly, $$G_{v_2} = 20 \log_{10} A_{v_2} = 20 \log_{10} 20 = 26 \text{ dB}$$

and $$G_{v_3} = 20 \log_{10} A_{v_3} = 20 \log_{10} 40 = 32 \text{ dB}$$

$\therefore$ Total dB voltage gain,

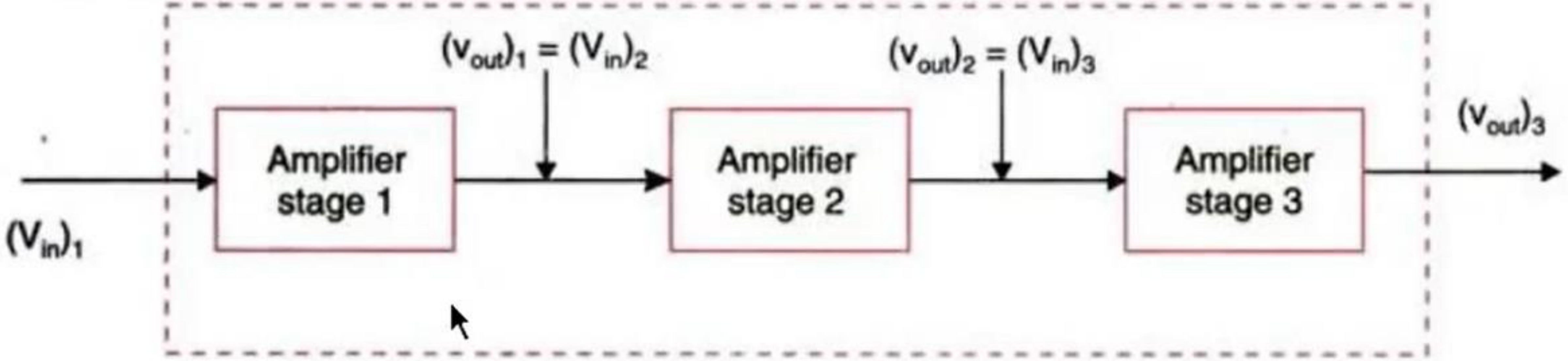
$$G_v = G_{v_1} + G_{v_2} + G_{v_3} = 20 + 26 + 32 \text{ dB} = 78 \text{ dB Ans.}$$

Note: Check $$G_v = 20 \log_{10} A_v = 20 \log_{10} 8000 = 78 \text{ dB.}$$

Example: Three amplifier stages are working in cascade with 0.05v peak to peak input providing 150v peak-to-peak output. If the voltage gain of the first stage is 20and input to the third stage is 15v peak-to-peak. Determine:

i. The overall voltage gain.
ii. Voltage gain of 2^{nd} and 3^{rd} stages.
iii. Input voltage of the 2^{nd} stage.

Gives : No. of amplifier stages = 3. Input to the first stage, $v_{in_1} = 0.05\ V_{pk-pk}$, Output of the final stage $(v_{out})_3 = 150\ V_{pk-pk}$. Voltage gain of the first stage $A_{v_1} = 20$; Input to the third stage $v_{in_3} = 15\ V_{pk-pk}$. Refer to Fig. 26.2 for clear explanation.



3-Stage Amplifier

(i) Overall Voltage gain

We know that overall voltage gain,

$$A_v = \frac{(v_{out})_3}{(v_{in})_1} = \frac{150}{0.05} = 3000 \quad \textbf{Ans.}$$

(ii) Voltage gain of 2nd and 3rd stage

We know that voltage gain of the 3rd stage,

$$A_{v_3} = \frac{(v_{out})_3}{(v_{in})_3} = \frac{150}{15} = 10 \quad \textbf{Ans.}$$

Let A_{v_2} = Gain of the 2nd stage.

We know that the overall voltage gain (A_v),

$$3000 = A_{v_1} \cdot A_{v_2} \cdot A_{v_3} = 20 \times A_{v_2} \times 10 = 200\ A_{v_2}$$

Multistage Amplifiers:

Example

A certain cascaded amplifier arrangement has the following voltage gains: $A_{v1} = 10$, $A_{v2} = 15$, and $A_{v3} = 20$. What is the overall voltage gain? Also express each gain in decibels (dB) and determine the total voltage gain in dB.

Solution:

$$A'_v = A_{v1}A_{v2}A_{v3} = (10)(15)(20) = \mathbf{3000}$$

$$A_{v1(\text{dB})} = 20 \log 10 = \mathbf{20.0\ dB}$$

$$A_{v2(\text{dB})} = 20 \log 15 = \mathbf{23.5\ dB}$$

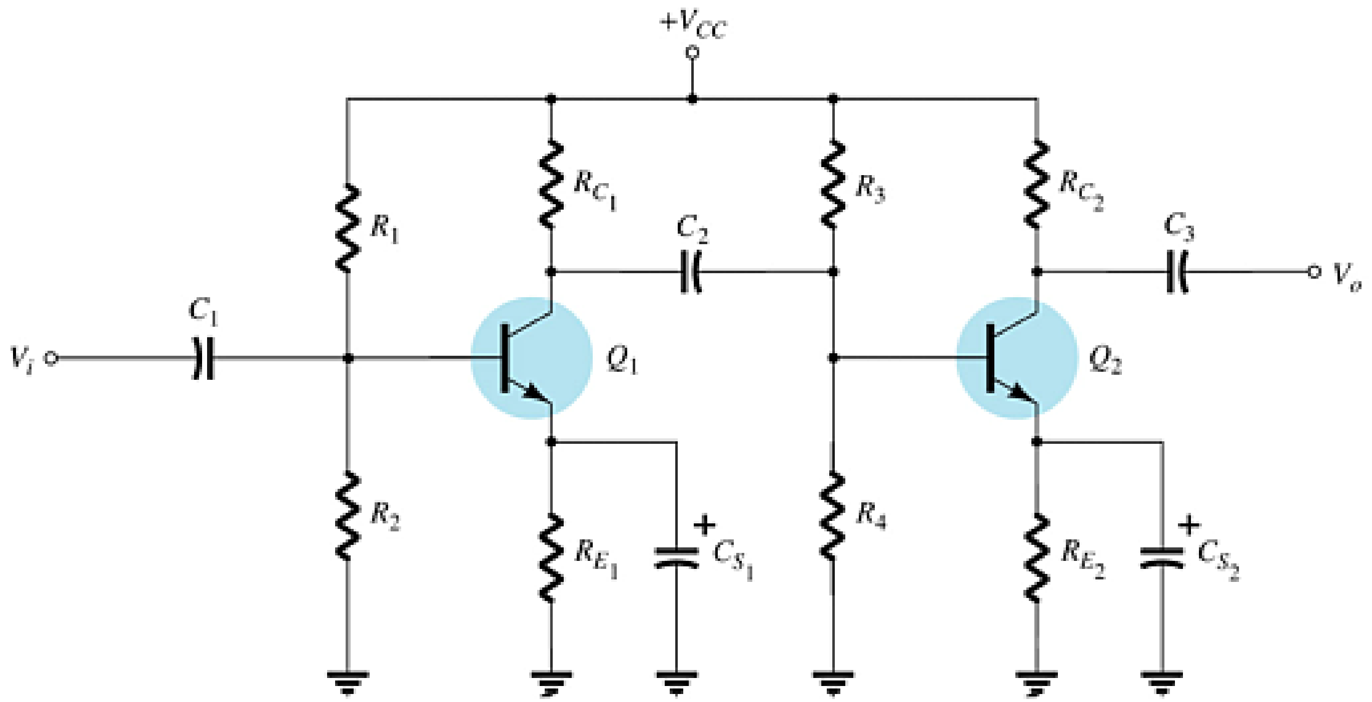
$$A_{v3(\text{dB})} = 20 \log 20 = \mathbf{26.0\ dB}$$

$$A'_{v(\text{dB})} = 20.0\ \text{dB} + 23.5\ \text{dB} + 26.0\ \text{dB} = \mathbf{69.5\ dB}$$

R-C Coupled BJT Amplifiers

As shown in figure below the collector output of the first stage is fed directly into the base of the next stage using coupling capacitor (C_C). Capacitive coupling prevents the dc bias of one stage from affecting that of the other but allows the ac signal to pass without attenuation because $X_C=0$ at the frequency of operation. The same coupling can be used between any combinations of networks. Substituting an open circuit equivalent for CC and other capacitors of the network will result in two voltage divider biasing networks so the introduced methods of analysis can be used.

Loading Effects: It means the effect of Zi of the second stage on the gain . where the total input impedance of the second stage is present as Load to the first stage.



R-C Coupled BJT Amplifiers

Input impedance, first stage:

$$Z_i = Z_{i1} = R_1 \parallel R_2 \parallel \beta r_{e1}$$

Output impedance, second stage:

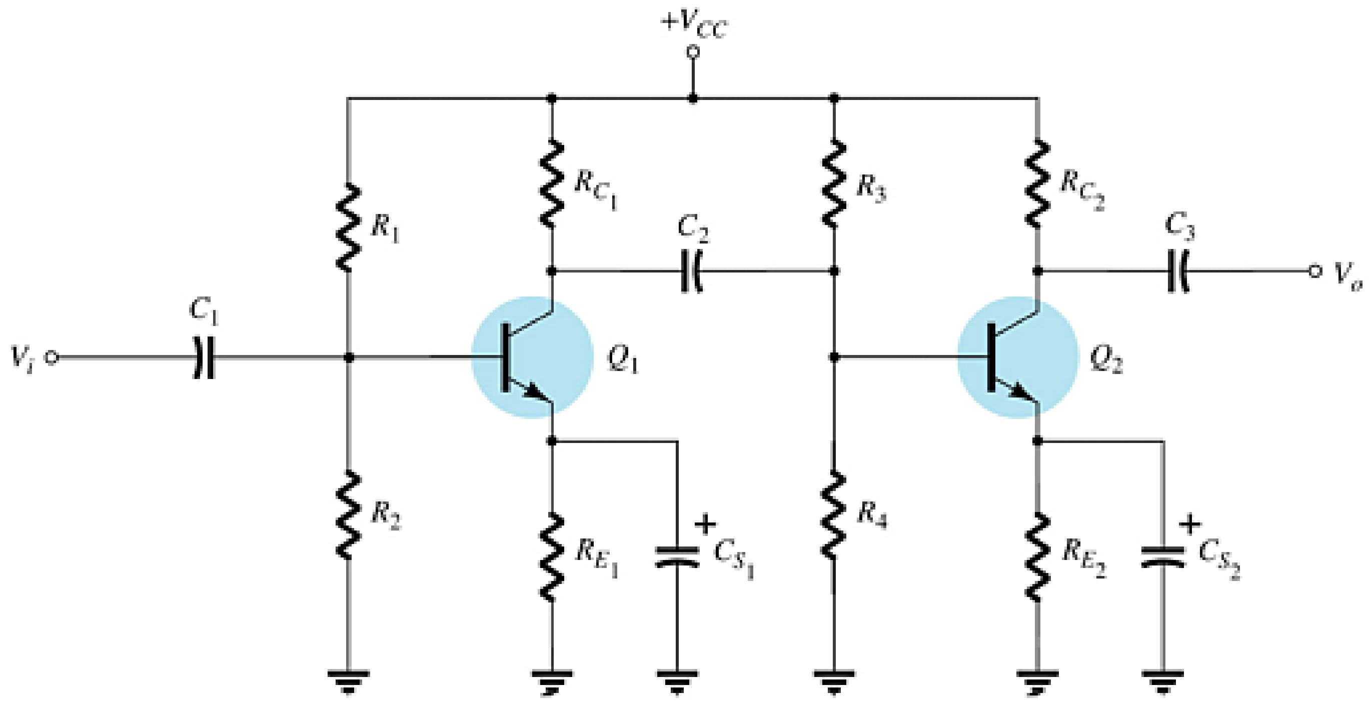
$$Z_o = R_{C2}$$

Voltage gain:

$$A_{V1} = -\frac{R_{C1} \parallel Z_{i2}}{r_{e1}} = \frac{R_{C1} \parallel R_3 \parallel R_4 \parallel \beta r_{e2}}{r_{e1}}$$

$$A_{V2} = -\frac{R_{C2}}{r_{e2}}$$

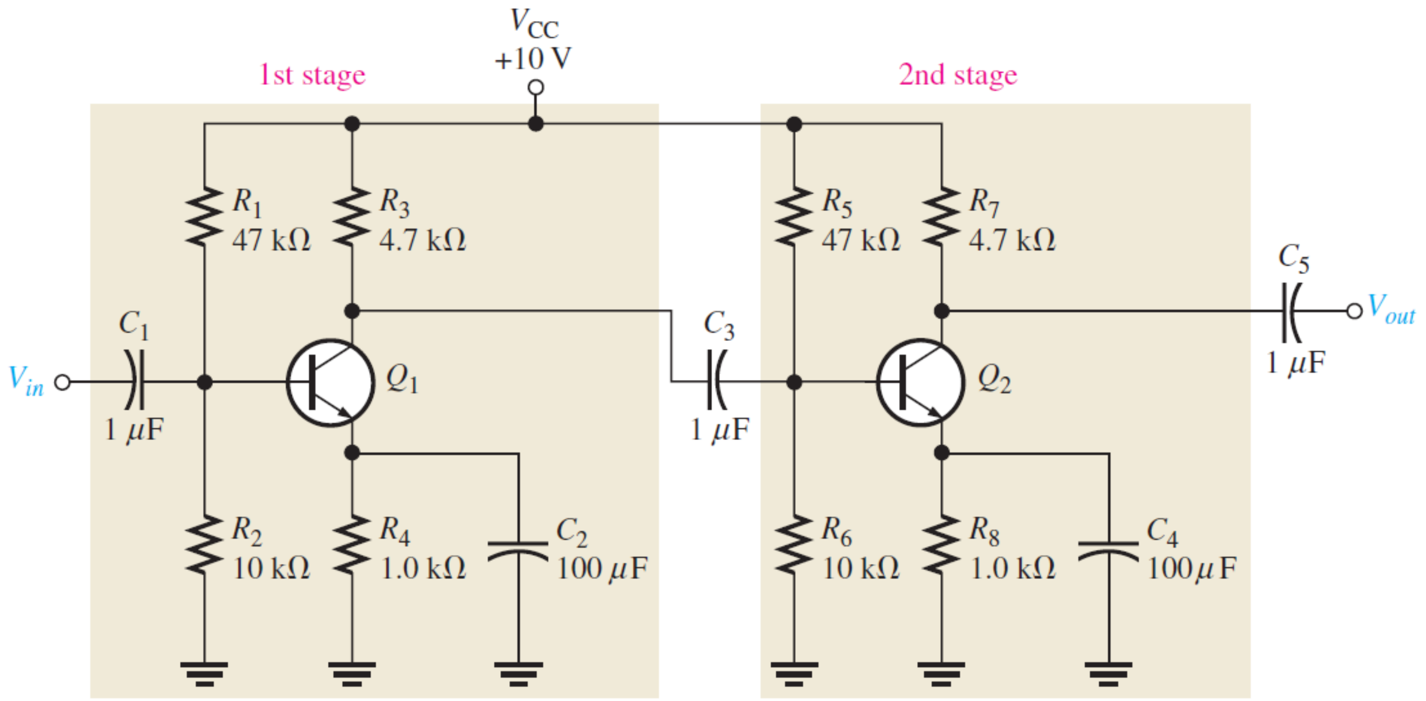
$$A_V = A_{V1} A_{V2}$$



$$Z_{i2} = R_3 \parallel R_4 \parallel \beta r_{e2}$$

Example :

Two-stage capacitively coupled amplifier is shown in Figure below. Notice that both stages are identical **common-emitter** amplifiers with the output of the first stage **capacitively coupled** to the input of the second stage. Capacitive coupling prevents the dc bias of one stage from affecting that of the other. Find overall voltage gain



$\beta_{DC} = \beta_{ac} = 150$ for Q_1 and Q_2

The DC biasing is same for both stages and is identical for common emitter dc biasing discussed before (V_B, V_E, V_C, I_B, I_E, I_C, and V_{CE})

Solution:

DC Voltages in the Capacitively Coupled Multistage Amplifier

Since both stages in Figure are identical, the dc voltages for Q_1 and Q_2 are the same. Since β R4≫ 10 $R2$ and β R8 ≫ 10 $R6$ and the dc base voltage for Q_1 and Q_2 is

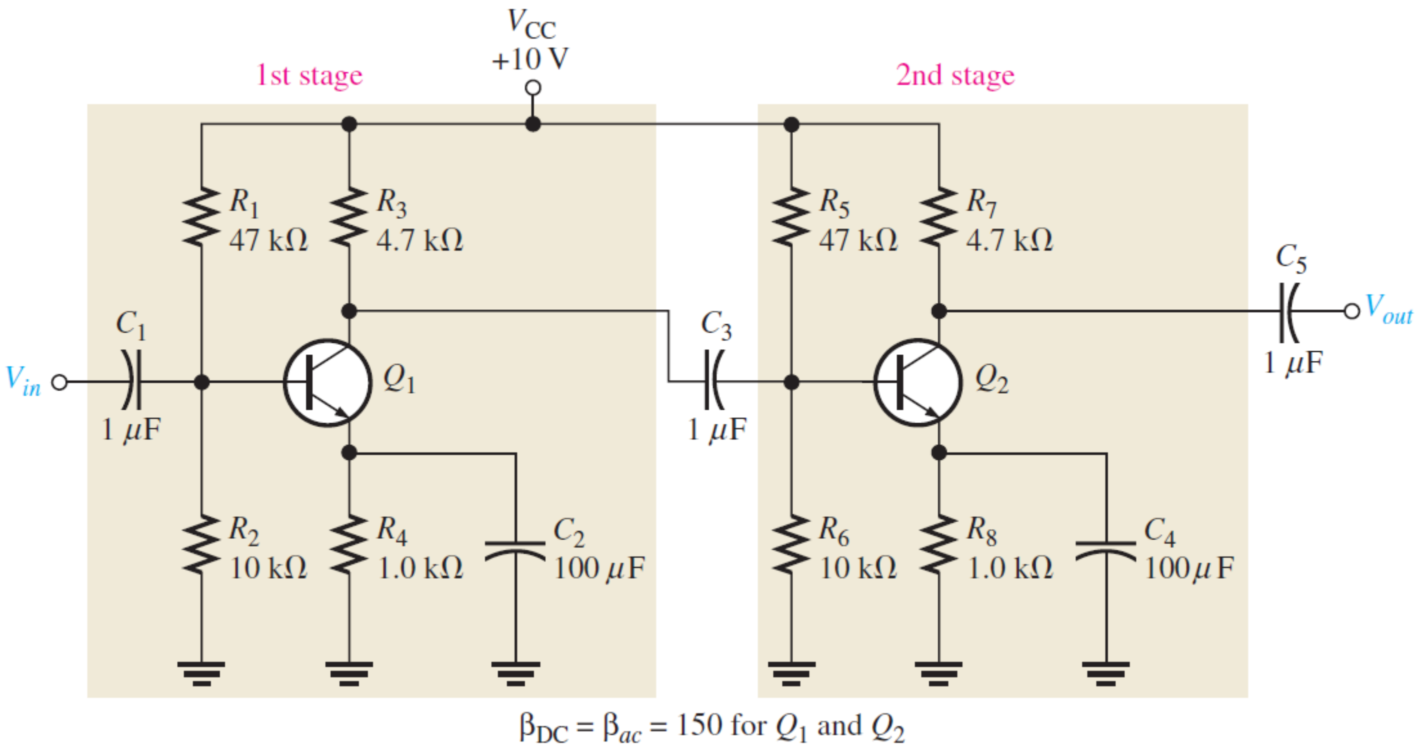
$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{10\text{ k}\Omega}{57\text{ k}\Omega}\right)10\text{ V} = 1.75\text{ V}$$

$$V_E = V_B - 0.7\text{ V} = 1.05\text{ V}$$

$$I_E = \frac{V_E}{R_4} = \frac{1.05\text{ V}}{1.0\text{ k}\Omega} = 1.05\text{ mA}$$

$$I_C \cong I_E = 1.05\text{ mA}$$

$$V_C = V_{CC} - I_C R_3 = 10\text{ V} - (1.05\text{ mA})(4.7\text{ k}\Omega) = 5.07\text{ V}$$



Solution:

Voltage Gain of the First Stage The ac collector resistance of the first stage is

$$R_{c1} = R_3 \| R_5 \| R_6 \| R_{in(base2)}$$

Remember that lowercase italic subscripts denote ac quantities such as for R_c.

You can verify that $I_E = 1.05$ mA, $r'_e = 23.8\,\Omega$, and $R_{in(base2)} = 3.57\text{ k}\Omega$. The effective ac collector resistance of the first stage is as follows:

$$R_{c1} = 4.7\text{ k}\Omega \| 47\text{ k}\Omega \| 10\text{ k}\Omega \| 3.57\text{ k}\Omega = 1.63\text{ k}\Omega$$

Therefore, the base-to-collector voltage gain of the first stage is

$$A_{v1} = \frac{R_{c1}}{r'_e} = \frac{1.63\text{ k}\Omega}{23.8\ \Omega} = 68.5$$

Voltage Gain of the Second Stage The second stage has no load resistor, so the ac collector resistance is R_7, and the gain is

$$A_{v2} = \frac{R_7}{r'_e} = \frac{4.7\text{ k}\Omega}{23.8\ \Omega} = 197$$

Compare this to the gain of the first stage, and notice how much the loading from the second stage reduced the gain.

Overall Voltage Gain The overall amplifier gain with no load on the output is

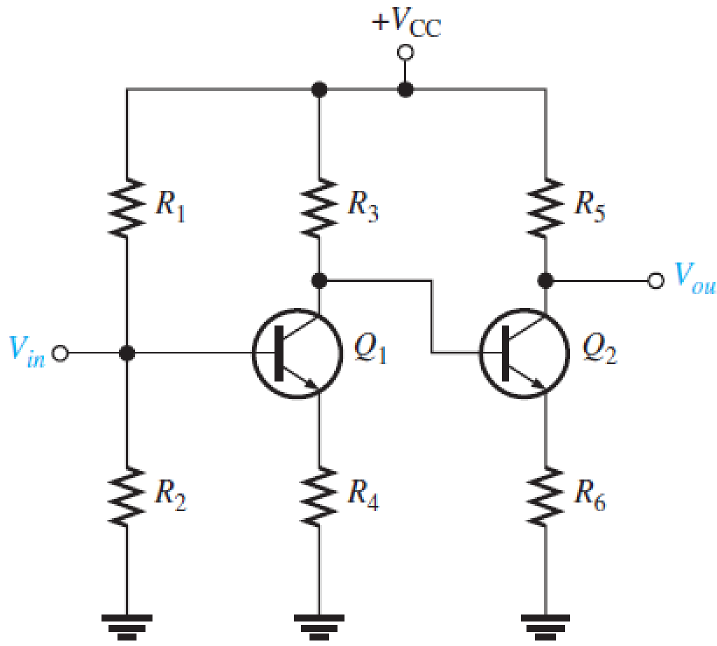
$$A'_v = A_{v1}A_{v2} = (68.5)(197) \cong 13{,}495$$

If an input signal of 100 μV, for example, is applied to the first stage and if there is no attenuation in the input base circuit due to the source resistance, an output from the second stage of $(100\ \mu\text{V})(13{,}495) \cong 1.35$ V will result. The overall voltage gain can be expressed in dB as follows:

$$A'_{v(\text{dB})} = 20 \log (13{,}495) = 82.6\text{ dB}$$

Direct-Coupled Multistage Amplifiers

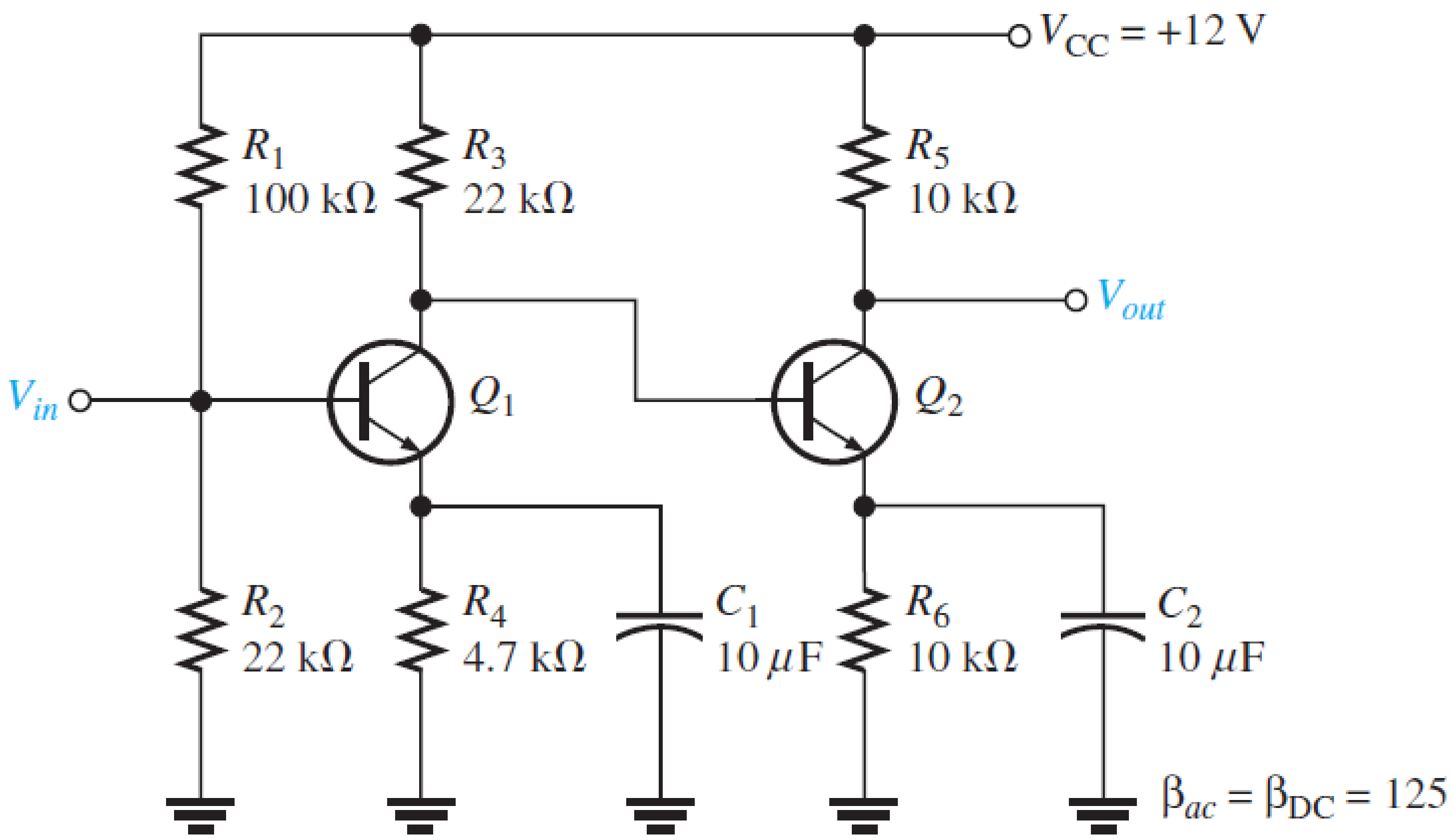
A basic two-stage, the direct-coupled amplifier is shown in Figure. Notice that there are no coupling or bypass capacitors in this circuit. The dc collector voltage of the first stage provides the base-bias voltage for the second stage. Because of the direct coupling, this type of amplifier has a better *low-frequency* response than the capacitively coupled type in which the reactance of coupling and bypass capacitors at very low frequencies may become excessive. The increased reactance of capacitors at lower frequencies produces gain reduction in capacitively coupled amplifiers.



Direct-coupled amplifiers can be used to amplify low frequencies all the way down to dc (0 Hz) without loss of voltage gain because there are no capacitive reactance in the circuit. The **disadvantage** of direct-coupled amplifiers, on the other hand, is that small changes in the dc bias voltages from temperature effects or power-supply variation are amplified by the succeeding stages, which can result in a significant drift in the dc levels throughout the circuit.

Example:

Figure below shows a direct-coupled (that is, with no coupling capacitors between stages) two-stage amplifier. The dc bias of the first stage sets the dc bias of the second. Determine all dc voltages for both stages and the overall ac voltage gain.



Solution:

$$V_{B1} = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC} = \left(\frac{22\ \text{k}\Omega}{122\ \text{k}\Omega}\right) 12\ \text{V} = \mathbf{2.16\ V}$$

$$V_{E1} = V_{B1} - 0.7\ \text{V} = \mathbf{1.46\ V}$$

$$I_{C1} \cong I_{E1} = \frac{V_{E1}}{R_4} = \frac{1.46\ \text{V}}{4.7\ \text{k}\Omega} = 0.311\ \text{mA}$$

$$V_{C1} = V_{CC} - I_{C1}R_3 = 12\ \text{V} - (0.311\ \text{mA})(22\ \text{k}\Omega) =$$

$$V_{B2} = V_{C1} = \mathbf{5.16\ V}$$

$$V_{E2} = V_{B2} - 0.7\ \text{V} = 5.16\ \text{V} - 0.7\ \text{V} = \mathbf{4.46\ V}$$

$$I_{C2} \cong I_{E2} = \frac{V_{E2}}{R_6} = \frac{4.46\ \text{V}}{10\ \text{k}\Omega} = 0.446\ \text{mA}$$

$$V_{C2} = V_{CC} - I_{C2}R_5 = 12\ \text{V} - (0.446\ \text{mA})(10\ \text{k}\Omega) =$$

$$r'_{e2} \cong \frac{25\ \text{mV}}{I_{E2}} = \frac{25\ \text{mV}}{0.446\ \text{mA}} = 56\ \Omega$$

$$R_{in(2)} = \beta_{ac} r'_{e2} = (125)(56\ \Omega) = 7\ \text{k}\Omega$$

$$r'_{e1} \cong \frac{25\ \text{mV}}{I_{E1}} = \frac{25\ \text{mV}}{0.311\ \text{mA}} = 80.4\ \Omega$$

$$A_{v1} = \frac{R_3 \parallel R_{in(2)}}{r'_{e1}} = \frac{22\ \text{k}\Omega \parallel 7\ \text{k}\Omega}{80.4\ \Omega} = \mathbf{66}$$

$$A_{v2} = \frac{R_5}{r'_{e2}} = \frac{10\ \text{k}\Omega}{56\ \Omega} = \mathbf{179}$$

$$A'_v = A_{v1}A_{v2} = (66)(179) = \mathbf{11{,}814}$$