Ninevah University

College of Electronics Engineering

Department of Electronic Engineering

2nd Class

Subject: Electronic I

2018 – 2019

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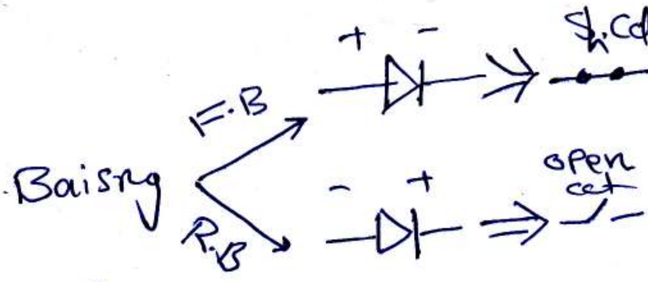
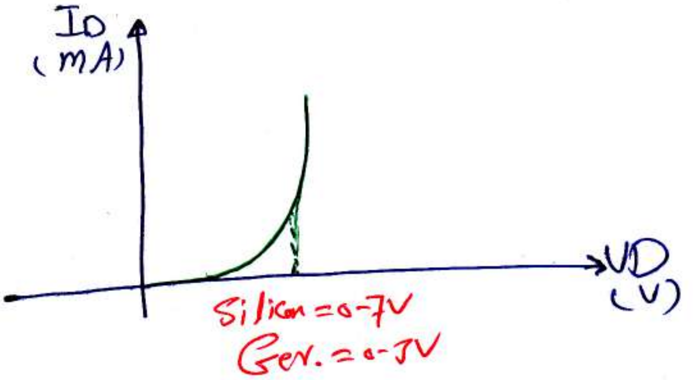
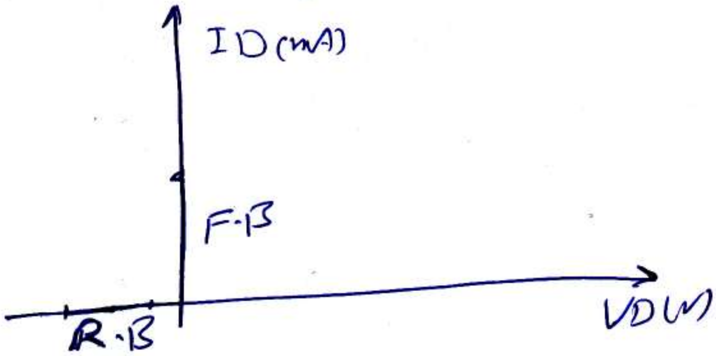
Lecture 1 : Review







$R_D \Rightarrow$ resistance of Diode $= \frac{\Delta V}{\Delta I}$

when the anode is more Positive voltage from Kathode, the Diode is F.B (Forward Baising)

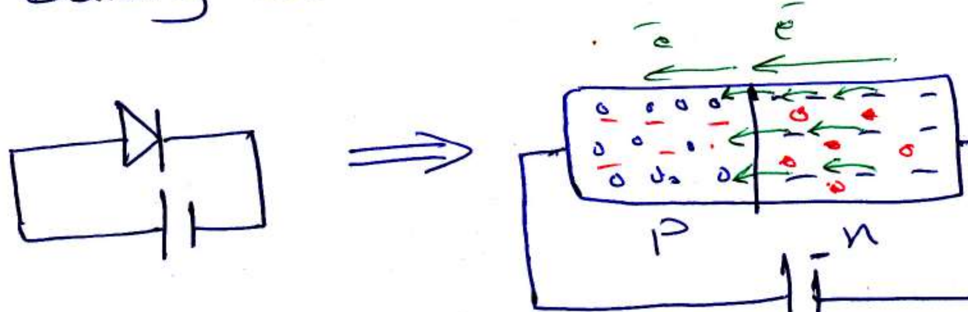
its mean

$\therefore R_D = \frac{\Delta V}{\Delta I} = \frac{0}{\Delta I} = 0\ \Omega$ (ideal case) $\Rightarrow$ short cct

when the anode is less positive voltage from Kathode, the Diode is R.F (reverse Baising)

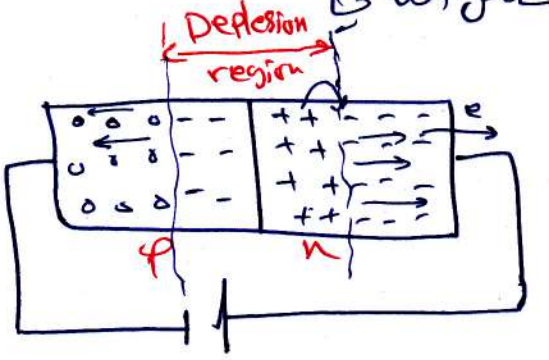
$\therefore R_D = \frac{\Delta V}{\Delta I} = \frac{\Delta V}{0} = \infty\ \Omega$ $\rightarrow$ its mean open cct

* Baising Diode



بما أن الـ n-region والذي يحتوي على عدد كبير من الإلكترونات قد ربط إلى الطرف السالب للمصدر فإن الإلكترونات ستتجه نحو الـ P-region مخترقة junction تاركة خلفها أيونات موجبة وبنفس الوقت تتحرك الـ holes في P-region بعكس اتجاه حركة الإلكترونات لتمثلان بذلك حركة التيار الكهربائي

عند عكس اتجاه القطبية للمصدر كما موضح في الشكل التالي



الالكترونات ستنجذب باتجاه القطب الموجب تاركة
وراءها أيونات موجبة وكذا الحال فيما يخص
الفجوات التي ستنجذب نحو القطب السالب
للمصدر وهذا سيؤدي الى زيادة عرض
منطقة الاستنزاف Depletion Region ويصبح الدايود في حالة انحياز عكسي
ويكون بثابة عازل تقريباً مادياً للصفر

ملاحظة: الفجوات القليلة في منطقة الـ n ستجذب لمنطقة P مولدة بذلك
تيار تيار جداً يسمى I reverse current

Transistor

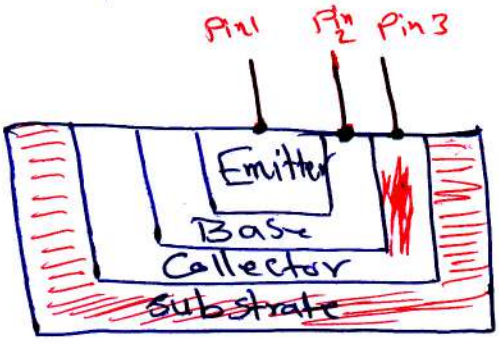
- Bipolar Junction Transistor (BJT)
- Field Effect Transistor (FET)

Bipolar Junction Transistor :-

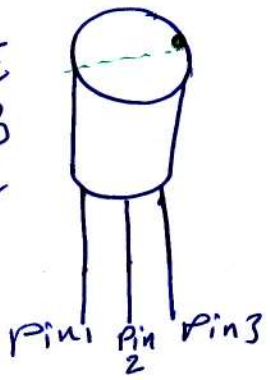
The transistor is a three-layer semiconductor device consisting of either two n- and one P-type layers of material or two P- and one n-type layers of material.

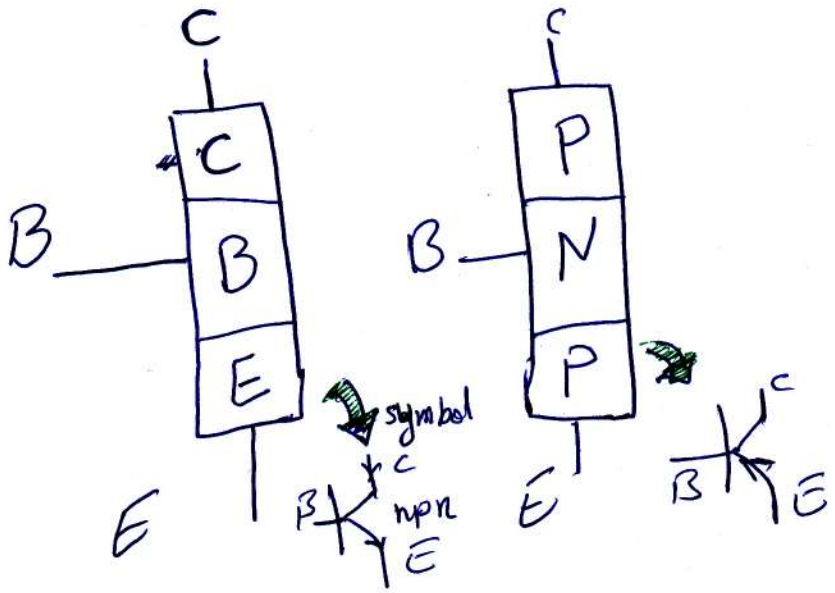
- BJT
  - NPN
  - PNP

Structure of BJT :-



Emitter = E
Base = B
Collector = C



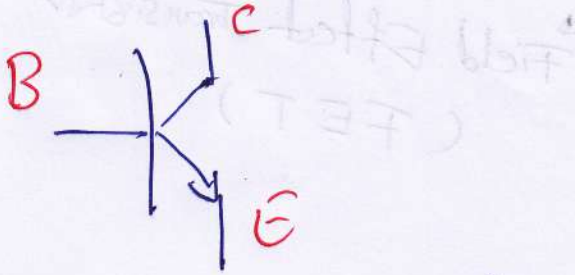


E ⇒ heavily doped

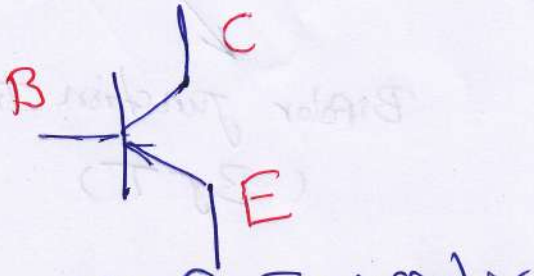
C ⇒ moderately doped

B ⇒ Lightly doped

Standard transistor symbol :-

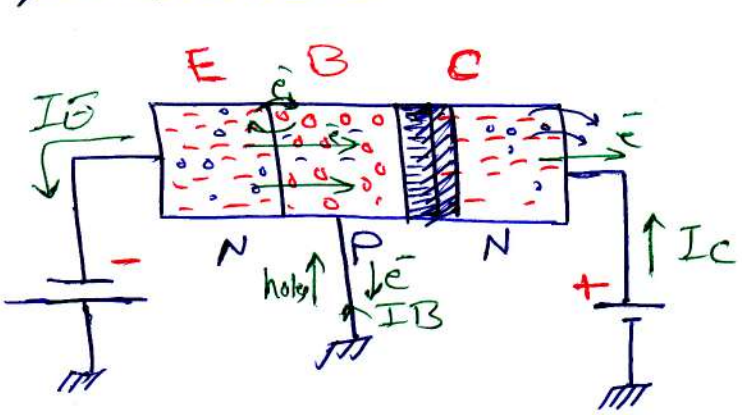


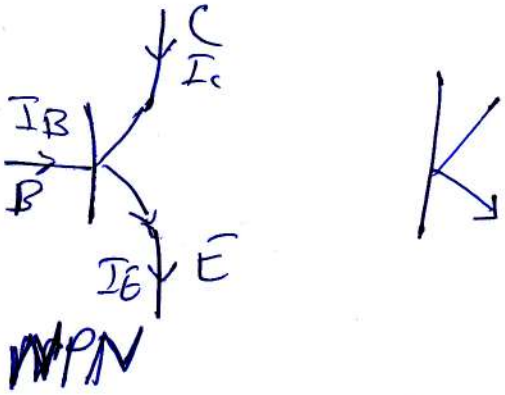
npn Transistor



pnp Transistor

* NPN Transistor :

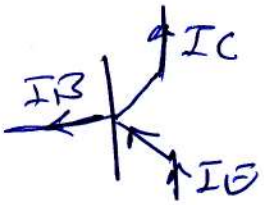




$$I_E = I_C + I_B \qquad I_C \gg I_B$$

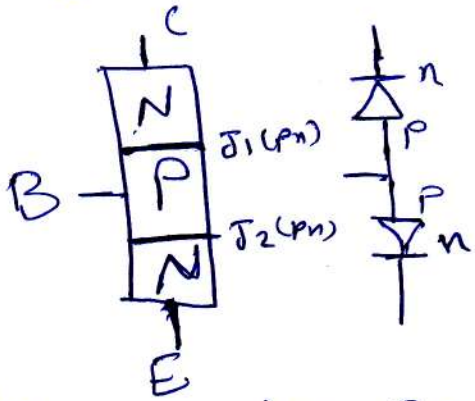
$I_C = I_{c\,majority} + I_{co\,minority}$

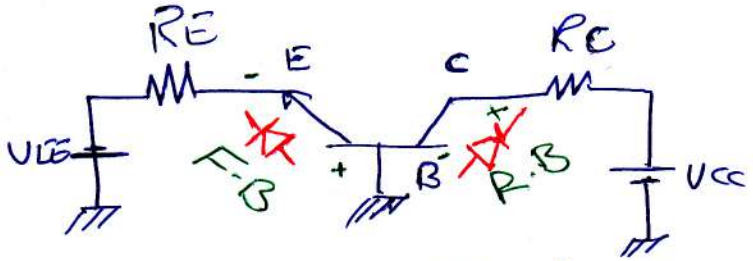
Also, Same that happen in PNP Transistor



Basic transistor operation

BJT Transistor has two pn Junction





How to work the Transistor ?

There are two Conditions must be acheived in Transister to work as Amplifier

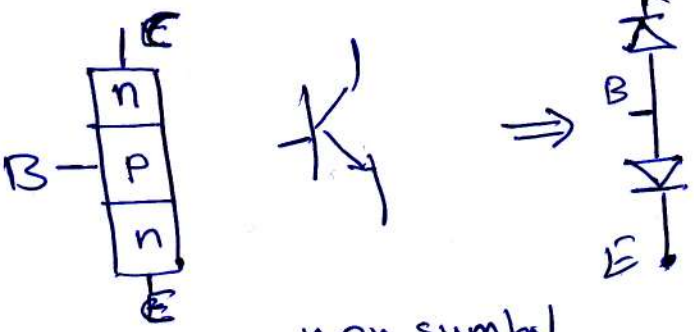
- BE Junction Forword Baising F-B
- BC Junction Reverse Baising R.B

* Transistor Applications

- As Amplifier (Active Region)
- As Switch (Saturation & cutoff) Region

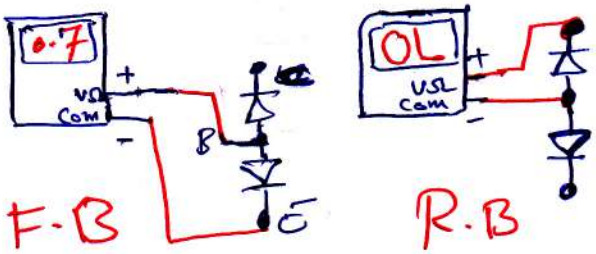
*The DMM Diode Test Position

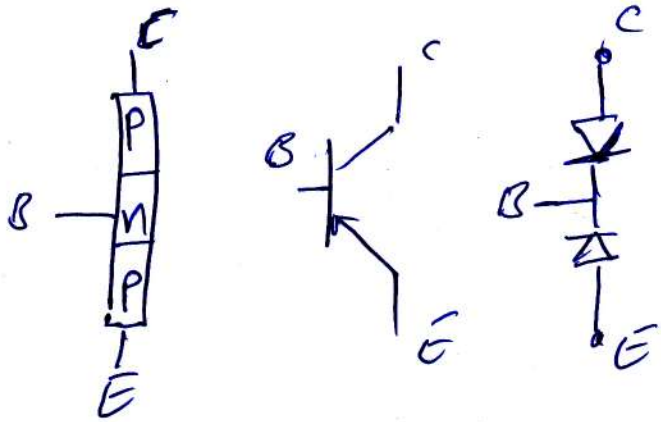
A digital multimeter can be used as a fast and simple way to check a transistor. for this test, you can view the transistor as two diodes connected as shown below



npn

npn symbol





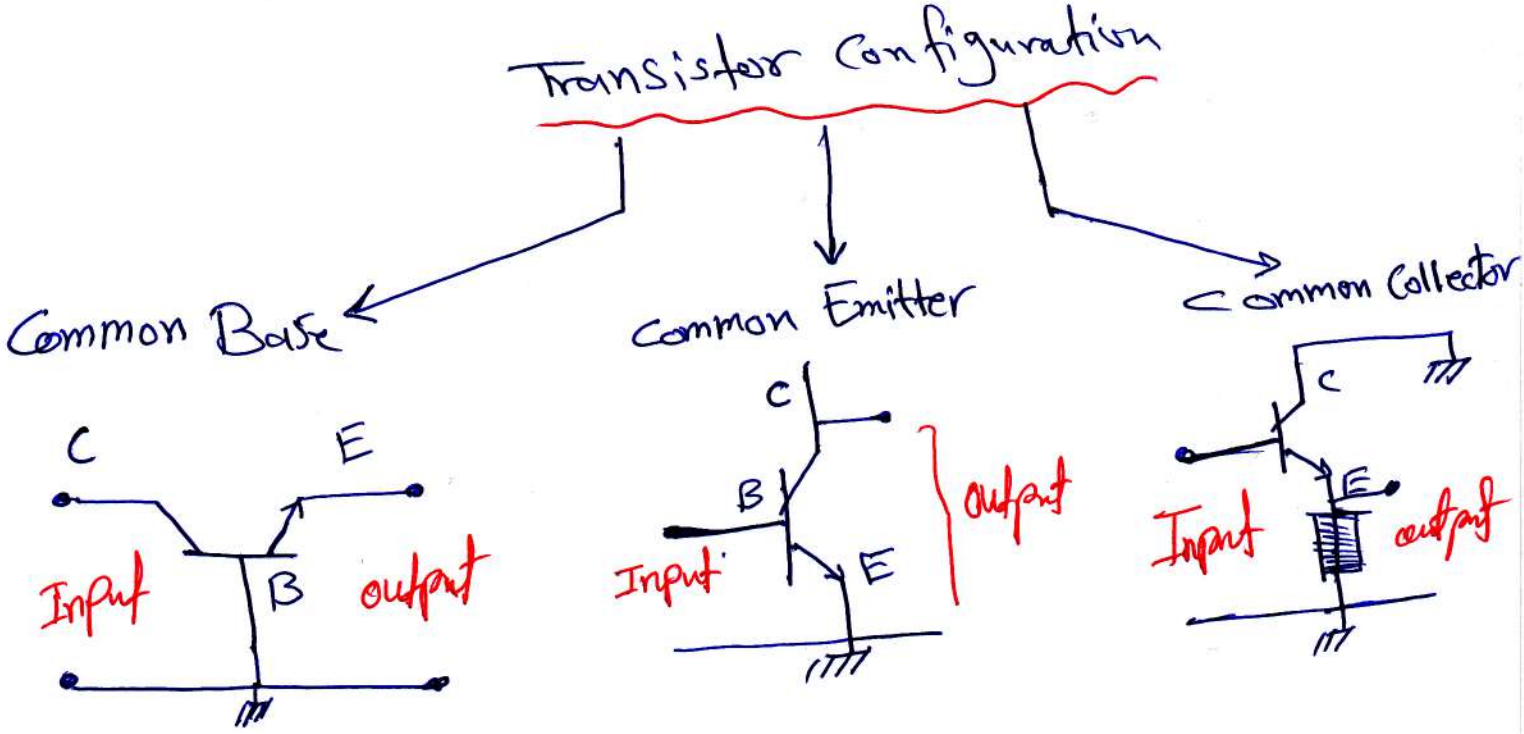
pnp

pnp symbols

Note If the junction is good, you will get a reading of between approximately 0.6V and 0.8V

Transistor Configurations

The bipolar transistor is a three terminal device. Three basic single transistor amplifier configurations can be formed depending on which of the three terminals is used as signal ground (i.e. which terminal is common to both the input and output side of the configuration.

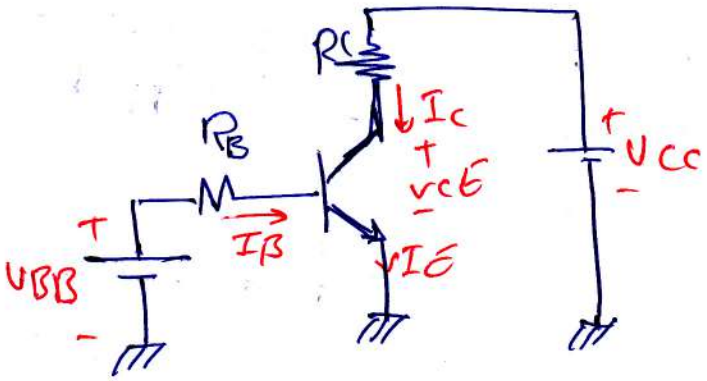


Common Base $\Longrightarrow$ C.B.

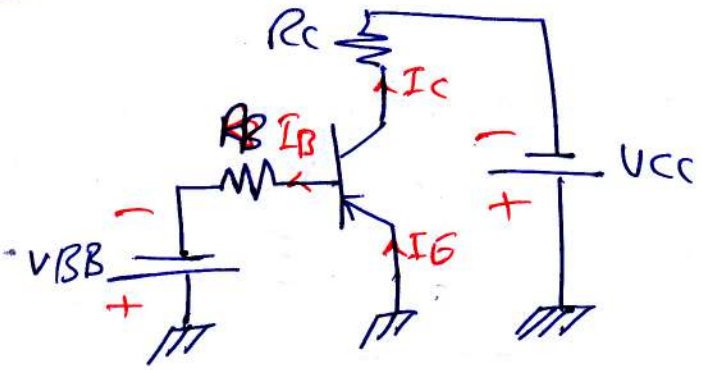
Common Emitter $\Longrightarrow$ C.E.

Common Collector $\Longrightarrow$ C.C.

Common Emitter Configuration :- (C.E)



npn Transistor
C.E



pnp Transistor
C.E

in C.E
- input ⟹ Base Terminal
- output ⟹ Collector "
- Common ⟹ Emitter "

Dc Beta :- Dc current gain (β_{DC})

$$\beta_{DC} = \frac{\text{Dc output current}}{\text{Dc input current}} \Rightarrow \beta_{DC} = \frac{I_C}{I_B}$$

typical values of β_{DC} 20 ~ 200 or higher

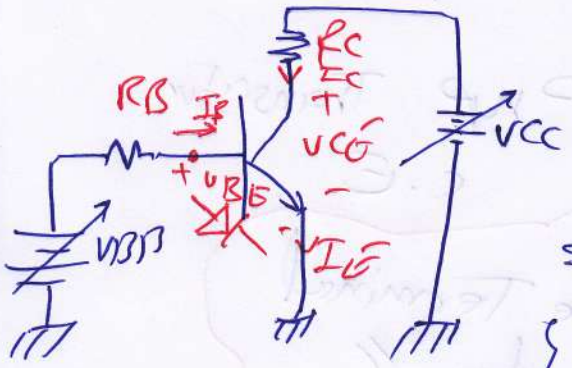
in Datasheet $\beta_{DC} = h_{FE}$

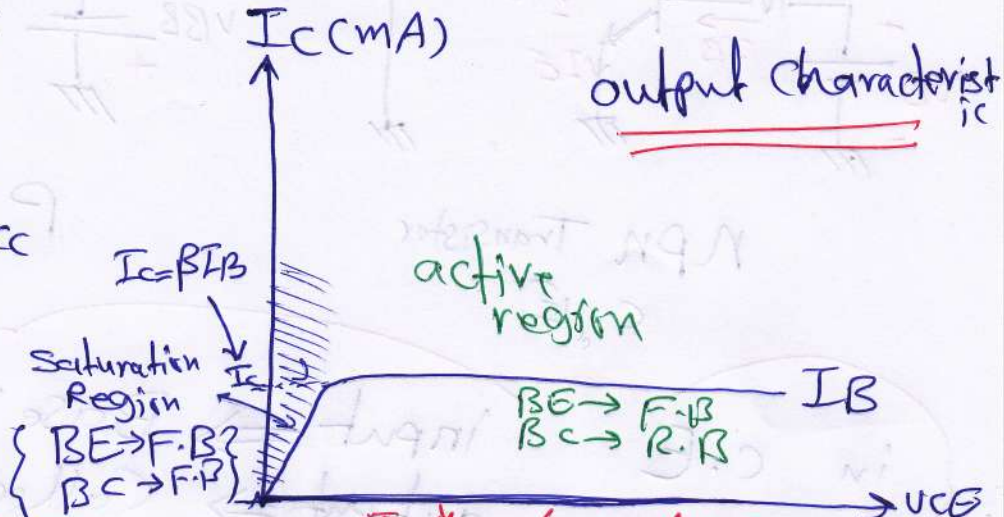
Ex Determine the dc current gain β_{DC} and the Emitter Current I_E for a transistor where $I_B = 50\mu A$, and $I_C = 3.65mA$

Solution $\beta_{DC} = \frac{I_C}{I_B} = \frac{3.65m}{50\mu} = \frac{3.65m}{50 * 10^{-3}m} = 73$

$$I_E = I_C + I_B = 3.65\,m + 50\,\mu = 3.7\,mA$$

To describe the behavior of the C.E Configuration we need to draw the characteristics of the input and o/p of C.E



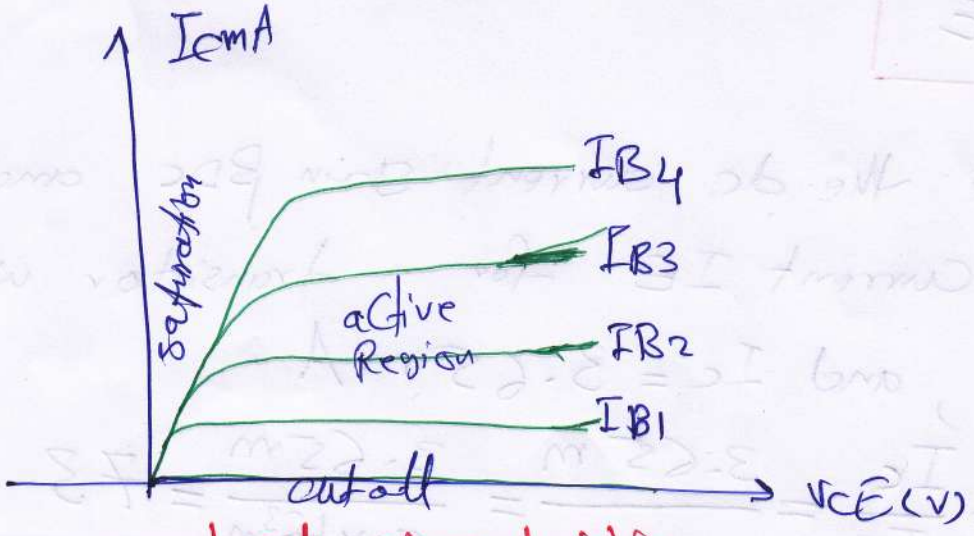


VBE = 0.7V for Silicon
= 0.3V for Germanium

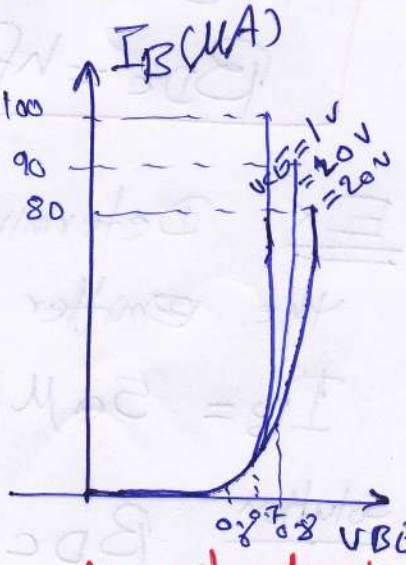
Ic = 0 (cut-off Region) when VBB is very small and IB ≅ 0

{ BE → R.B.
BC → R.B. }

The output characteristic above for one value of IB (i.e. one value of VBB), to get fully o/p characteristic curve we must be change the value of VBB and Vcc together.



output characteristic



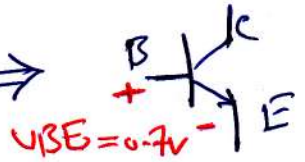
i/p Characteristic

From the characteristics of the transistor, its clear that there are three basic regions :-

① The active region :- (As Amplifier) Tr.

- state of Junctions of the transistor are

* BE → Forward Bias ⇒



* BC → Reverse Bias (Collector more positive from Base) ⇒

② The saturation region :-

BE Junction
BC Junction
→ Forward Bias

③ The cutoff region :

BE Junction
BC Junction
→ Reverse Bias

NoTe :- The transistor work as amplifier in active region whearas it work as switch in cutoff and saturation regions.

From the o/p C/C it is clear that the operating Point of transister is located in one of three regions

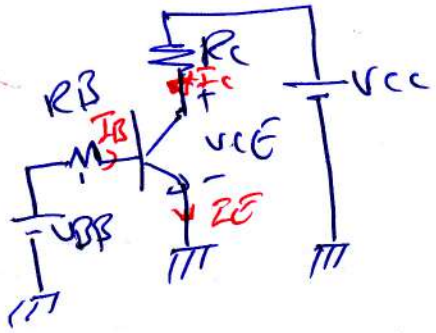
① active region ↔ Junction BE is Forward Biased
Junction BC is Reverse Biased

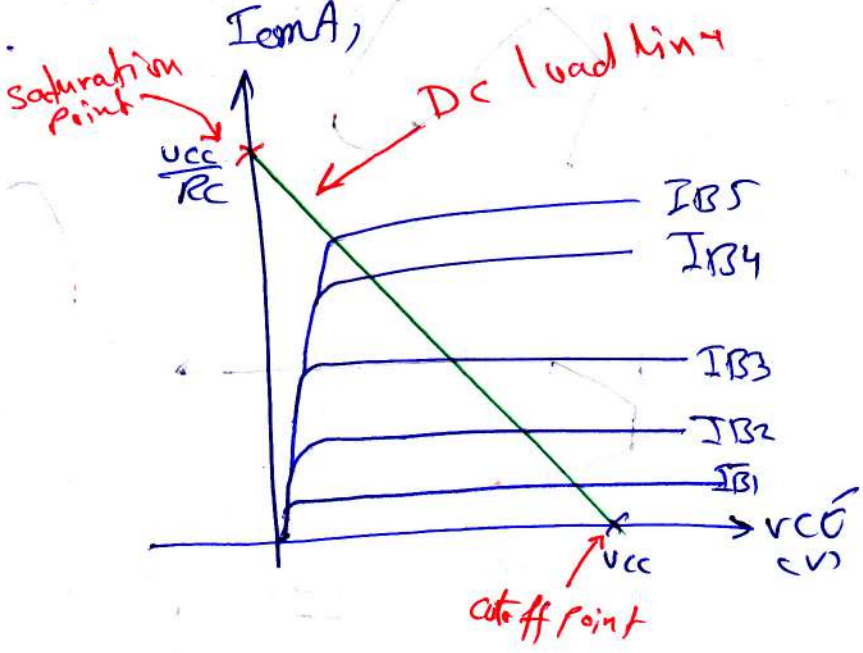
② Saturation region → Junction BE, Junction BC } ⇒ Forward Baised

③ Cutoff region → Junction BE, Junction BC } ⇒ Reverse Baised

Dc load line :-

It is a line that determine all the points that the transistor will operate. In other word, the operation Point (usually called Q) will be somewhere on the DC load line.





$$-V_{CE} - I_C R_C + V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

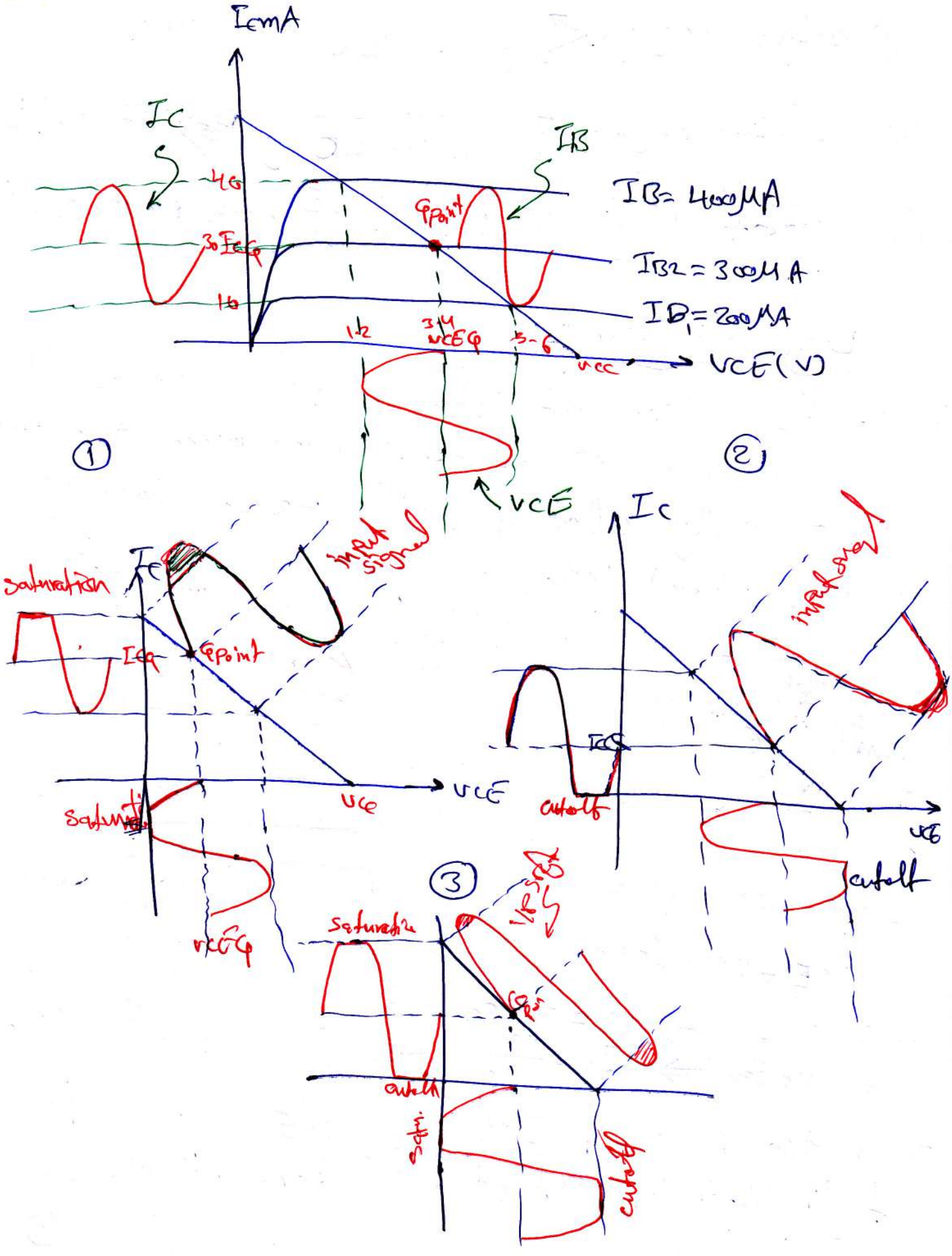
when $I_C = 0 \Rightarrow V_{CE} = V_{CC}$ — ①

& $V_{CE} = 0 \Rightarrow I_C = \frac{V_{CC}}{R_C}$ — ②

} ⇒ Dc load line

From values of IB, Ic and VCE, the Q Point of transister is defined and determined on DC load line.

If an amplifier is not biased with correct dc voltages on the input and output, it can go into Saturation or Cutoff when an input signal is applied

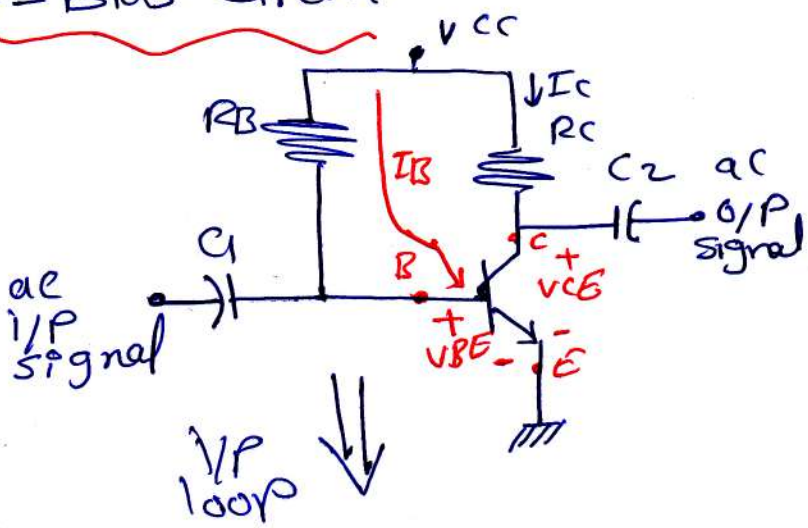


Dc Biasing circuits of BJTs

* Standard Baising circuits

1. Fixed-Bias Circuits
2. Emitter-Stabilized Bias circuits
3. Voltage divider Bias circuit
4. Collector-Feedback Bias circuit

① Fixed-Bias Circuit

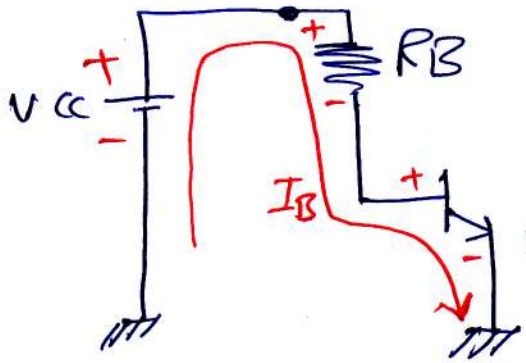


Analysis:

For the input loop:-

$-V_{CC} + R_B I_B + V_{BE} = 0$

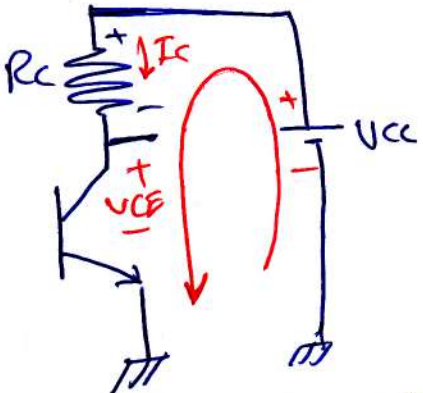
$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B}$$



From the output loop:-

$-V_{CC} + I_C R_C + V_{CE} = 0$

$$\Rightarrow V_{CE} = V_{CC} - I_C R_C$$

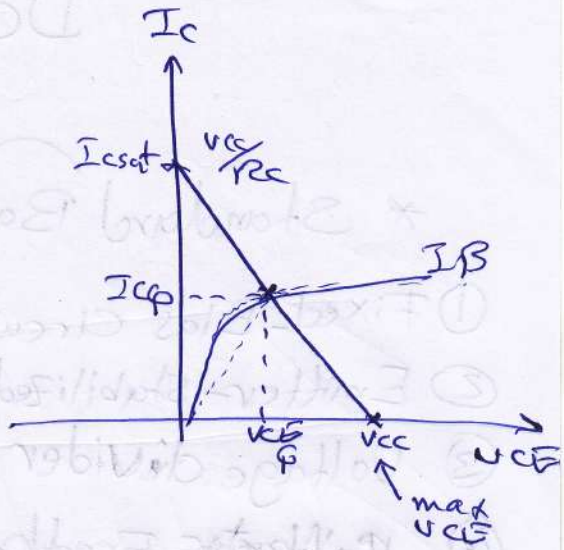


For Dc load line analysis :-

At cutoff $V_{CE} = V_{cc}\Big|_{I_c=0}$

At Saturation region

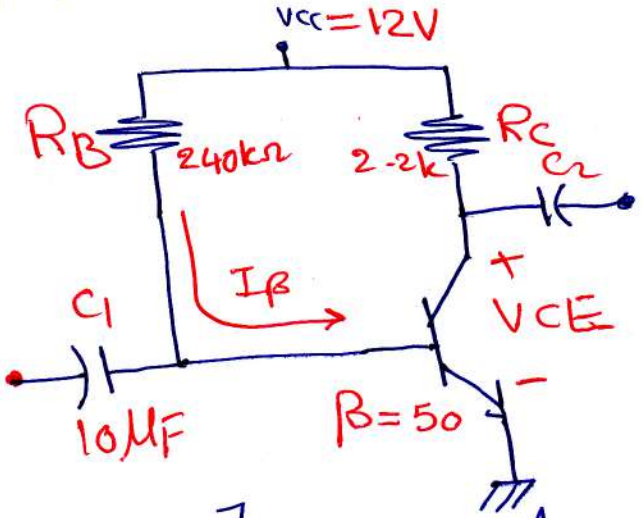
$$I_c = \frac{V_{cc}}{R_c}\Big|_{V_{CE}=0}$$



For an optimum design $V_{CEQ} = \frac{1}{2} V_{cc}$

$$I_{CQ} = \frac{1}{2} I_{C\,Sat} = \frac{V_{cc}}{2R_c}$$

Ex Determine the following parameters for the Fixed-bias Configuration



(a) I_{BQ} and I_{CQ}

(b) V_{CEQ}

(c) V_B and V_C

(d) V_{BC}

Solution (a) $I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{240K} = 47.08\mu A$

$I_{CQ} = \beta I_{BQ} = 50 * 47.08\mu = 2.35mA$

(b) $V_{CEQ} = V_{CC} - I_{CQ} R_C \Rightarrow V_{CEQ} = 12 - (2.35m)(2.2K)$

$= 6.83V$

(c) $V_B = V_{BE} = 0.7V$

$V_C = V_{CE} = 6.83V$

(d) $V_{BC} = V_B - V_C = 0.7 - 6.83 = -6.13V$

refer to the state of Base-collector Junction Biasing (reversed-biased)

Ex Given the device characteristics of the figure below, determine V_{CC}, R_B, and R_C

Solution

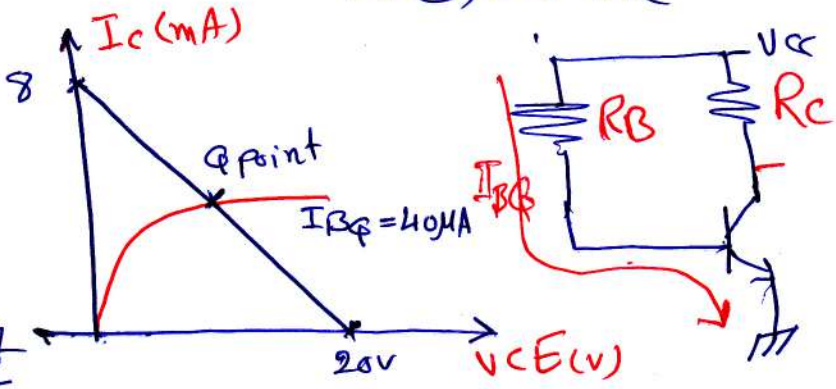
$V_{CC} = 20V$

$I_C = 8 = \frac{V_{CC}}{R_C} \Rightarrow R_C = \frac{V_{CC}}{8mA} \Rightarrow$

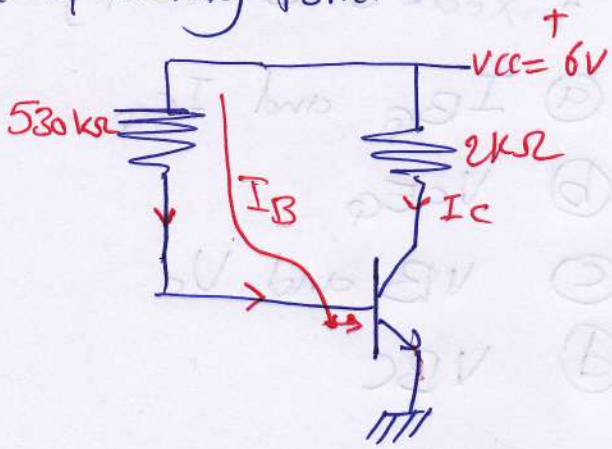
$\therefore R_C = \frac{20}{8m} = 2.5K\Omega$

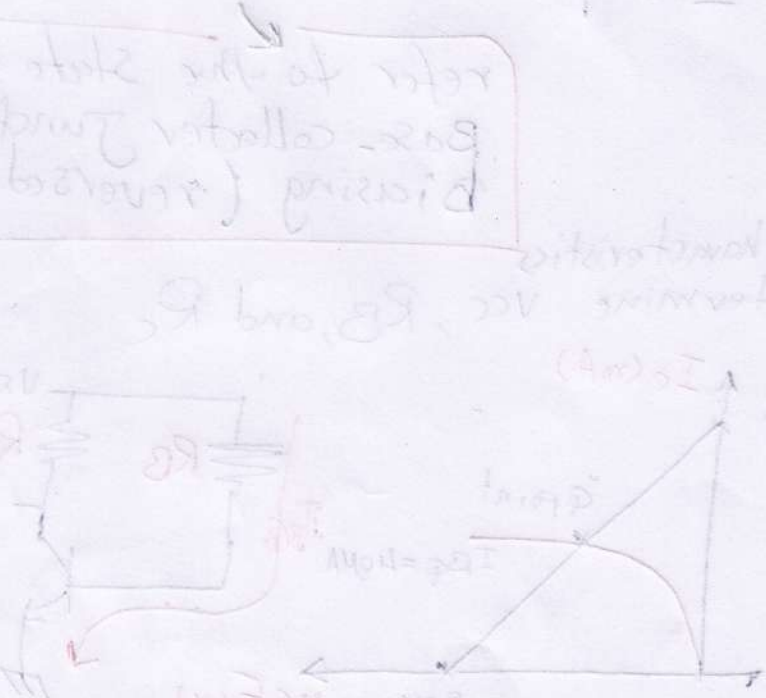
$R_B = \frac{V_{CC} - V_{BE}}{I_{BQ}} = \frac{20 - 0.7}{40\mu A}$

$R_B = 482.5K\Omega$

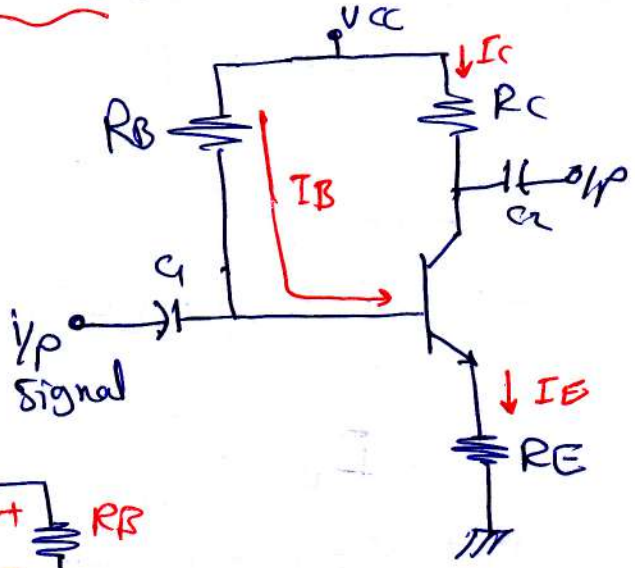


H.W For the circuit shown below, draw the d.c load line and determine the operating point.





② Emitter-Stabilized Bias circuit:

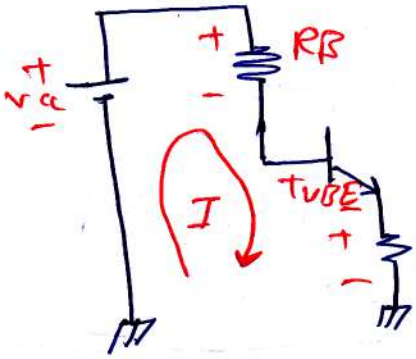


* for the input loop :

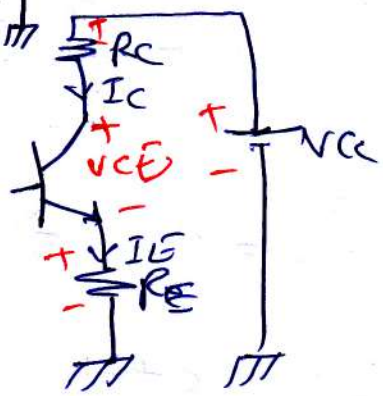
$$-V_{CC} + R_B I_B + V_{BE} + I_E R_E = 0$$

$$I_E = (1+\beta) I_B$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E}}$$



* for the output loop



$$-V_{CC} + R_C I_C + V_{CE} + R_E I_E = 0$$

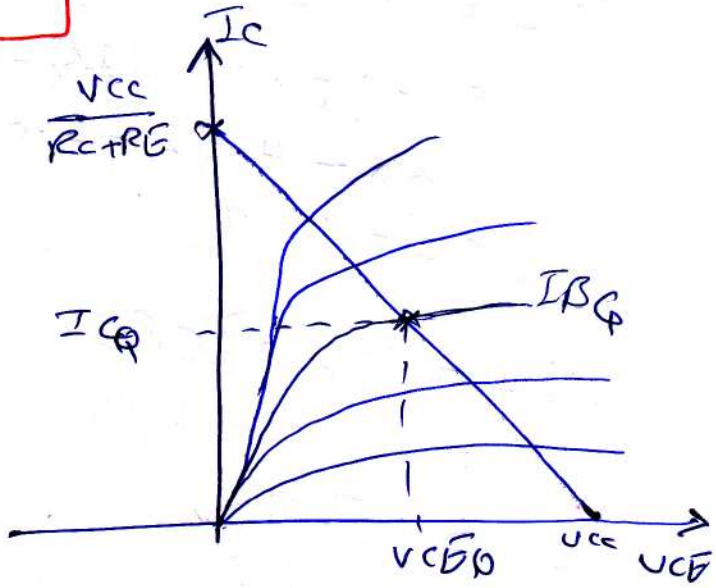
$$I_E \approx I_C$$

$$\therefore \boxed{V_{CE} = V_{CC} - (R_C + R_E) I_C}$$

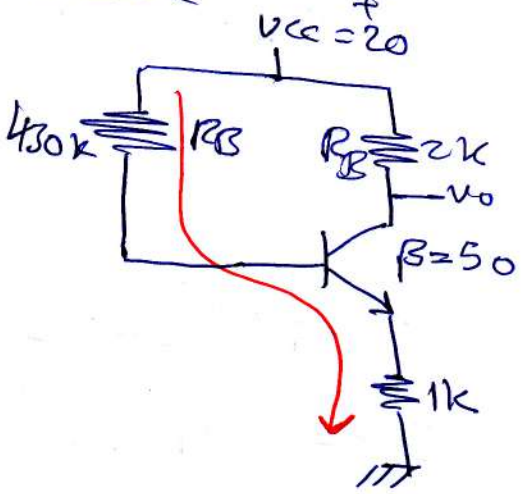
for an optimum design:

$$V_{CEQ} = \frac{V_{CC}}{2}$$

$$I_{CQ} = \frac{V_{CC}}{2(R_C + R_E)}$$



Ex For the Emitter-bias cct below determine $I_B, I_C, V_{CE}, V_C, V_E, V_B$ and V_{BC}



Solution:

$$-V_{CC} + R_B I_B + V_{BE} + I_E R_E = 0$$

$$I_E = I_C + I_B$$

$$= \beta I_B + I_B$$

$$\Rightarrow I_E = (1+\beta) I_B$$

$$\therefore -V_{CC} + R_B I_B + V_{BE} + (1+\beta) I_B R_E = 0$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E} = \frac{20 - 0.7}{430k + (51 \times 1k)} = \frac{19.3}{481k} = 40.1\mu A$$

$$I_C = \beta I_B \Rightarrow I_C = 50 * 40.1\mu A = 2.01\,mA$$

$$I_E = I_C + I_B = 2.01m + 40.1\mu A = 2.05\,mA$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$= 20 - (2.01m)(2K) - (2.05m)(1k)$$

$$= 20 - 4.02 - 2.05$$

$$\Rightarrow \boxed{V_{CE} = 13.93\,V}$$

$$V_C = V_{CE} + I_E R_E$$

$$V_C = 13.93 + (2.05)$$

$$\boxed{V_C = 15.98\,V}$$

$$V_E = V_{CC} - V_{CE} \quad \text{or} \quad V_E = I_E R_E$$

$$V_E = 15.98 - 13.93$$

$$\boxed{V_E = 2.05\,V}$$

$$V_B = V_{BE} + V_E$$

$$V_B = 0.7 + 2.05$$

$$\boxed{V_B = 2.09\,V}$$

$$V_{BC} = V_B - V_C \Rightarrow V_{BC} = 2.09 - 15.98 \Rightarrow V_{BC} = -13.89\,V$$

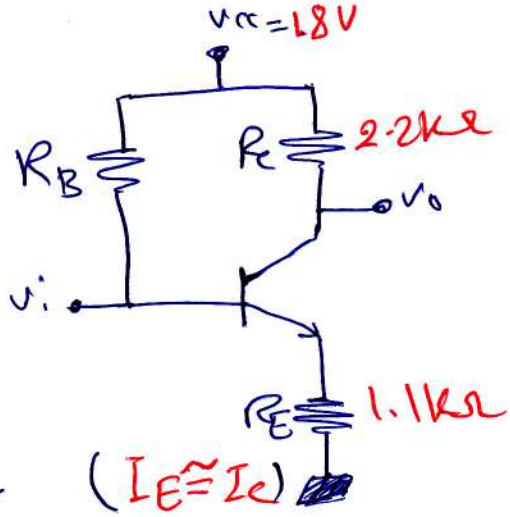
Ex For the circuit shown below:

(a) Draw the load line

(b) for a Q-point at the intersection of the load line with a base current of 15μA, find the values of I_{CQ} and V_{CEQ}.

(c) Determine the β_{DC} at the Q-point.

(d) find the value of R_B



Solution

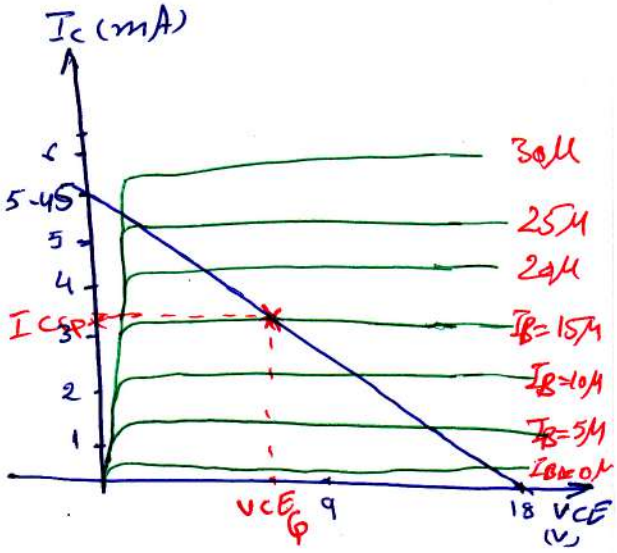
(a) Two points on the characteristics are required to draw the load line

At $V_{CE}=0$: $V_{CC} = I_C R_C + I_E R_E + V_{CE}$

$\Rightarrow V_{CC} = I_C(R_C+R_E) + V_{CE}$ $(I_E \cong I_C)$

when $V_{CE}=0 \Rightarrow V_{CC} = I_C(R_C+R_E) \Rightarrow I_C = \frac{V_{CC}}{R_C+R_E} = \frac{18}{3.3k} = 5.45mA$

At $I_C=0mA$: $V_{CE} = V_{CC} = 18V$



(b) $I_{CQ} \cong 3.3mA$

$V_{CEQ} \cong 7.5V$

(c) $\beta_{DC} = \frac{I_{CQ}}{I_{BQ}} = \frac{3.3mA}{15\mu A} = 220$

(d) $R_B = ?$

$V_{CC} = R_B I_B + V_{BE} + R_E I_E$

$V_{CC} = [R_B + R_E(1+\beta)] I_B + V_{BE}$

$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E}$

$I_E = I_C + I_B$

$= \beta I_B + I_B$

$= (1+\beta) I_B$

$\Rightarrow 15\mu = \frac{18-0.7}{R_B(1+220)(1.1k)}$

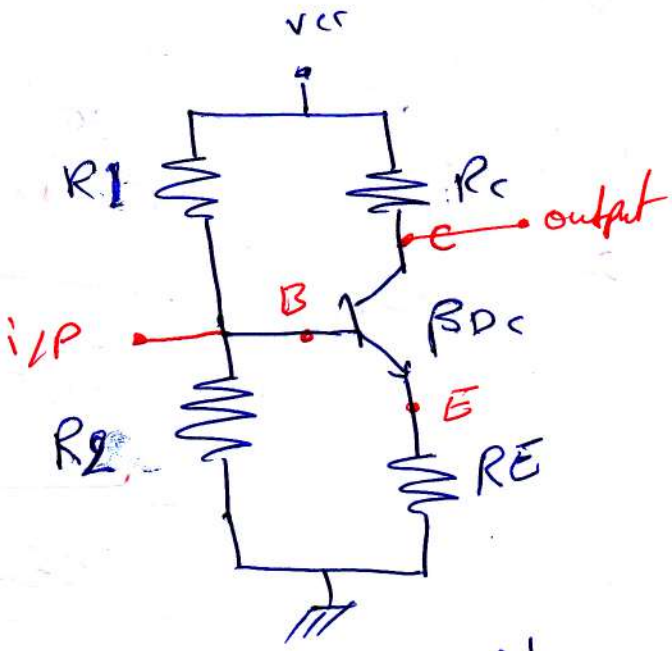
$\Rightarrow R_B = 910k\Omega$

③ Voltage-Divider Bias

There are two methods that can be applied to analyze the voltage divider configuration

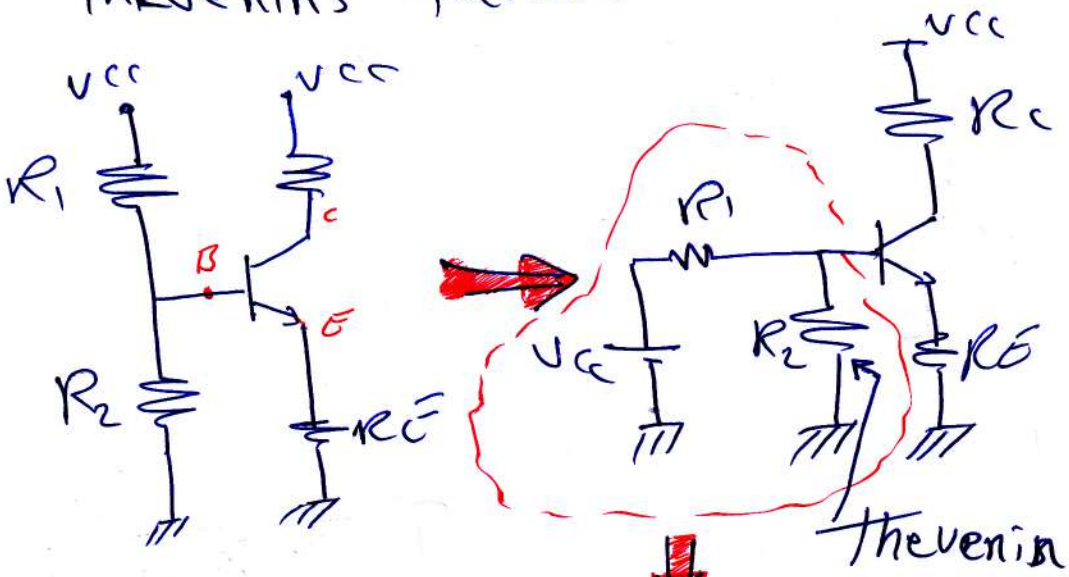
① The exact method

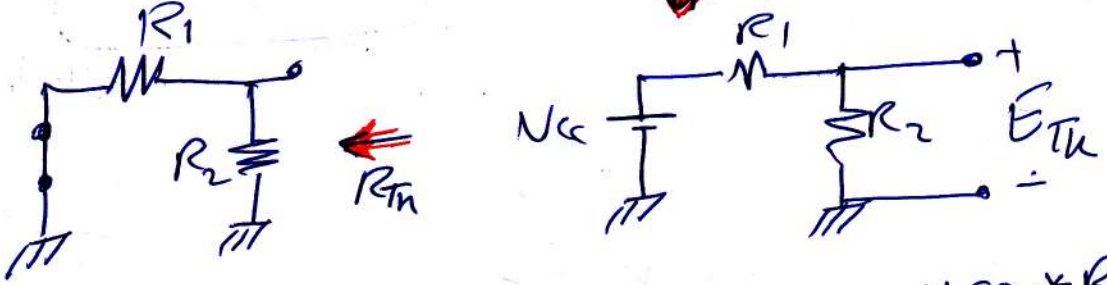
② The approximate method



① The exact analysis

The input side of the Voltagedivider circuit can be redrawn as circuit below then apply "Thevenin's theorem"





$$\therefore R_{Th} = R_1 // R_2 \qquad E_{Th} = V_{R_2} = \frac{V_{cc} * R_2}{R_1 + R_2}$$

③ Voltage-Divider Bias

There are two methods that can be applied to analyze the voltage divider configuration

① The exact method

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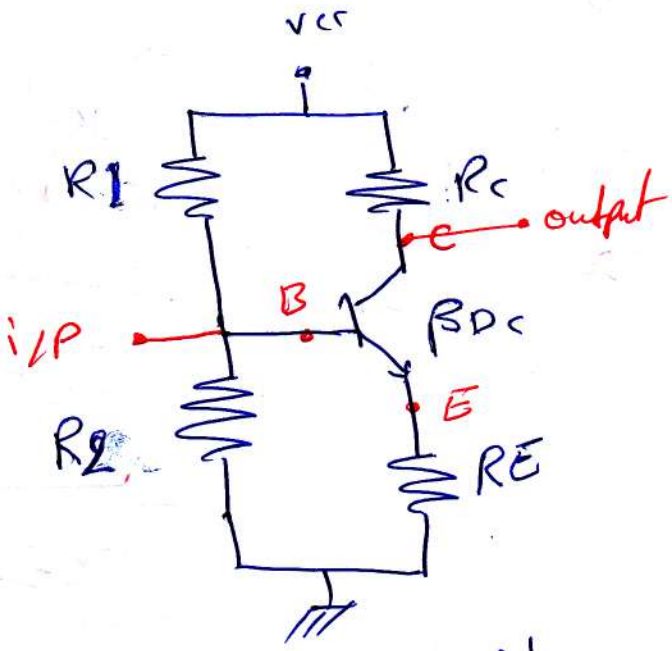

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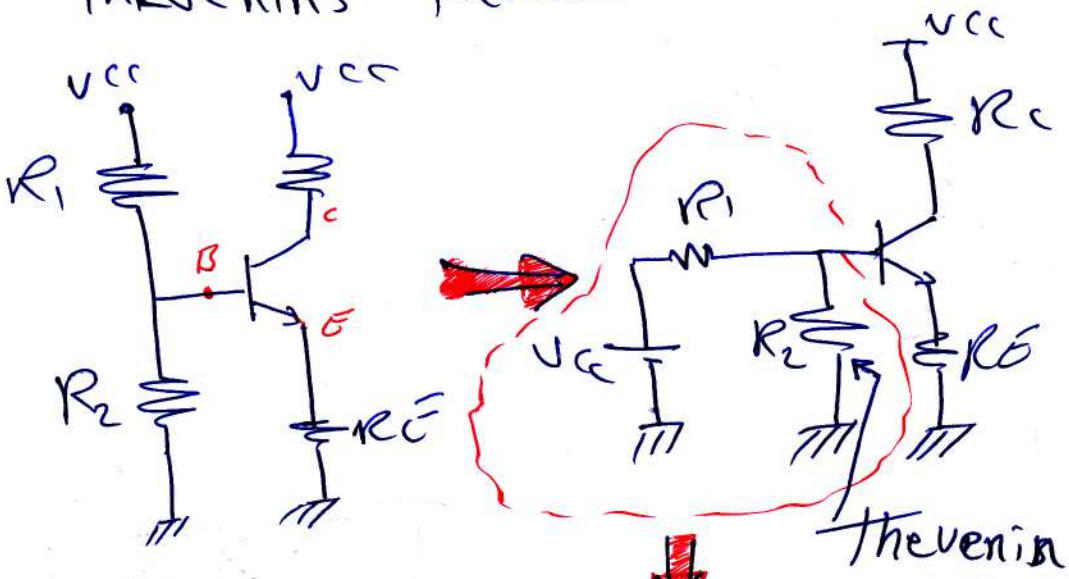
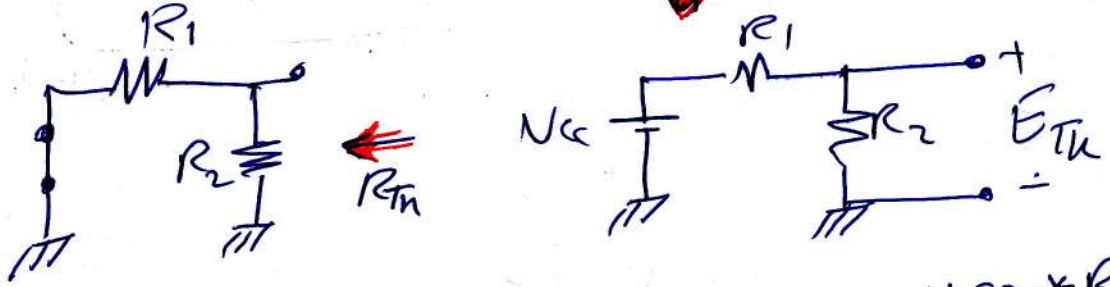
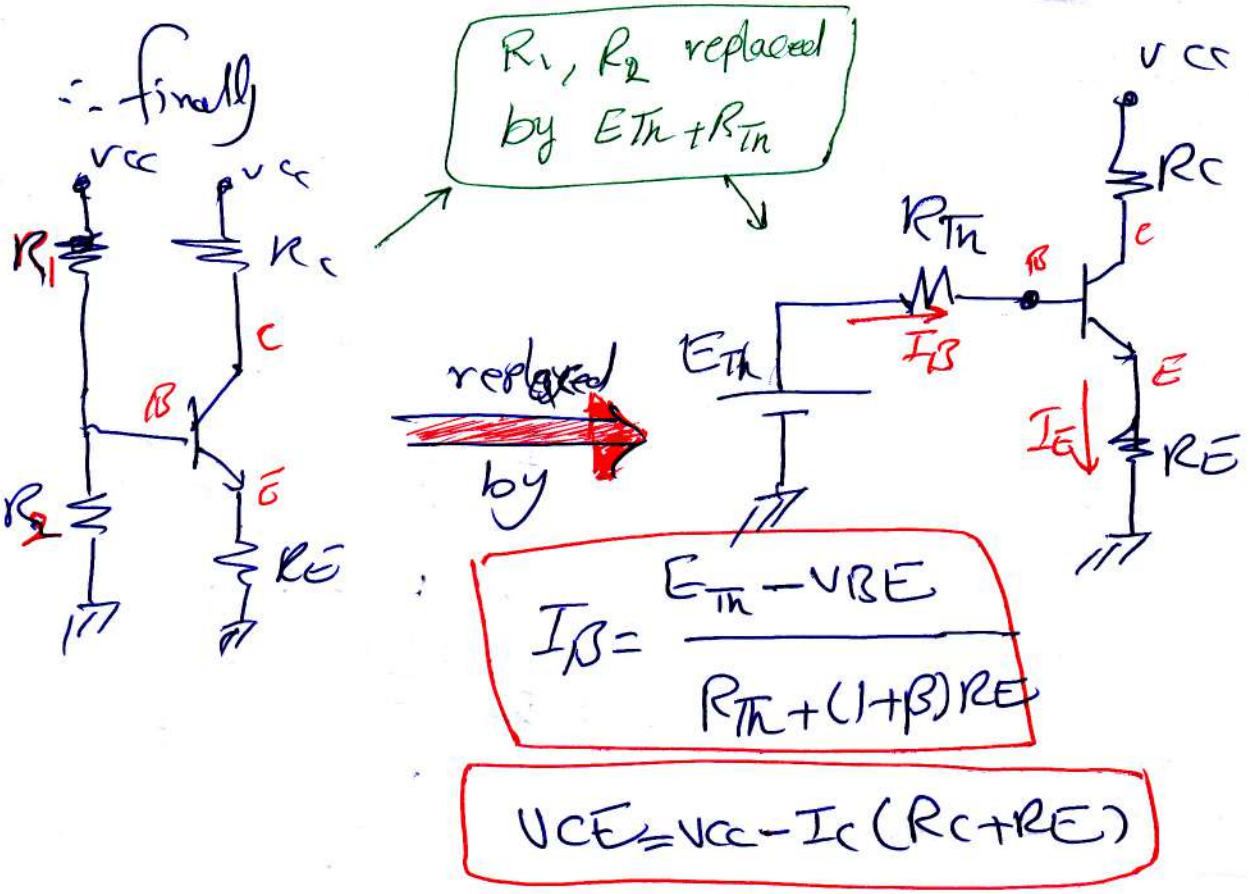




$$\therefore R_{Th} = R_1 // R_2 \qquad E_{Th} = V_{R_2} = \frac{V_{cc} * R_2}{R_1 + R_2}$$

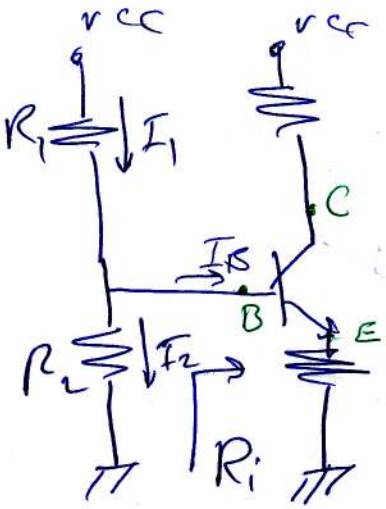
∴ finally

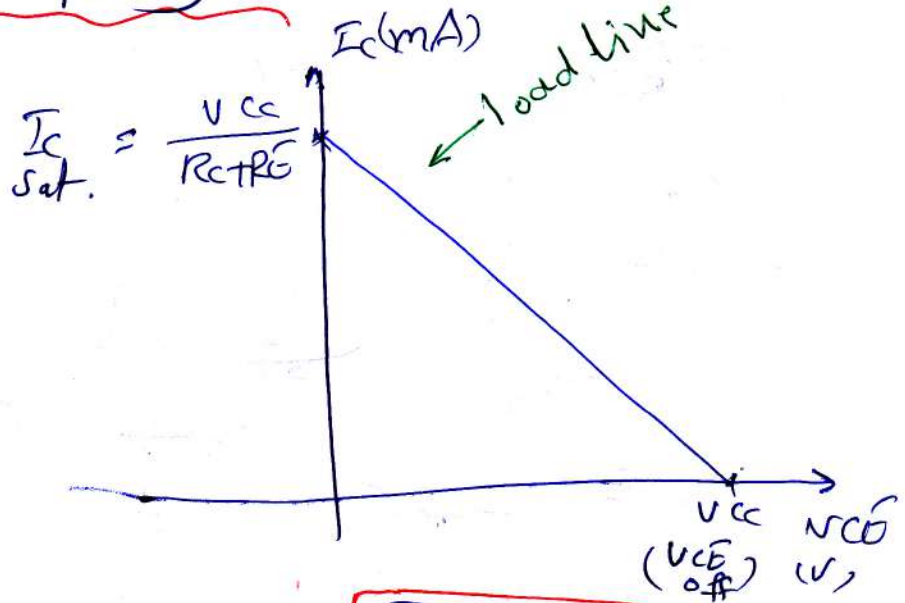


$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (1+\beta) R_E}$$

$$V_{CE} = V_{cc} - I_c (R_c + R_E)$$

2 Approximate Analysis





$\beta RE \geq 10 R_2$

$R_i = (1+\beta) R_E \approx \beta R_E$

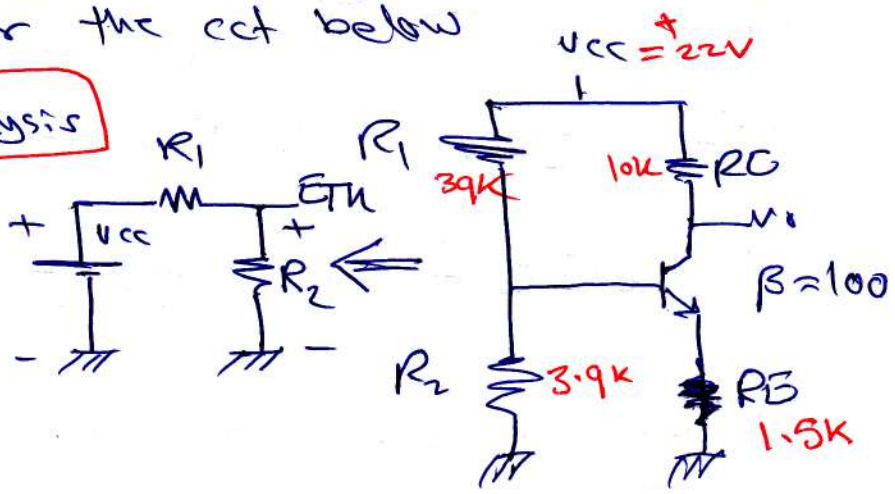
$R_i \gg R_2$

Therefore $I_1 \approx I_2$ (I_B very small current)

$$\therefore V_B = \frac{V_{cc} R_2}{R_1 + R_2}, \quad V_E = V_B - V_{BE}, \quad I_E = \frac{V_E}{R_E}$$

$$I_E \cong I_{CQ}, \quad V_{CEQ} = V_{cc} - I_c (R_c + R_E)$$

Ex Determine the dc bias voltage V_{CE} and the current I_C for the cct below



Solution Exact analysis

$$R_{Th} = R_1 // R_2$$

$$= 39k // 3.9k$$

$$= \frac{(39k)(3.9k)}{(39k)+(3.9k)}$$

$$\therefore \boxed{R_{Th} \simeq 3.55k\Omega}$$

$$E_{Th} = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{(22)(3.9k)}{39k + 3.9k} = 2V \quad \therefore \boxed{E_{Th} = 2V}$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (1+\beta) R_E} \Rightarrow I_B = \frac{2 - 0.7}{3.55k + (101)(1.5k)} = 8.38\mu A$$

$$\therefore \boxed{I_B = 8.38\mu A}$$

$$I_C = \beta I_B = (100)(8.38\mu) \Rightarrow \boxed{I_C = 0.84mA}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) = 22 - (0.84m)(10k + 1.5k)$$

$$\therefore \boxed{V_{CE} = 12.34V}$$

Now **Approximate analysis**

Condition $\boxed{\beta R_E \geq 10 R_2}$

Important Condition

$$(100)(1.5k) \geq 10(3.9k)$$

$$150k \geq 39k$$

$$\therefore \boxed{\text{Satisfied}}$$

$$V_B = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{(3.9k)(22)}{39k + 3.9k} = 2V \quad \therefore \boxed{V_B = 2V}$$

$$V_E = V_B - V_{BE} \Rightarrow V_E = 2 - 0.7 = 1.3V \quad \therefore \boxed{V_E = 1.3V}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{1.3}{1.5k} = \boxed{0.867\,mA}$$

$$V_{CEQ} = V_{CC} - I_C(R_C + R_E) = 22 - (0.867m)(10k + 1.5k)$$

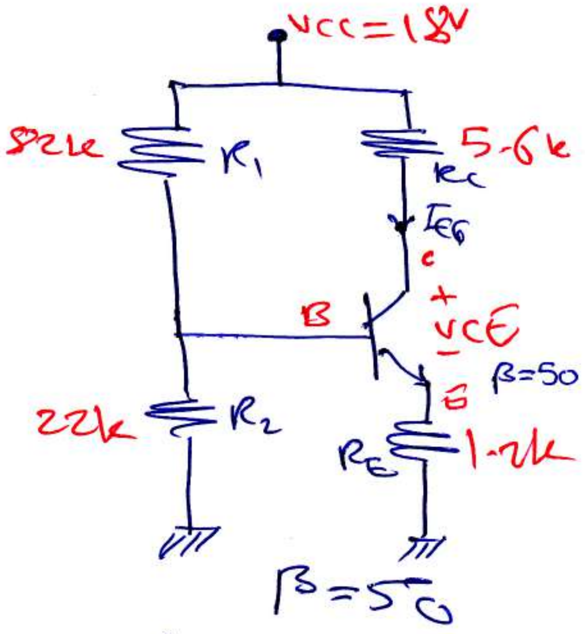
$$\Rightarrow \boxed{V_{CEQ} = 12.03V}$$

Comparing

	V_{CEQ}	I_{CQ}
Exact analysis ⇒	12.34V	0.84 mA
Approximate analysis ⇒	12.03V	0.867 mA

The results for I_{CQ} and V_{CEQ} are certainly close

Ex Determine the levels of I_{CQ} and V_{CEQ} for the voltage divider configuration of figure below, using the exact and approximate techniques and compare solutions.



Solution ① Exact analysis :-

$\beta R_E \geq 10 R_2$ Condition

$50 * (1.2k) \ngeq 10(22k)$

$60k \ngeq 220k$
(not satisfied)

$$R_{Th} = R_1 \parallel R_2 = \frac{(82k)(22k)}{(82k)+(22k)} = 17.35\,k\Omega$$

$$E_{Th} = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{(18)(22k)}{(82k)+(22k)} = 3.81\,V$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (1+\beta)R_E} = \frac{3.81 - 0.7}{17.35k + (51)(1.2k)} = 39.6\,\mu A$$

$$I_{CQ} = \beta I_B = (50)(39.6\mu) = 1.98\,mA$$

$$V_{CEQ} = V_{CC} - I_C (R_C + R_E) = 4.54\,V$$

② Approximate analysis :-

$V_B = E_{Th} = 3.81\,V$

$V_E = V_B - V_{BE} = 3.11\,V$

$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{3.11}{1.2k} = 2.59\,mA$, $V_{CEQ} = V_{CC} - I_C (R_C + R_E) = 3.88\,V$

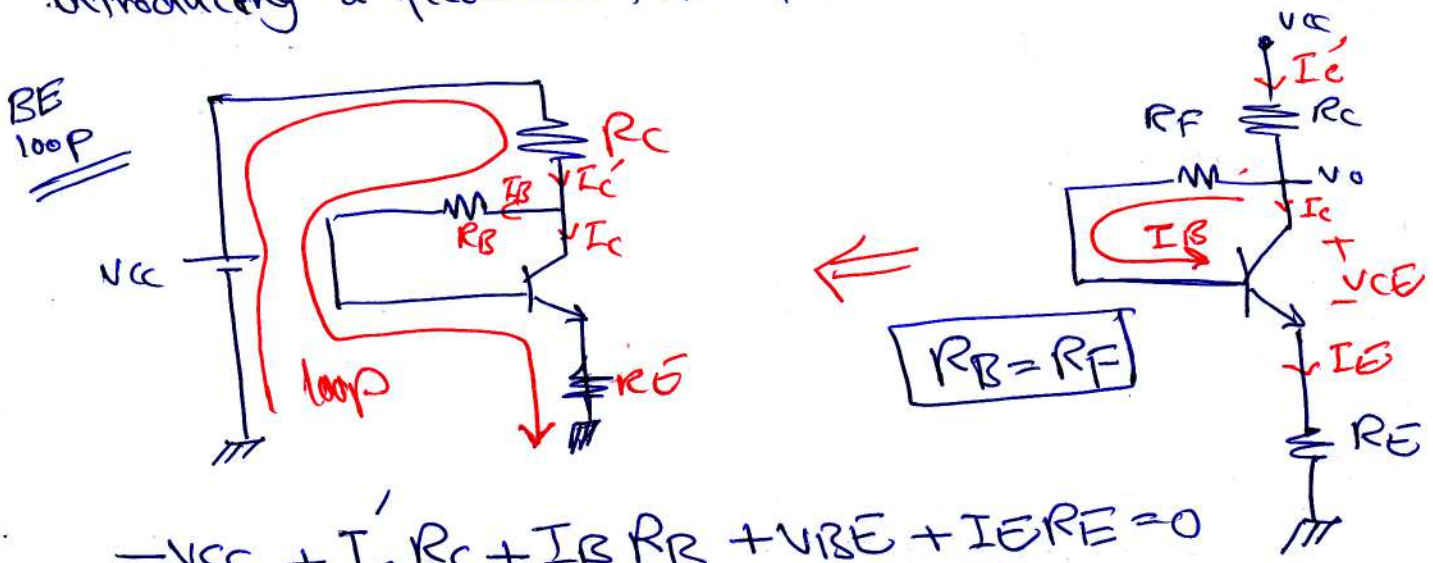
From the results

	I_{CQ}	V_{CEQ}
Exact	1.98mA	4.54V
approximate	2.59mA	3.88V

*من خلال مشاهدة النتائج للطريقتين
يتبين ان هناك فرق واضح بينهما
وهذا يعود الى عدم تحقق الشرط
الاساسي لاستخدام طريقة التقريب
وهو $\beta R_E \geq 10 R_2$
في الحل بدقة لذا exact.

(4) Collector Feedback Bias :-

An Improved level of stability can also obtained by introducing a feedback path from collector to base as shown



$$-V_{CC} + I'_C R_C + I_B R_B + V_{BE} + I_E R_E = 0$$

$$\Rightarrow V_{CC} = I'_C R_C + I_B R_B + V_{BE} + I_E R_E$$

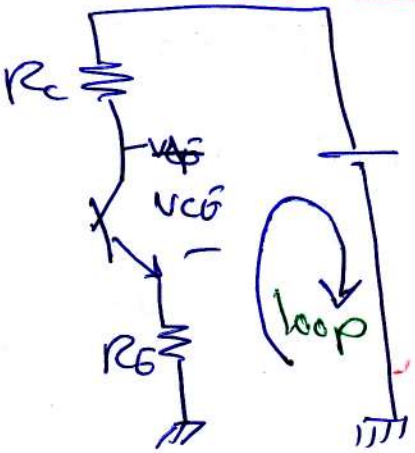
$$I'_C = I_C + I_B \cong I_C \cong \beta I_B \cong I_E$$

$$\Rightarrow V_{CC} = \beta I_B R_C + I_B R_B + V_{BE} + \beta I_B R_E$$

$$\therefore \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}} \Rightarrow \boxed{I_C = \frac{V_{CC} - V_{BE}}{\frac{R_B}{\beta} + R_E + R_C}}$$

$I_C = \beta I_B$

BE loop

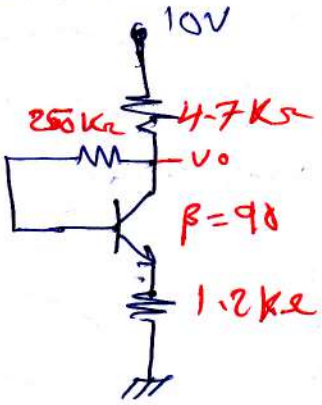


$$-V_{CC} + I_E R_E + I'_C R_C + V_{CE} = 0$$

$\boxed{I'_C \cong I_C}$, and $\boxed{I_E \cong I_C}$

$$\therefore \boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)}$$

Ex Determine I_{CQ} and V_{CEQ} for the circuit below?



Solution :- BE loop :-

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)} = \frac{10 - 0.7}{250k + (90)(4.7k + 1.2k)}$$

$$I_B = 11.91\,\mu A$$

$$\Rightarrow I_C = \beta I_B = 90 * 11.91\,\mu A \Rightarrow I_{CQ} = 1.07\,mA$$

CE loop :-

$$V_{CEQ} = V_{CC} - I_C(R_C + R_E)$$

$$= 10 - (1.07m)(4.7k + 1.2k) \Rightarrow V_{CEQ} = 3.79\,V$$

Ex Repeat Previous Example using a beta of 135 (50% increase)

Solution :-

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)} = \frac{10 - 0.7}{250k + 135(5.9k)} = 8.89\,\mu A = I_B$$

$$I_{CQ} = \beta I_B = 135 * 8.89\,\mu A \Rightarrow I_{CQ} = 1.2\,mA$$

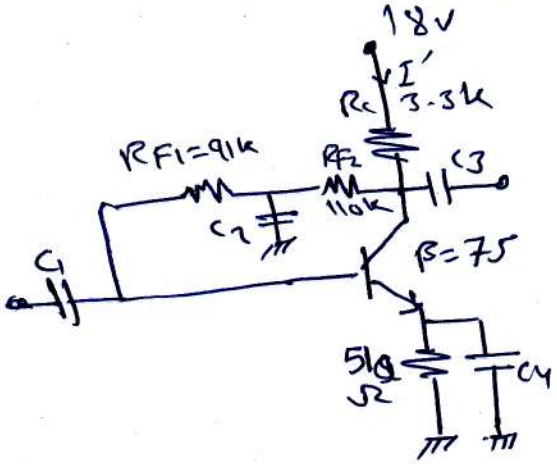
$$V_{CEQ} = V_{CC} - I_C(R_C + R_E) = 10 - (1.2m)(5.9k) \Rightarrow V_{CEQ} = 2.92$$

level of β increased 50%

" " I_{CQ} " 12.1%

" " V_{CE} decreased 20.9%

Ex Determine the d.c level of I_B and V_C for the circuit below?



Solution

$$I_B = \frac{V_{CC} - V_{BE}}{(R_{F1}+R_{F2}) + \beta(R_C + R_E)}$$

$$= \frac{18 - 0.7}{(91k + 110k) + (75)(3.3k + 510)}$$

$$\Rightarrow \boxed{I_B = 35.5\,\mu A}$$

$$\Rightarrow I_C = \beta I_B \Rightarrow I_C = 75 * 35.5\,\mu A \Rightarrow \boxed{I_C = 2.66\,mA}$$

$V_{CE_Q} =$

$$V_C = V_{CC} - I' R_C \cong V_{CC} - I_C R_C$$

$$\Rightarrow V_C = 18 - (2.66mA)(3.3k) \Rightarrow \boxed{V_C = 9.22V}$$

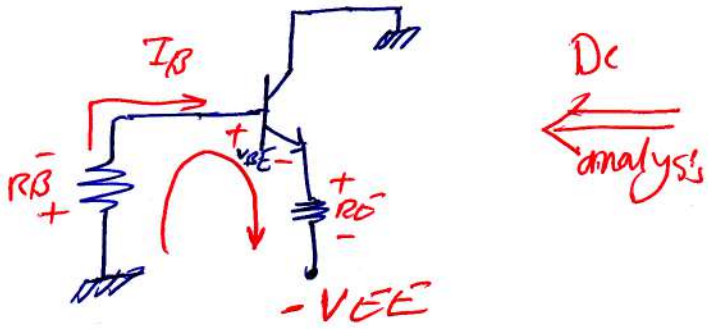
Ex

Common-Collector Configuration (C.C)

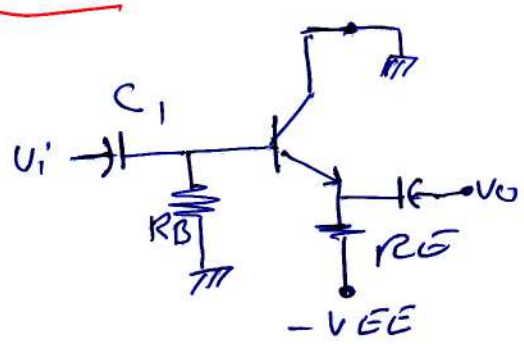
The second transistor configuration is the Common-Collector configuration. Its called Emitter-follower EF.

The Common-Collector (C.C) is used primarily for impedance matching purposes since it has a high input impedance and Low output impedance.

Emitter follower Biasing



Dc analysis



$$I_B R_B + V_{BE} + R_E I_E - V_{EE} = 0$$

$$I_E = I_B(1+\beta)$$

$$\Rightarrow I_B(R_B + R_E + \beta R_E) = V_{EE} - V_{BE}$$

$$\Rightarrow \boxed{I_B = \frac{V_{EE} - V_{BE}}{R_B + R_E(1+\beta)}}$$

$$\boxed{V_{CE} = V_{EE} - I_E R_E}$$

Ex Determine the V_{CEQ} and I_{EQ} for the circuit below

Solution

$$I_B = \frac{V_{EE} - V_{BE}}{R_B + R_E(1+\beta)} = \frac{20 - 0.7}{240k + (2k)(91)}$$

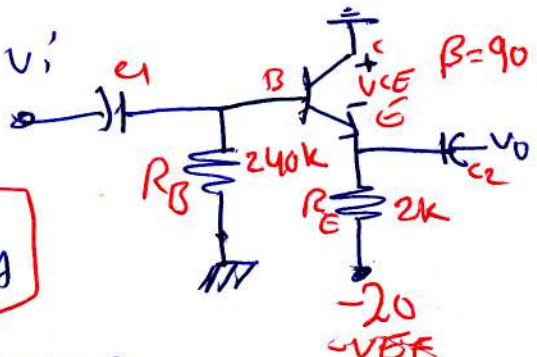
$$\Rightarrow \boxed{I_B = 45.73\,\mu A}$$

$$\boxed{I_{EQ} = (\beta+1) I_B \quad I_{EQ} = 4.16\,mA}$$

$$V_{CEQ} = V_{EE} - I_E R_E$$

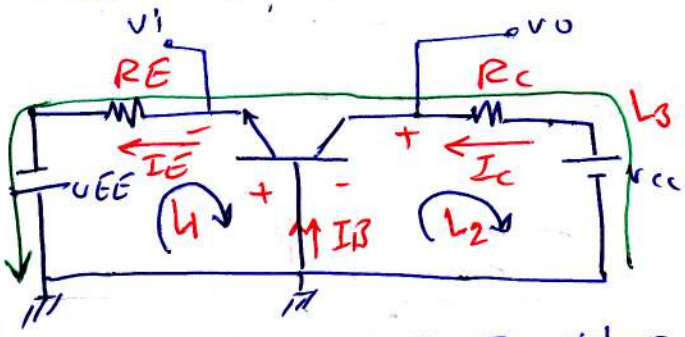
$$= V_{EE} - (1+\beta) I_B R_E = 20 - (91)(45.73)(2k)$$

$$\Rightarrow \boxed{V_{CEQ} = 11.68\,V}$$

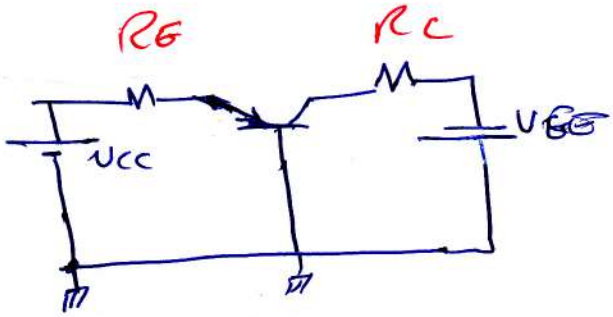


Common-Base Configuration (C.B.)

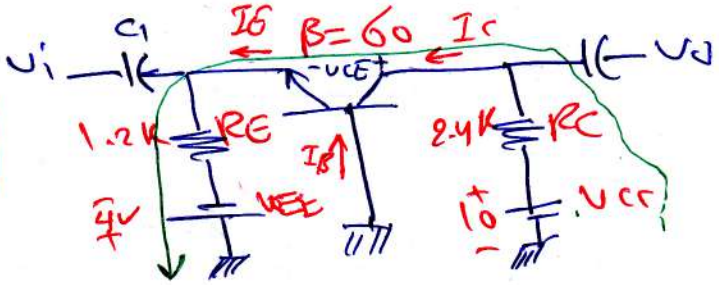
When a transistor is connected with the base as the common or grounded terminal, its called a common base Con



npn C.B Transistor



Ex Determine the currents I_E and I_B and the voltages V_{CE} and V_{CB} for the C.B configuration of figure below



Solution

Applying KVL (input loop)

$$V_{EE} - I_E R_E - V_{BE} = 0$$

$$\therefore I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{4 - 0.7}{1.2k} \Rightarrow \boxed{I_E = 2.75\,mA}$$

$$I_B = \frac{I_E}{1+\beta} = \frac{2.75m}{1+60} \Rightarrow \boxed{I_B = 45.08\,\mu A}$$

output loop This loop will be outside of the network

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E - V_{EE} = 0$$

$$\Rightarrow V_{CE} = V_{CC} + V_{EE} - I_C R_C - I_E R_E \quad , \quad \boxed{I_E \approx I_C}$$

$$\Rightarrow V_{CE} = V_{CC} + V_{EE} - I_E (R_C + R_E)$$

$$= 10 + 4 - (2.75m)(2.4k + 1.2k) \Rightarrow \boxed{V_{CE} = 4.1\,V}$$

$$V_{CB} = V_{CC} - I_C R_C = 10 - (60)(45.08\mu)(2.4k)$$

$$\boxed{V_{CB} = 3.51\,V}$$

In the DC mode the levels of I_C and I_E due to the majority carriers are related by a quantity called **alpha, α_{DC}** and defined by the following equation

$$\alpha_{DC} = \frac{I_C}{I_E}$$

I_C: output current
I_E: input current

$$I_C \cong I_E \Rightarrow \alpha_{DC} \cong 1$$

Practically
$0.900 \leq \alpha_{DC} \leq 0.998$

Ex
Solution
Calculate the value of α_{DC} in previous example?

$I_E = 2.75\ mA$

$I_B = 45.08\ \mu A \Rightarrow I_C = \beta I_B = 60 * 45.08\mu = 2.705mA$

$$\Rightarrow \alpha_{DC} = \frac{I_C}{I_E} = \frac{2.705mA}{2.75\ mA} = 0.98$$