The Bipolar Junction Transistor (BJT)

Introduction

The **transistor**, derived from **transfer resistor**, is a three terminal device whose resistance between two terminals is controlled by the third. The term bipolar reflects the fact that there are two types of carriers, holes and electrons which form the currents in the transistor. If only one carrier is employed (electron or hole), it is considered a unipolar device like field effect transistor (FET).

The transistor is constructed with three doped semiconductor regions separated by two pn junctions. The three regions are called **Emitter (E), Base (B), and Collector (C).**

Physical representations of the two types of BJTs are shown in Figure (1–1). One type consists of two n -regions separated by a p-region (npn), and the other type consists of two p-regions separated by an n-region (pnp).

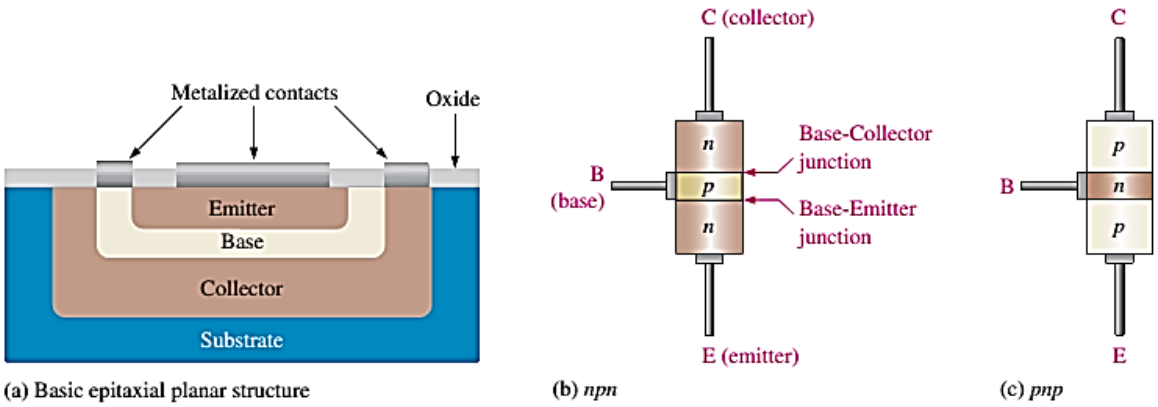


Figure (1-1) Transistor Basic Structure

The outer layers have widths much greater than the sandwiched p- or n-type layer. The doping of the sandwiched layer is also considerably less than that of the outer layers (typically, 10:1 or less).

This lower doping level decreases the conductivity of the base (increases the resistance) due to the limited number of "free" carriers. Figure (1-2) shows the schematic symbols for the npn and pnp transistors

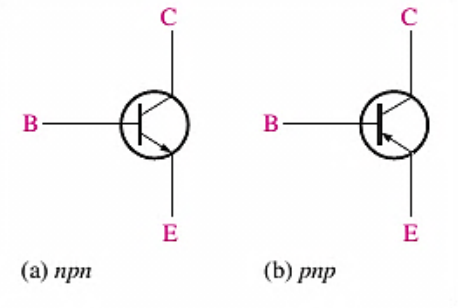


Figure (1-2) standard transistor symbol

Transistor operation

Objective: understanding the basic operation of the transistor and its naming

In order for the transistor to operate properly as an amplifier, the two pn junctions must be correctly biased with external voltages. The basic operation of the transistor will now be described using the npn transistor. The operation of the pnp transistor is the same as for the npn except that the roles of the electrons and holes, the bias voltage polarities and current directions are all reversed.

Figure (1-3) shows both the pnp and npn transistors with the proper DC biasing. Notice that in both cases the **base-emitter junction is forward biased and the base-collector is reverse biased**

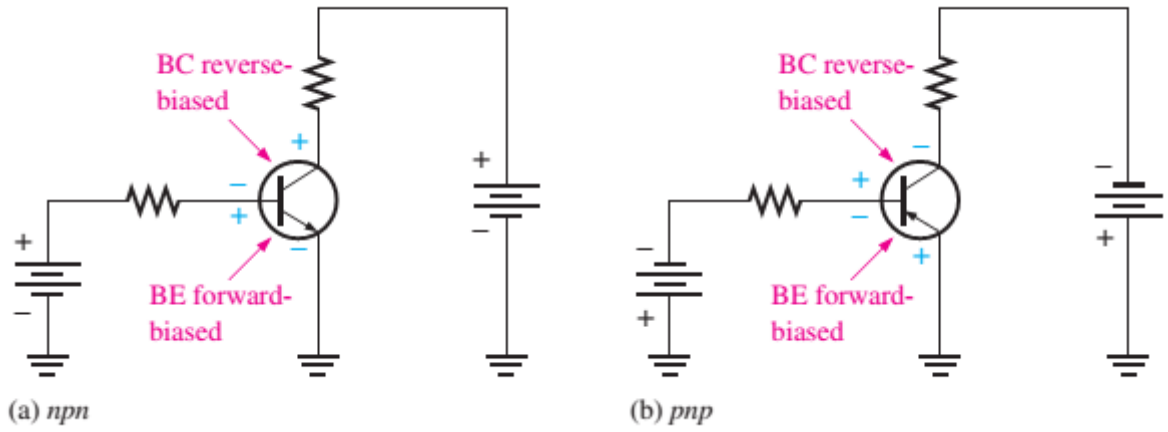


Figure (1-3) transistor forward reverse bias

Before the transistor is biased there are two depletion regions. What is happens inside the transistor when it is forward and reverse bias is the forward biased from the base to emitter narrows the BE depletion region as shown in figure (1-4). This will result in a heavy flow

of majority carriers (electrons) from the emitter to the base as indicated by the wide arrow.

The base region is slightly doped and very thin so that it has a very limited number of holes. Thus, only small percentage of all the electrons flowing across the BE junction combine with the available holes. These relatively few recombined electrons will form the small base current (I_B).

The reverse biased from base to collector widens the BC depletion region as shown in figure (1-4). Consider the similarity between this situation and that of the reversed biased diode. Recall that the flow of majority carriers is zero, resulting in only a minority carriers flow. The free electrons move through the collector region, into the external circuit, and then return into the emitter region along with the base current, as indicated. The emitter current is slightly greater than the collector current because of the small base current that splits off from the total current injected into the base region from the emitter.

Transistor currents

Applying Kirchhoff's current law to the transistor of figure (1-4) we obtain

$$I_E = I_B + I_C$$

The collector current comprises two components

$$I_C = I_{C\,majority} + I_{CO\,minority}$$

Those for a pnp transistor notice that the arrow on the emitter inside the transistor symbols points in the direction of conventional current (holes current).

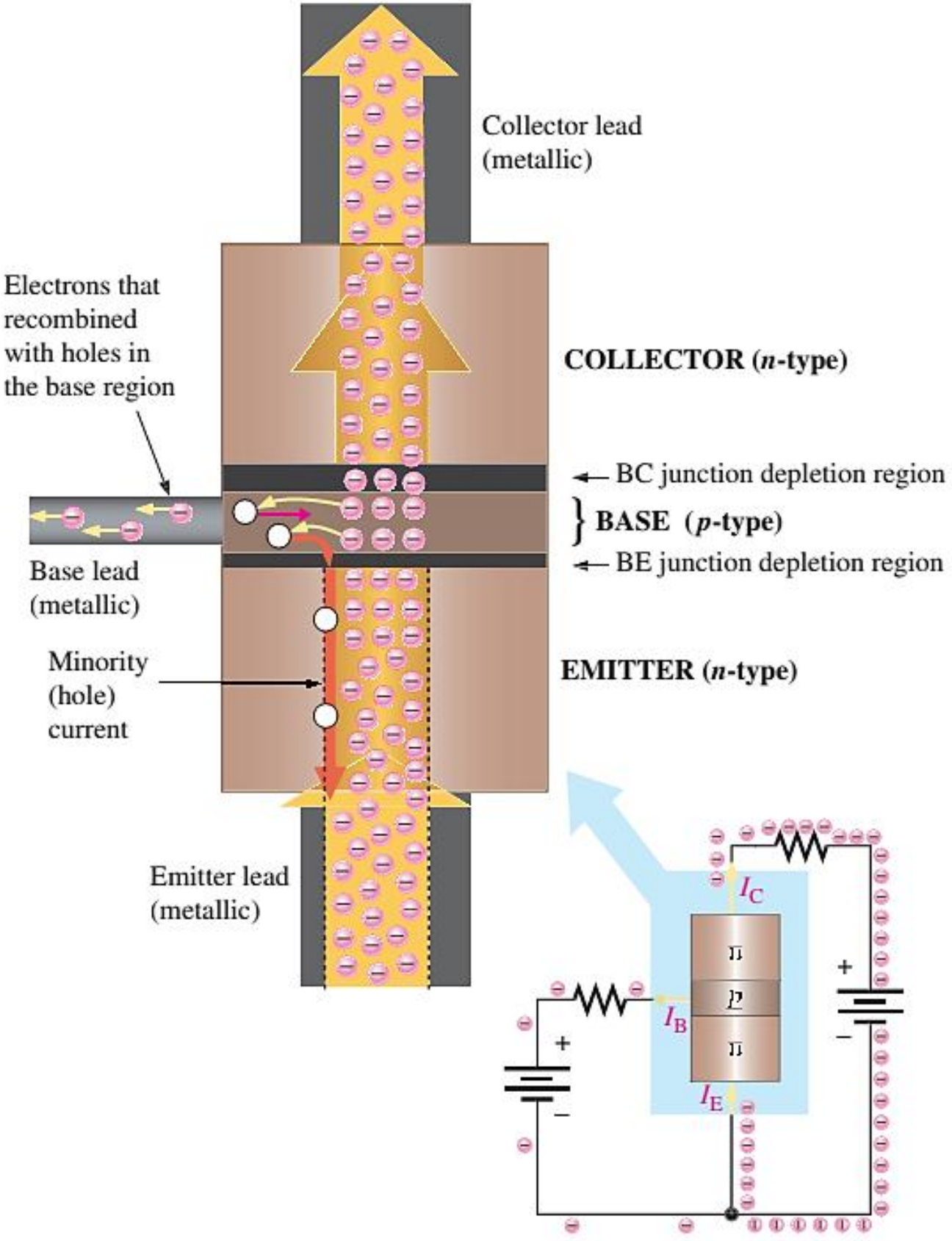


Figure (1-4) transistor operation

Transistor Categories

Manufacturers generally classify bipolar junction transistors into three broad categories:

1- **General-Purpose/Small-Signal Transistors:-** General-purpose/small-signal transistors are generally used for low- or medium-power amplifiers or switching circuits. Figure (1-5) show small signal transistors.

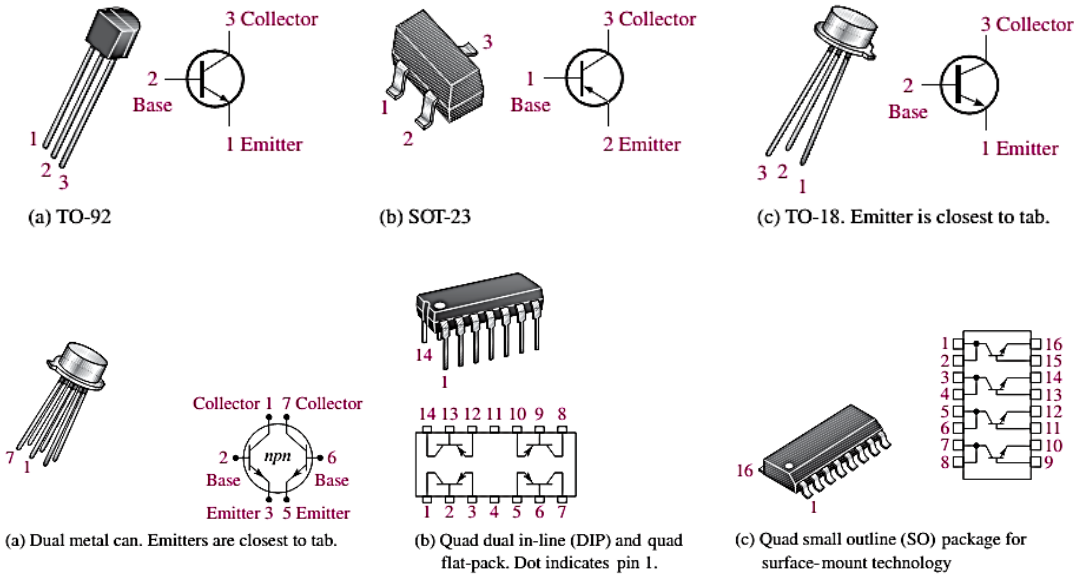


Figure (1-5) Small Signal Transistors

2- **Power Transistors**: - Power transistors are used to handle large currents (typically more than 1 A) and/or large voltages.

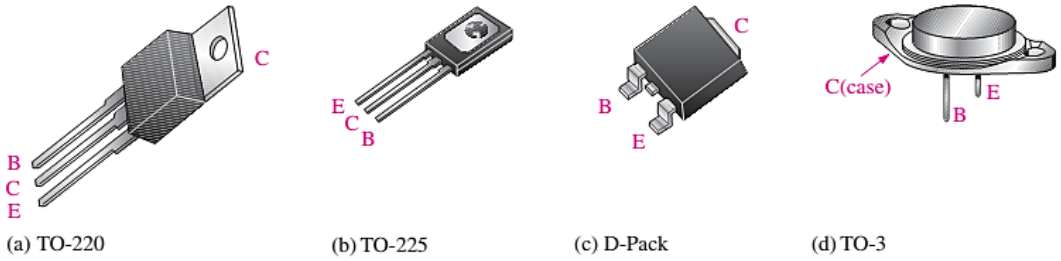


Figure (1-6) Examples of Power Transistors

3- **RF Transistors:** - RF transistors are designed to operate at extremely high frequencies and are commonly used for various purposes in communications systems and other high frequency applications. Figure (1-7) show examples of RF transistors.

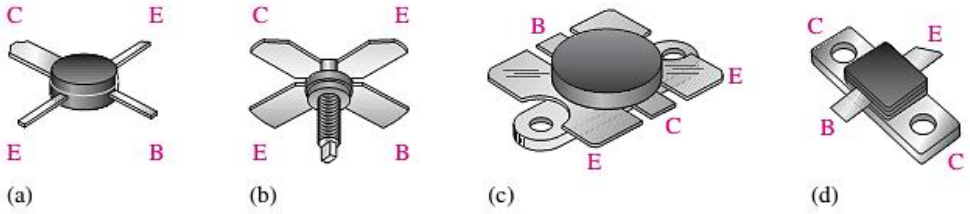


Figure (1-7) show examples of RF transistors

The DMM Diode Test Position

A digital multimeter can be used as a fast and simple way to check a transistor. For this test, you can view the transistor as two diodes connected as shown in Figure (1-8) for both npn and pnp transistors.

An ohmmeter or the resistance scales of DMM can be used to check the state of the transistor. A good diode will show an extremely high resistance (or open) with reverse bias and a very low resistance with forward bias.

A defective open diode will show an extremely high resistance (or open) for both forward and reverse bias.

A defective shorted or resistive diode will show zero or a very low resistance for both forward and reverse bias.

Many digital multimeters (DMMs) have a diode test position that provides a convenient way to test a transistor. In Figure (1-8a), the red (positive) lead of the meter is connected to the base of an npn transistor and the black (negative) lead is connected to the emitter to forward-bias the base-emitter junction.

If the junction is good, you will get a reading of between approximately 0.6 V and 0.8 V, with 0.7 V being typical for forward bias.

In Figure (1-8b), the leads are switched to reverse-bias the base-emitter junction, as shown. If the transistor is working properly, you will typically get an OL indication. The process just described is repeated for the base-collector junction as shown in Figure (1-8c) and (d).

For a pnp transistor, the polarity of the meter leads are reversed for each test.

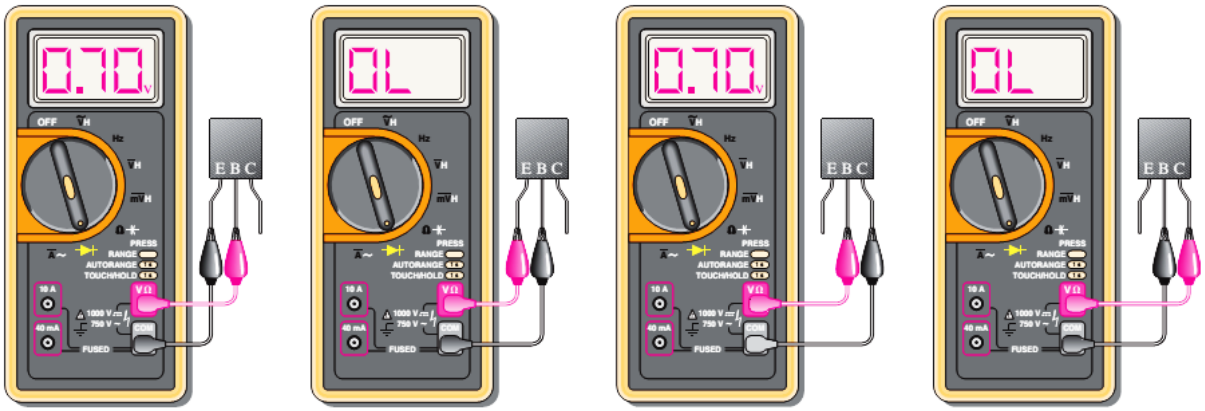


Figure (1-8) Typical DMM test of a properly functioning npn transistor. Leads are reversed for a pnp transistor.

Transistor configurations

Objective: shows the transistor connection configurations and the difference between them

As we have seen, the bipolar transistor is a three-terminal device. Three basic single transistor amplifier configurations can be formed; depending on which of the three transistor terminals is used as signal ground **(i.e. which terminal is common to both the input and the output side of the configuration)**. These three basic configurations are appropriately called **common emitter, common collector (emitter follower), and common base**. Figure (1-9) shows the three basic configurations for npn transistor.

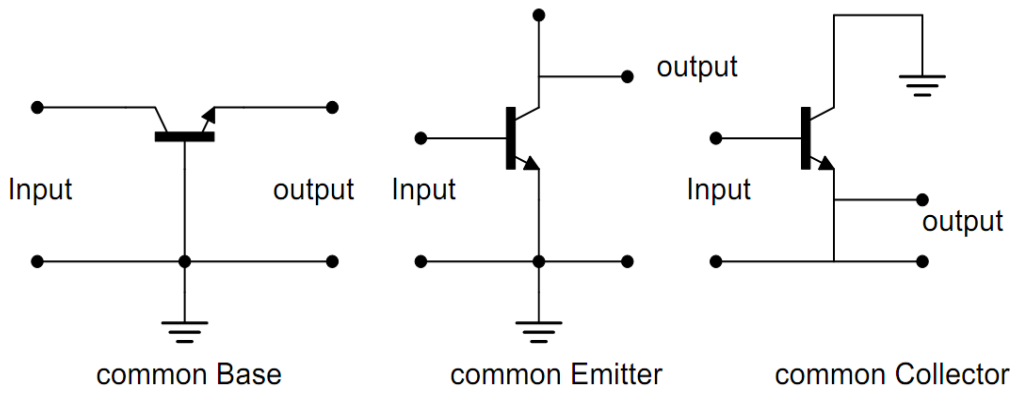


Figure (1-9) transistor configuration

Common Emitter Configuration

Figure (1-10) shows a common-emitter configuration for **pnp** and **npn** transistors. The common-emitter **(CE)** configuration has the emitter as the common terminal, or ground, to an ac signal. V_{BB} forward-biases the base-emitter junction, and V_{CC} reverse-biases the base-collector junction. This configuration is the most frequently encountered transistor configuration.

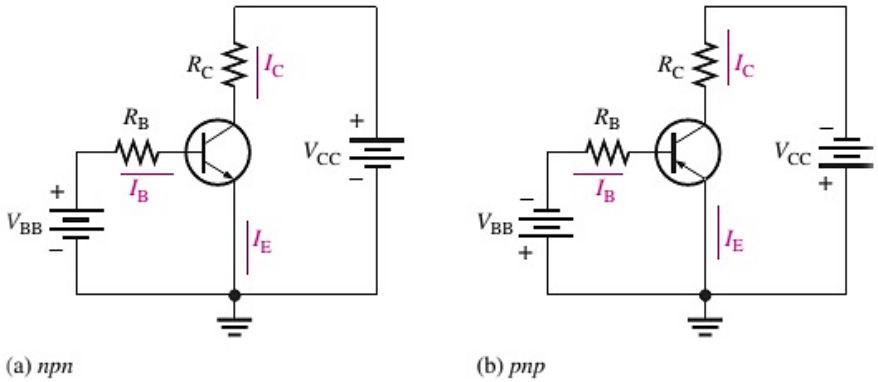


Figure (1-10) Common Emitter Configuration

DC Beta (β_{DC})

The **common-emitter, forward-current, amplification factor** (or dc current gain) is the ratio of the dc collector current (I_C) to the dc base current (I_B) and is designated DC Beta (β_{DC})

$$\beta_{DC} = \frac{I_C}{I_B} \cong \frac{I_E}{I_B}$$

Typical values of β_{DC} range from less than 20 to 200 or higher. β_{DC} is usually designated as an equivalent hybrid (h) parameter, h_{FE}, on transistor datasheets

$$\beta_{DC} = h_{FE}$$

Example Determine the dc current gain β_{DC} and the emitter current I_E for a transistor where $I_B = 50\mu A$ and $I_C = 3.65\ mA$.

Two sets of characteristics are necessary to describe fully the behavior of the common-emitter configuration: one for the output or

collector-emitter circuit and the other for the input or base-emitter circuit. Both are shown in Fig. (1-11).

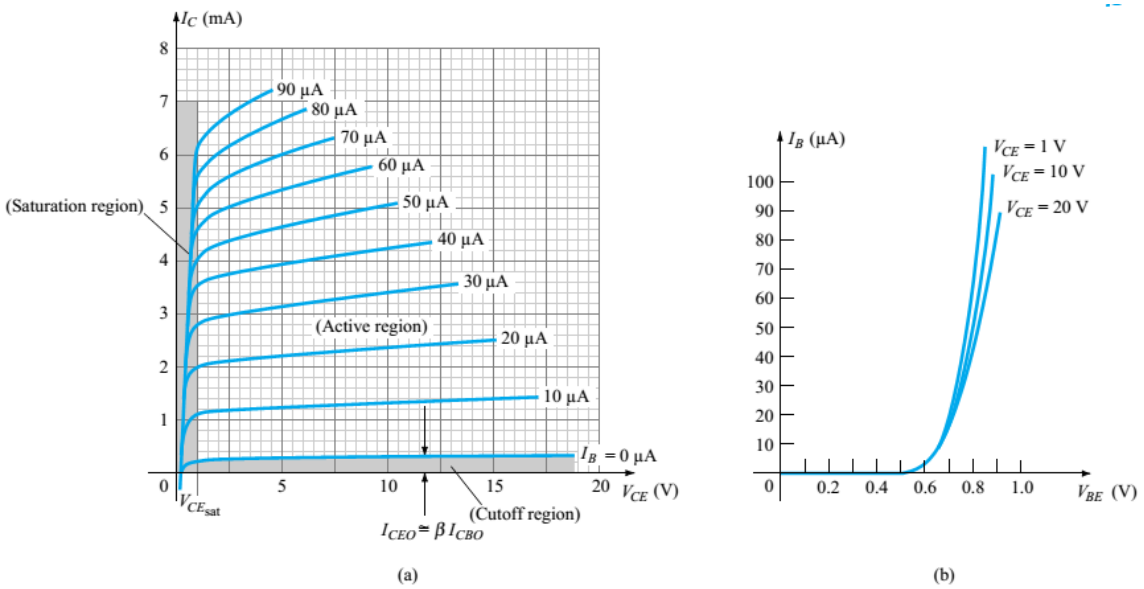


Figure (1-11) Characteristics of a silicon transistor in the common-emitter configuration: (a) collector characteristics; (b) base characteristics.

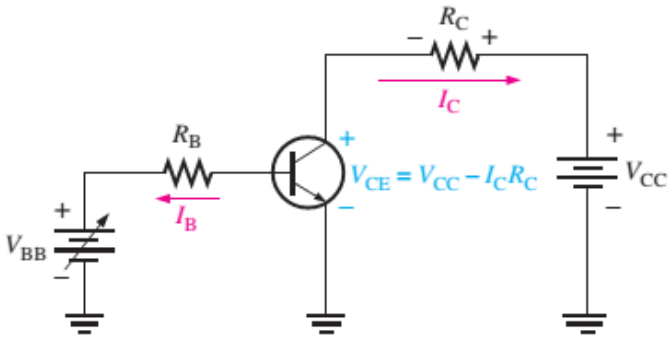
When the base-emitter junction is forward-biased, it is like a forward-biased diode and has a nominal forward voltage drop of transistor in the "on" or active region the base-to emitter voltage is 0.7 V

$$V_{BE} = 0.7\,V \quad for\ silicon \text{ and } 0.3\text{V for } germanium$$

There are three basic regions as indicated in the figure (1-11a). These regions are

1- **The Active region**: the collector-base junction is reverse-biased, while the base-emitter junction is forward-biased.
2- **The Saturation region**: the collector-base and base-emitter junctions are forward-biased. When the base-emitter junction becomes forward-biased and IB is increased, IC also increases and VCE decreases as a result of more drop across the collector resistor (VCE =VCC-ICRC). This is illustrated in Figure (1-12). When VCE reaches its saturation value, VCE(sat), the base-collector junction becomes forward-biased and IC can increase no further even with a continued increase in IB. VCE(sat) for a transistor occurs somewhere below the knee of the collector curves, and it is usually only a few tenths of a volt.

Figure (1-12)



3- The cutoff region: the collector-base and base-emitter junctions of a transistor are both reverse-biased. When $I_B=0$, the transistor is in the cutoff region of its operation. This is shown in Figure (1-13). With the base lead open, resulting in a base current of zero. Under this condition, there is a very small amount of collector leakage current, I_{CEO}, due mainly to thermally produced carriers. Because I_{CEO} is extremely small, it will usually be neglected in circuit analysis so that

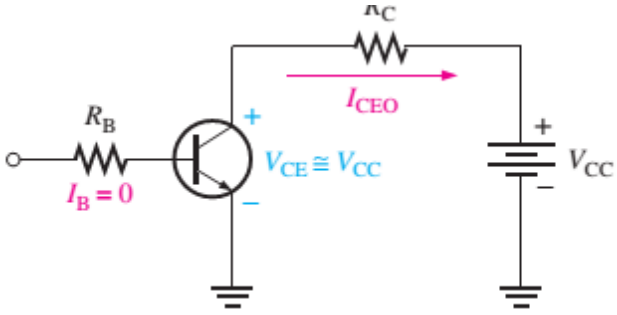


Figure (1-13)

$$V_{CE} = V_{CC}$$

DC Bias

Bias establishes the dc operating point (Q-point) for proper linear operation of an amplifier. The dc operation of a transistor circuit can be described graphically using a dc load line. This is a straight line drawn on the characteristic curves from the saturation value where $I_C=I_{C(sat)}$ on the y-axis to the cutoff value where $V_{CE}=V_{CC}$ on the x-axis, as shown in Figure (1-14).

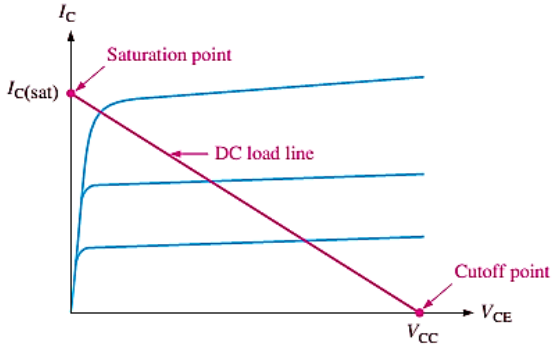


Figure (1-14) DC load line

The load line is determined by the external circuit (VCC and RC), not the transistor itself, which is described by the characteristic curves. The region along the load line including all points between saturation and cutoff is generally known as the linear region of the transistor's operation. As long as the transistor is operated in this region, the output voltage is ideally a linear reproduction of the input. Figure (1–15) shows an example of the linear operation of a transistor.

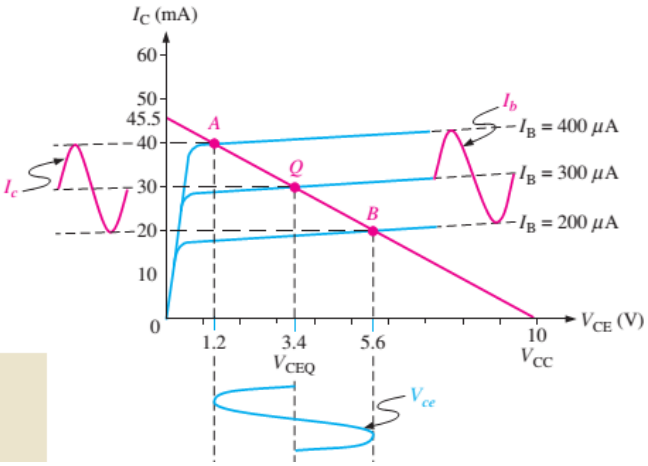


Figure (1–15)

If an amplifier is not biased with correct dc voltages on the input and output, it can go into saturation or cutoff when an input signal is applied. Figure (1–16) shows the effects of improper dc biasing of an inverting amplifier.

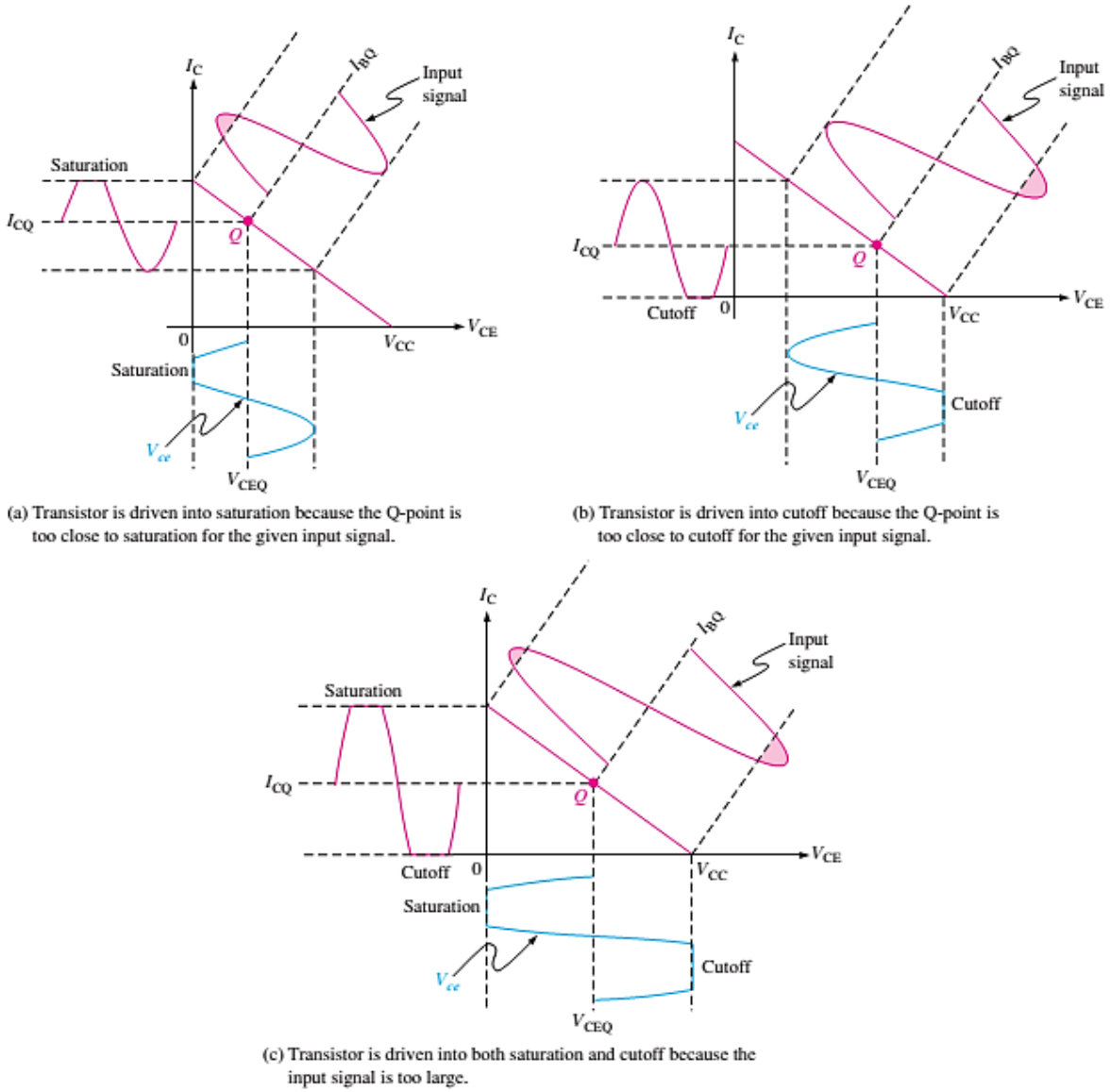


Figure (1-16) Graphical load line illustration of a transistor being driven into saturation and/or cutoff

We will now investigate how the network parameters define the possible range of Q-points and how the actual Q-point is determined

BJT AC Equivalent Circuit

Now we begin to examine the AC response of the BJT transistor by reviewing the models must frequently used to represent the transistor in the sinusoidal AC domain.

One of our first concerns in the sinusoidal AC analysis of transistor networks is the magnitude of the input signal. It will determine wither small-signal or large-signal techniques should be applied.

There are three modules commonly used in the small-signal AC analysis of transistor networks

1- The re model
2- The hybrid π model
3- The hybrid equivalent model

A model is a combination of circuit elements, properly chosen, that best approximates the actual behavior of a semiconductor device under specific operating conditions.

It is important as you progress through the modifications of the network to define the ac equivalent that the parameters of interest such as Zi, Zo, Ii and Io as defined by Fig. (1-17) be carried through properly.

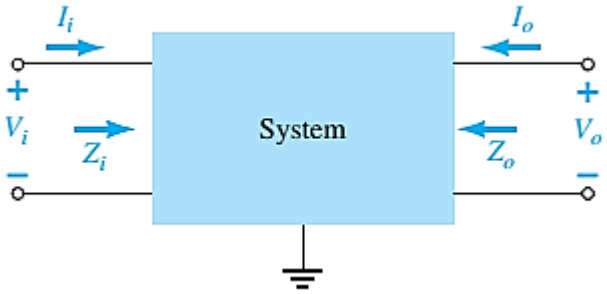


Figure (1-17) Defining the important parameters of any system

The re transistor Model for common emitter configuration

The equivalent circuit for the common-emitter configuration will be constructed using the device characteristics and a number of approximations. Starting with the input side, we find the applied voltage Vi is equal to the voltage Vbe with the input current being the base current Ib as shown in Fig. (1-18).

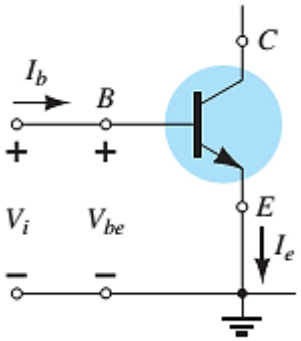
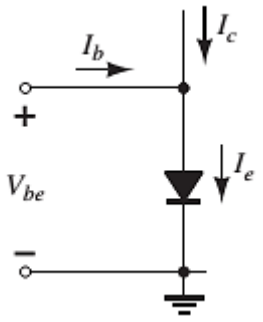


Figure (1-18) Finding the input equivalent circuit for a BJT transistor.

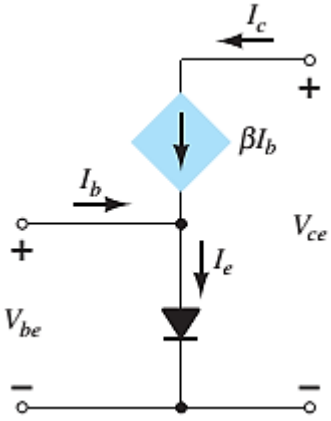
The characteristics for the input side appear as forward-biased diode. For the equivalent circuit, therefore, the input side is simply a single diode with a current Ie, as shown in Fig. (1-19).

Figure (1-19) Equivalent circuit for the input side of a BJT transistor.



However, we must now add a component to the network that will establish the current Ie of Fig. (1-19) using the output characteristics. If we assume β is constant then the entire characteristics at the output section can be replaced by a controlled source whose magnitude is (βIb) and the equivalent network for the common-emitter configuration becomes as shown in figure (1-20).

Figure (1-20) BJT equivalent circuit.



The equivalent model of Fig. (1-20) can be awkward to work with due to the direct connection between input and output networks. It can be improved by

1- replacing the diode by its equivalent resistance

$$r_D = r_e = \frac{26\ mV}{I_E}$$

2- the impedance seen by the base of the network is

$$(1+\beta)r_e$$

The collector output current is still linked to the input current by β as shown

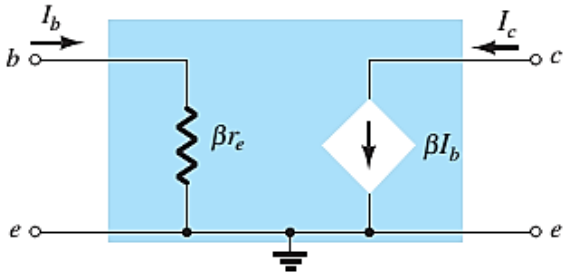


Figure (1-21) Improved BJT equivalent circuit

We now have a good representation for the input circuit, but aside from the collector output current being defined by the level of beta and IB, we do not have a good representation for the output impedance of the device. In any event, an output impedance can now be defined that will appear as a resistor in parallel with the output as shown in the equivalent circuit of Fig. (1-22) .

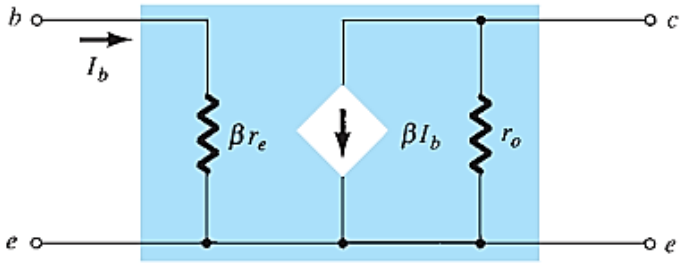


Figure (1-22) re model for the common-emitter transistor configuration including effects of ro.

Biasing Configurations

Fixed-Bias (Base Bias) Circuits

This method of biasing is common in switching circuits. Figure (1-23) shows a base-biased transistor. The analysis of this circuit for the linear region shows that it is directly dependent on β_{DC}. Starting with Kirchhoff's voltage law around the base circuit,

$$V_{CC} = I_B R_B + V_{BE} \Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

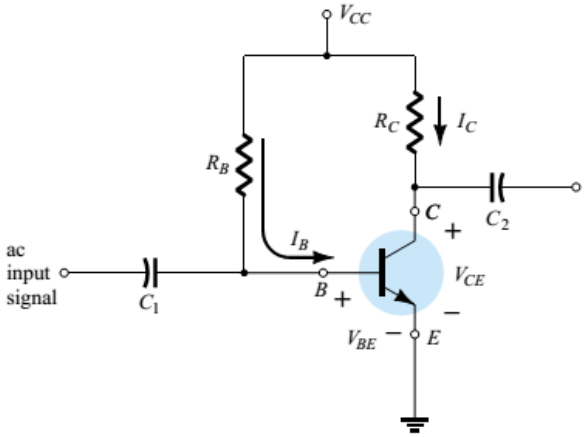


Figure (1-23)

Kirchhoff's voltage law applied around the collector circuit in Figure (1-23) gives the following equation:

$$V_{CC} = I_C R_C + V_{CE}$$

$$I_C = \beta I_B = \beta \left[\frac{V_{CC} - V_{BE}}{R_B}\right]$$

$$V_{CE} = V_{CC} - I_C R_C$$

Load-Line Analysis

The network of Figure (1-23) establishes an output equation that relates the variables I_C and V_{CE} in the following manner:

$$V_{CC} = I_C R_C + V_{CE}$$

The output characteristics of the transistor also relate the same two variables I_C and V_{CE}. We must now superimpose the straight line defined by the output equation on the characteristics. The most direct method of plotting the output equation on the output characteristics is to use the fact that a straight line is defined by two points. If we choose $I_C = 0\ mA$ and by substituting it in the output equation then

$$V_{CC} = 0R_C + V_{CE}$$

$$V_{CE(off)} = V_{CC}\Big|_{Ic=0}$$

If we now choose $V_{CE} = 0\ V$ then

$$V_{CC} = I_C R_C + 0 \qquad \Rightarrow \qquad I_{C(sat)} = \frac{V_{CC}}{R_C}$$

By joining the two points the straight line established by the output equation can be drawn. The resulting line on the graph of Figure (1-24) is called the load line since it is defined by the load resistor R_C

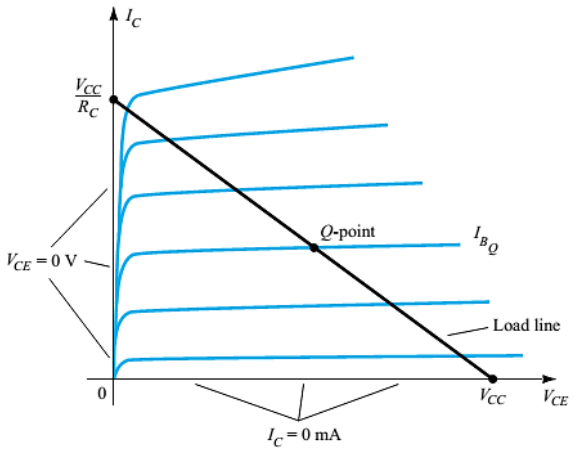


Figure (1-24) fixed bias load line

EXAMPLE 4.1 Determine the following for the fixed-bias configuration of Fig. 4.7.

a. I_{B_Q} and I_{C_Q}.
b. V_{CE_Q}.
c. V_B and V_C.
d. V_{BC}.

Solution:

a. Eq. (4.4): $$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$$

Eq. (4.5): $$I_{C_Q} = \beta I_{BQ} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\ mA}$$

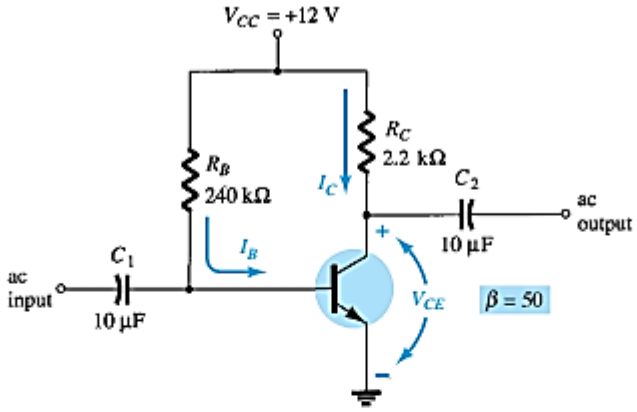


FIG. 4.7
DC fixed-bias circuit for Example 4.1.

b. Eq. (4.6): $$V_{CE_Q} = V_{CC} - I_C R_C$$
$$= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega)$$
$$= \mathbf{6.83\ V}$$

c. $V_B = V_{BE} = \mathbf{0.7\ V}$
$V_C = V_{CE} = \mathbf{6.83\ V}$

d. Using double-subscript notation yields
$$V_{BC} = V_B - V_C = 0.7\text{ V} - 6.83\text{ V}$$
$$= \mathbf{-6.13\ V}$$
with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

EXAMPLE 4.3 Given the load line of Fig. 4.16 and the defined Q-point, determine the required values of V_{CC}, R_C, and R_B for a fixed-bias configuration.

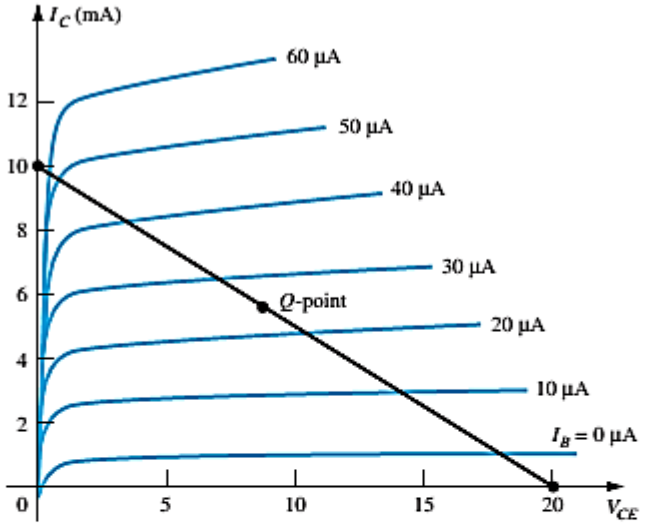


FIG. 4.16
Example 4.3.

Solution: From Fig. 4.16,

$$V_{CE} = V_{CC} = \mathbf{20\ V} \text{ at } I_C = 0\ \text{mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0\ \text{V}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\ \text{V}}{10\ \text{mA}} = \mathbf{2\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

and

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20\ \text{V} - 0.7\ \text{V}}{25\ \mu\text{A}} = \mathbf{772\ k\Omega}$$

AC equivalent circuit for Fixed-Bias (Base Bias) Amplifier

The first configuration to be analyzed in detail is the common-emitter fixed-bias network of Fig. (1-25) . Note that the input signal Vi is applied to the base of the transistor, whereas the output Vo is off the collector. In addition, recognize that the input current Ii is not the base current, but the source current, and the output current Io is the collector current.

The ac equivalent of a fixed bias network is obtained by:

1. Setting all dc sources to zero and replacing them by a short-circuit equivalent.
2. Replacing all capacitors by a short-circuit equivalent.
3. Substituting the re model for the common emitter configuration.

4. Redrawing the network in a more convenient and logical form.
5. Place the important network parameters Zi, Zo, Ii and Io on the redrawn network.

EXAMPLE 5.1 For the network of Fig. 5.25:

a. Determine r_e.
b. Find Z_i (with $r_o = \infty\,\Omega$).
c. Calculate Z_o (with $r_o = \infty\,\Omega$).
d. Determine A_v (with $r_o = \infty\,\Omega$).
e. Repeat parts (c) and (d) including $r_o = 50\,\text{k}\Omega$ in all calculations and compare results.

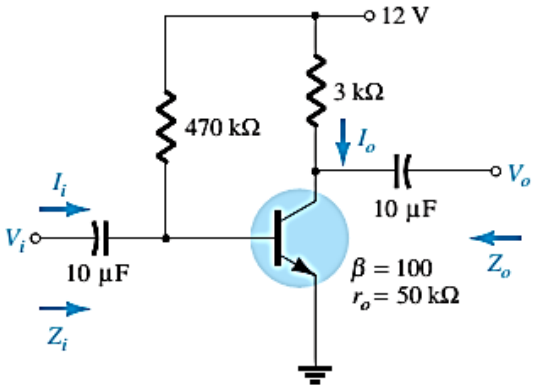


FIG. 5.25
Example 5.1.

Solution:

a. DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\,\text{V} - 0.7\,\text{V}}{470\,\text{k}\Omega} = 24.04\,\mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(24.04\,\mu\text{A}) = 2.428\,\text{mA}$$

$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{2.428\,\text{mA}} = \mathbf{10.71\,\Omega}$$

b. $\beta r_e = (100)(10.71\,\Omega) = 1.071\,\text{k}\Omega$

$$Z_i = R_B \| \beta r_e = 470\,\text{k}\Omega \| 1.071\,\text{k}\Omega = \mathbf{1.07\,k\Omega}$$

c. $Z_o = R_C = \mathbf{3\,k\Omega}$

d. $$A_v = -\frac{R_C}{r_e} = -\frac{3\,\text{k}\Omega}{10.71\,\Omega} = \mathbf{-280.11}$$

Emitter-Stabilized Bias Circuit

The dc bias network of Figure (1-27) contains an emitter resistor to improve the stability level over that of the fixed-bias configuration. To calculate I_B, you can write Kirchhoff's voltage law (KVL) around the base circuit

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

$$I_E = I_B + I_C$$

$$I_E = I_B + \beta I_B \quad \rightarrow \quad I_E = I_B(1+\beta)$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E}$$

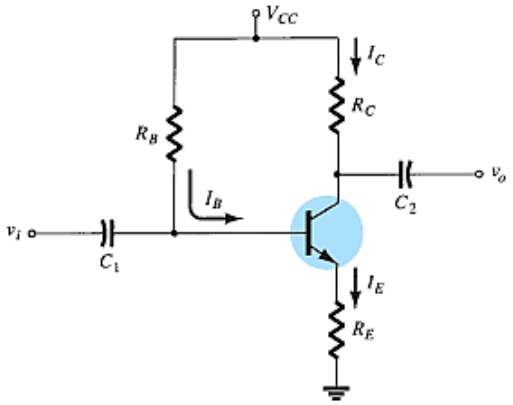


Figure (1-27) Emitter-Stabilized

There is an interesting result that can be derived from I_B equation if the equation is used to sketch a series network that would result in the same equation we will note that the emitter resistor, which is part of the collector emitter loop, "appears as" $(1+\beta)R_E$ in the base-emitter loop.

$$R_i = (1+\beta)R_E$$

Writing Kirchhoff's voltage law for the collector-emitter loop in the clockwise direction will result in

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

Substituting $I_E \cong I_C$ resulting in

$$V_{CE} = V_{CC} - I_E(R_E + R_C)$$

The single-subscript voltage V_E is the voltage from emitter to ground and is determined by

$$V_E = I_E V_E$$

While the voltage from collector to ground can be determined from

$$V_{CE} = V_C - V_E$$

$$V_C = V_{CE} + V_E$$

Or

$$V_C = V_{CC} - I_C R_C$$

The voltage at the base with respect to ground can be determined from

$$V_B = V_{CC} - I_B R_B$$

$$V_B = V_{BE} + V_E$$

Load-Line Analysis

The collector–emitter loop equation that defines the load line is the following

$$V_{CE} = V_{CC} - I_E(R_E + R_C)$$

The collector saturation level or maximum collector current for an emitter-bias design can be determined by apply a short circuit between the collector–emitter terminals *(V_{CE}=0)* gives

$$\mathrm{I_{C(sat)}} = \frac{\mathrm{V_{CC}}}{\mathrm{R_C + R_E}}$$

The maximum collector-emitter voltage can be determined by applying *(I_C=0) gives*

$$\mathrm{V_{CE(off)}} = \mathrm{V_{CC}}$$

The resulting load line for the emitter bias design is shown in figure (1-28)

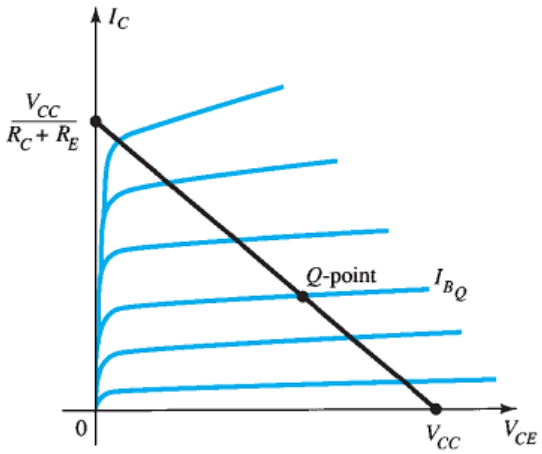


Figure (1-28) Emitter bias load line

EXAMPLE 4.4 For the emitter-bias network of Fig. 4.23, determine:

a. I_B.
b. I_C.
c. V_{CE}.
d. V_C.
e. V_E.
f. V_B.
g. V_{BC}.

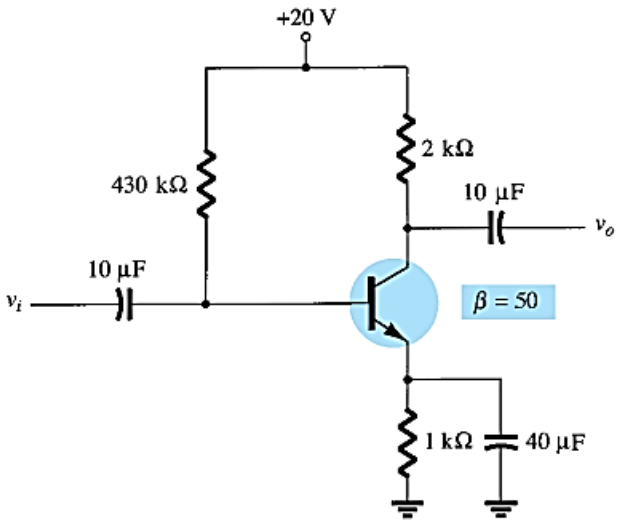


FIG. 4.23
Emitter-stabilized bias circuit for Example 4.4.

Solution:

a. Eq. (4.17): $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$

$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

b. $I_C = \beta I_B$

$= (50)(40.1\ \mu\text{A})$

$\cong$ **2.01 mA**

c. Eq. (4.19): $V_{CE} = V_{CC} - I_C(R_C + R_E)$

$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V}$

$=$ **13.97 V**

d. $V_C = V_{CC} - I_C R_C$

$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V}$

$=$ **15.98 V**

e. $V_E = V_C - V_{CE}$

$= 15.98\text{ V} - 13.97\text{ V}$

$=$ **2.01 V**

or $V_E = I_E R_E \cong I_C R_E$

$= (2.01\text{ mA})(1\text{ k}\Omega)$

$=$ **2.01 V**

f. $V_B = V_{BE} + V_E$

$= 0.7\text{ V} + 2.01\text{ V}$

$=$ **2.71 V**

g. $V_{BC} = V_B - V_C$

$= 2.71\text{ V} - 15.98\text{ V}$

$=$ **−13.27 V** (reverse-biased as required)

EXAMPLE 4.6 Determine the saturation current for the network of Example 4.4.

Solution:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

$$= \frac{20\text{ V}}{2\text{ k}\Omega + 1\text{ k}\Omega} = \frac{20\text{ V}}{3\text{ k}\Omega}$$

$$= \mathbf{6.67\ mA}$$

which is about three times the level of I_{C_Q} for Example 4.4.

EXAMPLE 4.7

a. Draw the load line for the network of Fig. 4.26a on the characteristics for the transistor appearing in Fig. 4.26b.
b. For a Q-point at the intersection of the load line with a base current of 15 μA, find the values of I_{C_Q} and V_{CE_Q}.
c. Determine the dc beta at the Q-point.
d. Using the beta for the network determined in part c, calculate the required value of R_B and suggest a possible standard value.

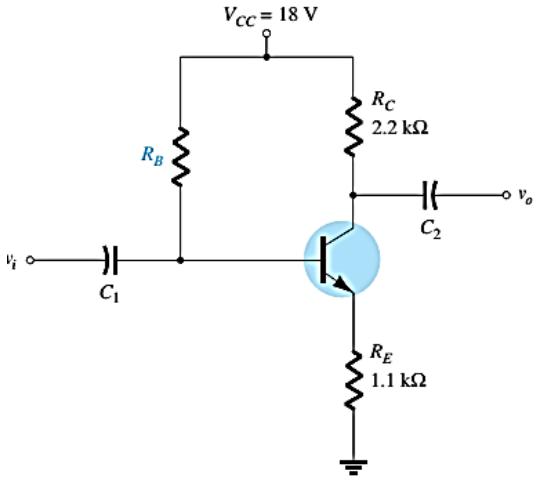


FIG. 4.26a
Network for Example 4.7.

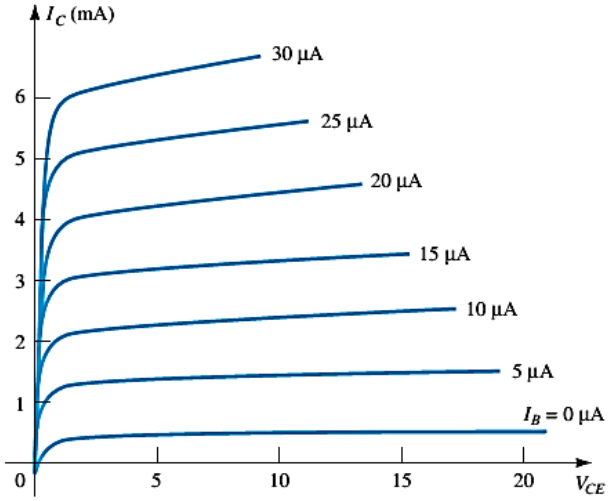


FIG. 4.26b
Example 4.7.

Solution:

a. Two points on the characteristics are required to draw the load line.

At $V_{CE} = 0$ V: $I_C = \dfrac{V_{CC}}{R_C + R_E} = \dfrac{18\text{ V}}{2.2\text{ k}\Omega + 1.1\text{ k}\Omega} = \dfrac{18\text{ V}}{3.3\text{ k}\Omega} = 5.45\text{ mA}$

At $I_C = 0$ mA: $V_{CE} = V_{CC} = 18$ V

The resulting load line appears in Fig. 4.27.

b. From the characteristics of Fig. 4.27 we find

$V_{CE_Q} \cong \mathbf{7.5\text{ V}}, I_{C_Q} \cong \mathbf{3.3\text{ mA}}$

c. The resulting dc beta is:

$$\beta = \frac{I_{C_Q}}{I_{B_Q}} = \frac{3.3\text{ mA}}{15\ \mu\text{A}} = \mathbf{220}$$

d. Applying Eq. 4.17:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{18\text{ V} - 0.7\text{ V}}{R_B + (220 + 1)(1.1\text{ k}\Omega)}$$

$$\text{and } 15\ \mu\text{A} = \frac{17.3\text{ V}}{R_B + (221)(1.1\text{ k}\Omega)} = \frac{17.3\text{ V}}{R_B + 243.1\text{ k}\Omega}$$

$$\text{so that } (15\ \mu\text{A})(R_B) + (15\ \mu\text{A})(243.1\text{ k}\Omega) = 17.3\text{ V}$$

$$\text{and } (15\ \mu\text{A})(R_B) = 17.3\text{ V} - 3.65\text{ V} = 13.65\text{ V}$$

$$\text{resulting in } R_B = \frac{13.65\text{ V}}{15\ \mu\text{A}} = \mathbf{910\text{ k}\Omega}$$

AC Analysis of Emitter-Stabilized Bias Amplifier Circuit

EXAMPLE 5.3 For the network of Fig. 5.32, without C_E (unbypassed), determine:

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.

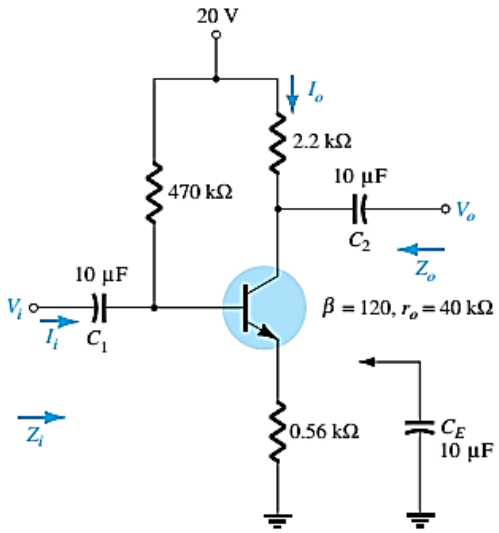


FIG. 5.32
Example 5.3.

EXAMPLE 5.4 Repeat the analysis of Example 5.3 with C_E in place.

Solution:

a. The dc analysis is the same, and $r_e = 5.99\ \Omega$.

b. R_E is "shorted out" by C_E for the ac analysis. Therefore,

$$Z_i = R_B \| Z_b = R_B \| \beta r_e = 470\ \text{k}\Omega \| (120)(5.99\ \Omega)$$
$$= 470\ \text{k}\Omega \| 718.8\ \Omega \cong \mathbf{717.70\ \Omega}$$

c. $Z_o = R_C = \mathbf{2.2\ k\Omega}$

d. $$A_v = -\frac{R_C}{r_e}$$
$$= -\frac{2.2\ \text{k}\Omega}{5.99\ \Omega} = \mathbf{-367.28}\ \text{(a significant increase)}$$

VOLTAGE-DIVIDER BIAS

In the previous bias configurations the bias current I_{CQ} and voltage V_{CEQ} were a function of the current gain (β) of the transistor.

However, since β is temperature sensitive, especially for silicon transistors, and the actual value of beta is usually not well defined, it would be desirable to develop a bias circuit that is independent of the transistor beta. The voltage-divider bias configuration of Figure (1-19) is such a network. A dc bias voltage at the base of the transistor can be developed by a resistive voltage divider that consists of R_1 and R_2, as shown in Figure (1-31).

There are two methods that can be applied to analyze the voltage divider configuration.

1. the exact method
2. the approximate method

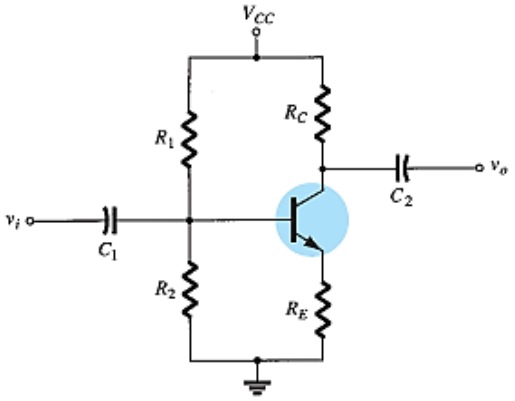


Figure (1-31).

Exact Analysis

The input side of the network of Figure (1-30) can be redrawn as shown in Figure (1-31) for the d analysis. Apply

Thevenin's theorem to the circuit left of point B, with V_{CC} replaced by a short to ground and the transistor disconnected from the circuit. The voltage at point B with respect to ground is

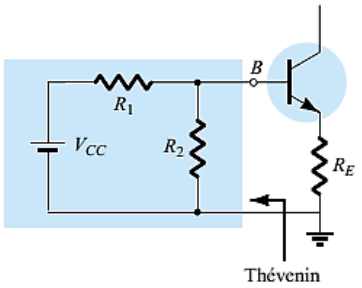


Figure (1-31)

$$E_{Th} = V_{CC}\left[\frac{R_2}{R_1 + R_2}\right]$$

And the resistance is

$$R_{Th} = \left[\frac{R_1 R_2}{R_1 + R_2}\right]$$

The Thévenin network is then redrawn as shown in Figure (1-32), and I_{BQ} can be determined by first applying Kirchhoff's voltage law

$$E_{Th} = I_B R_{Th} + V_{BE} + I_E R_E$$

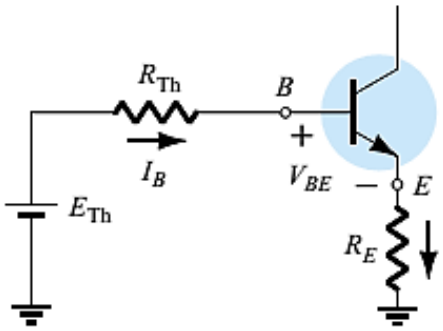


Figure (1-32) Inserting the Thévenin equivalent

Substituting $I_E = (1 + \beta)I_B$ and solving for I_B yields

$$I_B = \left[\frac{E_{Th} - V_{BE}}{R_{Th} + (1 + \beta)R_E}\right]$$

The remaining quantities of the network can be found in the same manner as developed for the emitter-bias configuration. That is,

$$V_{CE} = V_{CC} - I_E(R_E + R_C)$$

EXAMPLE 4.8 Determine the dc bias voltage V_{CE} and the current I_C for the voltage-divider configuration of Fig. 4.35.

Solution: Eq. (4.28): $R_{Th} = R_1 \| R_2$

$$= \frac{(39\,\text{k}\Omega)(3.9\,\text{k}\Omega)}{39\,\text{k}\Omega + 3.9\,\text{k}\Omega} = 3.55\,\text{k}\Omega$$

Eq. (4.29): $$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$= \frac{(3.9\,\text{k}\Omega)(22\,\text{V})}{39\,\text{k}\Omega + 3.9\,\text{k}\Omega} = 2\,\text{V}$$

Eq. (4.30): $$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$= \frac{2\,\text{V} - 0.7\,\text{V}}{3.55\,\text{k}\Omega + (101)(1.5\,\text{k}\Omega)} = \frac{1.3\,\text{V}}{3.55\,\text{k}\Omega + 151.5}$$

$$= 8.38\,\mu\text{A}$$

$$I_C = \beta I_B$$

$$= (100)(8.38\,\mu\text{A})$$

$$= \mathbf{0.84\,mA}$$

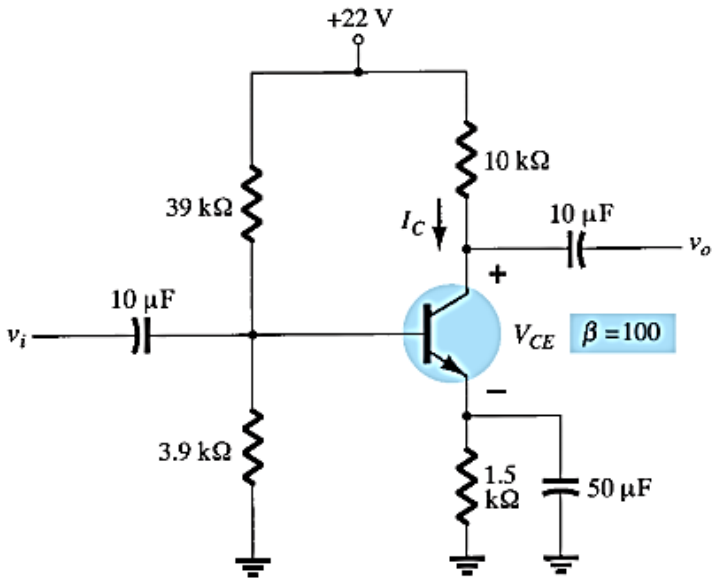


FIG. 4.35
Beta-stabilized circuit for Example 4.8.

Eq. (4.31): $$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 22\,\text{V} - (0.84\,\text{mA})(10\,\text{k}\Omega + 1.5\,\text{k}\Omega)$$

$$= 22\,\text{V} - 9.66\,\text{V}$$

$$= \mathbf{12.34\,V}$$

Approximate Analysis

The input section of the voltage-divider configuration can be represented by the network of Figure (1-33).

The reflected resistance between base and emitter is defined by

$$R_i = (1 + \beta)R_E$$

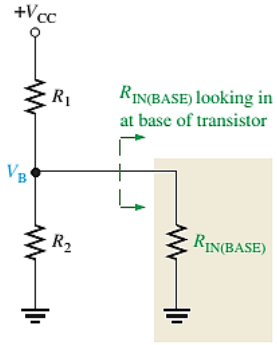


Figure (1-33)

If R_i is much larger than the resistance R_2 ($R_i \geq 10R_2$), the loading effect of the base current can be ignored so the current I_B will be much smaller than I_2 (current always seeks the path of least resistance) and I_2 will be approximately equal to I_1. If we accept the approximation that I_B is essentially zero amperes compared to I_1 or I_2, then $I_1=I_2$ and R_1 and R_2 can be considered series components. The voltage across R_2, which is actually the base voltage, can be determined using the voltage-divider rule

$$V_B = \left[\frac{V_{CC}R_2}{R_1 + R_2}\right]$$

And the complete analysis will be as following

$$V_E = V_B - V_{BE}$$

$$I_E = V_E/R_E$$

$$I_{CQ} \cong I_E$$

The collector-to-emitter voltage is determined by

$$V_{CEQ} = V_{CC} - I_C(R_C + R_E)$$

Note that the Q-point (as determined by I_{CQ} and V_{CEQ}) is independent of the value of β

Load-Line Analysis

The similarities with the output circuit of the emitter-biased configuration result in the same intersections for the load line of the voltage-divider configuration. The load line will therefore have the same appearance as that of Figure (1-28), with

$$I_{C(sat)} = \left(\frac{V_{CC}}{R_C + R_E}\right)$$

$$V_{CE(off)} = V_{CC}$$

EXAMPLE 4.9 Repeat the analysis of Fig. 4.35 using the approximate technique, and compare solutions for I_{C_Q} and V_{CE_Q}.

Solution: Testing:

$$\beta R_E \geq 10R_2$$
$$(100)(1.5\,\text{k}\Omega) \geq 10(3.9\,\text{k}\Omega)$$
$$150\,\text{k}\Omega \geq 39\,\text{k}\Omega \ (\textit{satisfied})$$

$$\text{Eq. (4.32):} \quad V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$
$$= \frac{(3.9\,\text{k}\Omega)(22\,\text{V})}{39\,\text{k}\Omega + 3.9\,\text{k}\Omega}$$
$$= 2\,\text{V}$$

Note that the level of V_B is the same as E_{Th} determined in Example 4.7. Essentially, therefore, the primary difference between the exact and approximate techniques is the effect of R_{Th} in the exact analysis that separates E_{Th} and V_B.

$$\text{Eq. (4.34):} \quad V_E = V_B - V_{BE}$$
$$= 2\,\text{V} - 0.7\,\text{V}$$
$$= 1.3\,\text{V}$$
$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{1.3\,\text{V}}{1.5\,\text{k}\Omega} = \mathbf{0.867\,mA}$$

compared to 0.84 mA with the exact analysis. Finally,

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$
$$= 22\,\text{V} - (0.867\,\text{mA})(10\,\text{kV} + 1.5\,\text{k}\Omega)$$
$$= 22\,\text{V} - 9.97\,\text{V}$$
$$= \mathbf{12.03\,V}$$

versus 12.34 V obtained in Example 4.8.

The results for I_{C_Q} and V_{CE_Q} are certainly close, and considering the actual variation in parameter values, one can certainly be considered as accurate as the other. The larger the level of R_i compared to R_2, the closer is the approximate to the exact solution. Example 4.11 will compare solutions at a level well below the condition established by Eq. (4.33).

EXAMPLE 4.10 Repeat the exact analysis of Example 4.8 if β is reduced to 50, and compare solutions for I_{C_Q} and V_{CE_Q}.

Solution: This example is not a comparison of exact versus approximate methods, but a testing of how much the Q-point will move if the level of β is cut in half. R_{Th} and E_{Th} are the same:

$$R_{\text{Th}} = 3.55\,\text{k}\Omega, \qquad E_{\text{Th}} = 2\,\text{V}$$
$$I_B = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E}$$

$$= \frac{2\text{ V} - 0.7\text{ V}}{3.55\text{ k}\Omega + (51)(1.5\text{ k}\Omega)} = \frac{1.3\text{ V}}{3.55\text{ k}\Omega + 76.5\text{ k}\Omega}$$

$$= 16.24\ \mu\text{A}$$

$$I_{C_Q} = \beta I_B$$

$$= (50)(16.24\ \mu\text{A})$$

$$= \mathbf{0.81\text{ mA}}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

$$= 22\text{ V} - (0.81\text{ mA})(10\text{ k}\Omega + 1.5\text{ k}\Omega)$$

$$= \mathbf{12.69\text{ V}}$$

Tabulating the results, we have:

Effect of β variation on the response of the voltage-divider configuration of Fig. 4.35.

β	I_{C_Q} (mA)	V_{CE_Q} (V)
100	0.84 mA	12.34 V
50	0.81 mA	12.69 V

The results clearly show the relative insensitivity of the circuit to the change in β. Even though β is drastically cut in half, from 100 to 50, the levels of I_{C_Q} and V_{CE_Q} are essentially the same.

AC Analysis of Voltage Divider Configuration

EXAMPLE 5.2 For the network of Fig. 5.28, determine:

a. r_e.
b. Z_i.
c. Z_o ($r_o = \infty\,\Omega$).
d. A_v ($r_o = \infty\,\Omega$).
e. The parameters of parts (b) through (d) if $r_o = 50\,\text{k}\Omega$ and compare results.

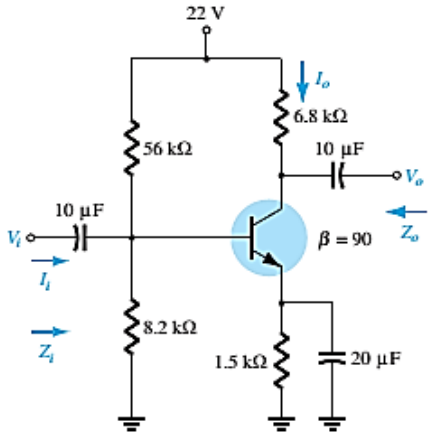


FIG. 5.28
Example 5.2.

Collector Feedback Bias

An improved level of stability can also be obtained by introducing a feedback path from collector to base as shown in Figure (1-36). The negative feedback creates an "offsetting" effect that tends to keep the Q-point stable. If I_C tries to increase, it drops more voltage across R_C, thereby causing V_C to decrease.

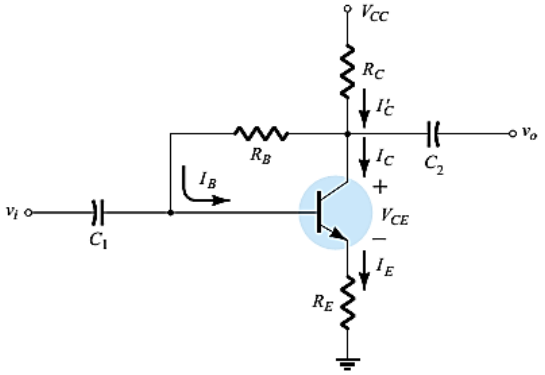


Figure (1-36) dc bias circuit with voltage feedback.

When V_C decreases, there is a decrease in voltage across RB, which decreases IB. The decrease in IB produces less I_C which, in turn, drops less voltage across RC and thus offsets the decrease in VC. Writing Kirchhoff's voltage law around the base-emitter loop will result in

$$V_{CC} = I'_C R_C + I_B R_B + V_{BE} + I_E R_E$$

$$I'_C = I_C + I_B \cong I_C \cong \beta I_B \cong I_E$$

Gathering terms, we have

$$V_{CC} = V_{BE} + I_B R_B + \beta I_B (R_C + R_E)$$

$$I_B = \left(\frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}\right)$$

The feedback path results in a reflection of the resistance R_C back to the input circuit, much like the reflection of R_E.

Applying Kirchhoff's voltage law around the collector–emitter loop for the network of Figure (1-34) will result in

$$V_{CC} = I'_C R_C + V_{CE} + I_E R_E$$

$$I'_C \cong I_C \cong I_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Which is exactly as obtained for the emitter-bias and voltage-divider bias configurations.

Load line analysis

Continuing with the approximation $I'_C \cong I_C \cong I_E$ will result in the same load line defined for the voltage-divider and emitter-biased configurations. The load line will therefore have the same appearance as that of Figure (1-28), with

$$I_{C(sat)} = \left(\frac{V_{CC}}{R_C + R_E}\right)$$

$$V_{CE(off)} = V_{CC}$$

EXAMPLE 4.12 Determine the quiescent levels of I_{C_Q} and V_{CE_Q} for the network of Fig. 4.41.

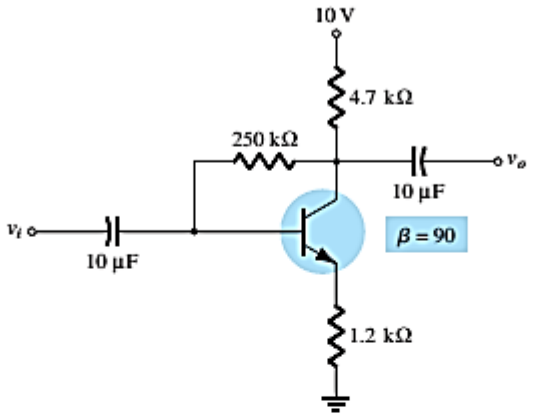


FIG. 4.41
Network for Example 4.12.

Solution: Eq. (4.41): $I_B = \dfrac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$

$$= \frac{10\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (90)(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)}$$

$$= \frac{9.3\text{ V}}{250\text{ k}\Omega + 531\text{ k}\Omega} = \frac{9.3\text{ V}}{781\text{ k}\Omega}$$

$$= 11.91\ \mu\text{A}$$

$$I_{C_Q} = \beta I_B = (90)(11.91\ \mu\text{A})$$

$$= \mathbf{1.07\text{ mA}}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

$$= 10\text{ V} - (1.07\text{ mA})(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)$$

$$= 10\text{ V} - 6.31\text{ V}$$

$$= \mathbf{3.69\text{ V}}$$

EXAMPLE 4.15 Given the network of Fig. 4.43 and the BJT characteristics of Fig. 4.44.

a. Draw the load line for the network on the characteristics.
b. Determine the dc beta in the center region of the characteristics. Define the chosen point as the *Q*-point.
c. Using the dc beta calculated in part b, find the dc value of I_B.
d. Find I_{C_Q} and I_{CE_Q}.

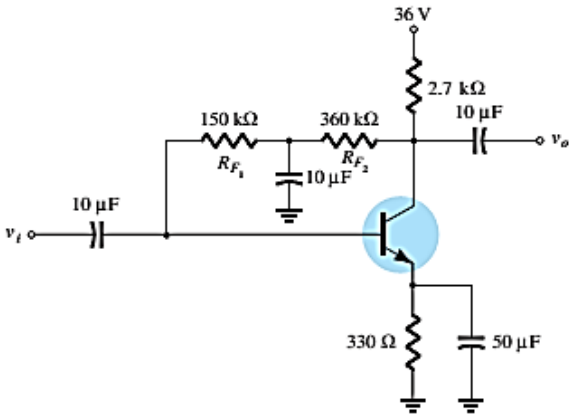


FIG. 4.43
Network for Example 4.15.

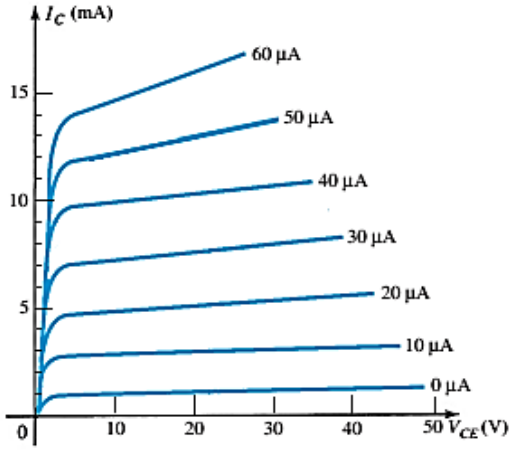


FIG. 4.44
BJT characteristics.

Solution:

a. The load line is drawn on Fig. 4.45 as determined by the following intersections:

$$V_{CE} = 0\text{ V}: I_C = \frac{V_{CC}}{R_C + R_E} = \frac{36\text{ V}}{2.7\text{ k}\Omega + 330\ \Omega} = \mathbf{11.88\text{ mA}}$$

$$I_C = 0\text{ mA}: V_{CE} = V_{CC} = \mathbf{36\text{ V}}$$

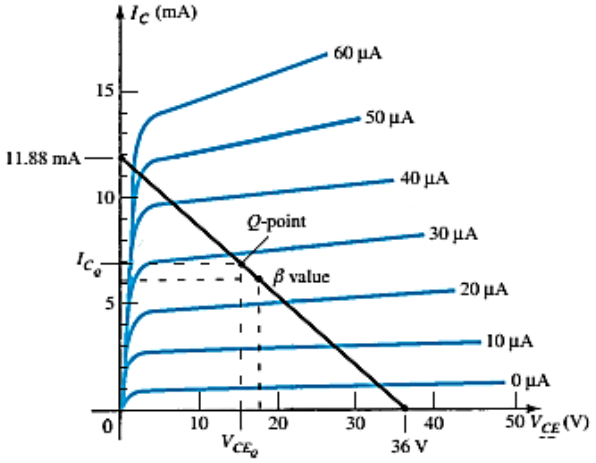


FIG. 4.45
Defining the Q-point for the voltage-divider bias configuration of Fig. 4.43.

b. The dc beta was determined using $I_B = 25\ \mu\text{A}$ and V_{CE} about 17 V.

$$\beta \cong \frac{I_{C_Q}}{I_{B_Q}} = \frac{6.2\text{ mA}}{25\ \mu\text{A}} = \mathbf{248}$$

c. Using Eq. 4.41:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} = \frac{36\text{ V} - 0.7\text{ V}}{510\text{ k}\Omega + 248(2.7\text{ k}\Omega + 330\ \Omega)}$$

$$= \frac{35.3\text{ V}}{510\text{ k}\Omega + 751.44\text{ k}\Omega}$$

$$\text{and } I_B = \frac{35.3\text{ V}}{1.261\text{ M}\Omega} = \mathbf{28\ \mu A}$$

d. From Fig. 4.45 the quiescent values are

$I_{C_Q} \cong$ **6.9 mA** and $V_{CE_Q} \cong$ **15 V**

AC Analysis of Collector Feedback Configuration

EXAMPLE 5.9 For the network of Fig. 5.48. determine:

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.
e. Repeat parts (b) through (d) with $r_o = 20\,\text{k}\Omega$ and compare results.

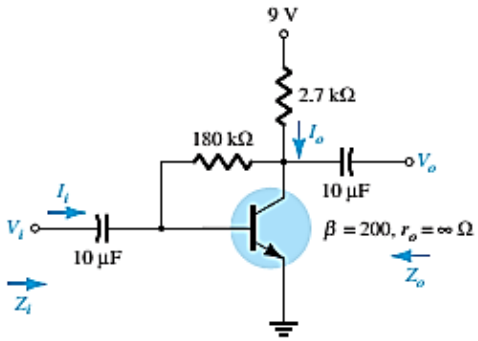


FIG. 5.48
Example 5.9.

Common-Collector Configuration

The second transistor configuration is the common-collector configuration. The common-collector (CC) amplifier is usually referred to as an emitter-follower (EF). The common-collector configuration is used primarily for impedance-matching purposes since it has a high input impedance and low output impedance.

The input current is the same for both the common-emitter and common collector characteristics. The horizontal voltage axis for the common-collector configuration is obtained by simply changing the sign of the collector-to-emitter voltage of the common-emitter characteristics. Finally, there is an almost unnoticeable change in the vertical scale of I_C of the common-emitter characteristics if I_C is replaced by I_E for the common-collector characteristics (since α=1). For the input circuit of the common-collector configuration the common-emitter base characteristics are sufficient for obtaining the required information.

Emitter Follower Biasing

An emitter-follower circuit with voltage-divider bias is shown in Figure (1-39). Notice that the input signal is capacitively coupled to the base, the output signal is capacitively coupled from the emitter, and the collector is at ac ground.

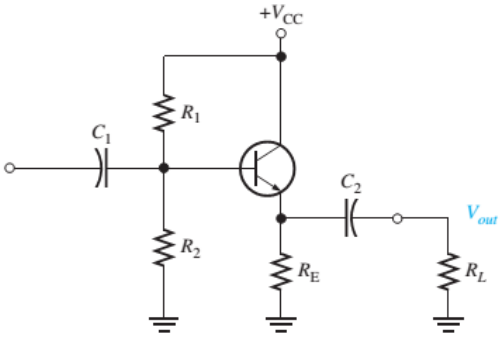


Figure (1-39) Emitter-follower with voltage-divider bias.

EXAMPLE 4.16 Determine V_{CE_Q} and I_{E_Q} for the network of Fig. 4.48.

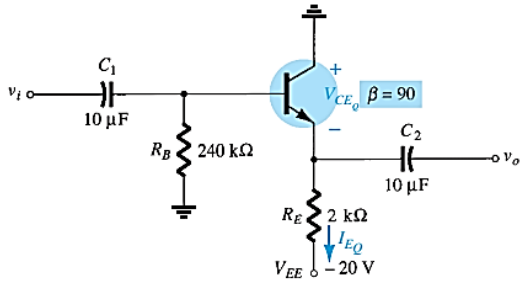


FIG. 4.48
Example 4.16.

Solution:

Eq. 4.44:
$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}$$
$$= \frac{20\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega + (90 + 1)2\text{ k}\Omega} = \frac{19.3\text{ V}}{240\text{ k}\Omega + 182\text{ k}\Omega}$$
$$= \frac{19.3\text{ V}}{422\text{ k}\Omega} = 45.73\ \mu\text{A}$$

and Eq. 4.45:
$$V_{CE_Q} = V_{EE} - I_E R_E$$
$$= V_{EE} - (\beta + 1)I_B R_E$$
$$= 20\text{ V} - (90 + 1)(45.73\ \mu\text{A})(2\text{ k}\Omega)$$
$$= 20\text{ V} - 8.32\text{ V}$$
$$= \mathbf{11.68\text{ V}}$$
$$I_{E_Q} = (\beta + 1)I_B = (91)(45.73\ \mu\text{A})$$
$$= 4.16\text{ mA}$$

AC Analysis of Common Collector Configuration

EXAMPLE 5.7 For the emitter-follower network of Fig. 5.39, determine:

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.
e. Repeat parts (b) through (d) with $r_o = 25\ \text{k}\Omega$ and compare results.

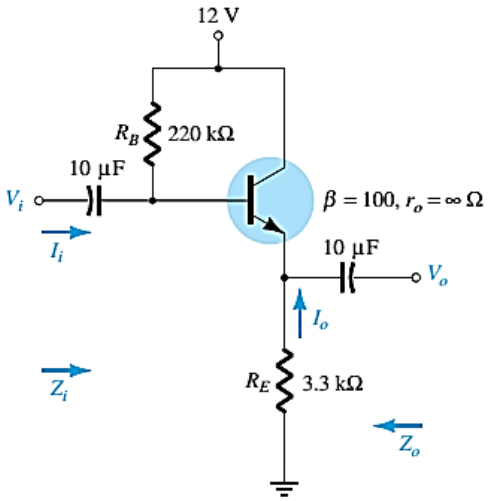


FIG. 5.39
Example 5.7.

Solution:

a. $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$= \frac{12\text{ V} - 0.7\text{ V}}{220\text{ k}\Omega + (101)3.3\text{ k}\Omega} = 20.42\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B$$

$$= (101)(20.42\ \mu\text{A}) = 2.062\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.062\text{ mA}} = \mathbf{12.61\ \Omega}$$

b. $$Z_b = \beta r_e + (\beta + 1)R_E$$

$$= (100)(12.61\ \Omega) + (101)(3.3\text{ k}\Omega)$$

$$= 1.261\text{ k}\Omega + 333.3\text{ k}\Omega$$

$$= 334.56\text{ k}\Omega \cong \beta R_E$$

$$Z_i = R_B \| Z_b = 220\text{ k}\Omega \| 334.56\text{ k}\Omega$$

$$= \mathbf{132.72\ k\Omega}$$

c. $$Z_o = R_E \| r_e = 3.3\text{ k}\Omega \| 12.61\ \Omega$$

$$= \mathbf{12.56\ \Omega} \cong r_e$$

d. $$A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e} = \frac{3.3\text{ k}\Omega}{3.3\text{ k}\Omega + 12.61\ \Omega}$$

$$= \mathbf{0.996 \cong 1}$$

Common Base Configuration

In figure (1-44) the npn transistor is shown in common base (CB) configuration. The common base terminology derived from the fact that the base is common to both the input and output sides of the configuration. In addition, the base is usually the terminal closest to, or at, ground potential.

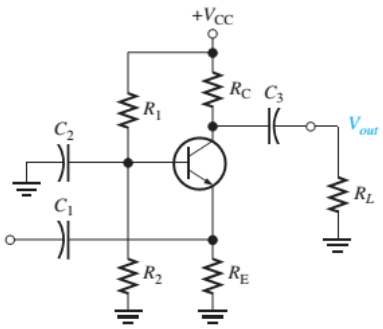


Figure (1-44) common base configuration for npn transistor

To fully describe the behavior of the common base amplifier of figure (1-44) requires two sets of characteristics one for the deriving point or input parameters and the other for the output side.

The input set for the common base amplifier as shown in figure (1-45) relates an input current (I_E) to input voltage (V_{BE}) for various levels of output voltage (V_{CB}).

The effect of (V_{CB}) in the input characteristics is because the increasing of (V_{CB}) will increase the width of the depletion region at the output junction diode. This decrease in the depletion region will less chance for recombination within the base region so that (I_E and also I_C) will increase.

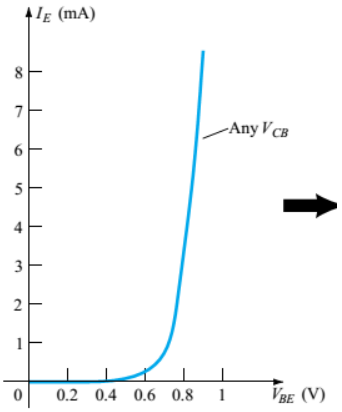


Figure (1-45) input characteristics for npn transistor

The curves of figure (1-46) are known as the output or collector characteristics. There are three basic regions as indicated in the figure. These regions are

4- **The Active region:** the collector-base junction is reverse-biased, while the base-emitter junction is forward-biased.
5- **The Saturation region:** the collector-base and base-emitter junctions are forward-biased
6- **The cutoff region:** the collector-base and base-emitter junctions of a transistor are both reverse-biased

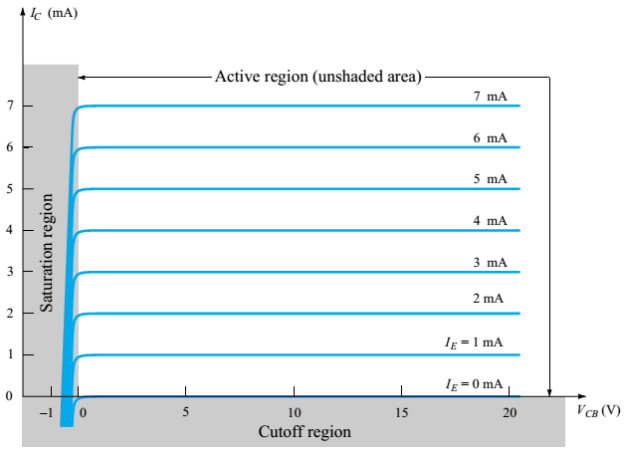


Figure (1-46) collector characteristics for npn transistor

When $I_E = 0$ the collector current is simply that due to the reverse saturation current I_{CO} The notation most frequently used for I_{CO} on data and specification sheets is I_{CBO} . Note in Fig. (1-28) that as I_E increases above zero, I_C increases to a magnitude essentially equal to that of I_E

$$I_C \cong I_E$$

As inferred by its name, the cutoff region is defined as that region where $I_C = 0$ A. The ratio of the dc collector current (I_C) to the dc emitter current (I_E) is the dc alpha α_{DC}

$$\alpha_{DC} = \frac{I_C}{I_E}$$

Typically, values of α_{DC} range from 0.95 to 0.99 or greater, but α_{DC} is always less than 1.

Common base biasing

A typical common base biasing configuration appears in figure (1-47). Note that two supplies are used in this configuration and the base is the common terminal between the input emitter terminal and the output collector terminal.

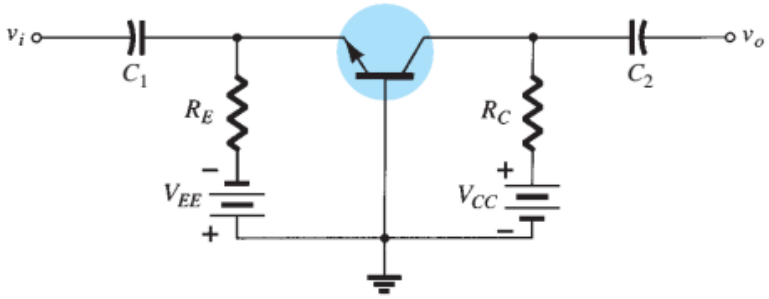


Figure (1-47) common base configuration

Applying KVL for the input loop will result in

$$V_{EE} = V_{BE} + I_E R_E$$

$$I_E = \left(\frac{V_{EE} - V_{BE}}{R_E}\right)$$

Applying KVL to the entire outside perimeter of the network of figure (1-29) will result in

$$V_{CC} + V_{EE} = I_E R_E + V_{CE} + I_C R_C$$

$$V_{CE} = V_{CC} + V_{EE} - I_C(R_C + R_E)$$

V_{CB} can be found by applying KVL to the output loop

$$V_{CB} = V_{CC} - I_C R_C$$

EXAMPLE 4.17 Determine the currents I_E and I_B and the voltages V_{CE} and V_{CB} for the common-base configuration of Fig. 4.52.

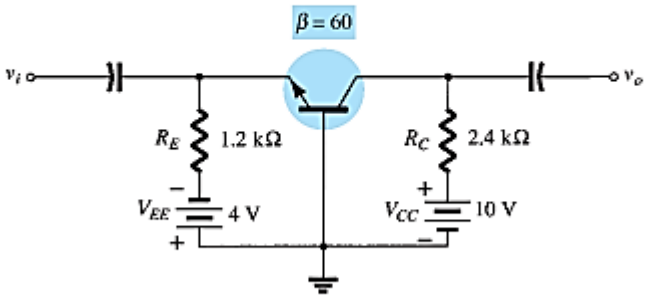


FIG. 4.52
Example 4.17.

Solution: Eq. 4.46:

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$= \frac{4\text{ V} - 0.7\text{ V}}{1.2\text{ k}\Omega} = \mathbf{2.75\text{ mA}}$$

$$I_B = \frac{I_E}{\beta + 1} = \frac{2.75\text{ mA}}{60 + 1} = \frac{2.75\text{ mA}}{61}$$

$$= \mathbf{45.08\ \mu A}$$

Eq. 4.47:

$$V_{CE} = V_{EE} + V_{CC} - I_E(R_C + R_E)$$
$$= 4\text{ V} + 10\text{ V} - (2.75\text{ mA})(2.4\text{ k}\Omega + 1.2\text{ k}\Omega)$$
$$= 14\text{ V} - (2.75\text{ mA})(3.6\text{ k}\Omega)$$
$$= 14\text{ V} - 9.9\text{ V}$$
$$= \mathbf{4.1\text{ V}}$$

Eq. 4.48:

$$V_{CB} = V_{CC} - I_C R_C = V_{CC} - \beta I_B R_C$$
$$= 10\text{ V} - (60)(45.08\ \mu\text{A})(24\text{ k}\Omega)$$
$$= 10\text{ V} - 6.49\text{ V}$$
$$= \mathbf{3.51\text{ V}}$$

AC Analysis of Common Base Configuration

EXAMPLE 5.8 For the network of Fig. 5.44, determine:

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.
e. A_i.

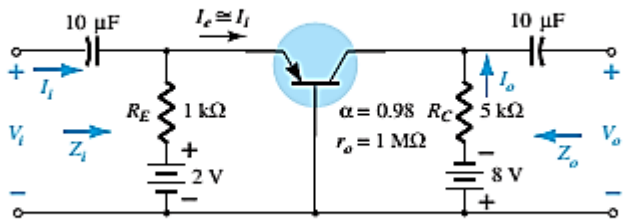


FIG. 5.44
Example 5.8.

Solution:

a. $$I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{2\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \frac{1.3\text{ V}}{1\text{ k}\Omega} = 1.3\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{1.3\text{ mA}} = \mathbf{20\ \Omega}$$

b. $$Z_i = R_E \| r_e = 1\text{ k}\Omega \| 20\ \Omega$$
$$= \mathbf{19.61\ \Omega} \cong r_e$$

c. $$Z_o = R_C = \mathbf{5\text{ k}\Omega}$$

d. $$A_v \cong \frac{R_C}{r_e} = \frac{5\text{ k}\Omega}{20\ \Omega} = \mathbf{250}$$

e. $$A_i = \mathbf{-0.98} \cong -1$$

Miscellaneous Bias Configurations

There are a number of BJT bias configurations that do not match the basic mold of those analyzed in the previous sections.

EXAMPLE 4.19 Determine V_C and V_B for the network of Fig. 4.54.

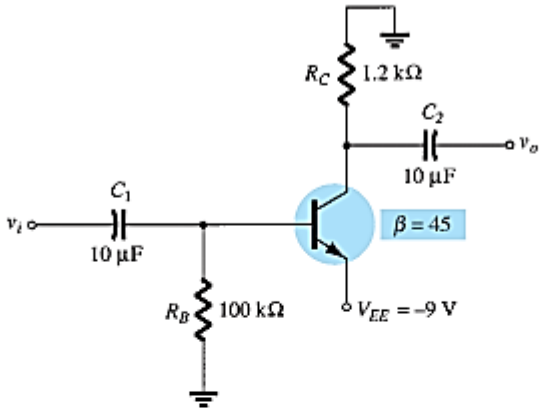


FIG. 4.54
Example 4.19.

Solution: Applying Kirchhoff's voltage law in the clockwise direction for the base–emitter loop results in

$$-I_B R_B - V_{BE} + V_{EE} = 0$$

and

$$I_B = \frac{V_{EE} - V_{BE}}{R_B}$$

Substitution yields

$$I_B = \frac{9\text{ V} - 0.7\text{ V}}{100\text{ k}\Omega} = \frac{8.3\text{ V}}{100\text{ k}\Omega} = 83\ \mu\text{A}$$

$$I_C = \beta I_B = (45)(83\ \mu\text{A}) = 3.735\text{ mA}$$

$$V_C = -I_C R_C = -(3.735\text{ mA})(1.2\text{ k}\Omega) = \mathbf{-4.48\text{ V}}$$

$$V_B = -I_B R_B = -(83\ \mu\text{A})(100\text{ k}\Omega) = \mathbf{-8.3\text{ V}}$$

Transistor Datasheet

A partial datasheet for the 2N3904 npn transistor is shown in Figure (1–50). Most specification sheets are broken down into maximum ratings, thermal characteristics, and electrical characteristics.
The electrical characteristics are further broken down into "on," "off," and small-signal characteristics. The "on" and "off" characteristics refer to dc limits, while the small signal characteristics include the parameters of importance to ac operation.
Notice that the maximum collector-emitter voltage (V_{CEO}) is 40 V. The CEO subscript indicates that the voltage is measured from collector (C) to emitter (E) with the base open (O). In the text, we use $V_{CE(max)}$ for this parameter. V_{CEsat} varies with I_C and V_{CE} (0.2v-0.3v)

Also notice that the maximum collector current (I_{Cmax}) is 200 mA. The maximum collector dissipation P_{Cmax} is 625mW. The derate factor under the maximum rating specifies that the maximum rating must be decreased 5 mW for every 1°rise in temperature above 25°C.

The $\beta_{DC}(h_{FE})$ is specified for several values of I_C. As you can see, h_{FE} varies with I_C as we previously discussed. The collector-emitter saturation voltage, $V_{CE(sat)}$ is 0.2 V maximum for $I_{C(sat)}$ 10 mA and increases with the current.

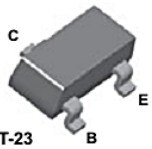
Limit of operation

$$0 \leq I_C \leq 200\ mA$$
$$0.2 - 0.3\ \leq V_{CE} \leq 40V$$
$$I_C V_{CE} \leq 625\ mW$$

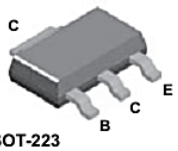
FAIRCHILD
SEMICONDUCTOR TM

2N3904 MMBT3904 PZT3904

TO-92



SOT-23
Mark: 1A



SOT-223

NPN General Purpose Amplifier

This device is designed as a general purpose amplifier and switch. The useful dynamic range extends to 100 mA as a switch and to 100 MHz as an amplifier.

Absolute Maximum Ratings* $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	60	V
V_{EBO}	Emitter-Base Voltage	6.0	V
I_C	Collector Current - Continuous	200	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics $T_A = 25°C$ unless otherwise noted

Symbol	Characteristic	Max			Units
		2N3904	*MMBT3904	**PZT3904	
P_D	Total Device Dissipation Derate above 25°C	625 5.0	350 2.8	1,000 8.0	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3			°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	357	125	°C/W

*Device mounted on FR-4 PCB 1.6" X 1.6" X 0.06."
**Device mounted on FR-4 PCB 36 mm X 18 mm X 1.5 mm; mounting pad for the collector lead min. 6 cm^2.

Electrical Characteristics $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 1.0 mA, I_B = 0	40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10 µA, I_E = 0	60		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10 µA, I_C = 0	6.0		V
I_{BL}	Base Cutoff Current	V_{CE} = 30 V, V_{EB} = 3V		50	nA
I_{CEX}	Collector Cutoff Current	V_{CE} = 30 V, V_{EB} = 3V		50	nA
ON CHARACTERISTICS*					
h_{FE}	DC Current Gain	I_C = 0.1 mA, V_{CE} = 1.0 V I_C = 1.0 mA, V_{CE} = 1.0 V I_C = 10 mA, V_{CE} = 1.0 V I_C = 50 mA, V_{CE} = 1.0 V I_C = 100 mA, V_{CE} = 1.0 V	40 70 100 60 30	 300 	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA I_C = 50 mA, I_B = 5.0 mA		0.2 0.3	V V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA I_C = 50 mA, I_B = 5.0 mA	0.65	0.85 0.95	V V
SMALL SIGNAL CHARACTERISTICS					
f_T	Current Gain - Bandwidth Product	I_C = 10 mA, V_{CE} = 20 V, f = 100 MHz	300		MHz
C_{obo}	Output Capacitance	V_{CB} = 5.0 V, I_E = 0, f = 1.0 MHz		4.0	pF
C_{ibo}	Input Capacitance	V_{EB} = 0.5 V, I_C = 0, f = 1.0 MHz		8.0	pF
NF	Noise Figure	I_C = 100µA, V_{CE} = 5.0 V, R_S =1.0kΩ,f=10 Hz to 15.7kHz		5.0	dB
SWITCHING CHARACTERISTICS					
t_d	Delay Time	V_{CC} = 3.0 V, V_{BE} = 0.5 V,		35	ns
t_r	Rise Time	I_C = 10 mA, I_{B1} = 1.0 mA		35	ns
t_s	Storage Time	V_{CC} = 3.0 V, I_C = 10mA		200	ns
t_f	Fall Time	I_{B1} = I_{B2} = 1.0 mA		50	ns

*Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%

Figure (1-50) Partial datasheet. For a complete 2N3904 datasheet, go to http://www.fairchildsemi.com/ds/2N%2F2N3904.pdf.Copyright Fairchild Semiconductor Corporation. Used by permission

Design Operations

The design process is one where a current and/or voltage may be specified and the elements required to establish the designated levels must be determined. The path toward a solution is less defined and in fact may require a number of basic assumptions that do not have to be made when simply analyzing a network. If the transistor and supplies are specified, the design process will simply determine the required resistors for a particular design. Once the theoretical values of the resistors are determined, the nearest standard commercial values are normally chosen and any variations due to not using the exact resistance values are accepted as part of the design.

One of the important and useful assumption is that the voltage from emitter to ground is typically around one-fourth to one-tenth of the supply voltage.

$$V_E \leq \left(\frac{1}{4} \rightarrow \frac{1}{10}\right) V_{CC}$$

EXAMPLE 4.21 Given the device characteristics of Fig. 4.59a, determine V_{CC}, R_B, and R_C for the fixed-bias configuration of Fig. 4.59b.

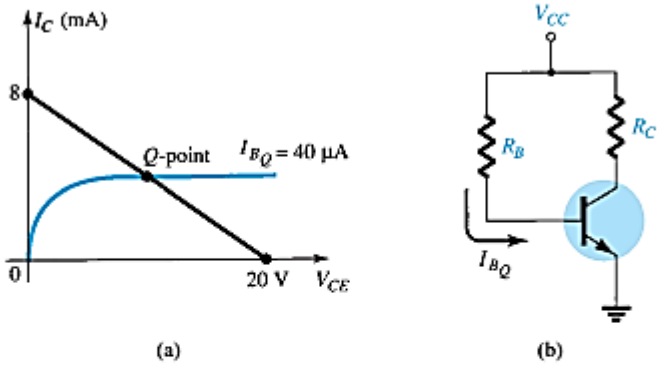


FIG. 4.59
Example 4.21.

Solution: From the load line

$$V_{CC} = \mathbf{20\ V}$$

$$I_C = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE}=0\ V}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\ V}{8\ mA} = \mathbf{2.5\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

with
$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$
$$= \frac{20\text{ V} - 0.7\text{ V}}{40\ \mu\text{A}} = \frac{19.3\text{ V}}{40\ \mu\text{A}}$$
$$= \mathbf{482.5\ k\Omega}$$

Standard resistor values are
$$R_C = 2.4\ \text{k}\Omega$$
$$R_B = 470\ \text{k}\Omega$$

Using standard resistor values gives
$$I_B = 41.1\ \mu\text{A}$$

which is well within 5% of the value specified.

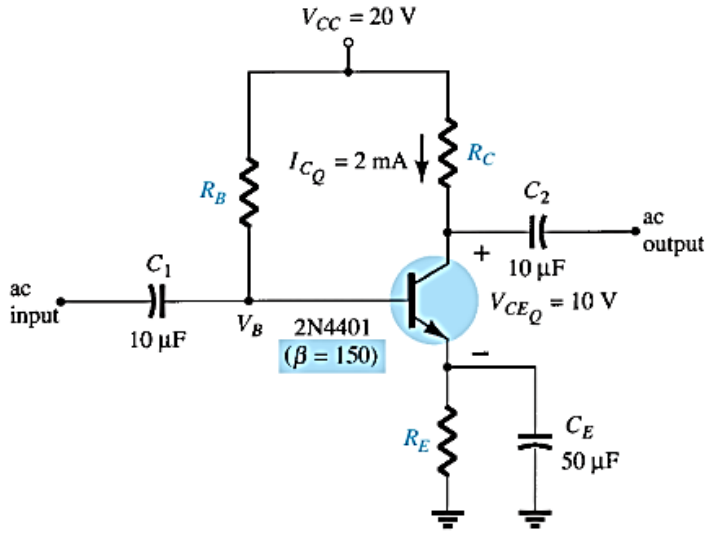


FIG. 4.62
Emitter-stabilized bias circuit for design consideration.

EXAMPLE 4.24 Determine the resistor values for the network of Fig. 4.62 for the indicated operating point and supply voltage.

Solution:

$$V_E = \tfrac{1}{10}V_{CC} = \tfrac{1}{10}(20\text{ V}) = 2\text{ V}$$
$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2\text{ V}}{2\text{ mA}} = \mathbf{1\ k\Omega}$$
$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20\text{ V} - 10\text{ V} - 2\text{ V}}{2\text{ mA}} = \frac{8\text{ V}}{2\text{ mA}}$$
$$= \mathbf{4\ k\Omega}$$
$$I_B = \frac{I_C}{\beta} = \frac{2\text{ mA}}{150} = 13.33\ \mu\text{A}$$
$$R_B = \frac{V_{R_B}}{I_B} = \frac{V_{CC} - V_{BE} - V_E}{I_B} = \frac{20\text{ V} - 0.7\text{ V} - 2\text{ V}}{13.33\ \mu\text{A}}$$
$$\cong \mathbf{1.3\ M\Omega}$$

Multiple BJT Networks

Two or more amplifiers can be connected in a cascaded arrangement with the output of one amplifier driving the input of the next. Each amplifier in a cascaded arrangement is known as a stage. The basic purpose of a multistage arrangement is to increase the overall voltage gain.

Capacitively (or RC) Coupled Multistage Amplifier

As shown in figure (1-51) the collector output of the first stage is fed directly into the base of the next stage using coupling capacitor (C_C). Capacitive coupling prevents the dc bias of one stage from affecting that of the other but allows the ac signal to pass without attenuation because $X_C=0$ at the frequency of operation. The same coupling can be used between any combinations of networks. Substituting an open circuit equivalent for CC and other capacitors of the network will result in tow voltage divider biasing networks so the introduced methods of analysis can be used.

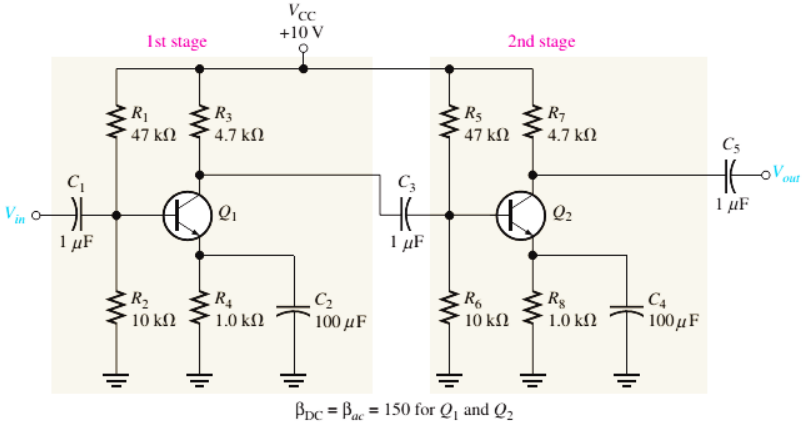


Figure (1-51) two-stage common-emitter amplifier

Direct-Coupled Multistage Amplifiers

A basic two-stage, direct-coupled amplifier is shown in Figure (1-52). Notice that there are no coupling or bypass capacitors in this circuit.

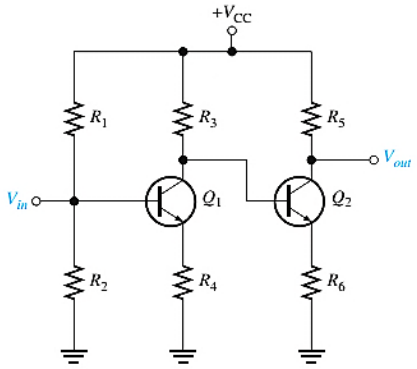


Figure (1-52) A basic two-stage direct-coupled amplifier.

Because of the direct coupling, this type of amplifier has a better low-frequency response than the capacitively coupled type in which the reactance of coupling and bypass capacitors at very low frequencies may become excessive. The increased reactance of capacitors at lower frequencies produces gain reduction in capacitively coupled amplifiers.

Direct-coupled amplifiers can be used to amplify low frequencies all the way down to dc (0 Hz) without loss of voltage gain because there are no capacitive reactances in the circuit. The disadvantage of direct-coupled amplifiers, on the other hand, is that small changes in the dc bias voltages from temperature effects or power-supply variation are amplified by the succeeding stages, which can result in a significant drift in the dc levels throughout the circuit.

EXAMPLE 4.26 Determine the dc levels for the currents and voltages of the direct-coupled amplifier of Fig. 4.72. Note that it is a voltage-divider bias configuration followed by a common-collector configuration; one that is excellent in cases wherein the input impedance of the next stage is quite low. The common-collector amplifier is acting like a **buffer** between stages.

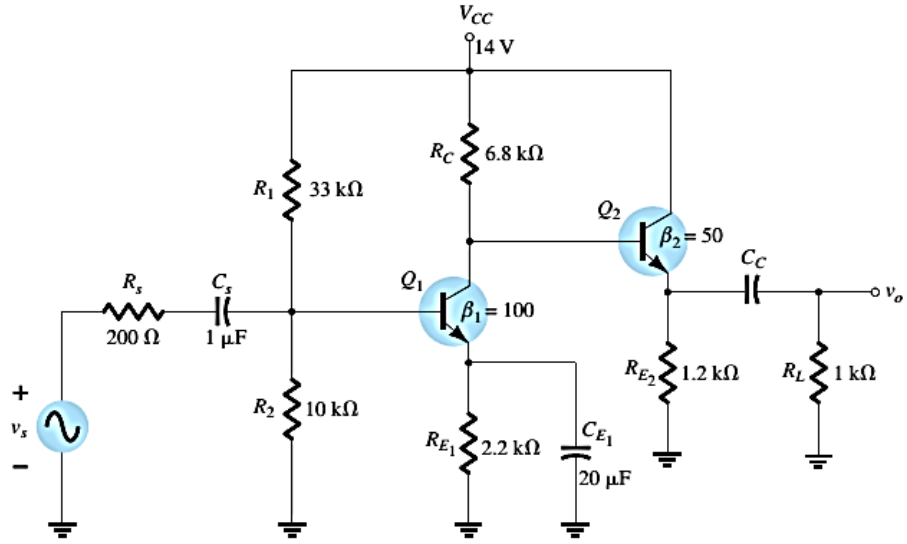


FIG. 4.72
Direct-coupled amplifier.

Solution: The dc equivalent of Fig. 4.72 appears as Fig. 4.73. Note that the load and source are no longer part of the picture. For the voltage-divider configuration, the following equations for the base current were developed in Section 4.5.

$$I_{B_1} = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_{E_1}}$$

with $$R_{\text{Th}} = R_1 \| R_2$$

and $$E_{\text{Th}} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

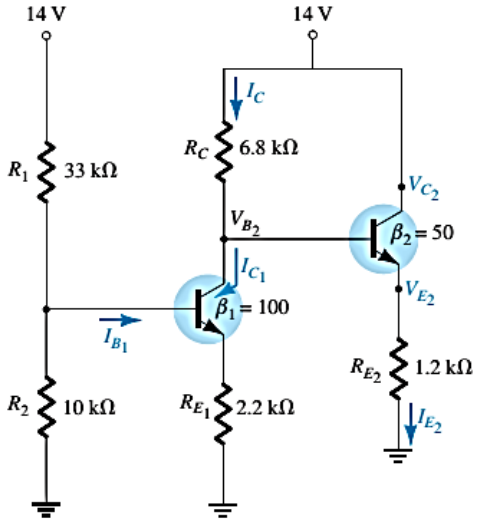


FIG. 4.73
DC equivalent of Fig. 4.72.

In this case,

$$R_{\text{Th}} = 33\,\text{k}\Omega \| 10\,\text{k}\Omega = 7.67\,\text{k}\Omega$$

and $$E_{\text{Th}} = \frac{10\,\text{k}\Omega(14\,\text{V})}{10\,\text{k}\Omega + 33\,\text{k}\Omega} = 3.26\,\text{V}$$

so that
$$I_{B_1} = \frac{3.26\text{ V} - 0.7\text{ V}}{7.67\text{ k}\Omega + (100 + 1)\,2.2\text{ k}\Omega}$$
$$= \frac{2.56\text{ V}}{229.2\text{ k}\Omega}$$
$$= \mathbf{11.17\ \mu A}$$

with
$$I_{C_1} = \beta I_{B_1}$$
$$= 100\,(11.17\ \mu\text{A})$$
$$= \mathbf{1.12\text{ mA}}$$

In Fig. 4.73 we find that

$$\boxed{V_{B_2} = V_{CC} - I_C R_C} \tag{4.76}$$
$$= 14\text{ V} - (1.12\text{ mA})(6.8\text{ k}\Omega)$$
$$= 14\text{ V} - 7.62\text{ V}$$
$$= \mathbf{6.38\text{ V}}$$

and
$$V_{E_2} = V_{B_2} - V_{BE_2}$$
$$= 6.38\text{ V} - 0.7\text{ V}$$
$$= \mathbf{5.68\text{ V}}$$

resulting in

$$\boxed{I_{E_2} = \frac{V_{E_2}}{R_{E_2}}} \tag{4.77}$$
$$= \frac{5.68\text{ V}}{1.2\text{ k}\Omega}$$
$$= \mathbf{4.73\text{ mA}}$$

Obviously,

$$\boxed{V_{C_2} = V_{CC}} \tag{4.78}$$
$$= 14\text{ V}$$

and
$$V_{CE_2} = V_{C_2} - V_{E_2}$$

$$\boxed{V_{CE_2} = V_{CC} - V_{E_2}} \tag{4.79}$$
$$= 14\text{ V} - 5.68\text{ V}$$
$$= \mathbf{8.32\text{ V}}$$

The Darlington Pair

One way to boost input resistance is to use a Darlington pair, as shown in Figure (1-53). The collectors of two transistors are connected, and the emitter of the first drives the base of the second.

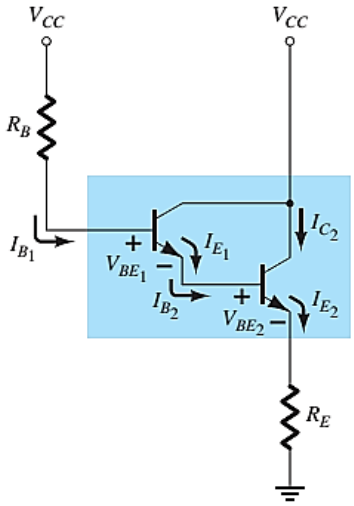


Figure (1-53) Darlington Pair

This configuration achieves multiplication as shown in the following steps. The emitter current of the first transistor is

$$I_{E1} = \beta_1 I_{B1}$$

This emitter current becomes the base current for the second transistor, producing a second emitter current of

$$I_{E2} = \beta_2 I_{E1} = \beta_1 \beta_2 I_{B1}$$

Therefore, the effective current gain of the Darlington pair is

$$\beta_D = \beta_1 \beta_2$$

As you have seen, β is a major factor in determining the input resistance of an amplifier so that the Darlington pair has a very high input impedance which equal

$$R_{in} = (1 + \beta_D) R_E$$

Applying the analysis similar to what we do for the previous circuits will result in the following equations for the base current (if there is R_B and V_{cc} in the circuit

$$I_{B1} = \frac{V_{CC} - V_{BE1} - V_{BE2}}{R_B + (1 + \beta_D) R_E}$$

The currents

$$I_{C2} = I_{E2} = \beta_D I_{B1}$$

And the DC voltage at the emitter terminal is

$$V_{E2} = I_{E2} R_E$$

The collector voltage of this configuration is

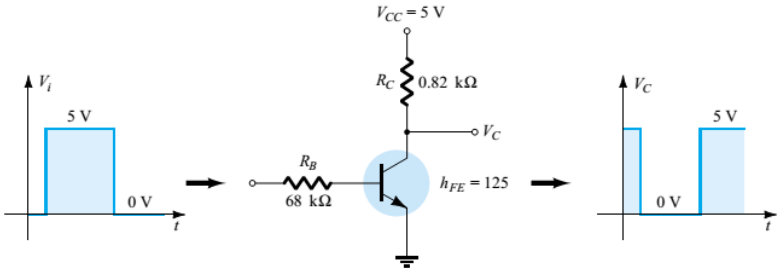
$$V_{C2} = V_{CC}$$

AC Analysis of Darlington Pairs

Transistor Switching Networks

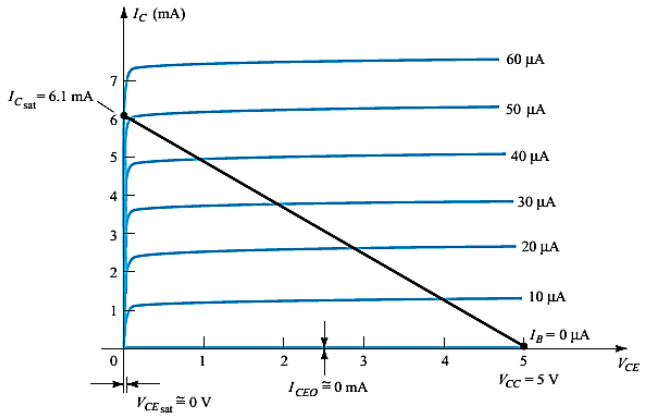
The second major application area is switching applications. When used as an electronic switch, a BJT is normally operated alternately in cutoff and saturation. Many digital circuits use the BJT as a switch and inverter. The network of Figure (1-56) can be employed as an inverter in computer logic circuitry.

Figure (1-56)



Proper design for the inversion process requires that the operating point switch from cutoff to saturation along the load line depicted in Figure (1-57).

Figure (1-57).



For our purpose we will assume

$$when\ I_B = 0\mu A \quad I_C = I_{CEO} = 0mA$$

$$V_{CE(sat)} = 0V$$

When $V_i = 5V$, the transistor will be "on"and the design must ensure that the network is heavily saturated this required

$$I_B > 50\mu A$$

The saturation level for the collector current for the circuit of Figure (1-32) is defined by

$$I_{C(sat)} = \frac{V_{CC}}{R_C}$$

For the saturation level we must therefore ensure that the following condition is satisfied

$$I_B > \frac{I_{C(sat)}}{\beta_{DC}}$$

For the network of Figure (1-32)

$$I_B = \frac{V_i - V_{BE}}{R_B} = \frac{5 - 0.7}{86\ K} = 63\ \mu A$$

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{5}{0.82\ K} \cong 6.1\ mA$$

Testing the condition

$$I_B > \frac{I_{C(sat)}}{\beta_{DC}}$$

$$63\ \mu A > \frac{6.1\ mA}{125} = 48.8\ \mu A$$

For $V_i = 0V$, $I_B = 0, I_C = 0$, $VR_C = 0$ then $V_C = 5V$

Figure (1-58) illustrates the basic operation of a BJT as a switching device. In part (a), the transistor is in the cutoff region because the base-emitter junction is not forward-biased. In this condition, there is, ideally, an open between collector and emitter, as indicated by the switch equivalent. The cutoff condition will result in a resistance level of the following magnitude:

$$R_{cutoff} = \frac{V_{CC}}{I_{CEO}}$$

In part (b), the transistor is in the saturation region because the base emitter junction and the base-collector junction are forward-biased and the base current is made large enough to cause the collector current to reach its saturation value. In this condition, there is, ideally, a short between collector and emitter, as indicated by the switch equivalent. Actually, a small voltage drop across the transistor of up to a few tenths of a volt normally occurs, which is the saturation voltage, $V_{CE(sat)}$. The result is a resistance level between the two terminals determined by

$$R_{sat} = \frac{V_{CE(sat)}}{I_{C(sat)}}$$

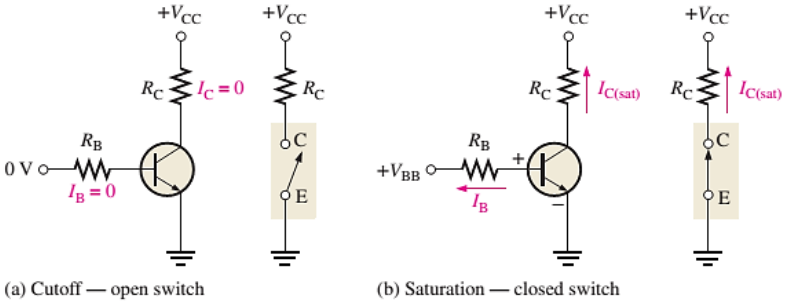


Figure (1-58)
Switching action of an ideal transistor

Example 4.32 page 213

Maximum Transistor Ratings

A BJT, like any other electronic device, has limitations on its operation. These limitations are stated in the form of maximum ratings and are normally specified on the manufacturer's datasheet. One must simply be sure that I_C, V_{CE}, and their product ($V_{CE} \times I_C$) fall into the range appearing in the following equations

$$I_{CEO} \leq I_C \leq I_{Cmax}$$
$$V_{CEsat} \leq V_{CE} \leq V_{CEmax}$$
$$V_{CE} I_C \leq P_{Cmax}$$

Bias Stabilization

The stability of a system is a measure of the sensitivity of a network to variations in its parameters. In any amplifier employing a transistor the collector current I_C is sensitive to each of the following parameters:

- **β: Increases with increase in temperature**
- **$|V_{BE}|$: decreases about 2.5 mV per degree Celsius (°C) increase in temperature.**
- **I_{CO} (reverse saturation current): doubles in value for every 10°C increase in temperature.**

Any or all of these factors can cause the bias point to drift from the designed point of operation.

Stability Factors, S(I_{CO}), S(V_{BE}), and S(β):

S(I_{CO}) : The rate of change of the collector current (IC) with respect to the leakage current (ICO) at a constant input voltage (VBE) and amplification factor (β).

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}}$$

As you see before I_C is comprised of two components: the majority and minority carriers. The minority current component is called the leakage current and is given the symbol I_{CO}.

$$I_C = I_{CMajorty} + I_{COMinority}$$

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

The derivative of above equation to I_C give us:

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta) \frac{\partial I_{CO}}{\partial I_C}$$

$$\mathbf{S_{I_{CO}} = \frac{\partial I_C}{\partial I_{CO}} = \frac{(1+\beta)}{1-\beta(\partial I_B/\partial I_C)}}$$

The last equation can be used for calculating the stability factor ($\mathbf{S_{I_{CO}}}$) for any biasing configuration.

S(VBE) : The rate of change of the collector current (IC) with respect to the input voltage (VBE) at a constant leakage current (ICO) and amplification factor (β).

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$

S(VBE) : The rate of change of the collector current (IC) with respect to the amplification factor (β) at a constant input voltage (VBE) leakage current (ICO) and.

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C1}}{\beta_1 \beta_2} S_{I_{CO2}}$$

Networks that are quite stable and relatively insensitive to temperature variations have low stability factors. The higher the stability factor, the more sensitive is the network to variations in that parameter.

The total change in the collector current due to the three stability factors can be determined using the following equation:

$$\sum \partial \mathbf{I_C} = \mathbf{S_{I_{CO_o}}} \times \partial \mathbf{I_{CO}} + \mathbf{S_{V_{BE_o}}} \times \partial \mathbf{V_{BE}} + \mathbf{S_\beta} \times \partial \boldsymbol{\beta}$$

For the fixed bias configuration shown in figure (1-37)
Applying KVL for the input circuit

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$\frac{\partial \mathrm{I_B}}{\partial \mathrm{I_C}} = 0$$

So

$$\mathbf{S_{I_{CO}}} = \frac{\partial \mathbf{I_C}}{\partial \mathbf{I_{CO}}} = \mathbf{1} + \boldsymbol{\beta}$$

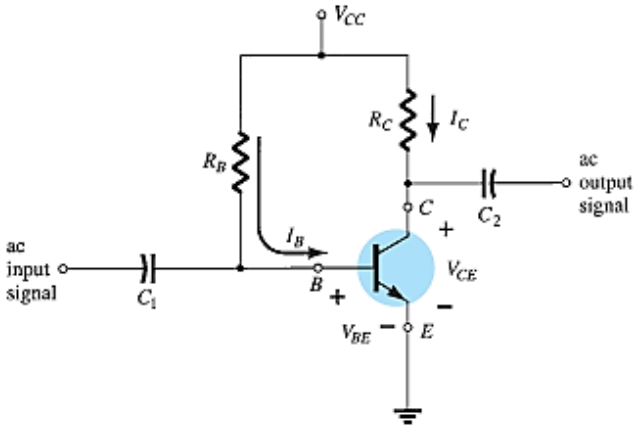


Figure (1-37)

$$I_C = \beta I_B = \beta \frac{V_{CC} - V_{BE}}{R_B}$$

$$\boldsymbol{S(V_{BE})} = \frac{\Delta \boldsymbol{I_C}}{\Delta \boldsymbol{V_{BE}}} = \frac{-\boldsymbol{\beta}}{\boldsymbol{R_B}}$$

$$\boldsymbol{S(\beta)} = \frac{\Delta \boldsymbol{I_C}}{\Delta \boldsymbol{\beta}} = \frac{\mathbf{I_{C1}}}{\boldsymbol{\beta_1 \beta_2}} \mathbf{S_{I_{CO2}}} = \frac{\mathbf{I_{C1}}}{\boldsymbol{\beta_1 \beta_2}} \boldsymbol{\beta_2} = \frac{\mathbf{I_{C1}}}{\boldsymbol{\beta_1}}$$

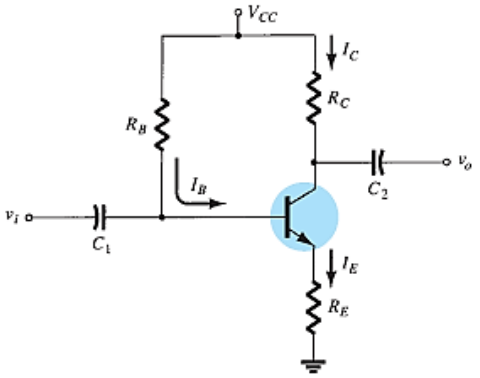
For emitter bias configuration

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$
$$I_E = I_B + I_C$$

$$V_{CC} = I_B(R_B + R_E) + V_{BE} + I_C R_E$$

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_E}{R_B + R_E}$$

$$\frac{\partial \mathrm{I_B}}{\partial \mathrm{I_C}} = \frac{-R_E}{R_B + R_E}$$



$$\mathbf{S_{I_{CO}} = \frac{\partial I_C}{\partial I_{CO}} = \frac{(1+\beta)}{1-\beta(\partial I_B/\partial I_C)} = \frac{(1+\beta)}{1+\beta\left(\frac{R_E}{R_B+R_E}\right)}}$$

$$I_C = \beta I_B = \beta \frac{V_{CC} - V_{BE} - I_C R_E}{R_B + R_E}$$

$$\boldsymbol{S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}} = \frac{-\beta}{R_B + (1+\beta)R_E}}$$

$$\mathbf{S_{I_{CO}2} = \frac{\partial I_C}{\partial I_{CO2}} = \frac{(1+\beta_2)}{1-\beta_2(\partial I_B/\partial I_C)} = \frac{(1+\beta_2)}{1+\beta_2\left(\frac{R_E}{R_B+R_E}\right)}}$$

$$\boldsymbol{S(\beta) = \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C1}}{\beta_1 \beta_2} S_{I_{CO2}}}$$

H.W Derive the expressions of ($S_{I_{CO}}$) for voltage divider bias configuration.

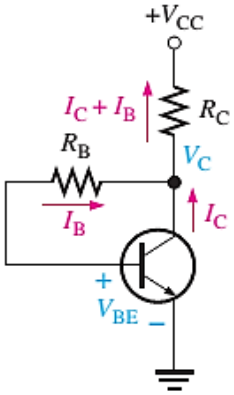
For collector feedback biasing circuit

$$V_{CC} = I_B R_B + V_{BE} + (I_c + I_B) R_C$$

$$V_{CC} = I_B (R_B + R_c) + V_{BE} + I_C R_C$$

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_B + R_C}$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_C}{R_B + R_C}$$



$$\mathbf{S_{I_{CO}} = \frac{\partial I_C}{\partial I_{CO}} = \frac{(1+\beta)}{1-\beta(\partial I_B/\partial I_C)} = \frac{(1+\beta)}{1+\beta\left(\frac{R_C}{R_B+R_C}\right)}}$$

$$I_C = \beta I_B = \beta \frac{V_{CC} - V_{BE} - I_C R_C}{R_B + R_C}$$

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}} = \frac{-\beta}{R_B + (1+\beta)R_C}$$

$$S_{I_{CO2}} = \frac{\partial I_C}{\partial I_{CO}} = \frac{(1+\beta_2)}{1-\beta_2(\partial I_B/\partial I_C)} = \frac{(1+\beta_2)}{1+\beta_2\left(\frac{R_C}{R_B+R_C}\right)}$$

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C1}}{\beta_1\beta_2} S_{I_{CO2}}$$

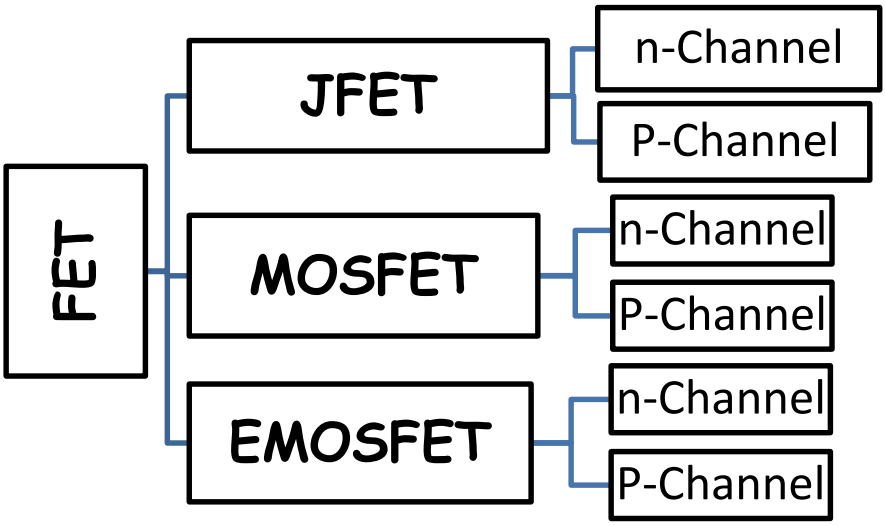
The Field Effect Transistor (FET)

The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor. The BJT transistor is a current-controlled device, whereas the FET transistor is a voltage-controlled device. The FET is a unipolar device depending solely on either electron (n-channel) or hole (p-channel) conduction.

The most important characteristics of the FET is

1- Its high input impedance. FETs are more temperature stable than BJTs.
2- FETs are usually smaller than BJTs, making them particularly useful in integrated-circuit (IC) chips.

There are three types of FETs:



MOSFETs are further broken down into depletion type and enhancement type.

The Junction Field Effect Transistor (JFET)

Construction and Characteristics of JFETS

Figure (2-1) shows the basic structure of an n-channel JFET (junction field-effect transistor). Wire leads are connected to each end of the n-channel; the **drain** is at the upper end, and the **source** is at the lower end. Two p-type regions are diffused in the n-type material to form a channel, and both p-type regions are connected to the **gate** lead.

The result is a depletion region at each junction, as shown in Figure (2-1) that resembles the same region of a diode under no-bias conditions. Recall also that a depletion region is void of free carriers and is therefore unable to support conduction.

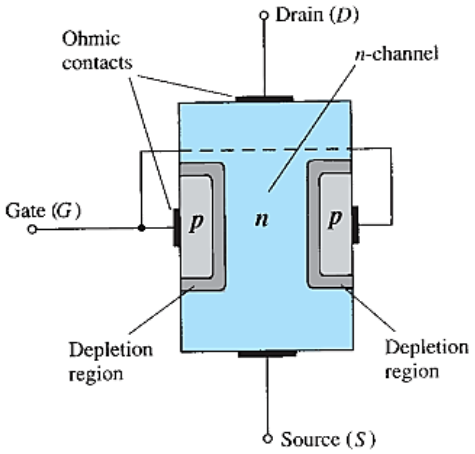


Figure (2-1) Junction field-effect transistor

Basic Operation of JFET

To illustrate the operation of a JFET, Figure (2–2) shows dc bias voltages applied to an n-channel device. VDD provides a drain-to-source voltage and supplies current from drain to source. VGG sets the reverse-bias voltage between the gate and the source, as shown. **The JFET is always operated with the gate-source pn junction reverse-biased.** Reverse biasing of the gate-source junction with a negative gate voltage produces a depletion region along the pn junction, which extends into the n channel and thus increases its resistance by restricting the channel width.

The channel width and thus the channel resistance can be controlled by varying the gate voltage, thereby controlling the amount of drain current, ID. Figure (2–3) illustrates this concept. The white areas represent the depletion region created by the reverse bias. It is wider toward the drain end of the channel because the reverse-bias voltage between the gate and the drain is greater than that between the gate and the source.

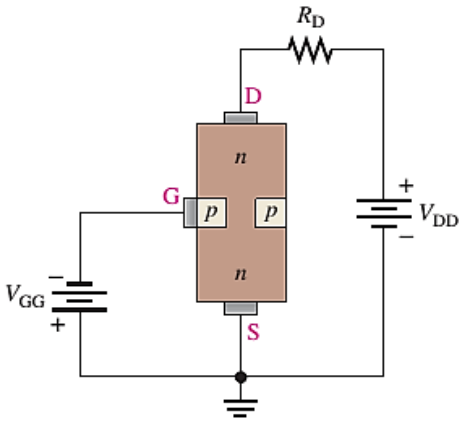
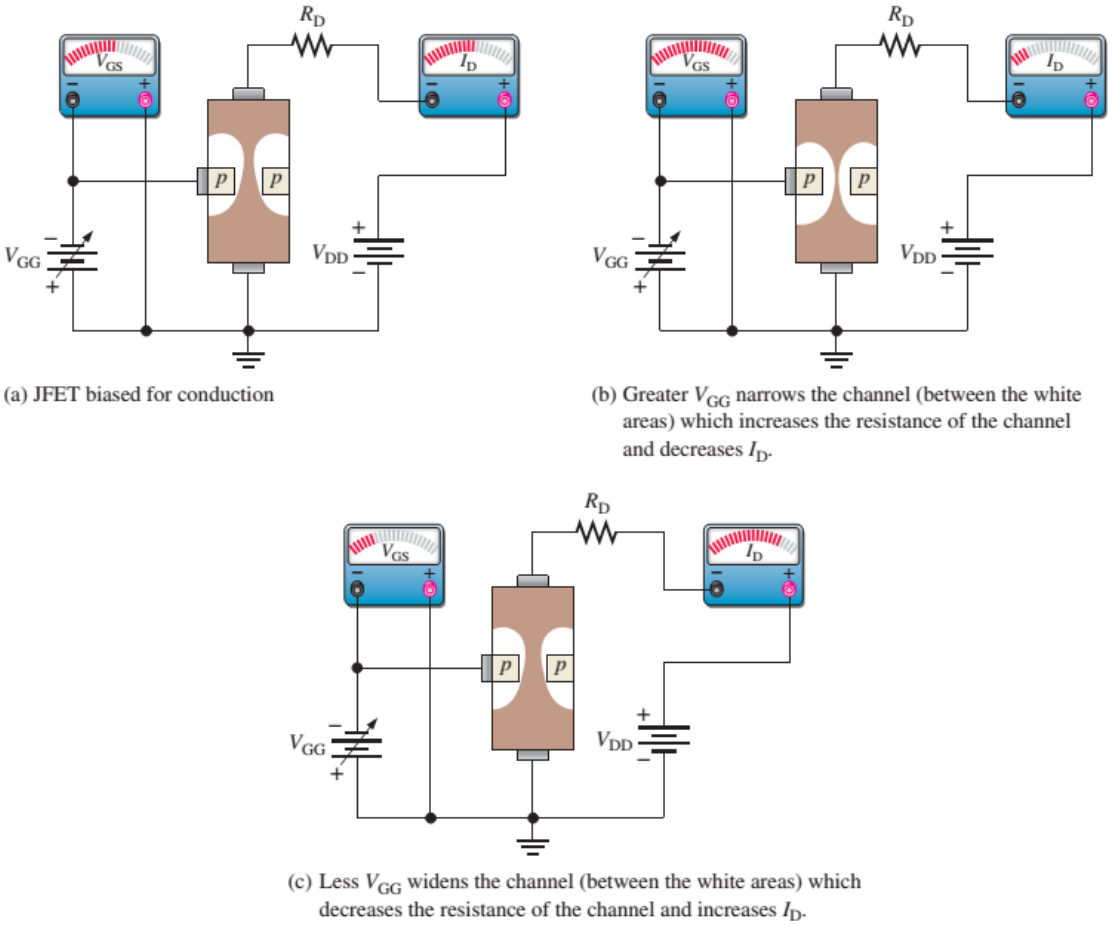


Figure (2-2) A biased n-channel JFET.



(a) JFET biased for conduction

(b) Greater V_{GG} narrows the channel (between the white areas) which increases the resistance of the channel and decreases I_D.

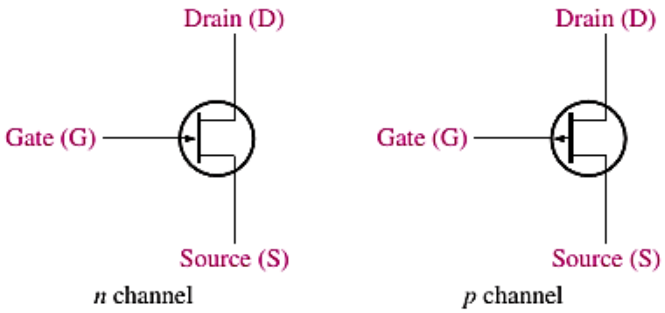
(c) Less V_{GG} widens the channel (between the white areas) which decreases the resistance of the channel and increases I_D.

Figure (2-3) Effects of VGS on channel width, resistance, and drain current (VGG =VGS).

JFET Symbols

The schematic symbols for both n-channel and p-channel JFETs are shown in Figure (2-4). Notice that the arrow on the gate points "in" for n channel and "out" for p channel.

Figure (2-4) JFET schematic symbols



JFET Characteristics and Parameters

Drain Characteristic Curve

Consider the case when the gate-to-source voltage is zero (VGS=0 V). As VDD (and thus VDS) is increased from 0 V, ID will increase proportionally, as shown in the graph of Figure (2-5b) between points A and B .In this area, the channel resistance is essentially constant because the depletion region is not large enough to have significant effect. This is called the Ohmic region because VDS and ID are related by Ohm's law. At point B in Figure (2-5b), the curve levels off and enters the active region where ID becomes essentially constant. As VDS increases from point B to point C, the reverse-bias voltage from gate to drain (VGD) produces a depletion region large enough to offset the increase in VDS, thus keeping ID relatively constant.

Pinch-Off Voltage: For VGS 0 V, the value of VDS at which ID becomes essentially constant (point B on the curve in Figure 2-5(b)) is the pinch-off voltage, VP. For a given JFET, VP has a fixed value. As you can see, a continued increase in VDS above the pinch-off voltage produces an almost constant drain current. This value of drain current is IDSS **(Drain to Source current with gate Shorted)** and is always specified on JFET datasheets. IDSS is the maximum drain current that a specific JFET can produce regardless of the external circuit, and it is always specified for the condition, VGS 0 V.

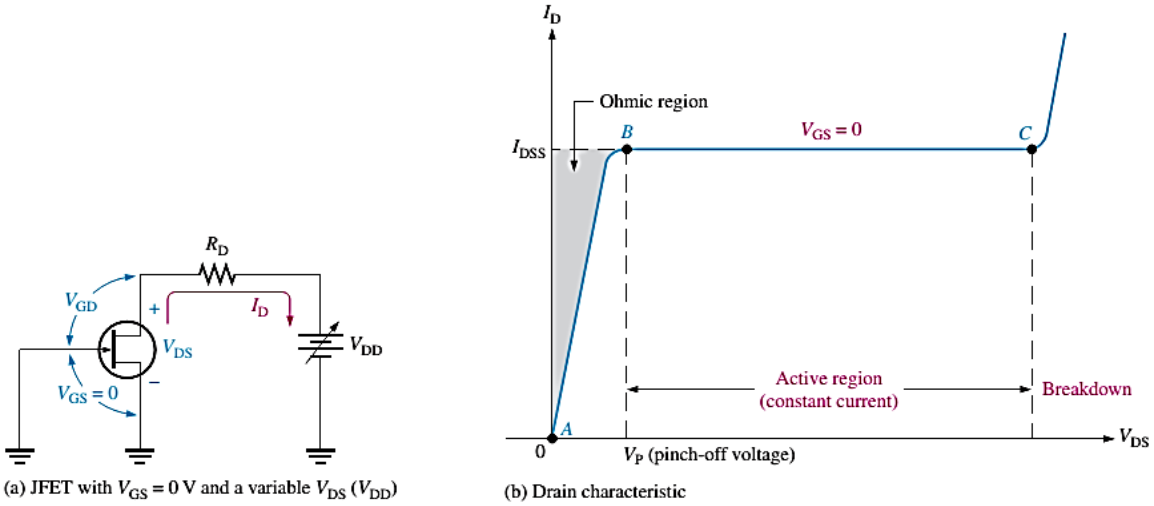
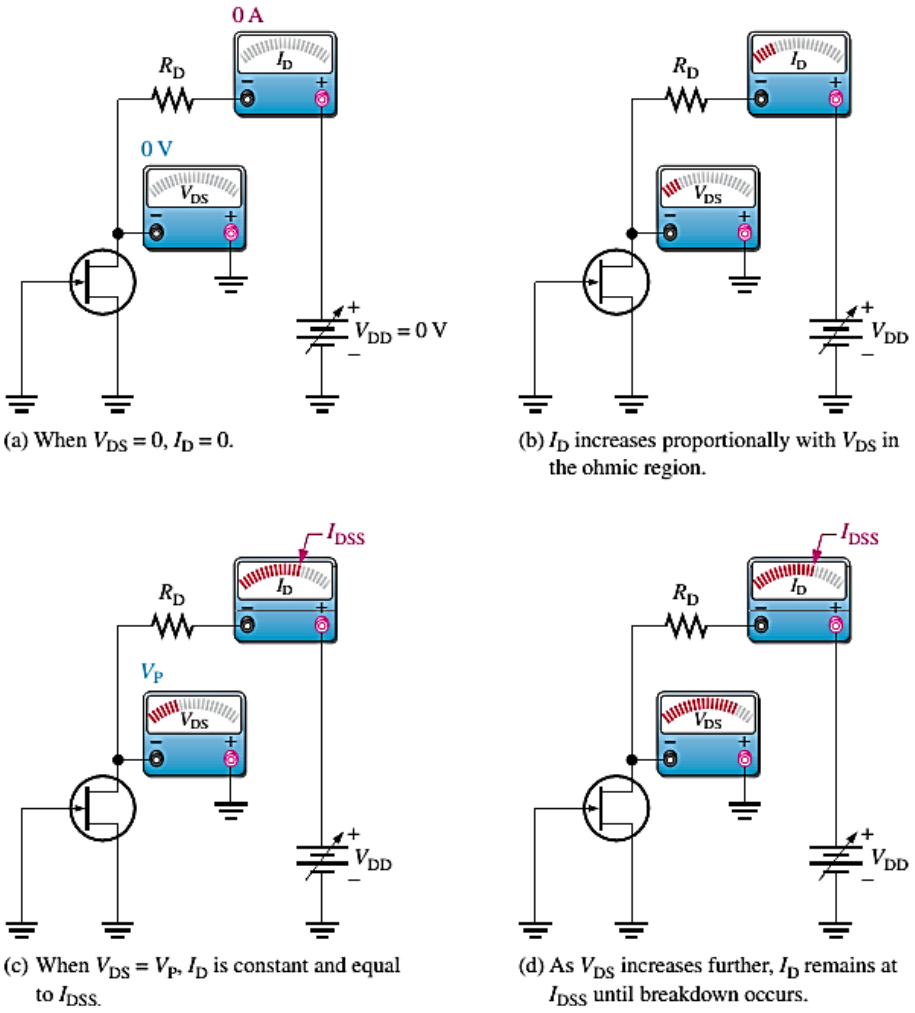


Figure (2-5) The drain characteristic curve of a JFET for VGS 0 showing pinch-off voltage.

Breakdown: As shown in the graph in Figure 2-5(b), breakdown occurs at point C when ID begins to increase very rapidly with any further

increase in VDS. Breakdown can result in irreversible damage to the device, so JFETs are always operated below breakdown and within the active region (constant current) (between points B and C on the graph). The JFET action that produces the drain characteristic curve to the point of breakdown for VGS = 0 V is illustrated in Figure 2-6.



(a) When $V_{DS} = 0$, $I_D = 0$.

(b) I_D increases proportionally with V_{DS} in the ohmic region.

(c) When $V_{DS} = V_P$, I_D is constant and equal to I_{DSS}.

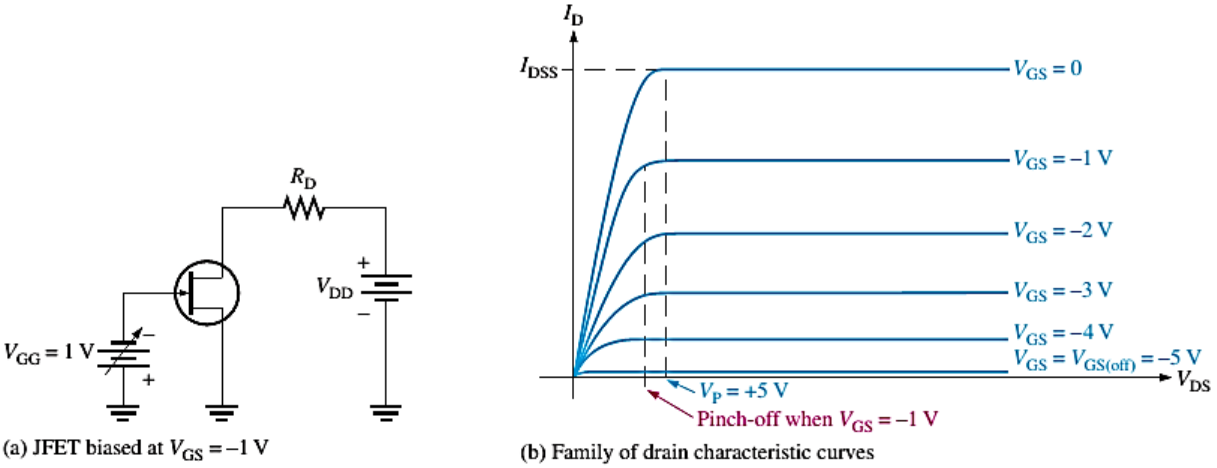
(d) As V_{DS} increases further, I_D remains at I_{DSS} until breakdown occurs.

Figure 2-6 JFET action that produces the characteristic curve for VGS 0 V.

VGS Controls ID

Let's connect a bias voltage, VGG, from gate to source as shown in Figure 2-7(a). As VGS is set to increasingly more negative values by adjusting VGG, a family of drain characteristic curves is produced, as shown in Figure 2-7(b). Notice that ID decreases as the magnitude of VGS is increased to larger negative values **because of the narrowing of the channel**. Also notice that, for each increase in VGS, the JFET reaches pinch-off (where constant current begins) at values of VDS less than VP. The term pinch-off is not the same as pinch-off voltage,

Vp. Therefore, the amount of drain current is controlled by VGS, as illustrated in Figure 2-8.



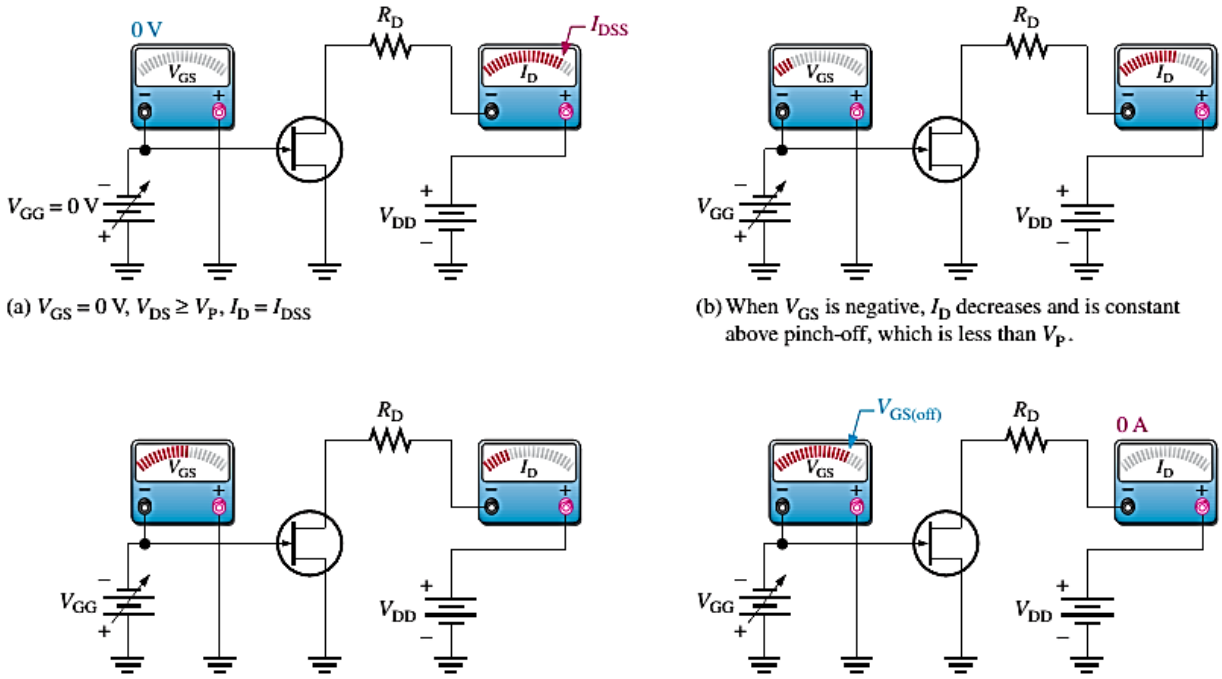
(a) JFET biased at $V_{GS} = -1$ V

(b) Family of drain characteristic curves

Figure 2-7 Pinch-off occurs at a lower VDS as VGS is increased to more negative values.

Cutoff Voltage

The value of VGS that makes ID approximately zero is the cutoff voltage, VGS(off), as shown in Figure 2-8(d). The JFET must be operated between VGS 0 V and VGS(off). For this range of gate-to source voltages, ID will vary from a maximum of IDSS to a minimum of almost zero



(a) $V_{GS} = 0$ V, $V_{DS} \geq V_P$, $I_D = I_{DSS}$

(b) When V_{GS} is negative, I_D decreases and is constant above pinch-off, which is less than V_P.

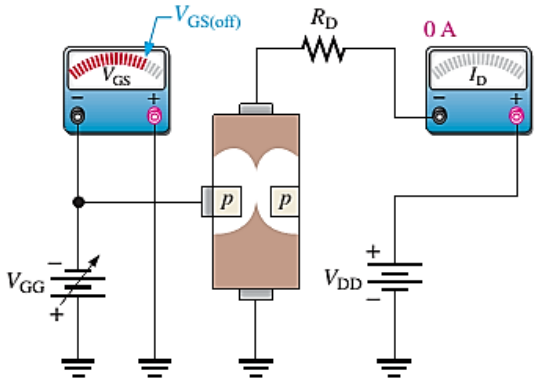
(c) As V_{GS} is made more negative, I_D continues to decrease but is constant above pinch-off, which has also decreased.

(d) Until $V_{GS} = -V_{GS(off)}$, I_D continues to decrease. When $V_{GS} \geq -V_{GS(off)}$, $I_D \cong 0$.

Figure 2-8 VGS controls ID.

As you have seen, for an n-channel JFET, the more negative VGS is, the smaller ID becomes in the active region. When VGS has a sufficiently large negative value, ID is reduced to zero. This cutoff effect is caused by the widening of the depletion region to a point where it completely closes the channel, as shown in Figure 2–9.

Figure 2-9 JFET at cutoff



Comparison of Pinch-Off Voltage and Cutoff Voltage

As you have seen, there is a difference between pinch-off and cutoff voltages. There is also a connection. The pinch-off voltage VP is the value of VDS at which the drain current becomes constant and equal to I_{DSS} and is always measured at VGS=0 V. However, pinch-off occurs for VDS values less than VP when VGS is nonzero. So, although VP is a constant, the minimum value of VDS at which ID becomes constant varies with VGS. VGS(off) and VP are always equal in magnitude but opposite in sign. A datasheet usually will give either VGS(off) or VP, but not both. However, when you know one, you have the other. For example, if VGS(off)=-5 V then VP = +5 V, as shown in Figure 2–7(b).

Transfer Characteristic

You have learned that a range of VGS values from zero to VGS(off) controls the amount of drain current. For an n-channel JFET, VGS(off) is negative, and for a p-channel JFET, VGS(off)is positive. Because VGS does control ID, the relationship between these two quantities is very important. The relationship between ID and VGS is defined by **Shockley's equation**

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The squared term in the equation results in a nonlinear relationship between I D and VGS , producing a curve that grows exponentially with decreasing magnitude of V GS .

Figure 2–12 is a general transfer characteristic curve that illustrates graphically the relationship between VGS and ID. This curve is also known as a trans-conductance curve.

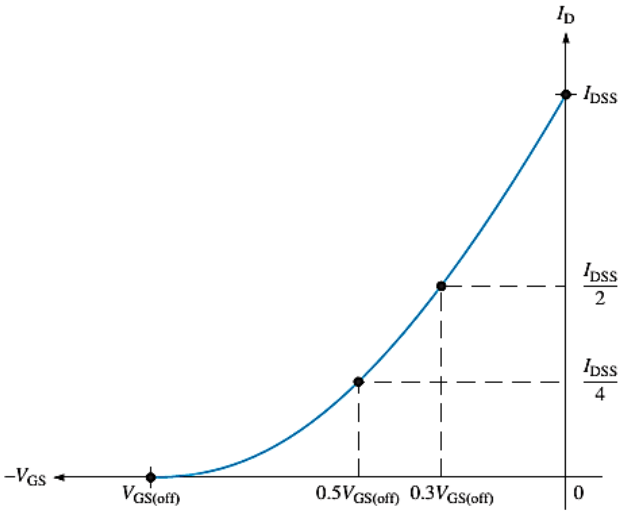


Figure 2-12 JFET universal transfer characteristic curve (n-channel).

Notice that the bottom end of the curve is at a point on the VGS axis equal to VGS(off), and the top end of the curve is at a point on the ID axis equal to IDSS. This curve shows that

$$I_D = 0 \; when \; V_{GS} = \; V_{GS(off)}$$

$$I_D = \frac{I_{DSS}}{4} \; when \; V_{GS} = 0.5 \; V_{GS(off)}$$

$$I_D = \frac{I_{DSS}}{2} \; when \; V_{GS} = 0.3 \; V_{GS(off)}$$

$$I_D = I_{DSS} \; when \; V_{GS} = 0$$

The transfer characteristic curve can also be developed from the drain characteristic curves by plotting values of ID for the values of VGS taken from the family of drain curves at pinch-off, as illustrated in Figure 2–13 for a specific set of curves. Each point on the transfer characteristic curve corresponds to specific values of VGS and ID on the drain curves.

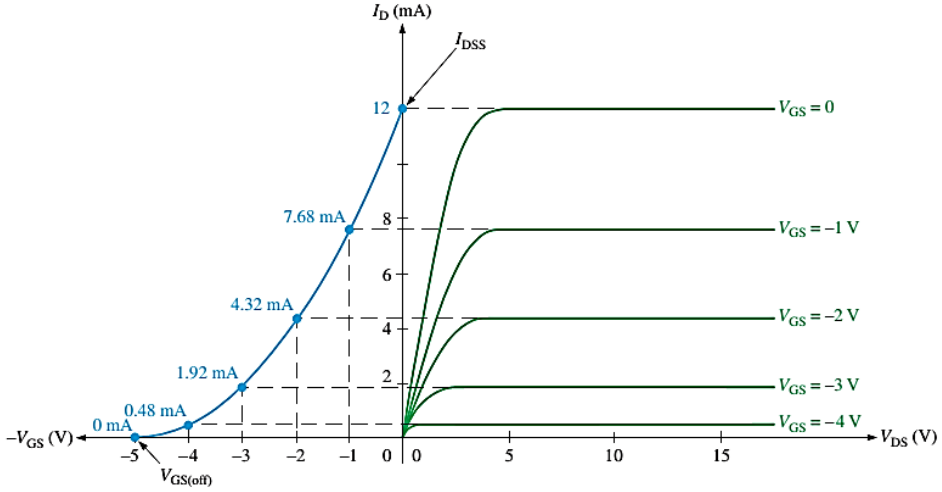


Figure 2-13 Example of the development of an n-channel JFET transfer characteristic curve (blue) from the JFET drain characteristic curves (green)

FET Datasheet

JFET Forward Trans-conductance

The forward trans-conductance (transfer conductance), gm, is the change in drain current for a given change in gate-to-source voltage with the drain-to-source voltage constant. It is expressed as a ratio and has the unit of siemens (S).

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

g_m is an important factor in determining the voltage gain of a FET amplifier.

Because the transfer characteristic curve for a JFET is nonlinear, g_m varies in value depending on the location on the curve as set by VGS. The value for g_m is greater near the top of the curve (near VGS = 0) than it is near the bottom (near VGS(off)), as illustrated in Figure 2-14.

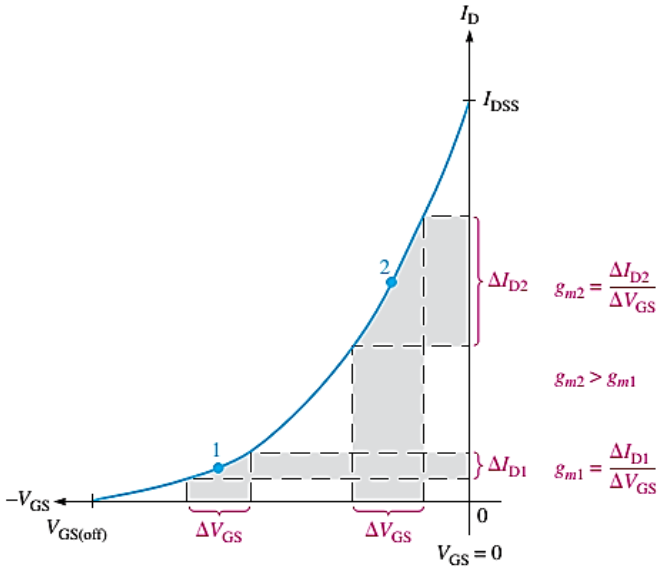
A datasheet normally gives the value of g_m measured at VGS=0 V (g_{m0}). Given g_{m0}, you can calculate an approximate value for g_m at any point on the transfer characteristic curve using the following formula:

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) = g_{m0}\left(\sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|}$$

On specification sheets, gm is often provided as g_{fs} or y_{fs}

Figure 2-14 g_m varies depending on the bias point (VGS).



EXAMPLE 8.1 Determine the magnitude of g_m for a JFET with $I_{DSS} = 8$ mA and $V_P = -4$ Vat the following dc bias points:

a. $V_{GS} = -0.5$ V.
b. $V_{GS} = -1.5$ V.
c. $V_{GS} = -2.5$ V.

Maximum Ratings

The maximum rating list usually appears at the beginning of the specification sheet, with the maximum voltages between specific terminals, maximum current levels, and the maximum power dissipation level of the device. The specified maximum levels for VDS , VDG and VGS must not be exceeded at any point in the design operation of the device. Any good design will try to avoid these levels by a good margin of safety. Although normally designed to operate with IG=0 mA, if forced to accept a gate current, it could withstand 10 mA (IGF) before damage would occur.

Thermal Characteristics

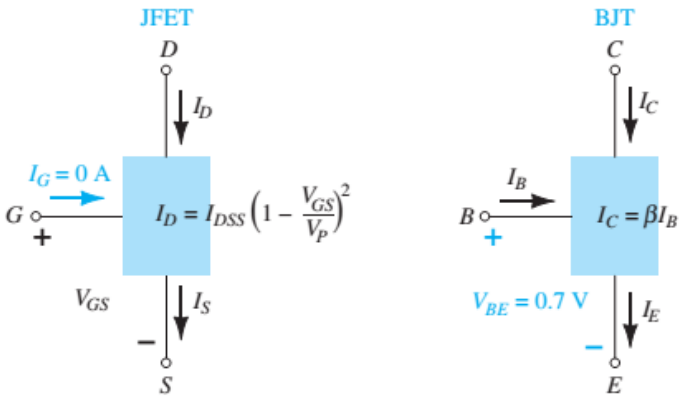
The total device dissipation at 25°C (room temperature) is the maximum power the device can dissipate under normal operating conditions and is defined by

$$P_D = V_{DS} I_D$$

Electrical Characteristics

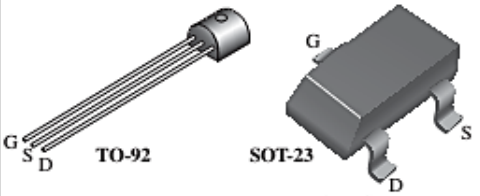
The electrical characteristics include the level of VP in the "off" characteristics and IDSS in the "on" characteristics. In this case VP=VGS(off) has a range from -0.5 V to -6.0 V and IDSS from 1 mA to 5 mA.

JFET		BJT
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0\ \text{A}$	$\Leftrightarrow$	$V_{BE} \cong 0.7\ \text{V}$



FAIRCHILD
SEMICONDUCTOR TM

2N5457 **MMBF5457**



NOTE: Source & Drain are interchangeable

N-Channel General Purpose Amplifier

This device is a low-level audio amplifier and switching transistor, and can be used for analog switching applications.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	25	V
V_{DG}	Drain-Gate Voltage	25	V
V_{GS}	Gate-Source Voltage	–25	V
I_{GF}	Forward Gate Current	10	mA
T_j, T_{stg}	Operating and Storage Junction Temperature Range	–55 to +150	°C

THERMAL CHARACTERISTICS

Symbol	Characteristic	Max		Units
		2N5457	*MMBF5457	
P_D	Total Device Dissipation Derate above 25°C	625 5.0	350 2.8	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	125		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	357	556	°C/W

ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	I_G = 10 µA, V_{DS} = 0		–25			V
I_{GSS}	Gate Reverse Current	V_{GS} = –15 V, V_{DS} = 0 V_{GS} = –15 V, V_{DS} = 0, T_A = 100°C				–1.0 –200	nA nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 15 V, I_D = 10 nA	5457	–0.5		–6.0	V
V_{GS}	Gate-Source Voltage	V_{DS} = 15 V, I_D = 100 µA	5457		–2.5		V
ON CHARACTERISTICS							
I_{DSS}	Zero-Gate Voltage Drain Current	V_{DS} = 15 V, V_{GS} = 0	5457	1.0	3.0	5.0	mA
SMALL SIGNAL CHARACTERISTICS							
g_{fs}	Forward Transfer Conductance	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 kHz	5457	1000		5000	µmhos
g_{os}	Output Conductance	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 MHz			10	50	µmhos
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 MHz			4.5	7.0	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 MHz			1.5	3.0	pF
NF	Noise Figure	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 kHz, R_G = 1.0 megohm, BW = 1.0 Hz				3.0	dB

Figure 2-15 JFET partial datasheet

Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

The MOSFET (metal oxide semiconductor field-effect transistor) is another category of field-effect transistor. The MOSFET, different from the JFET, has no pn junction structure; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO2) layer. The two basic types of MOSFETs are enhancement (E) and depletion (D). **These devices are generally operated in the depletion mode so it is called D-MOSFET.**

Basic Structure of MOSFET

Figure 2–16 illustrates the basic structure of the both n-channel and p-channel MOSFET. We will use the n-channel device to describe the basic structure and operation.

- A slab of p-type material is formed from a silicon base and is referred to as the substrate. In some cases the substrate is internally connected to the source terminal.
- The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel.
- The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon dioxide (SiO_2) layer.

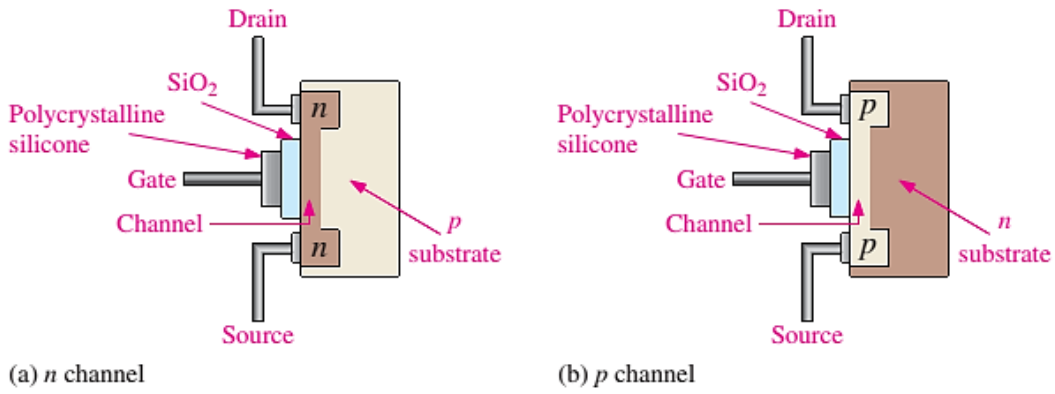


Figure 2-16 the basic structure of MOSFETs.

Basic Operation and Characteristics of MOSFET

The MOSFET can be operated in either of two modes—**the depletion mode or the enhancement mode**—and is sometimes called a depletion/enhancement MOSFET.

1- **Depletion Mode** The n-channel MOSFET operates in the depletion mode when a **negative** gate-to-source voltage is applied. With a negative gate voltage, the negative charges on the gate repel conduction electrons from the channel, leaving positive ions in their place. Thereby, the n channel is depleted of some of its electrons, thus decreasing the channel conductivity. The resulting current with VGS = 0 V continues to be labeled IDSS , as shown in Figure 2-18 .

The greater the negative voltage on the gate, the greater the depletion of n-channel electrons. At a sufficiently negative gate-to-source voltage, VGS(off), the channel is totally depleted and the drain current is zero as shown in figure (2-18). The resulting levels of drain current and the plotting of the transfer curve proceed exactly as described for the JFET. This depletion mode is illustrated in Figure 2–17(a).

2- **Enhancement Mode** With a positive gate voltage, more conduction electrons are attracted into the channel, thus increasing (enhancing) the channel conductivity, as illustrated in Figure 2-17(b). As VGS continues to increase in the positive direction, Figure 2-18 reveals that the drain current will increase at a rapid rate.

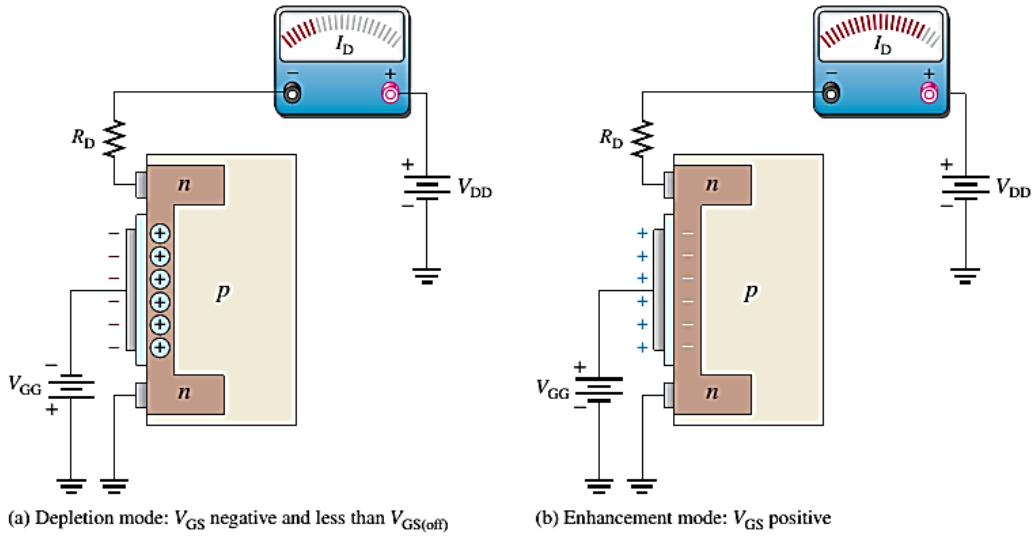


Figure 2-17 Operation of n-channel D-MOSFET

It is particularly interesting and helpful that Shockley's equation will continue to be applicable for the depletion-type MOSFET characteristics in both the depletion and enhancement regions.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

For both regions, it is simply necessary that the proper sign be included with VGS in the equation and the sign be carefully monitored in the mathematical operations.

The fact that Shockley's equation is also applicable to depletion-type MOSFETs (D-MOSFETs) results in the same equation for gm.

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) = g_{m0}\left(\sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|}$$

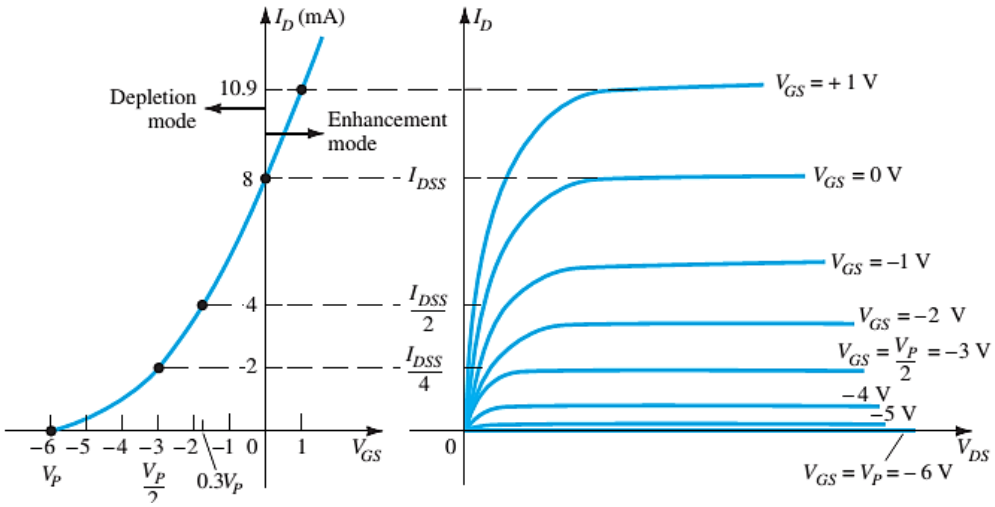


Figure 2-18 Drain and transfer characteristics for an n-channel depletion-type MOSFET

P-Channel Depletion-Type MOSFET

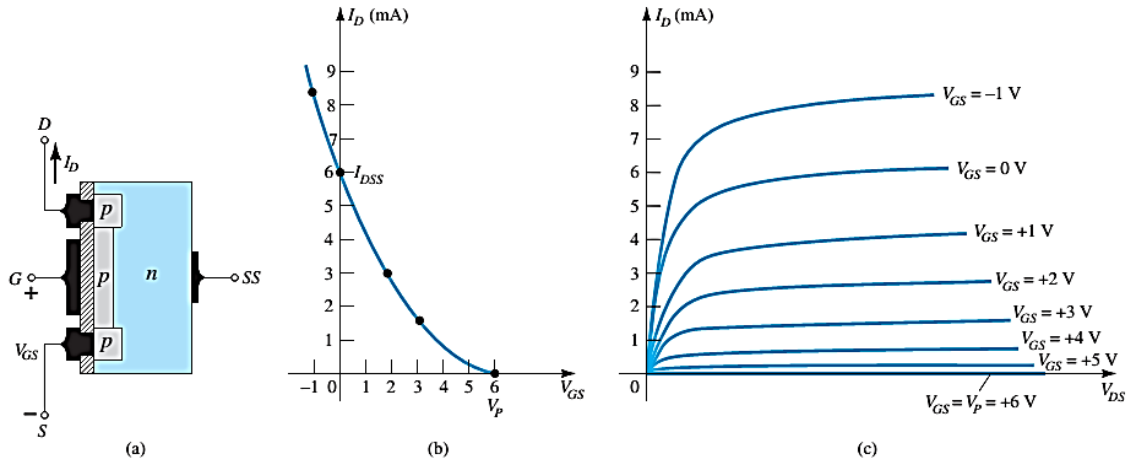
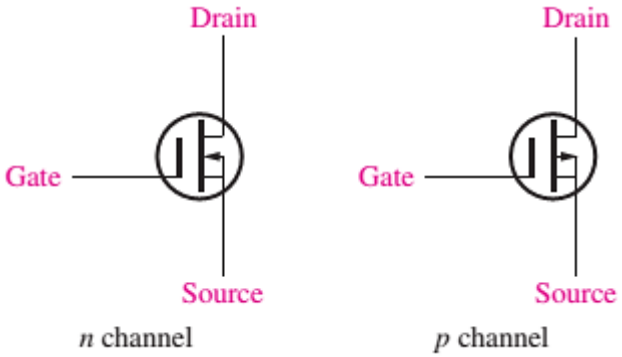


Figure 2-19 p-Channel depletion-type MOSFET with I_{DSS} =6 mA and V_P = +6V

MOSFET Symbols: The schematic symbols for both the n-channel and the p-channel depletion MOSFETs are shown in Figure 2–20. The substrate, indicated by the arrow, is normally (but not always) connected internally to the source. Sometimes, there is a separate substrate pin.

Figure 2-20 D-MOSFET schematic symbols.



Enhancement MOSFET (E-MOSFET)

The E-MOSFET operates only in the enhancement mode and has no depletion mode.

Basic Construction

Figure (2-21a) illustrates the basic structure of the both n-channel EMOSFET. We will use the n-channel device to describe the basic structure and operation.

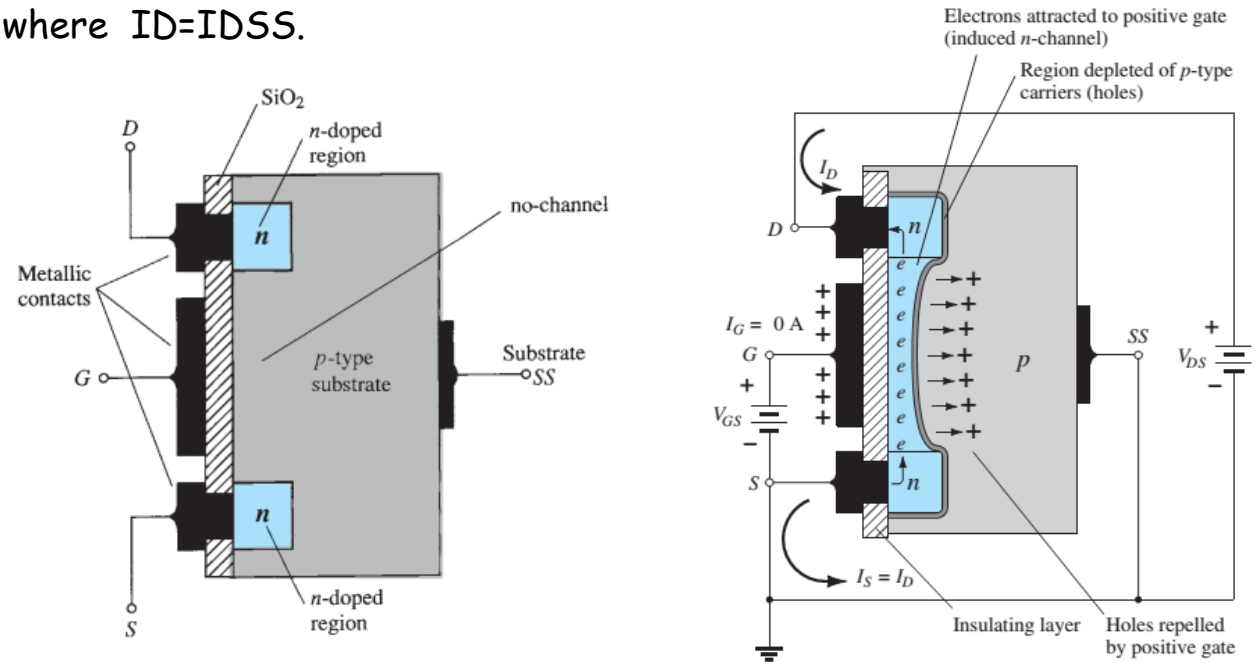
- A slab of p-type material is formed from a silicon base and is again referred to as the substrate.
- The source and drain terminals are again connected through metallic contacts to n-doped regions, but note in figure (2-21) the

absence of a channel between the two n-doped regions and the substrate extends completely to the SiO2 layer. This is the primary difference between the construction of depletion-type and enhancement-type MOSFETs.

- The SiO2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material.

Basic Operation and Characteristics of EMOSFET

If VGS is set at 0 V and a voltage applied between the drain and the source of the device of Figure 2-21a, the absence of an n-channel will result in a current of effectively 0A,quite different from the depletion-type MOSFET and JFET,
where ID=IDSS.



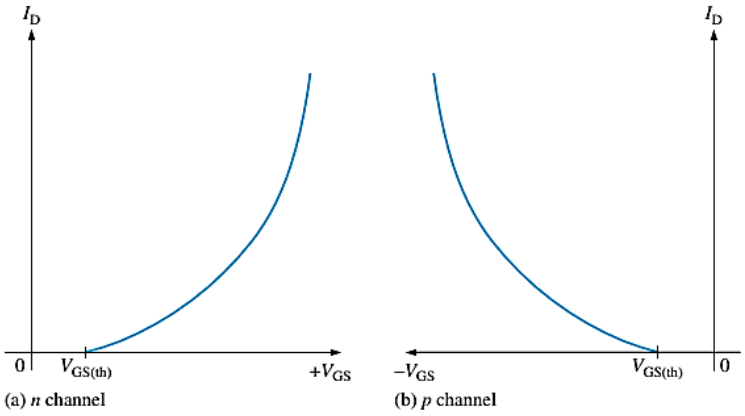
(a)Basic Structure (b) EMOSFET Operation

Figure 2-21 Representation of the basic E-MOSFET construction and operation (n-channel)

If both VDS and V GS have been set at some positive voltage greater than 0 V the electrons in the p-substrate will be attracted to the positive gate and accumulate in the region near the surface of the SiO2 layer. The SiO2 layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal. As VGS

increases in magnitude, the concentration of electrons near the SiO2 surface increases until eventually the induced n-type region can support a measurable flow between drain and source. The level of VGS that results in the significant increase in drain current is called the threshold voltage and is given the symbol VT. On specification sheets it is referred to as VGS(Th). As VGS is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. Figure 2–22 shows the general transfer characteristic curves for both types of E-MOSFETs.

Figure 2-22 E-MOSFET general transfer characteristic curves.



The equation for the parabolic transfer characteristic curve of the E-MOSFET differs from that of the JFET and the D-MOSFET because the curve starts at VGS(th) rather than VGS(off)on the horizontal axis and never intersects the vertical axis. The equation for the E MOSFET transfer characteristic curve is

$$I_D = K\left(V_{GS} - V_{(GSTh}\right)^2$$

The constant **K** depends on the particular MOSFET and can be determined from the datasheet.

The forward trans-conductance (transfer conductance), gm

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = 2K\left(V_{GS} - V_{(GSTh}\right)$$

MOSFET Symbols

The schematic symbols for the n-channel and p-channel E-MOSFETs are shown in Figure 2–23.

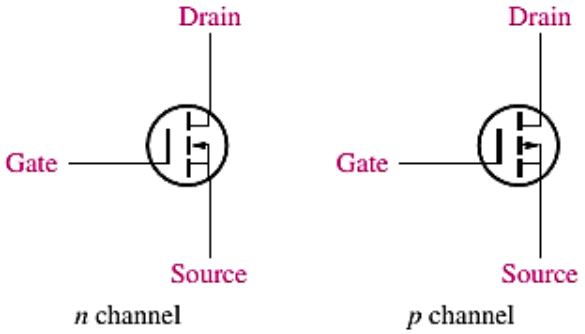


Figure 2-23 E-MOSFET schematic symbols.

FET SMALL-SIGNAL MODEL

The ac analysis of a FET configuration requires that a small-signal ac model for the FET be developed. A major component of the ac model will reflect the fact that an ac voltage applied to the input gate-to-source (Vgs) terminals will control the level of current from drain to source (Id).

The control of Id by Vgs is included as a current source gmVgs connected from drain to source. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages as will occur in actual operation.

The input impedance of FETs is approximate an open circuit

$$Z_{in} = \infty\,\Omega$$

The output impedance of FETs is similar in magnitude to that of conventional BJTs. On FET specification sheets, the output impedance will typically appear as g_{os} or y_{os} with the units of (S).

$$\boldsymbol{Z_{out} = r_d = \frac{\Delta V_{DS}}{\Delta I_D}\Big|_{V_{GS}=constant} = \frac{1}{g_{os}} = \frac{1}{y_{os}}}$$

Figure (2-24) show the definition of r_d using drain char.

Figure (2-24) Definition of r_d using JFET drain characteristics.

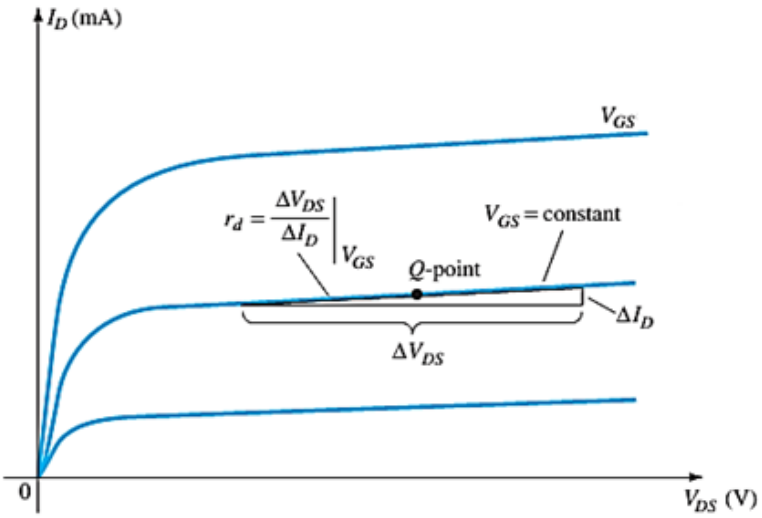
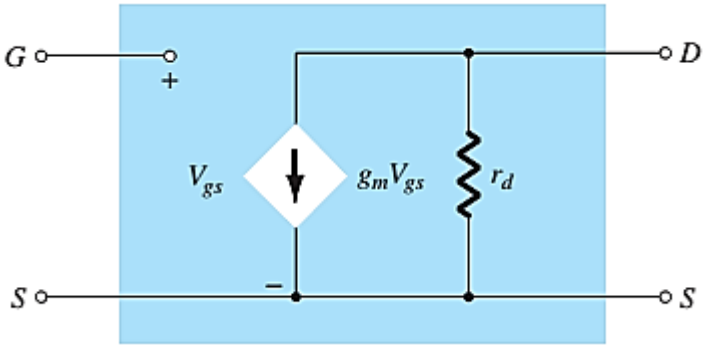


Figure (2-25) shows the ac equivalent circuit for the FET.

Figure (2-25) FET ac equivalent circuit.



Where g_m for JFET and D-MOSFET

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) = g_{m0}\left(\sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|}$$

And for EMOSFET

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = 2K\left(V_{GS} - V_{(GSTh)}\right)$$

FET Amplifier Biasing

For the field-effect transistor, the relationship between input and output quantities is nonlinear due to the squared term in Shockley's equation. The nonlinear relationship between ID and VGS can complicate the mathematical approach to the dc analysis of FET configurations. A graphical approach may limit solutions to tenths-place accuracy, but it is a quicker method for most FET amplifiers.

The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$I_G \cong 0$$
$$I_D \cong I_S$$

For JFETs and depletion-type MOSFETs and MESFETs, Shockley's equation is applied to relate the input and output quantities

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

For enhancement-type MOSFETs and MESFETs, the following equation is applicable:

$$I_D = K\left(V_{GS} - V_{(GSTh}\right)^2$$

It is particularly important to realize that all of the equations above are for the field effect transistor only! They do not change with each network configuration so long as the device is in the active region.

Fixed-Bias Configuration:

DC Analysis of fixed biased configuration

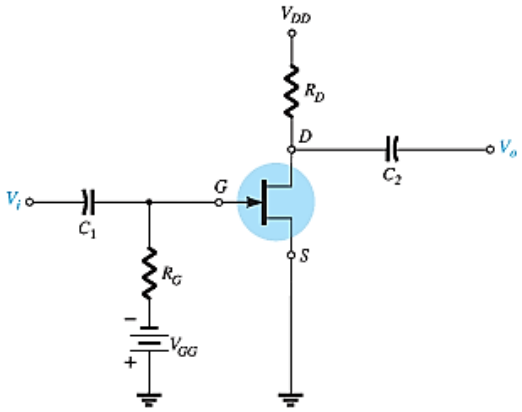


Figure 2-26 Fixed Bias Configuration

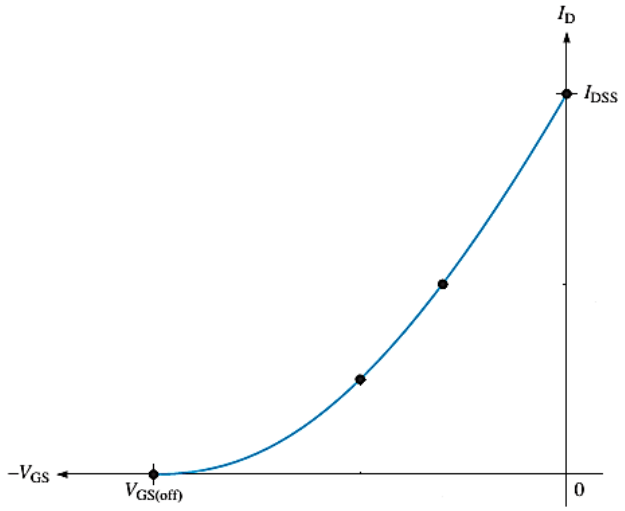


Figure 2-26 finding the solution for the fixed bias configuration using plot

AC Analysis for Fixed Biased configuration

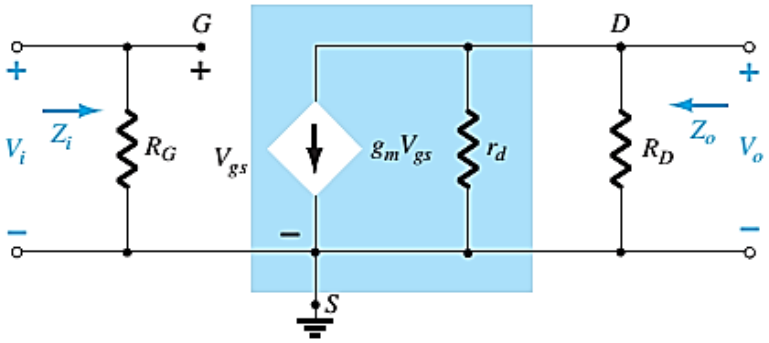
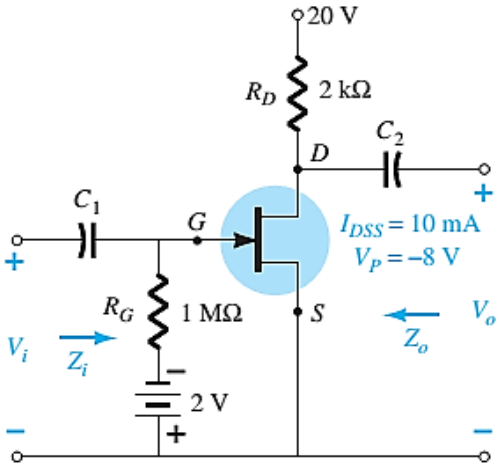


Figure (2-27) AC equivalent circuit for fixed biased configuration

Example 2.1: for the circuit shown, if **yos=40µs** determine

a. VGSQ
b. IDQ
c. VDS
d. VD
e. VS
f. VG
g. Gm
h. rd
i. Zin
j. Zout
k. Av



Self-Bias Configuration

DC Analysis of self-bias configuration

The self-bias configuration eliminates the need for two dc supplies. The controlling gate-to-source voltage is now determined by the voltage across a resistor RS introduced in the source leg of the configuration as shown in Figure 2-28.

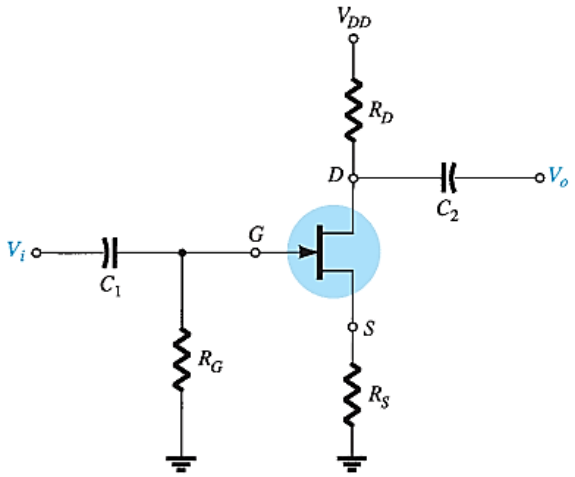


Figure 2-28 Self Bias Configuration

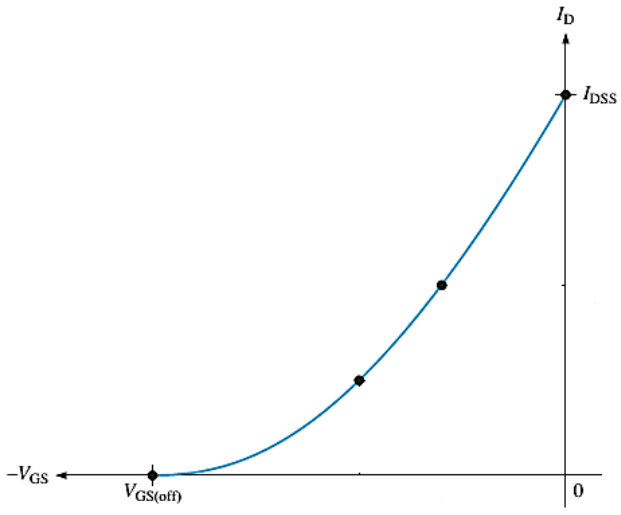


Figure 2-29 sketching the self-bias line.

AC analysis of self-bias configuration (Un-bypassed)

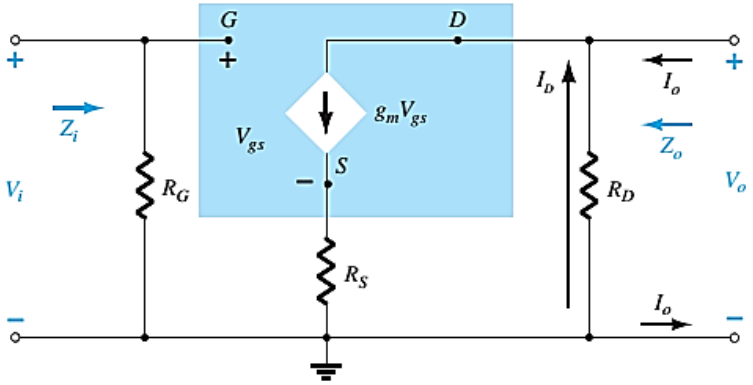


Figure (2-30) Ac equivalent circuit for un-bypassed self-biased configuration

AC analysis of self-bias configuration (bypassed)

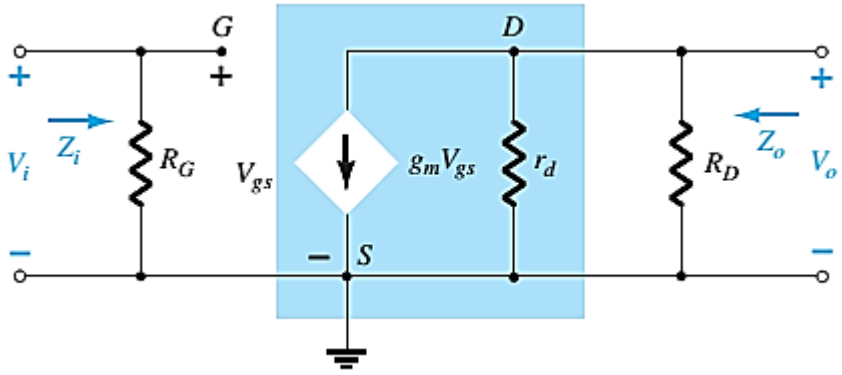
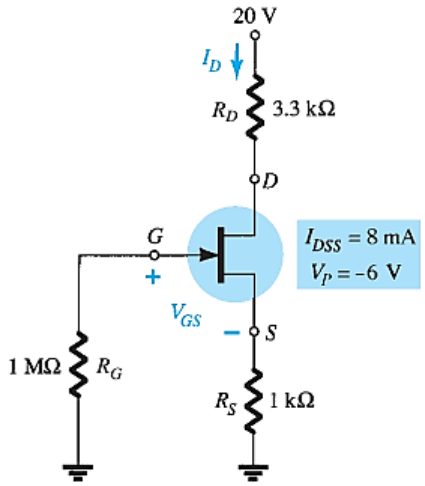


Figure (2-31) Ac equivalent circuit for un-bypassed self-biased configuration

Example 2.2: for the circuit shown, if **yos=20μs** determine

a. VGSQ
b. IDQ
c. VDS
d. VD
e. VS
f. VG
g. Gm
h. rd
i. Zin
j. Zout
k. Av



Voltage-Divider Biasing Configuration

DC analysis of voltage-divider biasing configuration

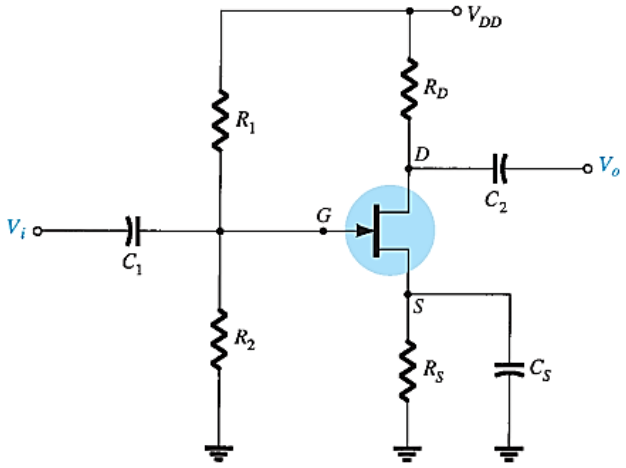


Figure 2-32 Voltage-Divider Biased amplifier

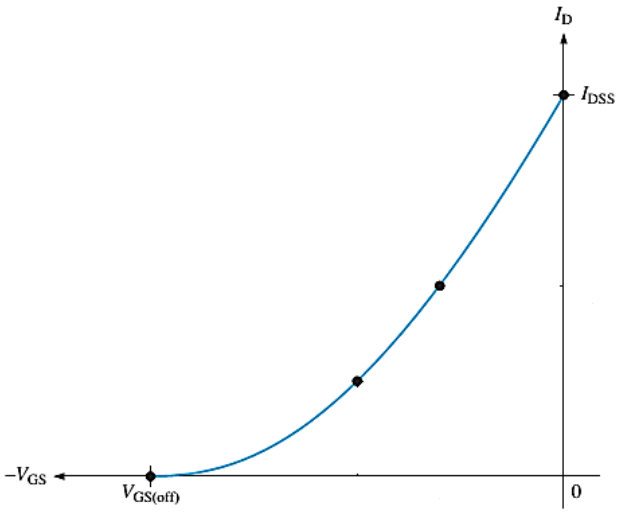


Figure 2-33 Sketching the network equation for the voltage-divider configuration.

AC analysis of voltage-divider biasing configuration (Bypassed)

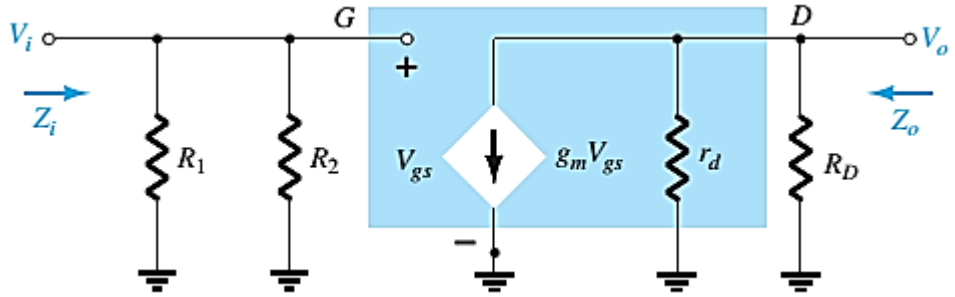
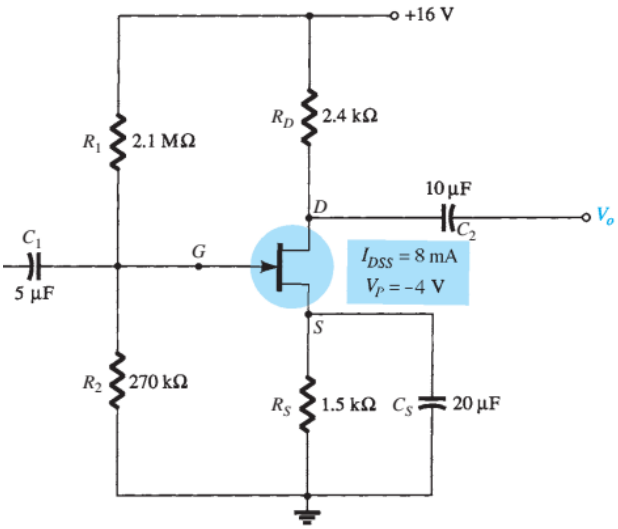


Figure (2-34) ac equivalent circuit for bypassed voltage divider configuration

AC analysis of voltage-divider biasing configuration (Un-Bypassed)

Example 2.3: for the circuit shown, determine

l. VGSQ
m. IDQ
n. VDS
o. VD
p. VS
q. VG
r. gm
s. rd
t. Zin
u. Zout
v. Av



Common-Drain (Source Follower) Configuration

DC analysis of common-drain (source follower) configuration

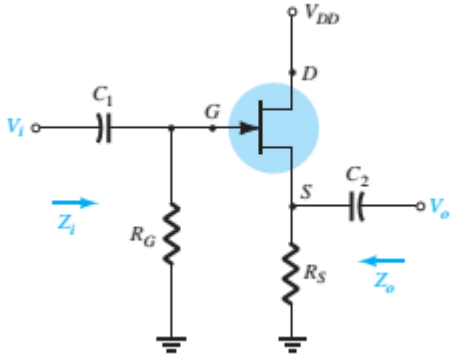


Figure 2-35 common drain Biased amplifier

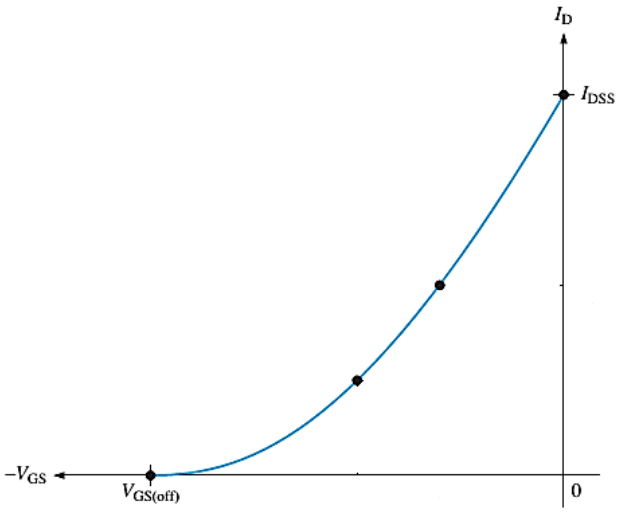


Figure 2-36 sketching the common drain line.

AC analysis of common-drain (source follower) configuration

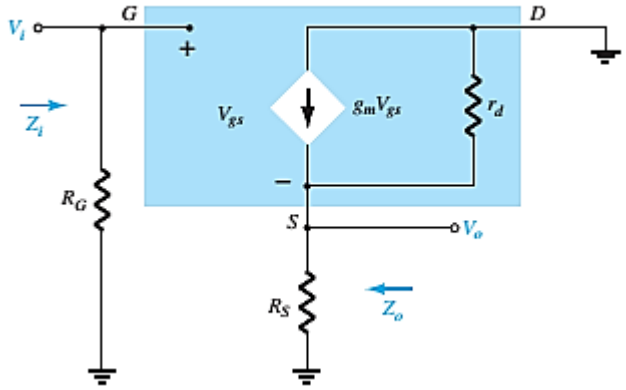
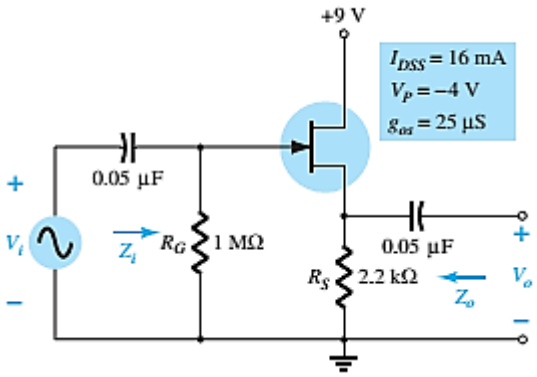


Figure (2-37) ac equivalent circuit for the common

Example 2.4: for the circuit shown, if **yos=25μs** determine

a. VGSQ
b. IDQ
c. VDS
d. VD
e. VS
f. VG
g. Gm
h. rd
i. Zin
j. Zout
k. Av



Common-Gate Configuration:

DC analysis of common-gate configuration:

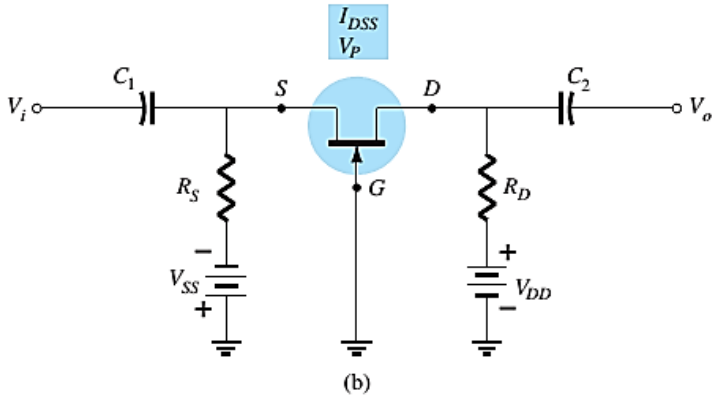


Figure 2-38common gate configuration

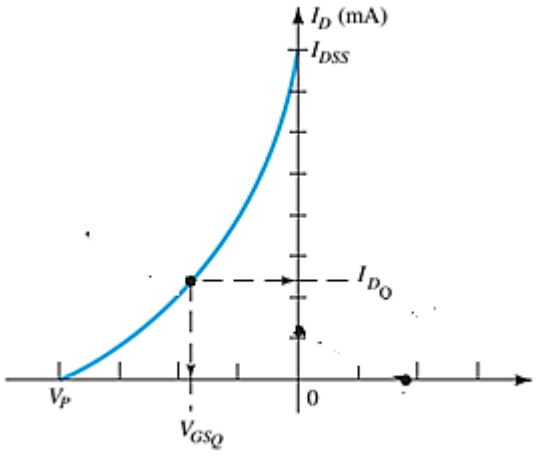


Figure 2-39 determining the Q-point for the network of Figure 2-35

AC analysis of common-gate configuration:

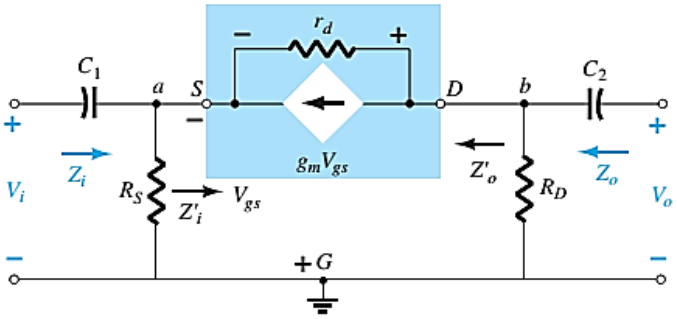
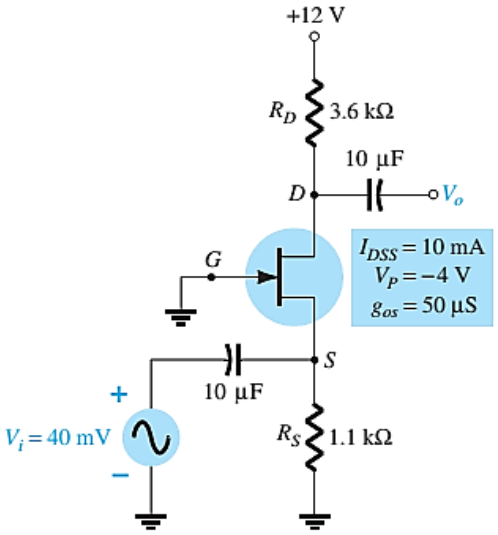


Figure (2-40) ac equivalent model for the common gate.

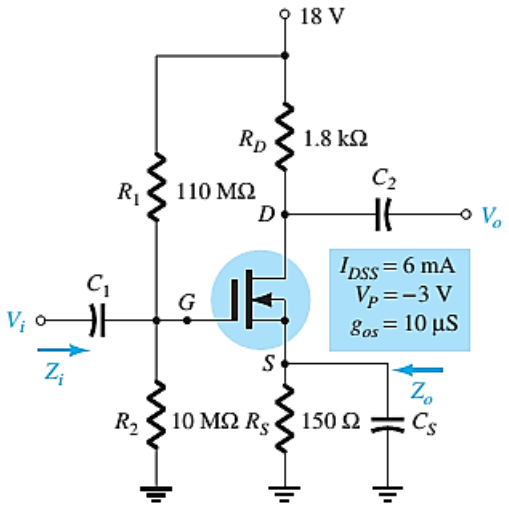
Example 2.5: for the circuit shown, determine

a. VGSQ
b. IDQ
c. VDS
d. VD
e. VS
f. VG
g. Gm
h. rd
i. Zin
j. Zout
k. Av



Example 2.6: for the circuit shown, determine

a. VGSQ
b. IDQ
c. VDS
d. VD
e. VS
f. VG
g. Gm
h. rd
i. Zin
j. Zout
k. Av



EMOS Amplifier

The transfer characteristics of the enhancement-type MOSFET are quite different from those encountered for the JFET and depletion-type MOSFETs, resulting in a graphical solution (which is shown in figure (2-41)) quite different from those of the preceding sections.

Since specification sheets typically provide the threshold voltage and a level of drain current (ID(on)) and its corresponding level of VGS(on), two points are defined immediately as shown in figure (2-41). To complete the curve, the constant k of transfer characteristics equation must be determined as follows.

$$I_{D(on)} = K\left(V_{GS(on)} - V_{(GSTh)}\right)^2$$

Once **k** is defined, other levels of ID can be determined for chosen values of V GS.

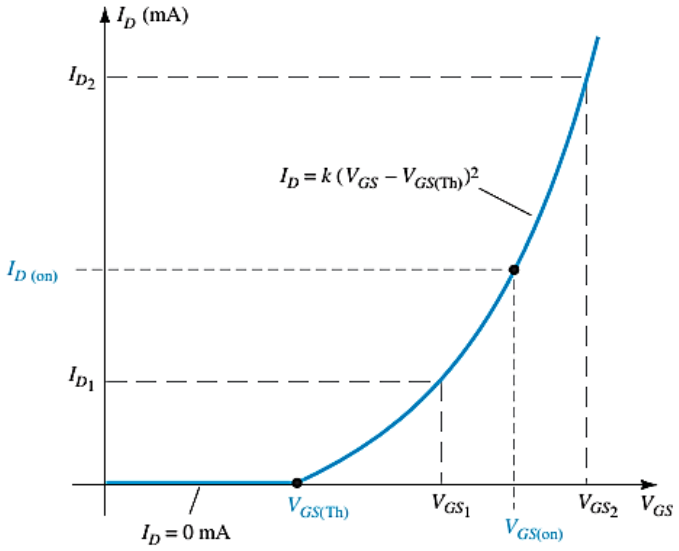


Figure (2-41) Transfer characteristics of an n-channel enhancement-type MOSFET.

E-MOSFET Drain-Feedback Configuration

DC Analysis E-MOSFET Drain-Feedback Configuration

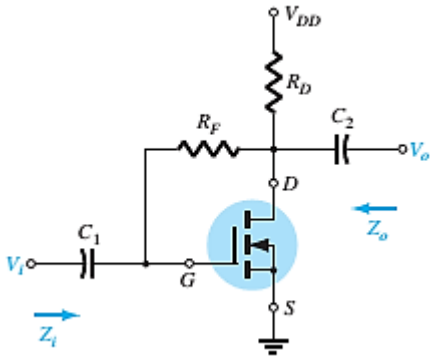
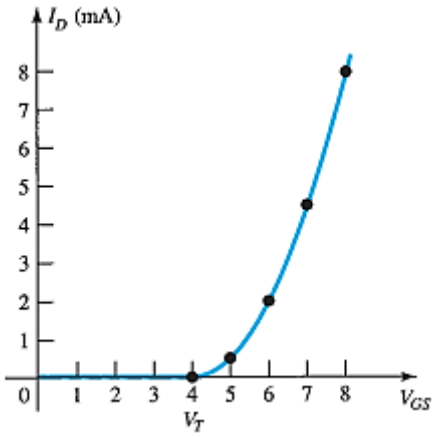


Figure (2-42) E-MOSFET drain-feedback configuration.



AC Analysis E-MOSFET Drain-Feedback Configuration

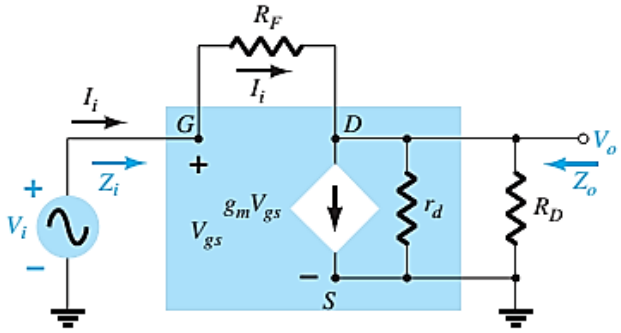
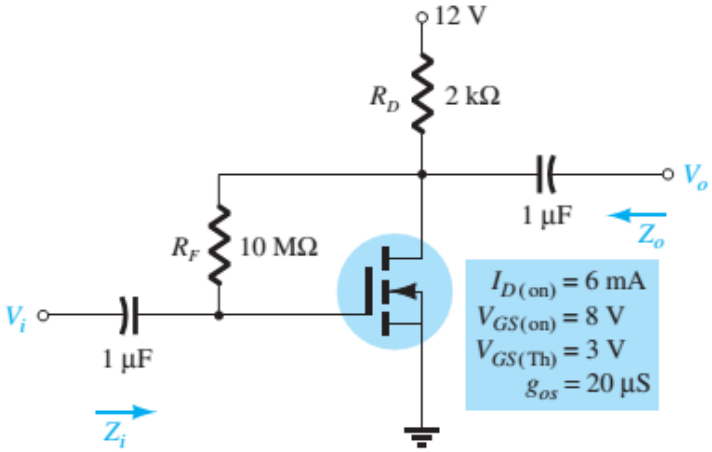


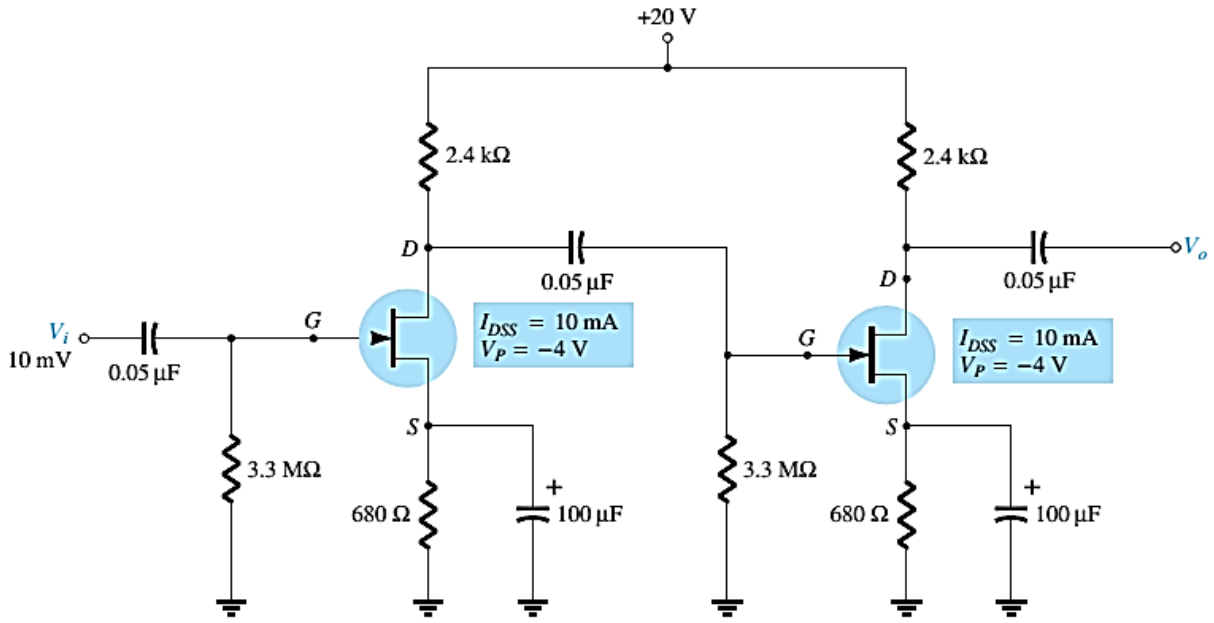
Figure (2-43) AC equivalent of the network of figure (2-42)

Example 2.6: for the circuit shown, determine

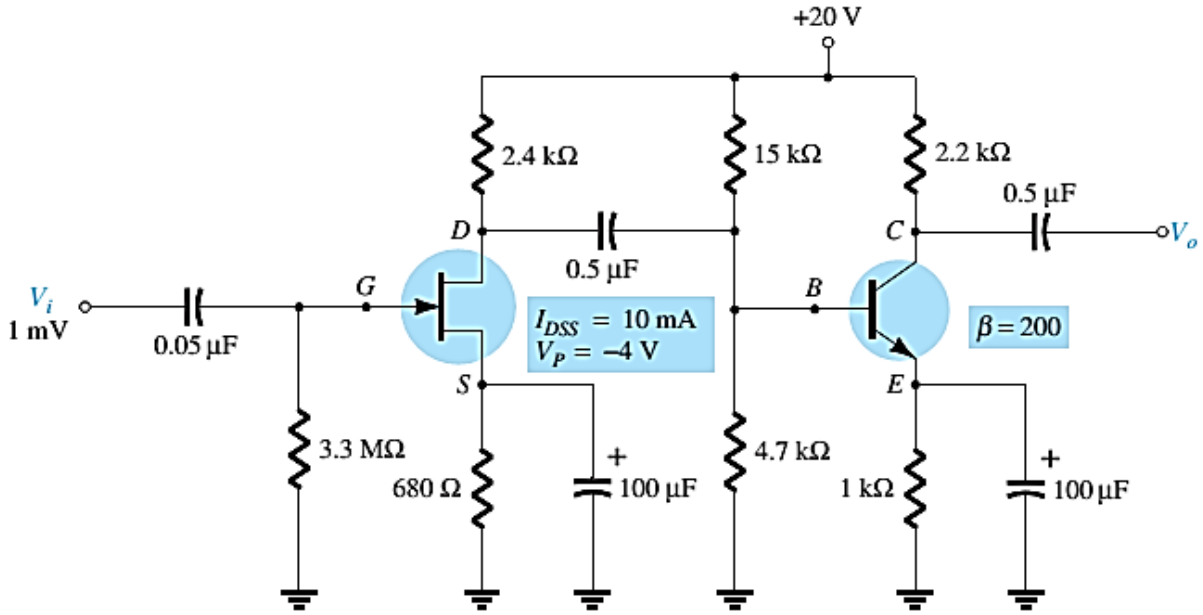
l. VGSQ
m. IDQ
n. VDS
o. VD
p. VS
q. VG
r. Gm
s. rd
t. Zin
u. Zout
v. Av



Example 2.8 (H.W): for the circuit shown, determine **Vo**



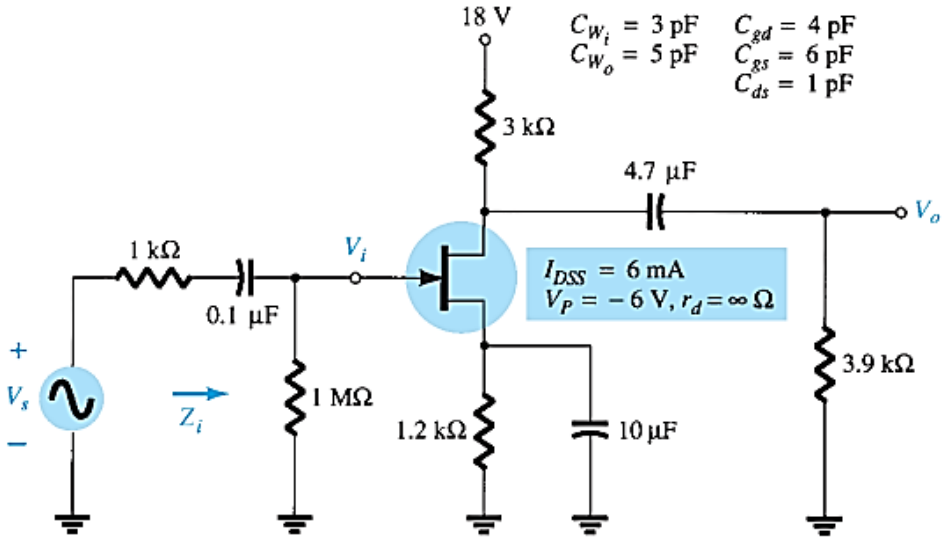
Example 2.9 : for the circuit shown, determine **Vo**



FET Frequency Response

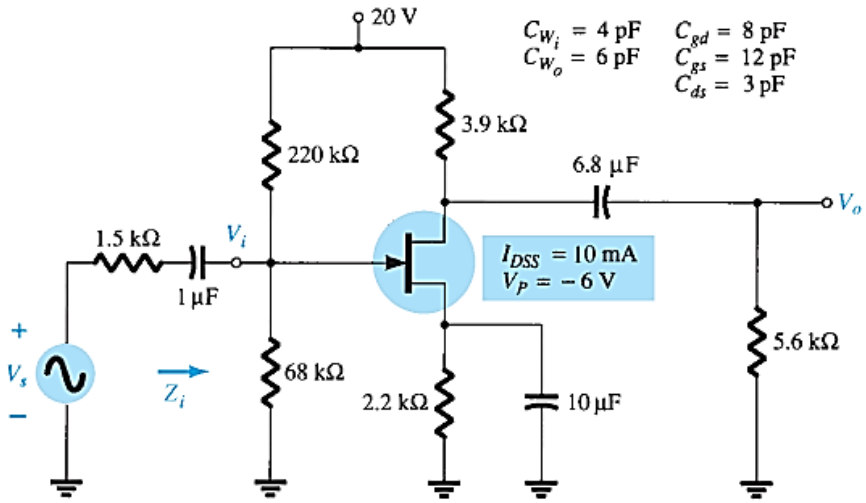
Q1:- For the network of the self-biased amplifier shown:

a. Determine VGSQ and IDQ.
b. Find gm0 and gm .
c. Calculate the midband gain (Av).
d. Determine Zi.
e. Calculate Avs.
f. Determine fL(C1), fL(C2) and fL(CS)
g. Determine the low-cutoff frequency (fL).
h. Determine fH(in) and fH(out).
i. Determine the high-cutoff frequency (fH).
j. Determine the bandwidth (BW).
k. Determine the Gain-Bandwidth product (GBP).



Q2:- For the network of the voltage divider amplifier shown:

a. Determine VGSQ and IDQ.
b. Find gm0 and gm .
c. Calculate the midband gain (Av).
d. Determine Zi.
e. Calculate Avs.
f. Determine fL(C1), fL(C2) and fL(CS)
g. Determine the low-cutoff frequency (fL).
h. Determine fH(in) and fH(out).
i. Determine the high-cutoff frequency (fH).
j. Determine the bandwidth (BW).
k. Determine the Gain-Bandwidth product (GBP).

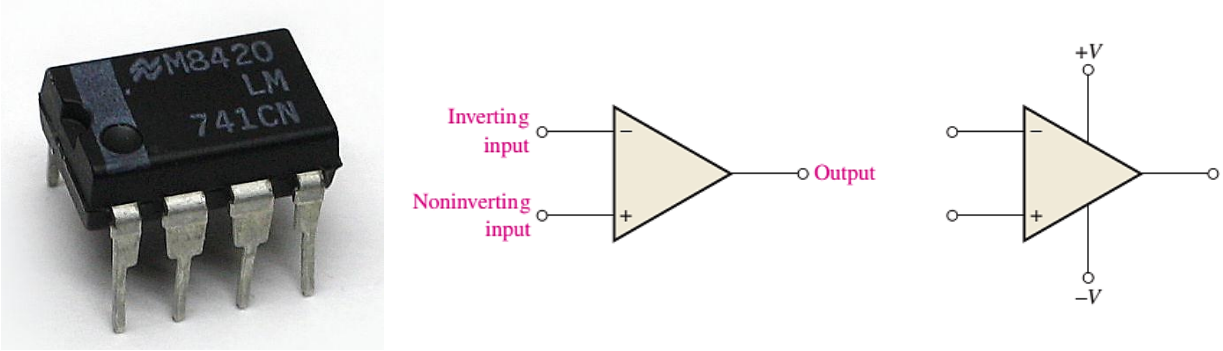


Chapter Three

The Operational Amplifier (Op-Amp)

An operational amplifier, or op-amp, is a very high gain differential amplifier with high input impedance and low output impedance. Typical uses of the operational amplifier are to provide voltage amplitude changes (amplitude and polarity), oscillators, filter circuits, and many types of instrumentation circuits. An op-amp contains a number of differential amplifier stages to achieve a very high voltage gain. Figure (1a) shows one of the most famous operation amplifiers which is known as 741 Op-Amp.

The standard operational amplifier (op-amp) symbol is shown in Figure (1b). It has two input terminals, the inverting (-) input and the non-inverting (+) input, and one output terminal. Most op-amps operate with two dc supply voltages, one positive and the other negative, as shown in Figure (1c), although some have a single dc supply.



(a) (b) (c)

Figure (1) Op-Amp package and symbol

Figure (2) shows the IC pin distribution

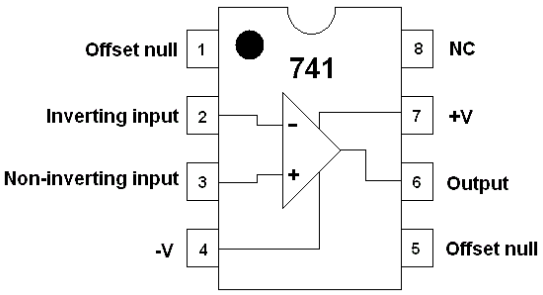


Figure (2) Op-Amp pin distribution

Ideal and Practical Op-Amp

The ideal op-amp has infinite voltage gain and infinite bandwidth. Also, it has an infinite input impedance (open) so that it does not load the driving source. Finally, it has a zero output impedance. Op-amp characteristics are illustrated in Figure (3a).

Characteristics of a practical op-amp are very high voltage gain, very high input impedance, and very low output impedance. These are labelled in Figure (3b).

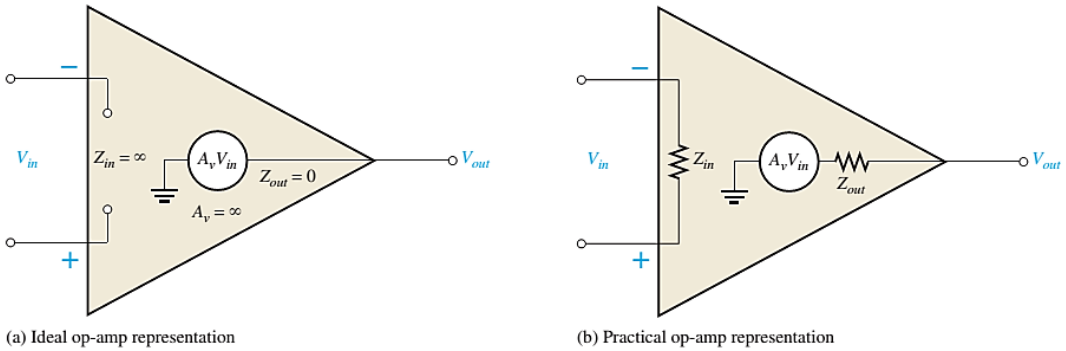


Figure (3) Basic op-amp representations.

The op-amp can be connected in a large number of circuits to provide various operating characteristics. In this experiment, we cover a few of the most common of these circuit connections.

Internal Block Diagram of an Op-Amp: A typical op-amp is made up of three types of amplifier circuits: a differential amplifier, a voltage amplifier, and a push-pull amplifier, as shown in Figure (4)

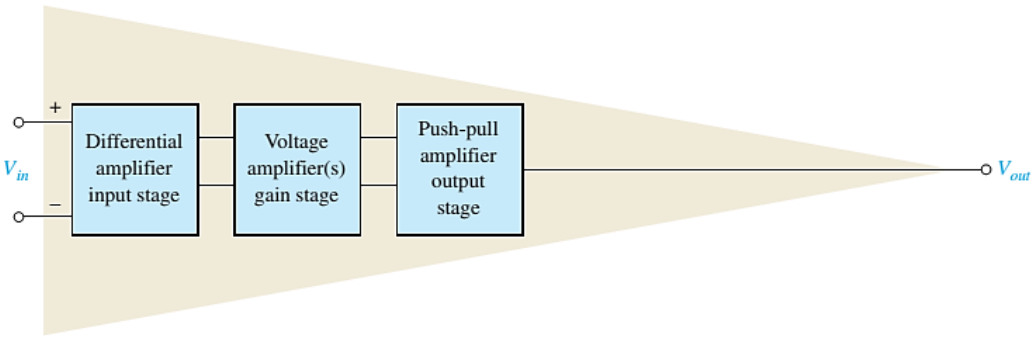


Figure (4) Basic internal arrangement of an op-amp.

Input Signal Modes

1- Single-ended differential mode

When an op-amp is operated in the single-ended differential mode, one input is grounded and a signal voltage is applied to the other input, as

shown in Figure (5). In the case where the signal voltage is applied to the inverting input as in part (a), an inverted, amplified signal voltage appears at the output. In the case where the signal is applied to the non-inverting input with the inverting input grounded, as in Figure (5b), a non-inverted, amplified signal voltage appears at the output.

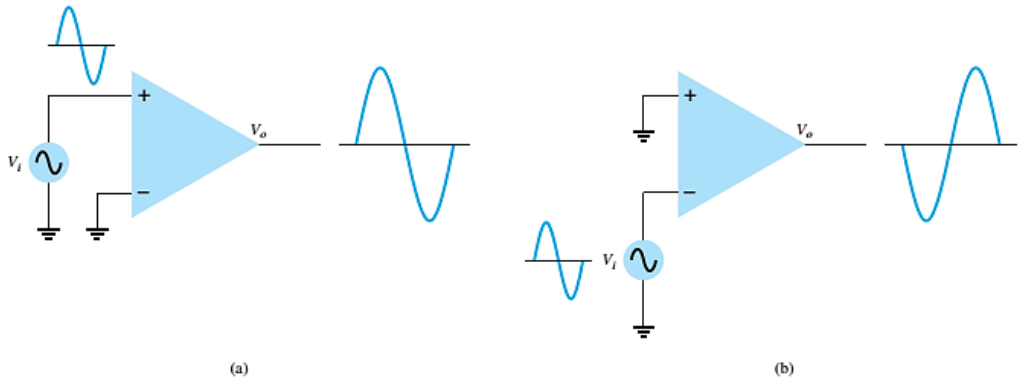


Figure (5) Single-ended differential mode.

2- Double-ended differential mode

The double-ended differential mode, two opposite-polarity (out-of-phase) signals are applied to the inputs, as shown in Figure (6a). The amplified difference between the two inputs appears on the output. Equivalently, the double-ended differential mode can be represented by a single source Figure (6b).

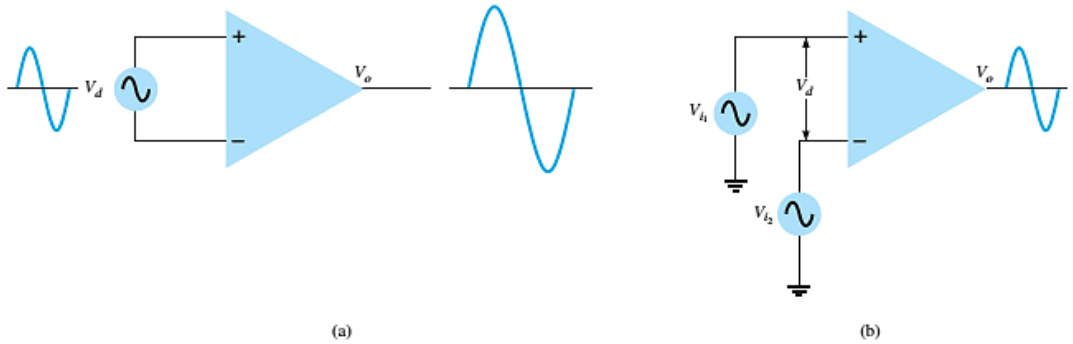


Figure (6) Double-ended differential mode

3-Common Mode

In the common mode, two signal voltages of the same phase, frequency, and amplitude are applied to the two inputs, as shown in Figure (7). When equal input signals are applied to both inputs, they tend to cancel, resulting in a zero output voltage.

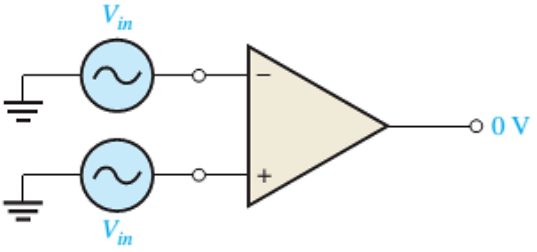


Figure (7) Common-mode operation.

This action is called common-mode rejection. Its importance lies in the situation where an unwanted signal appears commonly on both op-amp inputs. Common-mode rejection means that this unwanted signal will not appear on the output and distort the desired signal.

Op-Amp Parameters

1- Common-Mode Rejection Ratio

Desired signals can appear on only one input or with opposite polarities on both input lines. These desired signals are amplified and appear on the output as previously discussed. Unwanted signals (noise) appearing with the same polarity on both input lines are essentially cancelled by the op-amp and do not appear on the output. The measure of an amplifier's ability to reject common-mode signals is a parameter called the CMRR (common-mode rejection ratio).

Practical op-amps, however, do exhibit a very small common-mode gain (A_{cm} usually much less than 1), while providing a high open-loop differential voltage gain (A_{ol} usually several thousand)

$$CMRR = \frac{A_{ol}}{A_{cm}}$$

$$CMRR\,(db) = 20\,log\left(\frac{A_{ol}}{A_{cm}}\right)$$

2- Maximum Output Voltage Swing (VO(p-p)):

With no input signal, the output of an op-amp is ideally 0 V. This is called the quiescent output voltage. When an input signal is applied, the ideal limits of the peak-to-peak output signal are $\mp Vcc$

3- Input Offset Voltage

The ideal op-amp produces zero volts out for zero volts in. In a practical op-amp, however, a small dc voltage, VOUT(error), appears at the output when no differential input voltage is applied.

The input offset voltage, VOS, is the differential dc voltage required between the inputs to force the output to zero volts.

4- The input bias current

The input bias current is the dc current required by the inputs of the amplifier to properly operate the first stage

$$I_{BIAS} = \frac{I_1 + I_2}{2}$$

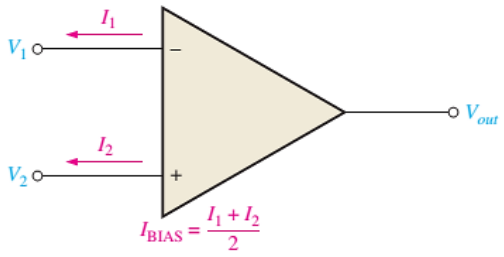


Figure (8)

5- Input Offset Current

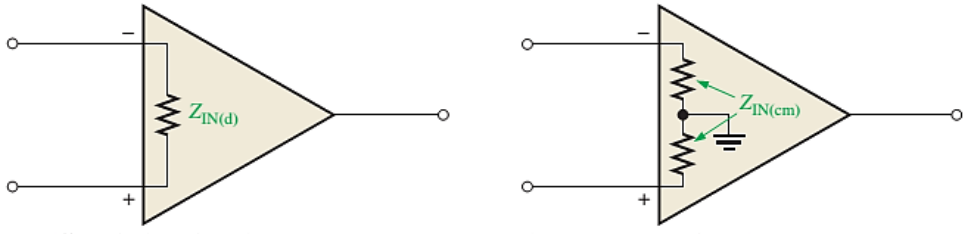
Ideally, the two input bias currents are equal, and thus their difference is zero. In a practical op-amp, however, the bias currents are not exactly equal.

The input offset current, $\mathbf{I_{os}}$, is the difference of the input bias currents, expressed as an absolute value.

$$I_{OS} = |I_1 - I_2|$$

6- Input Impedance

Two basic ways of specifying the input impedance of an op-amp are the differential and the common mode. The differential input impedance is the total resistance between the inverting and the non-inverting inputs, as illustrated in Figure (9a). The common-mode input impedance is the resistance between each input and ground



(a) Differential input impedance (b) Common-mode input impedance

Figure (9)

Closed-Loop Voltage Gain, Acl

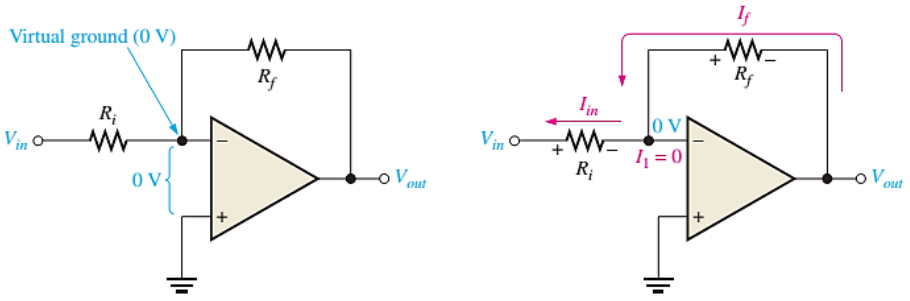
The closed-loop voltage gain is the voltage gain of an op-amp with external feedback. The amplifier configuration consists of the op-amp and an external negative feedback circuit that connects the output to the inverting input. The closed-loop voltage gain is determined by the external component values and can be precisely controlled by them.

Op-Amp Applications

1- Inverting Amplifier

An op-amp connected as an inverting amplifier with a controlled amount of voltage gain is shown in Figure (10). The input signal is applied through a series input resistor Ri to the inverting input. Also, the output is fed back through Rf to the same input. The non-inverting (+) input is grounded.

At this point, the ideal op-amp parameters mentioned earlier are useful in simplifying the analysis of this circuit. In particular, the concept of infinite input impedance is of great value. An infinite input impedance implies zero current at the inverting input. If there is zero current through the input impedance, then there must be no-voltage drop between the inverting and non-inverting inputs. This means that the voltage at the inverting input is zero because the non-inverting (+) input is grounded. This zero voltage at the inverting input terminal is referred to as virtual ground. This condition is illustrated in Figure (10a).



(a) Virtual ground

(b) $I_{in} = I_f$ and current at the inverting input (I_1) is 0.

Figure (10) Virtual ground concept and closed loop voltage gain development for the inverting amplifier.

Since there is no current at the inverting input, the current through Ri and the current through Rf are equal, as shown in Figure (4b).

$$I_{in} = I_f$$

The voltage across Ri equals Vin because the resistor is connected to virtual ground at the inverting input of the op-amp. Therefore,

$$I_{in} = \frac{V_{in}}{R_i}$$

Also, the voltage across Rf equals because of virtual ground, and therefore

$$I_f = \frac{-V_{out}}{R_f}$$

Since $I_{in} = I_f$

$$\frac{V_{in}}{R_i} = \frac{-V_{out}}{R_f}$$

$$\boxed{\frac{V_{out}}{V_{in}} = \frac{-R_f}{R_i}}$$

2- Non-inverting Amplifier

The connection of figure (11a) shows an op-amp circuit that works as a non-inverting amplifier or constant-gain multiplier. To determine the voltage gain of the circuit, we can use the equivalent representation shown in figure (10b). Note that the voltage across R1 is V1 since Vi ≈ 0V. This must be equal to the output voltage, through a voltage divider of R1 and Rf, so that

$$V_1 = \frac{R_1}{R_1 + R_f} V_o$$

Which results in

$$\boxed{\frac{V_o}{V_1} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1}}$$

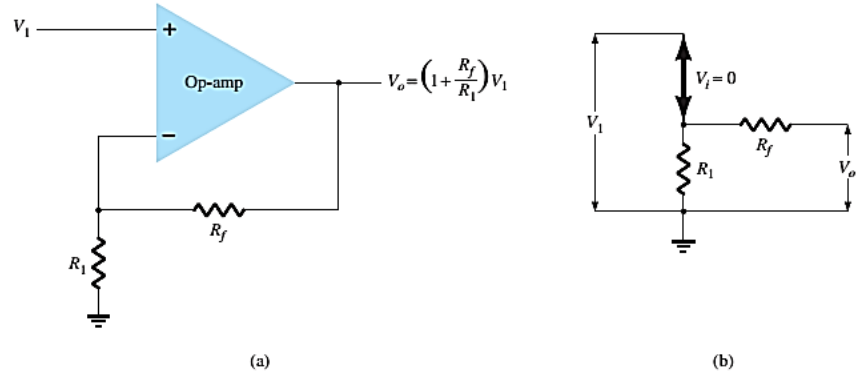


Figure (10) Non-inverting Amplifier

3- Voltage-Follower

The voltage-follower configuration is a special case of the non-inverting amplifier where all of the output voltage is fed back to the inverting input (-) by a straight connection, as shown in figure (12). As you can see, the straight feedback connection has a voltage gain of 1 (which means there is no gain).

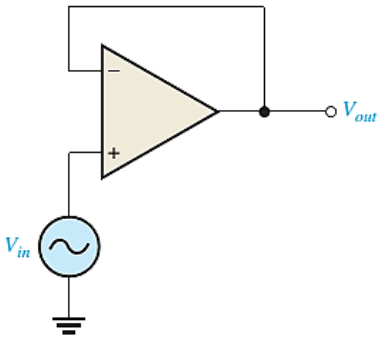
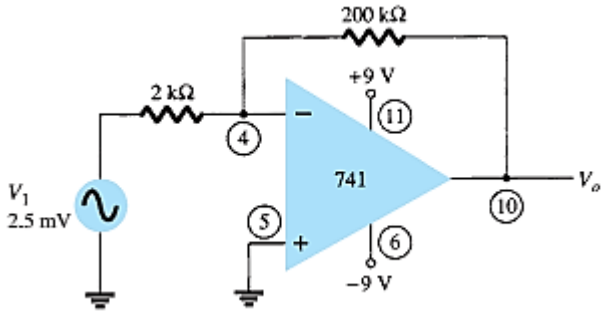
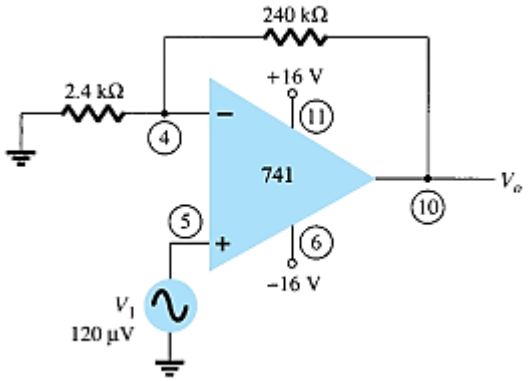
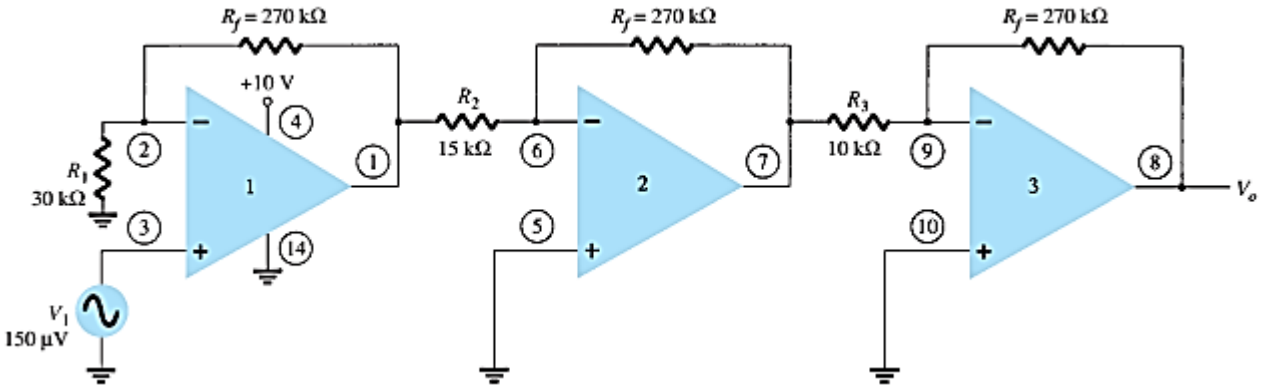


Figure (12) Op-Amp Voltage Follower

Ex:-







4- Inverting summing Amplifier

Probably the most used of the op-amp circuits is the summing amplifier circuit shown in figure (13a). The circuit shows a three-input summing amplifier circuit, which provides a means of algebraically summing (adding) three voltages, each multiplied by a constant-gain factor. Using the equivalent representation shown in figure (13b), we can express the output voltage in terms of the inputs as

$$\frac{V_o}{V_i} = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

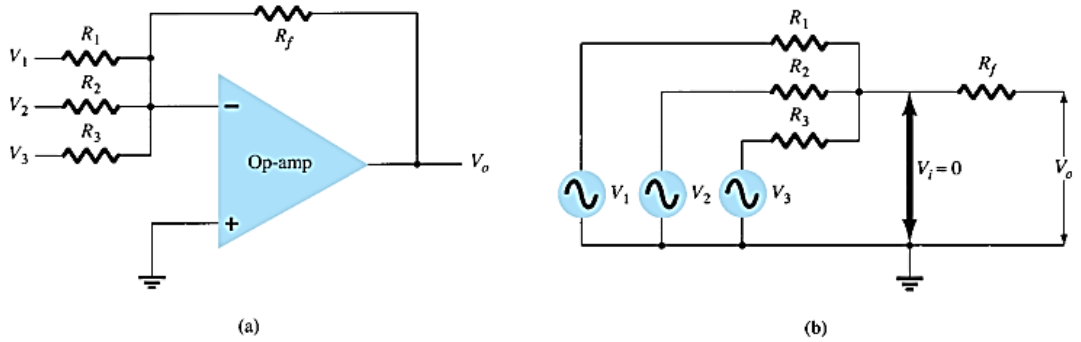
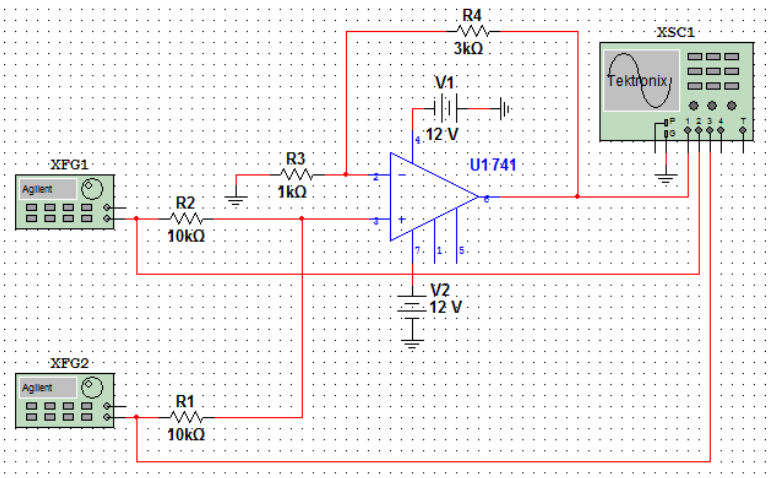


Figure (13) (a) inverting summing amplifier (b) equivalent circuit

In other words, each input adds a voltage to the output multiplied by its separate constant-gain multiplier. If more inputs are used, they each add an additional component to the output.

In the same way we can construct a non-inverting summing amplifier



Example:- design an op-amp circuit that will produce an output -(4v1+v2+0.1v3)

Write an expression for the output and sketch the waveform when

V1=2sinwt , v2=5V dc , v3=-100v dc

5- Comparator

A comparator is a specialized op-amp circuit that compares two input voltages and produces an output that is always at either one of two states, indicating the greater or less than relationship between the inputs. For less critical applications, an op-amp running without negative feedback (open-loop) is often used as a comparator.

One application of an op-amp used as a comparator is to determine when an input voltage exceeds a certain level. Figure (14a) shows a zero-level detector. Notice that the inverting input is grounded to produce a zero level and that the input signal voltage is applied to the non-inverting input. Because of the high open-loop voltage gain, a very small difference voltage between the two inputs drives the amplifier into saturation, causing the output voltage to go to its limit.

Figure (14b) shows the result of a sinusoidal input voltage applied to the non-inverting input (+) of the zero-level detector. When the sine wave is positive, the output is at its maximum positive level. When the sine wave crosses 0, the amplifier is driven to its opposite state and the output goes to its maximum negative level, as shown. As you can see, the zero level detector can be used as a squaring circuit to produce a square wave from a sine wave.

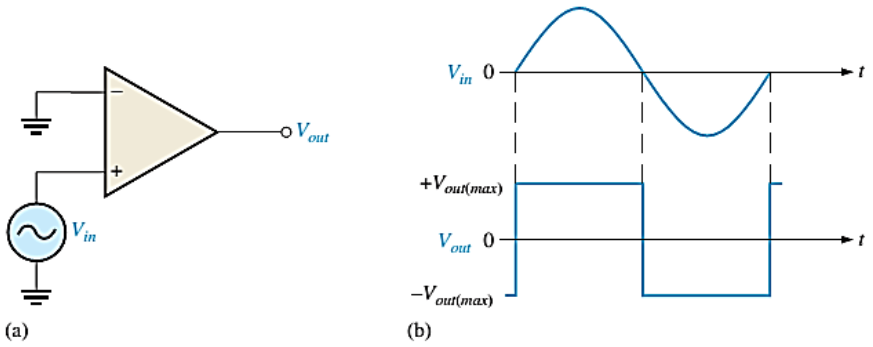


Figure (14) The op-amp as a zero-level detector.

6- Differential (Subtraction) Amplifier

Another connection to provide subtraction of two signals is shown in figure (15). This connection uses only one op-amp stage to provide subtracting two input signals. Using superposition, we can show the output to be

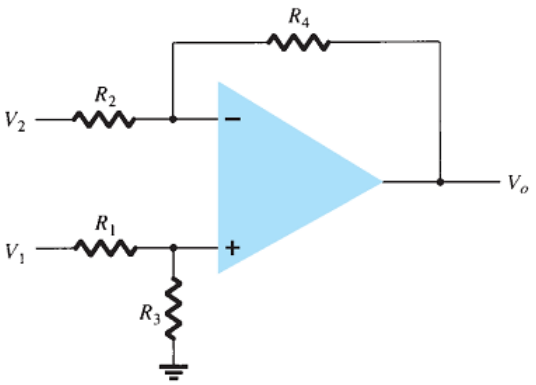


Figure (15) Difference Amplifier

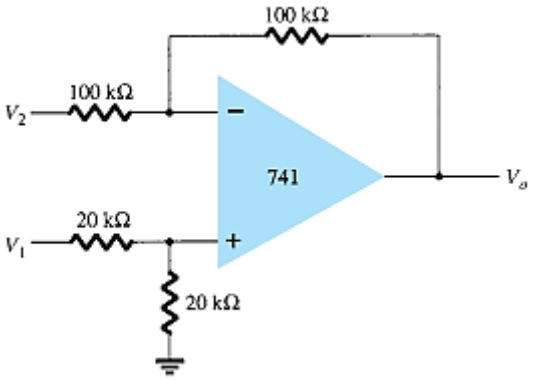
$$\mathbf{V_o = V_{o1} + V_{o2}}$$

$$\boldsymbol{V_{o1} = \left(\frac{R_3}{R_1 + R_3}\left(1 + \frac{R_4}{R_2}\right)V_1\right)}$$

$$\mathbf{V_{o2} = -\left(\frac{R_4}{R_2}\,V_2\right)}$$

$$\boldsymbol{V_o = \left(\frac{R_3}{R_1 + R_3}\left(1 + \frac{R_4}{R_2}\right)V_1\right) - \left(\frac{R_4}{R_2}\,V_2\right)}$$

Example



In order to reject common mode signals. We have to make the two gain magnitudes equal.

$$\mathbf{\frac{R_3}{R_1 + R_3}\left(1 + \frac{R_4}{R_2}\right) = \frac{R_4}{R_2}}$$

Which can be put in the form:

$$\frac{R_3}{R_1+R_3}=\frac{R_4}{R_2+R_4}$$

This condition is satisfied by selecting

$$\frac{R_3}{R_1}=\frac{R_4}{R_2}$$

$$V_o = V_{o1} + V_{o2}$$

$$V_o = \frac{R_4}{R_2}(V_1 - V_2)$$

$$V_{DM} = V_2 - V_1 \ \ (\textbf{Difference mode voltage})$$

$$V_{CM} = \frac{1}{2}(V_2 + V_1) \ \ (\textbf{Common mode voltage})$$

$$V_2 = V_{CM} + \frac{V_{DM}}{2}$$

$$V_1 = V_{CM} - \frac{V_{DM}}{2}$$

Substituted the V_2 and V_1 values in V_o equation, we estimate that only the V_{DM} is appears at the output. While the V_{CM} is eliminated (Which appears the noise signals)

If the amplifier is required to have a large differential gain (R_4/R_2), then R_2 of necessity will be relatively small and the input resistance will be correspondingly low, a problem of this circuit. Another problem of the circuit is that it is not easy to vary the differential gain of the amplifier. Both of these problems are overcome in the instrumentation amplifier discussed next.

Instrumentation Amplifier

A circuit providing an output based on the difference between two inputs (times a scale factor) is shown in Figure (16). A potentiometer is provided to permit adjusting the scale factor of the circuit

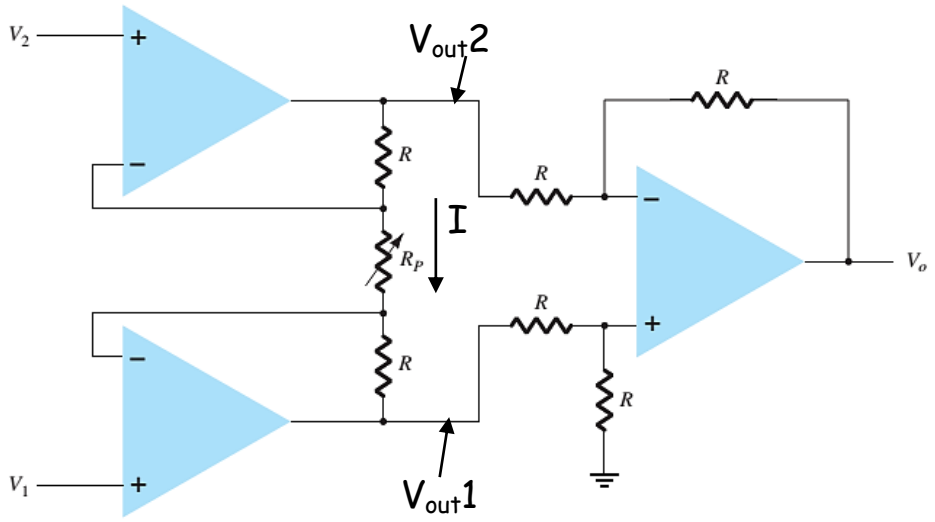


Figure (16) instrumentation amplifier

Since we have $\mathbf{V_i^+ = V_i^-}$

And the current pass through the resistors $(\mathbf{R, R_p}$ **and** $\mathbf{R})$ is $\mathbf{I}$, due to the high input resistances of the op–amps. So we can say that:

$$I = \frac{V_1 - V_{out1}}{R}$$

$$V_1 - V_{out1} = IR \qquad \Rightarrow \qquad \mathbf{V_{o1} = V_1 - IR}$$

$$I = \frac{V_{out2} - V_2}{R}$$

$$V_{out2} - V_2 = IR \qquad \Rightarrow \qquad \mathbf{V_{o2} = V_2 + IR}$$

$$V_o = V_{o1} - V_{o2}$$

$$V_o = \frac{R_f}{R_1}(V_1 - IR - V_2 - IR) = \frac{R_f}{R_1}(V_1 - V_2 - 2 \times IR)$$

$$\text{Since } I = \frac{V_2 - V_1}{R_A}$$

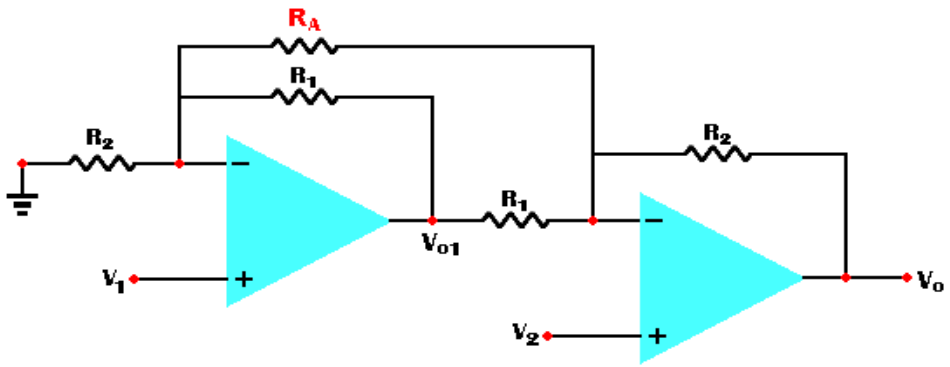
$$V_o = \frac{R_f}{R_1}\left(V_1 - V_2 - 2R \times \frac{V_2 - V_1}{R_A}\right) = \frac{R_f}{R_1}\left(V_1 - V_2 + 2R \times \frac{V_1 - V_2}{R_A}\right)$$

$$V_o = (V_1 - V_2)\frac{R_f}{R_1}\left(1 + \frac{2R}{R_A}\right)$$

but $V_{in} = (V_1 - V_2)$

$$\mathbf{A_V = \frac{V_o}{V_{in}} = \left(1 + \frac{2R}{R_A}\right)}$$

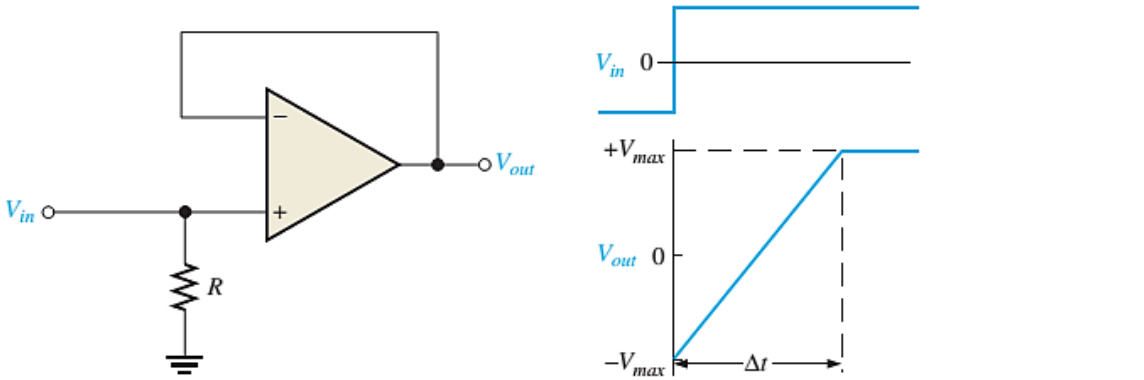
Another circuit used to reduce CMRR



$$\mathbf{V_o = (V_2 - V_1)\left(1 + \frac{R_2}{R_1} + \frac{2R_2}{R_A}\right)} \qquad \boldsymbol{H.W}$$

Slew Rate

The maximum rate of change of the output voltage in response to a step input voltage is the slew rate of an op-amp. Slew rate is measured with an op-amp connected as shown in Figure (17a). This particular op-amp connection gives a worst-case (slowest) slew rate.



(a) Test circuit (b) Step input voltage and the resulting output voltage

Figure (17) slew rate measurement

A pulse is applied to the input and the resulting ideal output voltage is indicated in Figure (17b). The width of the input pulse must be sufficient to allow the output to "slew" from its lower limit to its upper limit. A certain time interval, Δt is required for the output voltage to go from its lower limit $-V_{max}$ to its upper limit $+V_{max}$ once the input step is applied. The slew rate is expressed as

$$\boldsymbol{Slew\ Rate} = \frac{\boldsymbol{\Delta V_{out}}}{\boldsymbol{\Delta t}} \qquad \boldsymbol{V/\mu S}$$

Integrator and Differentiator

An op-amp integrator simulates mathematical integration, which is basically a summing process that determines the total area under the curve of a function. An op-amp differentiator simulates mathematical differentiation, which is a process of determining the instantaneous rate of change of a function. It is not necessary for you to understand mathematical integration or differentiation, at this point, in order to learn how an integrator and differentiator work.

The Op-Amp Integrator

The Ideal Integrator: An ideal integrator is shown in Figure (18). Notice that the feedback element is a capacitor that forms an RC circuit with the input resistor.

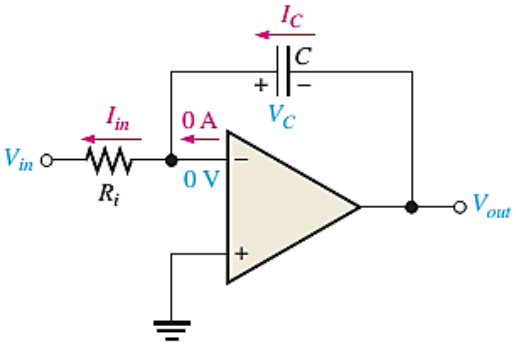


Figure (18) Ideal Integrator

In Figure (18), the inverting input of the op-amp is at virtual ground (0 V), so the voltage across Ri equals Vin. Therefore, the input current is

$$I_i = \frac{V_{in}}{R_i}$$

If Vin is a constant voltage, then Iin is also a constant because the inverting input always remains at 0 V, keeping a constant voltage across Ri. Because of the very high input impedance of the op-amp, there is negligible current at the inverting input. This makes all of the input current go through the capacitor, as indicated in Figure (1), so

$$I_{in} = -I_C$$

$$-\frac{V_{in}}{R_i C} = \frac{dV_{out}}{dt} \qquad this\ called\ the\ rate\ of\ change\ of\ the\ output$$

$$dV_{out} = -\frac{1}{R_i C} V_{in} dt$$

$$V_{out} = -\frac{1}{R_i C}\int V_{in}dt \qquad in\ time\ domain$$

$$\frac{V_{in}}{R_i} = \frac{-V_{out}}{Xc}$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{-Xc}{R_i} = \frac{-1}{wR_i C} \qquad infrequency\ domain$$

The Practical Integrator The ideal integrator uses a capacitor in the feedback path, which is open to dc. This implies that the gain at dc is the open-loop gain of the op-amp. In a practical integrator, any dc error voltage due to offset error will cause the output to produce a ramp that moves toward either positive or negative saturation (depending on the offset), even when no signal is present.

Practical integrators must have some means of overcoming the effects of offset and bias current. Various solutions are available, the simplest solution is to use a resistor in parallel with the capacitor in the feedback path, as shown in Figure (19). The feedback resistor, Rf, should be large compared to the input resistor Rin , in order to have a negligible effect on the output waveform. In addition, a compensating resistor, Rc, may be added to the non-inverting input to balance the effects of bias current.

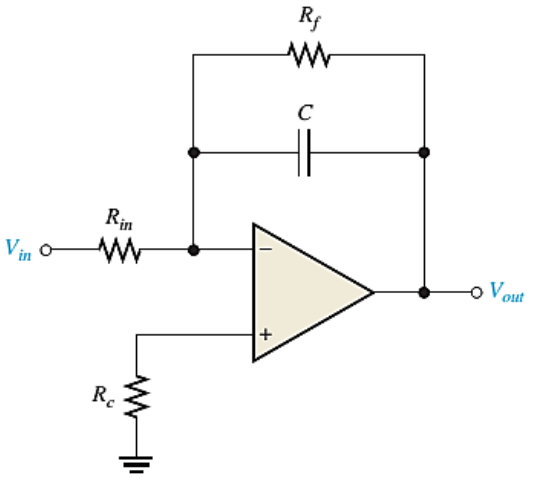


Figure (19) Practical Integrator

In the practical circuit it will operate as inverting amplifier at frequencies less than the cutoff frequency (fC). The gain is

$$G = -\frac{R_f}{R_{in}}$$

And as integrator at frequencies higher than the cutoff frequency (fC).

$$f_c = \frac{1}{2\pi R_f C}$$

The Op-Amp Differentiator

The Ideal Differentiator: An ideal differentiator is shown in Figure (20). Notice how the placement of the capacitor and resistor differ from the integrator. The capacitor is now the input element, and the resistor is the feedback element. A differentiator produces an output that is proportional to the rate of change of the input voltage.

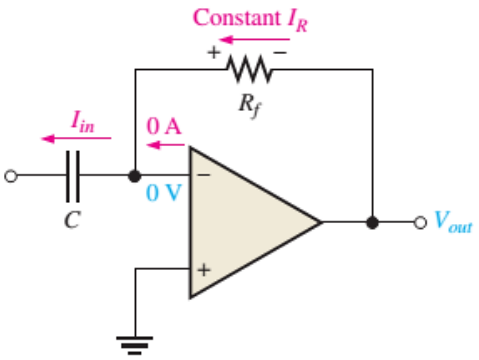


Figure (20) Ideal Differentiator

$$I_{in} = -I_R$$

$$C\frac{dV_{in}}{dt} = \frac{-V_{out}}{R_f} =$$

$$V_{out} = -CR_f\frac{dV_{in}}{dt} \qquad \text{the output is the differentiator of the input}$$

$$A_v = \frac{V_{out}}{V_{in}} = -jwCR_f$$

The Practical Differentiator: The last equations shows that the ideal differentiator has a very high gain amplifier at high frequencies. This means that a differentiator circuit tends to be noisy because electrical noise mainly consists of high frequencies. The solution to this problem is simply to add a resistor, Rin, in series with the capacitor to act as a low-pass filter and reduce the gain at high frequencies. The resistor should be small compared to the feedback resistor in order to have a negligible effect on the desired signal.

Figure (21) shows a practical differentiator. A bias compensating resistor may also be used on the non-inverting input.

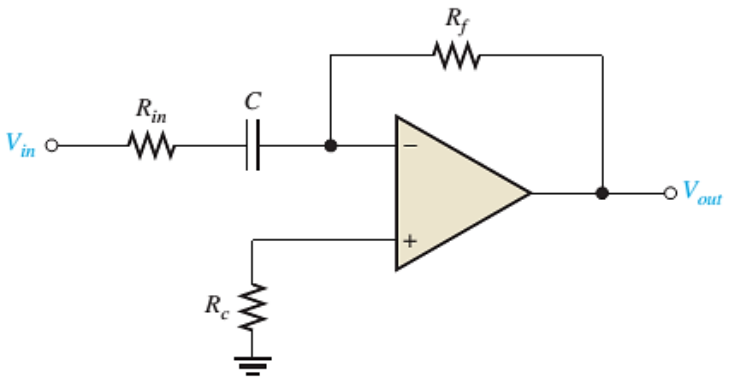


Figure (4) Practical Differentiator

In the practical circuit it will operate as inverting amplifier at frequencies higher than the cutoff frequency (fC). The gain is

$$G = -\frac{R_f}{R_{in}}$$

And as differentiator at frequencies less than the cutoff frequency (fC).

$$f_c = \frac{1}{2\pi R_{in} C}$$

Chapter Four
Other Devices

The Unijunction Transistor (UJT)

The UJT (unijunction transistor) is a three-terminal device whose basic construction is shown in Figure (4-1a). A slab of lightly doped (increased resistance characteristic) n-type silicon material has two contacts attached to both ends of one surface labelled as **Base 1 and Base 2** (B1 and B2). The p region of the device is formed at the other boundary of the n-type silicon slab at a point closer to B2 contact than the B1 contact. The p region terminal is labelled as **Emitter** (E). The single p–n junction accounts for the terminology unijunction.

The schematic symbol appears in Figure (4-1b). Notice the terminals are labelled Emitter (E), Base 1 and Base 2. Do not confuse this symbol with that of a JFET; the difference is that the arrow is at an angle for the UJT.

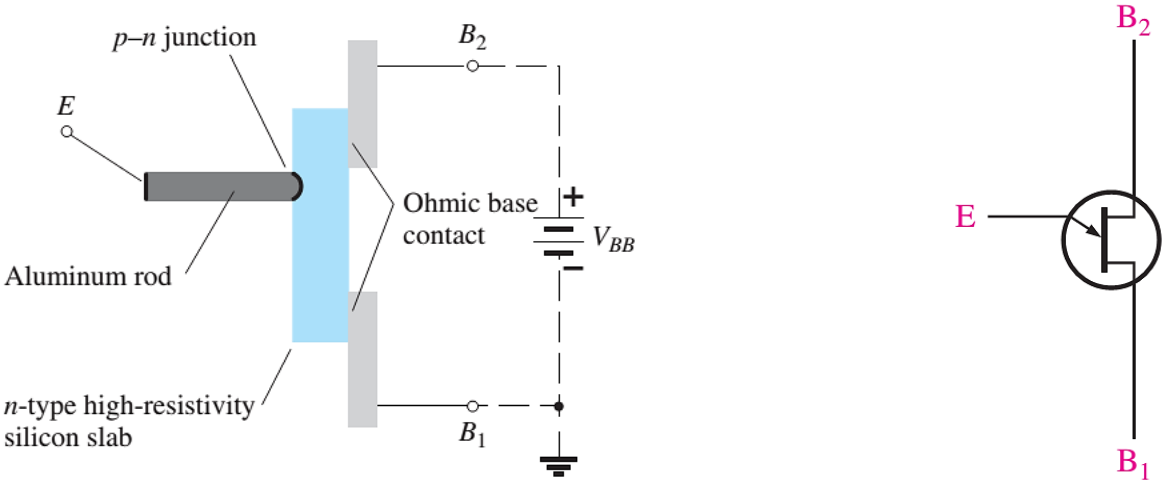


Figure (4-1) UJT transistor (a) Basic Structure (b) Symbol

UJT Equivalent Circuit

The equivalent circuit for the UJT, shown in Figure (4-2), will aid in understanding the basic operation. The diode shown in the figure represents the pn junction. **RB1** represents the internal dynamic resistance of the silicon bar between the emitter and base 1. The resistance RB1 is shown as a variable resistor since its magnitude will vary inversely with the current IE. **RB2** represents the dynamic resistance between the emitter and base 2.

The **Interbase resistance** RBB is the resistance of the device between terminals B1 and B2 when IE=0. In equation form

$$\boldsymbol{R_{BB} = R_{B1} + R_{B2} \qquad when\ I_E = 0}$$

The magnitude of V_{RB1} (with IE=0) is determined by the voltage-divider rule in the following manner:

$$\boldsymbol{V_{RB1} = V_{BB}\ \frac{R_{B1}}{R_{B1} + R_{B2}} = V_{BB}\ \frac{R_{B1}}{R_{BB}}}$$

The ratio $(\frac{\boldsymbol{R_{B1}}}{\boldsymbol{R_{B1}+R_{B2}}})$ is a UJT characteristic called **the intrinsic standoff ratio** and is designated by

$$\eta = \frac{\boldsymbol{R_{B1}}}{\boldsymbol{R_{B1} + R_{B2}}} = \frac{\boldsymbol{R_{B1}}}{\boldsymbol{R_{BB}}}$$

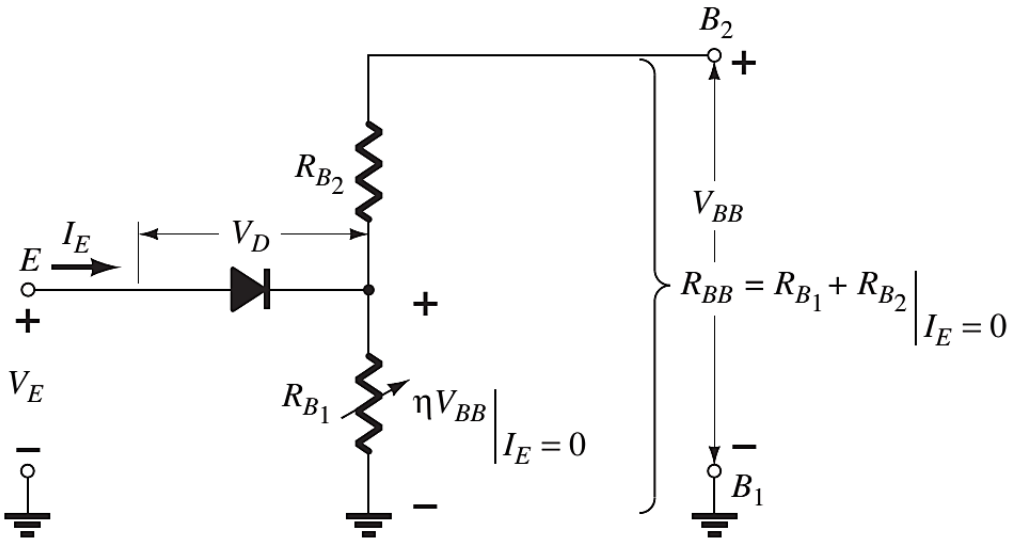


Figure (4-2) UJT equivalent circuit

UJT Emitter Characteristics Curve

The characteristics of a unijunction transistor are shown for VBB=10 V in Figure (4-3). As indicated in the figure there are four regions of operations for the UJT.

Cutoff Region: As long as the applied emitter voltage (VE) is less than (VRB1), there is no emitter current because the pn junction is not forward-biased. The magnitude of IE is never greater than IEO (measured in microamperes).

Negative Resistance Region: The value of emitter voltage that causes the pn junction to become forward biased is called (peak-point voltage) and is expressed as V_P.

$$V_P = VR_{B1} + V_D = \eta V_{BB} + V_D$$

Once conduction is established at VE=VP, the pn junction becomes forward-biased and IE begins. Holes are injected into the n-type bar from the p-type emitter. This increase in holes causes an increase in free electrons, thus increasing the conductivity between emitter and B1 (decreasing RB1).

After turn-on, the UJT operates in a negative resistance region up to a certain value of as shown by the characteristic curve in Figure (4-3). As you can see, after the peak point ($V_E = V_P$ and $I_E = I_P$), VE decreases as I_E continues to increase. This corresponds exactly to the decreasing resistance RB1 for increasing current I_E thus producing the **negative resistance characteristic.**

Saturation Region: Eventually, the valley point will be reached ($V_E = V_V$ and $I_E = I_V$), and any further increase in I_E will place the device in the saturation region. In this region, the characteristics approach those of the semiconductor diode in the equivalent circuit of Figure (4-2).

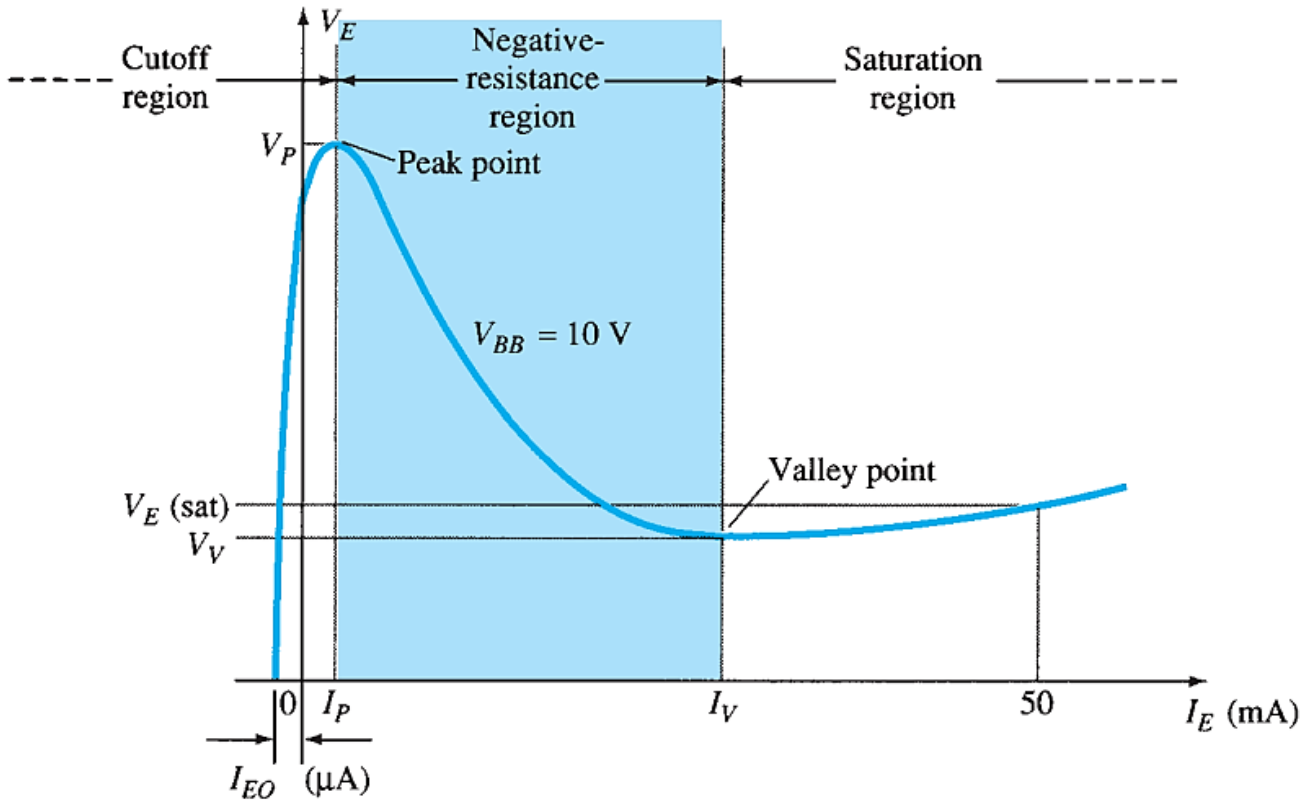


Figure (4-3) UJT emitter characteristic curve

UJT Applications

UJT used in a various applications include nonsinusoidal oscillators, sawtooth generators, phase control, and timing circuits. Figure (4-4) shows a UJT relaxation oscillator as an example of one application. The resistor R1 must be chosen to ensure that the load line determined by R1 passes through the device characteristics in the negative-resistance region.

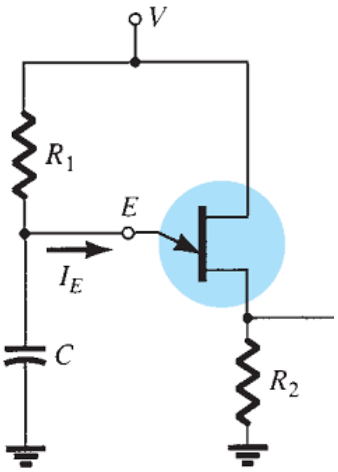
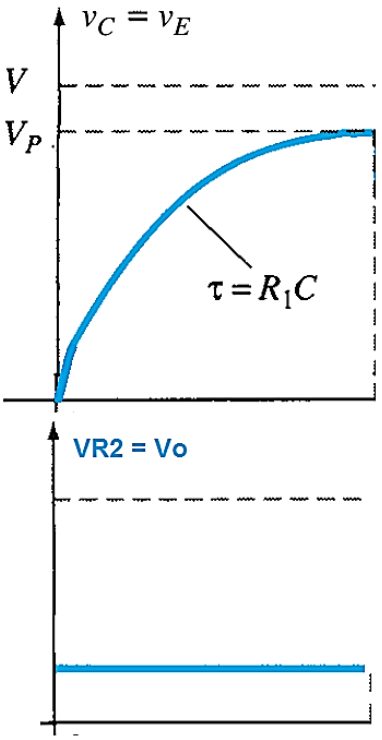


Figure (4-4) UJT Relaxation Oscillator

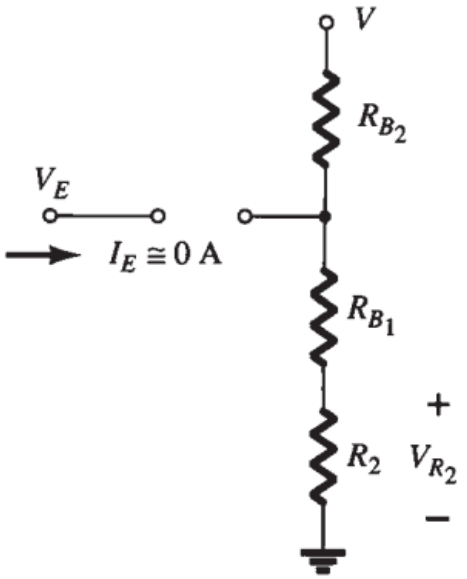
The operation is as follows.

When dc power is applied, the capacitor C charges exponentially through R1 until it reaches the peak-point voltage V_P as shown in figure (4-5a). As V_C (and therefore V_E) is less than V_P the diode is off and the value of the output voltage, as shown in figure (4-5b), is

$$V_o = VR_2 = \frac{V \times R_2}{R_2 + R_{BB}}$$



(a) Capacitor and output voltages

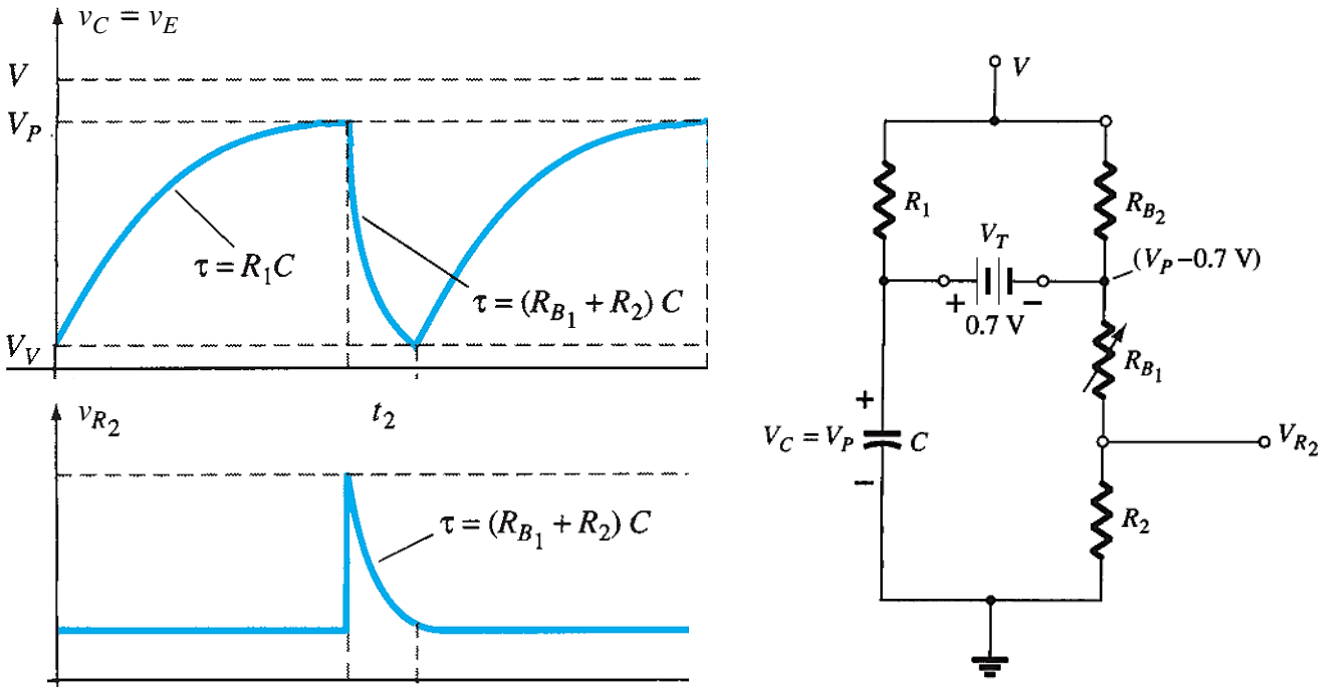


(b) Equivalent circuit

Figure (4-5) the action of the circuit during charging

As the capacitor voltage reaches the pick point (V_P), the pn junction becomes forward-biased, and the emitter characteristic goes into the negative resistance region (V_E decreases and I_E increases). The capacitor then quickly discharges through the forward-biased junction, RB1 and R2.

Figure (4-6a) shows the capacitor and output waveforms and Figure (4-6b) shows the equivalent circuit during this operation.



(a) Capacitor and output voltages *(b) Equivalent circuit*

Figure (4-6) the action of the circuit during discharging

When the capacitor voltage decreases to the valley-point voltage the UJT turns off, the capacitor begins to charge again, and the cycle is repeated.

SHOCKLEY DIODE

The4-layer diode(also known as Shockley diode and SUS) is a type of Thyristor, which is a class of devices constructed of four semiconductor layers. The basic construction of a 4-layer diode and its schematic symbol are shown in Figure (4-7).

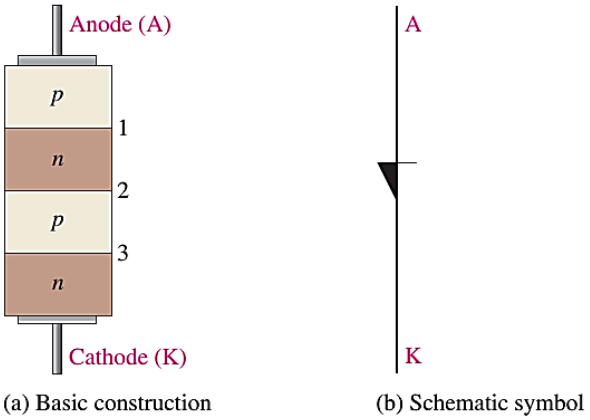


Figure (4-7) Shockley Diode

The pnpn structure can be represented by an equivalent circuit consisting of a pnp transistor and an npn transistor, as shown in Figure (4-8a).